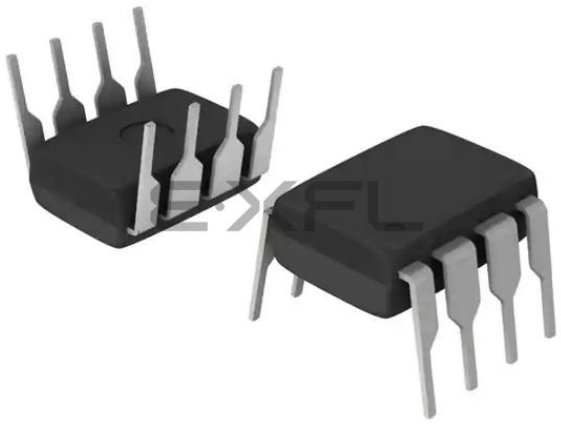

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## What is "Embedded - Microcontrollers"?

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## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | PIC |
| Core Size | 8-Bit |
| Speed | 4MHz |
| Connectivity | - |
| Peripherals | POR, WDT |
| Number of I/O | 5 |
| Program Memory Size | 1.75KB (1K x 14) |
| Program Memory Type | OTP |
| EEPROM Size | 16 x 8 |
| RAM Size | 128 x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.5V ~ 5.5V |
| Data Converters | A/D 4x8b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Through Hole |
| Package / Case | 8-DIP (0.300", 7.62mm) |
| Supplier Device Package | 8-PDIP |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic12lce673-04i-p |

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**PIN FUNCTION DESCRIPTIONS**

| Mnemonic | Type | Function |
|---|---|---|
| $DV_{DD}$ | P | Digital Positive Supply Voltage, 3 V or 5 V Nominal. |
| $AV_{DD}$ | P | Analog Positive Supply Voltage, 3 V or 5 V Nominal. |
| $C_{REF}$ | I | Decoupling Input for On-Chip Reference. Connect 0.1 μF between this pin and AGND. |
| $V_{REF}$ | I/O | Reference Input/Output. This pin is connected to the internal reference through a series resistor and is the reference source for the ADC. The nominal internal reference voltage is 2.5 V, which appears at the pin. This pin can be overdriven by an external reference. |
| AGND | G | Analog Ground. Ground reference point for the analog circuitry. |
| P1.0–P1.7 | I | Port 1 is an 8-bit input port only. Unlike other ports, Port 1 defaults to Analog Input mode. To configure any of these Port Pins as a digital input, write a 0 to the port bit. Port 1 pins are multifunctional and share the following functionality. |
| ADC0–ADC7 | I | Analog Inputs. Eight single-ended analog inputs. Channel selection is via ADCCON2 SFR. |
| T2 | I | Timer 2 Digital Input. Input to Timer/Counter 2. When enabled, Counter 2 is incremented in response to a 1 to 0 transition of the T2 input. |
| T2EX | I | Digital Input. Capture/Reload trigger for Counter 2; also functions as an Up/Down control input for Counter 2. |
| $\overline{SS}$ | I | Slave Select Input for the SPI Interface. |
| SDATA | I/O | User selectable, $I^2C$ Compatible or SPI Data Input/Output Pin. |
| SCLOCK | I/O | Serial Clock Pin for $I^2C$ Compatible or SPI Serial Interface Clock. |
| MOSI | I/O | SPI Master Output/Slave Input Data I/O Pin for SPI Interface. |
| MISO | I/O | SPI Master Input/Slave Output Data I/O Pin for SPI Serial Interface. |
| DAC0 | O | Voltage Output from DAC0. |
| DAC1 | O | Voltage Output from DAC1. |
| RESET | I | Digital Input. A high level on this pin for 24 master clock cycles while the oscillator is running resets the device. External power-on reset (POR) circuity must be implemented to drive the RESET pin as described in the Power-On Reset Operation section. |
| P3.0–P3.7 | I/O | Port 3 is a bidirectional port with internal pull-up resistors. Port 3 pins that have 1s written to them are pulled high by the internal pull-up resistors; in that state they can be used as inputs. As inputs, Port 3 pins being pulled externally low will source current because of the internal pull-up resistors. Port 3 pins also contain various secondary functions that are described below. |
| RxD | I/O | Receiver Data Input (Asynchronous) or Data Input/Output (Synchronous) of Serial (UART) Port |
| TxD | O | Transmitter Data Output (Asynchronous) or Clock Output (Synchronous) of Serial (UART) Port |
| $\overline{INT0}$ | I | Interrupt 0, programmable edge or level triggered Interrupt input, $\overline{INT0}$ can be programmed to one of two priority levels. This pin can also be used as a gate control input to Timer 0. |
| $\overline{INT1}$ | I | Interrupt 1, programmable edge or level triggered Interrupt input, $\overline{INT1}$ can be programmed to one of two priority levels. This pin can also be used as a gate control input to Timer 1. |
| T0 | I | Timer/Counter 0 Input. |
| T1 | I | Timer/Counter 1 Input. |
| $\overline{CONVST}$ | I | Active Low Convert Start Logic Input for the ADC Block when the External Convert Start Function is Enabled. A low-to-high transition on this input puts the track-and-hold into its hold mode and starts conversion. |
| $\overline{WR}$ | O | Write Control Signal, Logic Output. Latches the data byte from Port 0 into the external data memory. |
| $\overline{RD}$ | O | Read Control Signal, Logic Output. Enables the external data memory to Port 0. |
| XTAL2 | O | Output of the Inverting Oscillator Amplifier. |
| XTAL1 | I | Input to the Inverting Oscillator Amplifier and to the Internal Clock Generator Circuits. |
| DGND | G | Digital Ground. Ground reference point for the digital circuitry. |
| P2.0–P2.7<br>(A8–A15)<br>(A16–A23) | I/O | Port 2 is a bidirectional port with internal pull-up resistors. Port 2 pins that have 1s written to them are pulled high by the internal pull-up resistors; in that state they can be used as inputs. As inputs, Port 2 pins being pulled externally low will source current because of the internal pull-up resistors. Port 2 emits the high order address bytes during fetches from external program memory and middle and high order address bytes during accesses to the external 24-bit external data memory space. |

**PIN FUNCTION DESCRIPTIONS (continued)**

| Mnemonic | Type | Function |
|---|---|---|
| $\overline{\text{PSEN}}$ | O | Program Store Enable, Logic Output. This output is a control signal that enables the external program memory to the bus during external fetch operations. It is active every six oscillator periods except during external data memory accesses. This pin remains high during internal program execution. $\overline{\text{PSEN}}$ can also be used to enable serial download mode when pulled low through a resistor on power-up or RESET. |
| ALE | O | Address Latch Enable, Logic Output. This output is used to latch the low byte (and page byte for 24-bit address space accesses) of the address into external memory during normal operation. It is activated every six oscillator periods except during an external data memory access. |
| $\overline{\text{EA}}$ | I | External Access Enable, Logic Input. When held high, this input enables the device to fetch code from internal program memory locations 0000H to 1FFFH. When held low, this input enables the device to fetch all instructions from external program memory. |
| P0.7–P0.0 (A0–A7) | I/O | Port 0 is an 8-bit open-drain bidirectional I/O port. Port 0 pins that have 1s written to them float and in that state can be used as high impedance inputs. Port 0 is also the multiplexed low order address and data bus during accesses to external program or data memory. In this application, it uses strong internal pull-ups when emitting 1s. |
| EP | | Exposed Pad. For the LFCSP, the exposed pad must be soldered and left unconnected. |

## TERMINOLOGY

### ADC SPECIFICATIONS

**Integral Nonlinearity**

This is the maximum deviation of any code from a straight line passing through the endpoints of the ADC transfer function. The endpoints of the transfer function are zero scale, a point 1/2 LSB below the first code transition, and full scale, a point 1/2 LSB above the last code transition.

**Differential Nonlinearity**

This is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

**Offset Error**

This is the deviation of the first code transition (0000 . . . 000) to (0000 . . . 001) from the ideal, i.e., +1/2 LSB.

**Full-Scale Error**

This is the deviation of the last code transition from the ideal AIN voltage (Full Scale – 1.5 LSB) after the offset error has been adjusted out.

**Signal-to-(Noise + Distortion) Ratio**

This is the measured ratio of signal-to-(noise + distortion) at the output of the ADC. The signal is the rms amplitude of the fundamental. Noise is the rms sum of all nonfundamental signals up to half the sampling frequency ($f_S/2$), excluding dc. The ratio is dependent upon the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal-to-(noise + distortion) ratio for an ideal N-bit converter with a sine wave input is given by:

$$\textit{Signal-to-(Noise + Distortion)} = (6.02N + 1.76)\ dB$$

Thus for a 12-bit converter, this is 74 dB.

**Total Harmonic Distortion**

Total Harmonic Distortion is the ratio of the rms sum of the harmonics to the fundamental.

### DAC SPECIFICATIONS

**Relative Accuracy**

Relative accuracy or endpoint linearity is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for zero-scale error and full-scale error.

**Voltage Output Settling Time**

This is the amount of time it takes for the output to settle to a specified level for a full-scale input change.

**Digital-to-Analog Glitch Impulse**

This is the amount of charge injected into the analog output when the inputs change state. It is specified as the area of the glitch in nV sec.

## SPECIAL FUNCTION REGISTERS

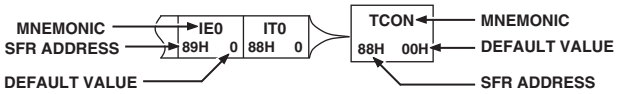
All registers except the program counter and the four general-purpose register banks reside in the special function register (SFR) area. The SFR registers include control, configuration, and data registers that provide an interface between the CPU and other on-chip peripherals.

Figure 4 shows a full SFR memory map and SFR contents on reset. Unoccupied SFR locations are shown dark shaded (NOT USED). Unoccupied locations in the SFR address space are not implemented, i.e., no register exists at this location. If an unoccupied location is read, an unspecified value is returned. SFR locations reserved for on-chip testing are shown lighter shaded (RESERVED) and should not be accessed by user software. Sixteen of the SFR locations are also bit addressable and denoted by "1" i.e., the bit addressable SFRs are those whose address ends in 0H or 8H.

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| ISPI FFH 0 | WCOL FEH 0 | SPE FDH 0 | SPIM FCH 0 | CPOL FBH 0 | CPHA FAH 0 | SPR1 F9H 0 | SPR0 F8H 0 | BITS | SPICON[1] F8H 00H |
| F7H 0 | F6H 0 | F5H 0 | F4H 0 | F3H 0 | F2H 0 | F1H 0 | F0H 0 | BITS | B[1] F0H 00H |
| MDO EFH 0 | MDE EEH 0 | MCO EDH 0 | MDI ECH 0 | I2CM EBH 0 | I2CRS EAH 0 | I2CTX E9H 0 | I2CI E8H 0 | BITS | I2CCON[1] E8H 00H |
| E7H 0 | E6H 0 | E5H 0 | E4H 0 | E3H 0 | E2H 0 | E1H 0 | E0H 0 | BITS | ACC[1] E0H 00H |
| ADCI DFH 0 | DMA DEH 0 | CCONV DDH 0 | SCONV DCH 0 | CS3 DBH 0 | CS2 DAH 0 | CS1 D9H 0 | CS0 D8H 0 | BITS | ADCCON2[1] D8H 00H |
| CY D7H 0 | AC D6H 0 | F0 D5H 0 | RS1 D4H 0 | RS0 D3H 0 | OV D2H 0 | FI D1H 0 | P D0H 0 | BITS | PSW[1] D0H 00H |
| TF2 CFH 0 | EXF2 CEH 0 | RCLK CDH 0 | TCLK CCH 0 | EXEN2 CBH 0 | TR2 CAH 0 | CNT2 C9H 0 | CAP2 C8H 0 | BITS | T2CON[1] C8H 00H |
| PRE2 C7H 0 | PRE1 C6H 0 | PRE0 C5H 0 | C4H 0 | WDR1 C3H 0 | WDR2 C2H 0 | WDS C1H 0 | WDE C0H 0 | BITS | WDCON[1] C0H 00H |
| PSI BFH 0 | PADC BEH 0 | PT2 BDH 0 | PS BCH 0 | PT1 BBH 0 | PX1 BAH 0 | PT0 B9H 0 | PX0 B8H 0 | BITS | IP[1] B8H 00H |
| RD B7H 1 | WR B6H 1 | T1 B5H 1 | T0 B4H 1 | INT1 B3H 1 | INT0 B2H 1 | TxD B1H 1 | RxD B0H 1 | BITS | P3[1] B0H FFH |
| EA AFH 0 | EADC AEH 0 | ET2 ADH 0 | ES ACH 0 | ET1 ABH 0 | EX1 AAH 0 | ET0 A9H 0 | EX0 A8H 0 | BITS | IE[1] A8H 00H |
| A7H 1 | A6H 1 | A5H 1 | A4H 1 | A3H 1 | A2H 1 | A1H 1 | A0H 1 | BITS | P2[1] A0H FFH |
| SM0 9FH 0 | SM1 9EH 0 | SM2 9DH 0 | REN 9CH 0 | TB8 9BH 0 | RB8 9AH 0 | TI 99H 0 | RI 98H 0 | BITS | SCON[1] 98H 00H |
| 97H 1 | 96H 1 | 95H 1 | 94H 1 | 93H 1 | 92H 1 | T2EX 91H 1 | T2 90H 1 | BITS | P1[1, 3] 90H FFH |
| TF1 8FH 0 | TR1 8EH 0 | TF0 8DH 0 | TR0 8CH 0 | IE1 8BH 0 | IT1 8AH 0 | IE0 89H 0 | IT0 88H 0 | BITS | TCON[1] 88H 00H |
| 87H 1 | 86H 1 | 85H 1 | 84H 1 | 83H 1 | 82H 1 | 81H 1 | 80H 1 | BITS | P0[1] 80H FFH |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| DAC0L F9H 00H | DAC0H FAH 00H | DAC1L FBH 00H | DAC1H FCH 00H | DACCON FDH 04H | RESERVED | NOT USED | | |
| ADCOFSL[2] F1H 00H | ADCOFSH[2] F2H 20H | ADCGAINL[2] F3H 00H | ADCGAINH[2] F4H 00H | ADCCON3 F5H 00H | RESERVED | SPIDAT F7H 00H | | |
| RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | ADCCON1 EFH 20H | | |
| RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | | |
| ADCDATAL D9H 00H | ADCDATAH DAH 00H | RESERVED | RESERVED | RESERVED | RESERVED | PSMCON DFH DEH | | |
| RESERVED | DMAL D2H 00H | DMAH D3H 00H | DMAP D4H 00H | RESERVED | RESERVED | RESERVED | | |
| RESERVED | RCAP2L CAH 00H | RCAP2H CBH 00H | TL2 CCH 00H | TH2 CDH 00H | RESERVED | RESERVED | | |
| NOT USED | NOT USED | NOT USED | ETIM3 C4H C9H | RESERVED | EDARL C6H 00H | RESERVED | | |
| ECON B9H 00H | ETIM1 BAH 52H | ETIM2 BBH 04H | EDATA1 BCH 00H | EDATA2 BDH 00H | EDATA3 BEH 00H | EDATA4 BFH 00H | | |
| NOT USED | NOT USED | NOT USED | NOT USED | NOT USED | NOT USED | NOT USED | | |
| IE2 A9H 00H | NOT USED | NOT USED | NOT USED | NOT USED | NOT USED | NOT USED | | |
| NOT USED | NOT USED | NOT USED | NOT USED | NOT USED | NOT USED | NOT USED | | |
| SBUF 99H 00H | I2CDAT 9AH 00H | I2CADD 9BH 55H | NOT USED | NOT USED | NOT USED | NOT USED | | |
| NOT USED | NOT USED | NOT USED | NOT USED | NOT USED | NOT USED | NOT USED | | |
| TMOD 89H 00H | TL0 8AH 00H | TL1 8BH 00H | TH0 8CH 00H | TH1 8DH 00H | NOT USED | NOT USED | | |
| SP 81H 07H | DPL 82H 00H | DPH 83H 00H | DPP 84H 00H | RESERVED | RESERVED | PCON 87H 00H | | |

SFR MAP KEY:




SFR NOTES

[1]SFRs WHOSE ADDRESS ENDS IN 0H OR 8H ARE BIT ADDRESSABLE.
[2]CALIBRATION COEFFICIENTS ARE PRECONFIGURED ON POWER-UP TO FACTORY CALIBRATED VALUES.
[3]THE PRIMARY FUNCTION OF PORT 1 IS AS AN ANALOG INPUT PORT; THEREFORE, TO ENABLE THE DIGITAL SECONDARY FUNCTIONS ON THESE PORT PINS, WRITE A "0" TO THE CORRESPONDING PORT 1 SFR BIT.

*Figure 4. Special Function Register Locations and Reset Values*

**ADCCON1—(ADC Control SFR #1)**

The ADCCON1 register controls conversion and acquisition times, hardware conversion modes and power-down modes as detailed below.

SFR Address EFH
SFR Power-On Default Value 20H

| MD1 | MD0 | CK1 | CK0 | AQ1 | AQ0 | T2C | EXC |
|---|---|---|---|---|---|---|---|

**Table III. ADCCON1 SFR Bit Designations**

| Bit | Name | Description |
|---|---|---|
| ADCCON1.7<br>ADCCON1.6 | MD1<br>MD0 | The mode bits (MD1, MD0) select the active operating mode of the ADC as follows:<br>MD1 MD0 Active Mode<br>0 0 ADC powered down<br>0 1 ADC normal mode<br>1 0 ADC powered down if not executing a conversion cycle<br>1 1 ADC standby if not executing a conversion cycle<br>Note: In power-down mode the ADC $V_{REF}$ circuits are maintained on, whereas all ADC peripherals are powered down, thus minimizing current consumption. |
| ADCCON1.5<br>ADCCON1.4 | CK1<br>CK0 | The ADC clock divide bits (CK1, CK0) select the divide ratio for the master clock used to generate the ADC clock. A typical ADC conversion will require 17 ADC clocks. The divider ratio is selected as follows:<br>CK1 CK0 MCLK Divider<br>0 0 1<br>0 1 2<br>1 0 4<br>1 1 8 |
| ADCCON1.3<br>ADCCON1.2 | AQ1<br>AQ0 | The ADC acquisition select bits (AQ1, AQ0) select the time provided for the input track-and-hold amplifier to acquire the input signal, and are selected as follows:<br>AQ1 AQ0 #ADC Clks<br>0 0 1<br>0 1 2<br>1 0 4<br>1 1 8 |
| ADCCON1.1 | T2C | The Timer 2 conversion bit (T2C) is set by the user to enable the Timer 2 overflow bit be used as the ADC convert start trigger input. ADC conversions are initiated on the second Timer 2 overflow. |
| ADCCON1.0 | EXC | The external trigger enable bit (EXC) is set by the user to allow the external CONVST pin to be used as the active low convert start input. This input should be an active low pulse (minimum pulsewidth >100 ns) at the required sample rate. |

**ADCCON2—(ADC Control SFR #2)**
The ADCCON2 register controls ADC channel selection and conversion modes as detailed below.

SFR Address D8H
SFR Power-On Default Value 00H

| ADCI | DMA | CCONV | SCONV | CS3 | CS2 | CS1 | CS0 |
|---|---|---|---|---|---|---|---|

**Table IV. ADCCON2 SFR Bit Designations**

| Location | Name | Description |
|---|---|---|
| ADCCON2.7 | ADCI | The ADC interrupt bit (ADCI) is set by hardware at the end of a single ADC conversion cycle or at the end of a DMA block conversion. ADCI is cleared by hardware when the PC vectors to the ADC Interrupt Service Routine. |
| ADCCON2.6 | DMA | The DMA mode enable bit (DMA) is set by the user to enable a preconfigured ADC DMA mode operation. A more detailed description of this mode is given in the ADC DMA Mode section. |
| ADCCON2.5 | CCONV | The continuous conversion bit (CCONV) is set by the user to initiate the ADC into a continuous mode of conversion. In this mode, the ADC starts converting based on the timing and channel configuration already set up in the ADCCON SFRs; the ADC automatically starts another conversion once a previous conversion has completed. |
| ADCCON2.4 | SCONV | The single conversion bit (SCONV) is set to initiate a single conversion cycle. The SCONV bit is automatically reset to "0" on completion of the single conversion cycle. |
| ADCCON2.3<br>ADCCON2.2<br>ADCCON2.1<br>ADCCON2.0 | CS3<br>CS2<br>CS1<br>CS0 | The channel selection bits (CS3–0) allow the user to program the ADC channel selection under software control. When a conversion is initiated, the channel converted will be the one pointed to by these channel selection bits. In DMA mode, the channel selection is derived from the channel ID written to the external memory.<br>CS3 CS2 CS1 CS0 CH#<br>0 0 0 0 0<br>0 0 0 1 1<br>0 0 1 0 2<br>0 0 1 1 3<br>0 1 0 0 4<br>0 1 0 1 5<br>0 1 1 0 6<br>0 1 1 1 7<br>1 0 0 0 Temp Sensor<br>1 1 1 1 DMA STOP<br>All other combinations reserved. |

**ADCCON3—(ADC Control SFR #3)**
The ADCCON3 register gives user software an indication of ADC busy status.

SFR Address F5H
SFR Power-On Default Value 00H

| BUSY | RSVD | RSVD | RSVD | RSVD | RSVD | RSVD | RSVD |
|---|---|---|---|---|---|---|---|

**Table V. ADCCON3 SFR Bit Designations**

| Bit Location | Bit Status | Description |
|---|---|---|
| ADCCON3.7 | BUSY | The ADC busy status bit (BUSY) is a read-only status bit that is set during a valid ADC conversion or calibration cycle. BUSY is automatically cleared by the core at the end of conversion or calibration. |
| ADCCON3.6<br>ADCCON3.5<br>ADCCON3.4<br>ADCCON3.3<br>ADCCON3.2<br>ADCCON3.1<br>ADCCON3.0 | RSVD<br>RSVD<br>RSVD<br>RSVD<br>RSVD<br>RSVD<br>RSVD | ADCCON3.0–3.6 are reserved (RSVD) for internal use. These bits will read as "0" and should only be written as "0" by user software. |

**Using the Flash/EE Program Memory**

This 8K byte Flash/EE program memory array is mapped into the lower 8K bytes of the 64K bytes program space addressable by the ADuC812 and will be used to hold user code in typical applications.

The program memory array can be programmed in one of two modes:

***Serial Downloading (In-Circuit Programming)***

As part of its embedded download/debug kernel, the ADuC812 facilitates serial code download via the standard UART serial port. Serial download mode is automatically entered on power-up if the external pin $\overline{\text{PSEN}}$ is pulled low through an external resistor as shown in Figure 15. Once in this mode, the user can download code to the program memory array while the device is sited in its target application hardware. A PC serial download executable is provided as part of the ADuC812 QuickStart development system.

The Serial Download protocol is detailed in a MicroConverter Applications Note uC004, available from the ADI MicroConverter website at www.analog.com/microconverter.

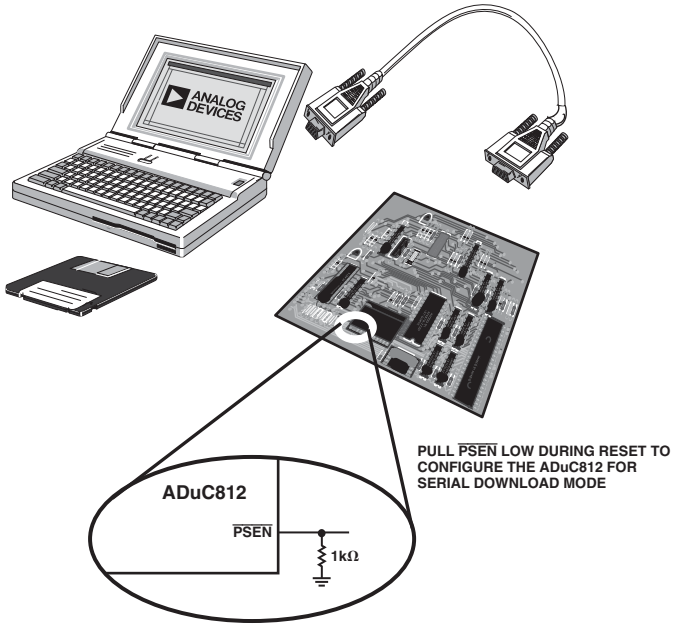



*Figure 15. Flash/EE Memory Serial Download Mode Programming*

***Parallel Programming***

The parallel programming mode is fully compatible with conventional third party Flash or EEPROM device programmers. In this mode, Ports P0, P1, and P2 operate as the external data and address bus interface, ALE operates as the Write Enable strobe, and Port P3 is used as a general configuration port that configures the device for various program and erase operations during parallel programming.

The high voltage (12 V) supply required for Flash programming is generated using on-chip charge pumps to supply the high voltage program lines.

The complete parallel programming specification is available on the MicroConverter homepage at www.analog.com/microconverter.

**Using the Flash/EE Data Memory**

The user Flash/EE data memory array consists of 640 bytes that are configured into 160 (Page 00H to Page 9FH) 4-byte pages, as shown in Figure 16.

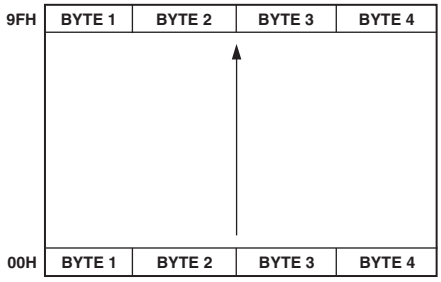



*Figure 16. User Flash/EE Memory Configuration*

As with other ADuC812 user peripheral circuits, the interface to this memory space is via a group of registers mapped in the SFR space. A group of four data registers (EDATA1–4) is used to hold the 4-byte page being accessed. EADRL is used to hold the 8-bit address of the page being accessed. Finally, ECON is an 8-bit control register that may be written with one of five Flash/EE memory access commands to trigger various read, write, erase, and verify functions. These register can be summarized as follows:

| | | |
|---|---|---|
| ECON: | SFR Address | B9H |
| | Function | Controls access to 640 bytes Flash/EE data space. |
| | Default | 00H |
| EADRL: | SFR Address | C6H |
| | Function | Holds the Flash/EE data page address. 0H through 9FH |
| | Default | 00H |
| EDATA1–4: | | |
| | SFR Address | BCH to BFH, respectively |
| | Function | Holds the Flash/EE data memory page write or page read data bytes. |
| | Default | EDATA1–4→00H |

A block diagram of the SFR registered interface to the data Flash/EE memory array is shown in Figure 17.

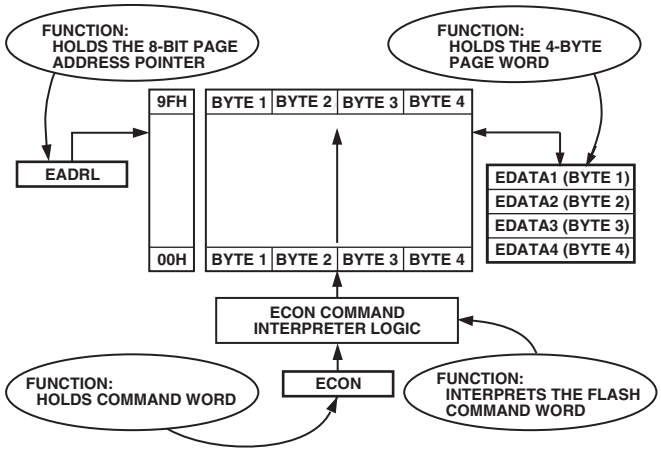



*Figure 17. User Flash/EE Memory Control and Configuration*

**USER INTERFACE TO OTHER ON-CHIP ADuC812 PERIPHERALS**

The following section gives a brief overview of the various peripherals also available on-chip. A summary of the SFRs used to control and configure these peripherals is also given.

**DAC**

The ADuC812 incorporates two 12-bit voltage output DACs on-chip. Each has a rail-to-rail voltage output buffer capable of driving 10 kΩ/100 pF. Each has two selectable ranges, 0 V to $V_{REF}$ (the internal band gap 2.5 V reference) and 0 V to $AV_{DD}$. Each can operate in 12-bit or 8-bit mode. Both DACs share a control register, DACCON, and four data registers, DAC1H/L, DAC0H/L. It should be noted that in 12-bit asynchronous mode, the DAC voltage output will be updated as soon as the DACL data SFR has been written; therefore, the DAC data registers should be updated as DACH first, followed by DACL.

| **DACCON** | **DAC Control Register** |
|---|---|
| SFR Address | FDH |
| Power-On Default Value | 04H |
| Bit Addressable | No |

| MODE | RNG1 | RNG0 | CLR1 | CLR0 | SYNC | $\overline{PD1}$ | PD0 |
|---|---|---|---|---|---|---|---|

**Table VIII. DACCON SFR Bit Designations**

| Bit | Name | Description |
|---|---|---|
| 7 | MODE | The DAC MODE bit sets the overriding operating mode for both DACs.<br>Set to "1" = 8-bit mode (Write eight Bits to DACxL SFR).<br>Set to "0" = 12-bit mode. |
| 6 | RNG1 | DAC1 Range Select Bit.<br>Set to "1" = DAC1 range 0–$V_{DD}$.<br>Set to "0" = DAC1 range 0–$V_{REF}$. |
| 5 | RNG0 | DAC0 Range Select Bit.<br>Set to "1" = DAC0 range 0–$V_{DD}$.<br>Set to "0" = DAC0 range 0–$V_{REF}$. |
| 4 | CLR1 | DAC1 Clear Bit.<br>Set to "0" = DAC1 output forced to 0 V.<br>Set to "1" = DAC1 output normal. |
| 3 | CLR0 | DAC0 Clear Bit.<br>Set to "0" = DAC1 output forced to 0 V.<br>Set to "1" = DAC1 output normal. |
| 2 | SYNC | DAC0/1 Update Synchronization Bit.<br>When set to "1" the DAC outputs update as soon as DACxL SFRs are written. The user can simultaneously update both DACs by first updating the DACxL/H SFRs while SYNC is "0." Both DACs will then update simultaneously when the SYNC bit is set to "1." |
| 1 | $\overline{PD1}$ | DAC1 Power-Down Bit.<br>Set to "1" = Power-on DAC1.<br>Set to "0" = Power-off DAC1. |
| 0 | PD0 | DAC0 Power-Down Bit.<br>Set to "1" = Power-on DAC0.<br>Set to "0" = Power-off DAC0. |

| **DACxH/L** | **DAC Data Registers** |
|---|---|
| Function | DAC data registers, written by user to update the DAC output. |
| SFR Address | DAC0L (DAC0 Data Low Byte) →F9H; DAC1L (DAC1 data low byte)→FBH<br>DAC0H (DAC0 Data High Byte) →FAH; DAC1H(DAC1 data high byte)→FCH |
| Power-On Default Value | 00H →All four registers |
| Bit Addressable | No →All four registers |

The 12-bit DAC data should be written into DACxH/L, right-justified such that DACL contains the lower eight bits, and the lower nibble of DACH contains the upper four bits.

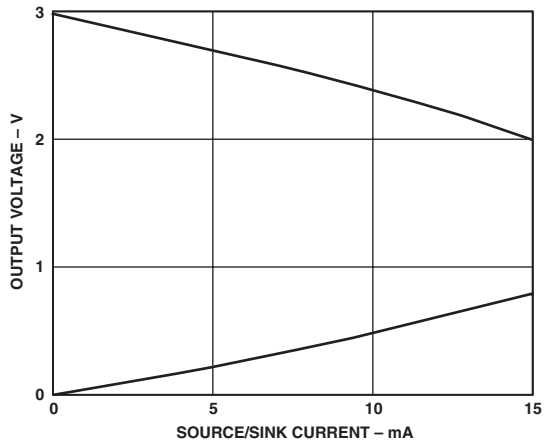



*Figure 21. Source and Sink Current Capability with $V_{REF} = V_{DD} = 3$ V*

To drive significant loads with the DAC outputs, external buffering may be required, as illustrated in Figure 22.

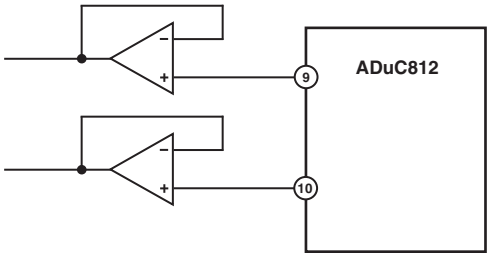



*Figure 22. Buffering the DAC Outputs*

The DAC output buffer also features a high impedance disable function. In the chip's default power-on state, both DACs are disabled, and their outputs are in a high impedance state (or "three-state") where they remain inactive until enabled in software. This means that if a zero output is desired during power-up or power-down transient conditions, then a pull-down resistor must be added to each DAC output. Assuming this resistor is in place, the DAC outputs will remain at ground potential whenever the DAC is disabled. However, each DAC output will still spike briefly when power is first applied to the chip, and again when each DAC is first enabled in software. Typical scope shots of these spikes are given in Figure 23 and Figure 24, respectively.

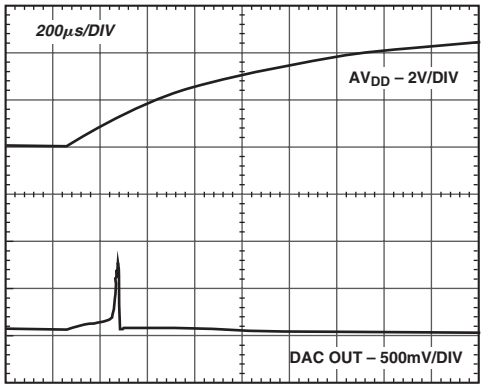



*Figure 23. DAC Output Spike at Chip Power-Up*

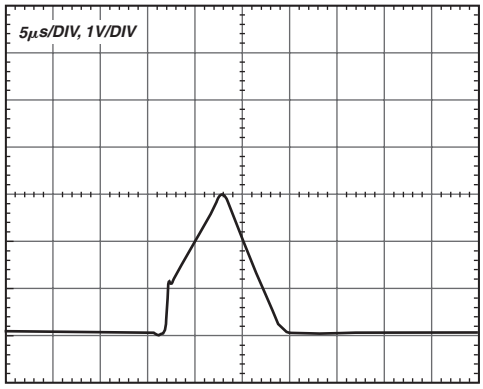



*Figure 24. DAC Output Spike at DAC Enable*

**MOSI (Master Out, Slave In Pin)**
The MOSI (master out, slave in) pin is configured as an output line in master mode and an input line in slave mode. The MOSI line on the master (data out) should be connected to the MOSI line in the slave device (data in). The data is transferred as byte wide (8-bit) serial data, MSB first.

**SCLOCK (Serial Clock I/O Pin)**
The master serial clock (SCLOCK) is used to synchronize the data being transmitted and received through the MOSI and MISO data lines. A single data bit is transmitted and received in each SCLOCK period. Therefore, a byte is transmitted/received after eight SCLOCK periods. The SCLOCK pin is configured as an output in master mode and as an input in slave mode. In master mode, the bit rate, polarity, and phase of the clock are controlled by the CPOL, CPHA, SPR0, and SPR1 bits in the SPICON SFR (see Table XI). In slave mode, the SPICON register will have to be configured with the phase and polarity (CPHA and CPOL) of the expected input clock. In both master and slave modes, the data is transmitted on one edge of the SCLOCK signal and sampled on the other. It is important therefore that the CPHA and CPOL are configured the same for the master and slave devices.

**$\overline{SS}$ (Slave Select Input Pin)**
The Slave Select ($\overline{SS}$) input pin is shared with the ADC5 input. To configure this pin as a digital input, the bit must be cleared, e.g., CLR P1.5.

This line is active low. Data is only received or transmitted in slave mode when the $\overline{SS}$ pin is low, allowing the ADuC812 to be used in single master, multislave SPI configurations. If CPHA = 1, then the $\overline{SS}$ input may be permanently pulled low. With CPHA = 0, the $\overline{SS}$ input must be driven low before the first bit in a byte wide transmission or reception, and return high again after the last bit in that byte wide transmission or reception. In SPI Slave mode, the logic level on the external $\overline{SS}$ pin can be read via the SPR0 bit in the SPICON SFR. The following SFR registers are used to control the SPI interface.

| **SPICON** | **SPI Control Register** |
|---|---|
| SFR Address | F8H |
| Power-On Default Value | OOH |
| Bit Addressable | Yes |

| ISPI | WCOL | SPE | SPIM | CPOL | CPHA | SPR1 | SPR0 |
|---|---|---|---|---|---|---|---|

**Table XI. SPICON SFR Bit Designations**

| Bit | Name | Description |
|---|---|---|
| 7 | ISPI | SPI Interrupt Bit.<br>Set by MicroConverter at the end of each SPI transfer.<br>Cleared directly by user code or indirectly by reading the SPIDAT SFR. |
| 6 | WCOL | Write Collision Error Bit.<br>Set by MicroConverter if SPIDAT is written to while an SPI transfer is in progress.<br>Cleared by user code. |
| 5 | SPE | SPI Interface Enable Bit.<br>Set by user to enable the SPI interface.<br>Cleared by user to enable $I^2C$ interface. |
| 4 | SPIM | SPI Master/Slave Mode Select Bit.<br>Set by user to enable Master mode operation (SCLOCK is an output).<br>Cleared by user to enable Slave mode operation (SCLOCK is an input). |
| 3 | CPOL* | Clock Polarity Select Bit.<br>Set by user if SCLOCK idles high.<br>Cleared by user if SCLOCK idles low. |
| 2 | CPHA* | Clock Phase Select Bit.<br>Set by user if leading SCLOCK edge is to transmit data.<br>Cleared by user if trailing SCLOCK edge is to transmit data. |
| 1 | SPR1 | SPI Bit Rate Select Bits. |
| 0 | SPR0 | These bits select the SCLOCK rate (bit rate) in Master mode as follows:<br>SPR1 SPR0 Selected Bit Rate<br>0 0 $f_{OSC}/4$<br>0 1 $f_{OSC}/8$<br>1 0 $f_{OSC}/32$<br>1 1 $f_{OSC}/64$<br>In SPI Slave mode, i.e., SPIM = 0, the logic level on the external $\overline{SS}$ pin can be read via the SPR0 bit. |

*The CPOL and CPHA bits should both contain the same values for master and slave devices.

## 8051 COMPATIBLE ON-CHIP PERIPHERALS

This section gives a brief overview of the various secondary peripheral circuits that are also available to the user on-chip. These remaining functions are fully 8051 compatible and are controlled via standard 8051 SFR bit definitions.

### Parallel I/O Ports 0–3

The ADuC812 uses four input/output ports to exchange data with external devices. In addition to performing general-purpose I/O, some ports are capable of external memory operations; others are multiplexed with an alternate function for the peripheral features on the device. In general, when a peripheral is enabled, that pin may not be used as a general-purpose I/O pin.

Port 0 is an 8-bit, open-drain, bidirectional I/O port that is directly controlled via the P0 SFR (SFR address = 80H). Port 0 pins that have 1s written to them via the Port 0 SFR will be configured as open-drain and will therefore float. In that state, Port 0 pins can be used as high impedance inputs. An external pull-up resistor will be required on Port 0 outputs to force a valid logic high level externally. Port 0 is also the multiplexed low order address and data bus during accesses to external program or data memory. In this application, it uses strong internal pull-ups when emitting 1s.

Port 1 is also an 8-bit port directly controlled via the P1 SFR (SFR address = 90H). Port 1 is an input only port. Port 1 digital output capability is not supported on this device. Port 1 pins can be configured as digital inputs or analog inputs.

By (power-on) default these pins are configured as analog inputs, i.e., "1" written in the corresponding Port 1 register bit. To configure any of these pins as digital inputs, the user should write a "0" to these port bits to configure the corresponding pin as a high impedance digital input.

These pins also have various secondary functions described in Table XIII.

**Table XIII. Port 1, Alternate Pin Functions**

| Pin | Alternate Function |
|---|---|
| P1.0 | T2 (Timer/Counter 2 External Input) |
| P1.1 | T2EX (Timer/Counter 2 Capture/Reload Trigger) |
| P1.5 | $\overline{SS}$ (Slave Select for the SPI Interface) |

Port 2 is a bidirectional port with internal pull-up resistors directly controlled via the P2 SFR (SFR address = A0H). Port 2 pins that have 1s written to them are pulled high by the internal pull-up resistors and, in that state, can be used as inputs. As inputs, Port 2 pins being pulled externally low will source current because of the internal pull-up resistors. Port 2 emits the high order address bytes during fetches from external program memory, and middle and high order address bytes during accesses to the 24-bit external data memory space.

Port 3 is a bidirectional port with internal pull-ups directly controlled via the P3 SFR (SFR address = B0H). Port 3 pins that have 1s written to them are pulled high by the internal pull-ups and, in that state, can be used as inputs. As inputs, Port 3 pins being pulled externally low will source current because of the internal pull-ups. Port 3 pins also have various secondary functions described in Table XIV.

**Table XIV. Port 3, Alternate Pin Functions**

| Pin | Alternate Function |
|---|---|
| P3.0 | RxD (UART Input Pin)<br>(or Serial Data I/O in Mode 0) |
| P3.1 | TxD (UART Output Pin)<br>(or Serial Clock Output in Mode 0) |
| P3.2 | $\overline{INT0}$ (External Interrupt 0) |
| P3.3 | $\overline{INT1}$ (External Interrupt 1) |
| P3.4 | T0 (Timer/Counter 0 External Input) |
| P3.5 | T1 (Timer/Counter 1 External Input) |
| P3.6 | $\overline{WR}$ (External Data Memory Write Strobe) |
| P3.7 | $\overline{RD}$ (External Data Memory Read Strobe) |

The alternate functions of P1.0, P1.1, P1.5, and Port 3 pins can be activated only if the corresponding bit latch in the P1 and P3 SFRs contains a 1. Otherwise, the port pin is stuck at 0.

### Timers/Counters

The ADuC812 has three 16-bit Timer/Counters: Timer 0, Timer 1, and Timer 2. The Timer/Counter hardware has been included on-chip to relieve the processor core of the overhead inherent in implementing timer/counter functionality in software. Each Timer/Counter consists of two 8-bit registers, THx and TLx (x = 0, 1, and 2). All three can be configured to operate either as timers or event counters.

In Timer function, the TLx register is incremented every machine cycle. Thus, think of it as counting machine cycles. Since a machine cycle consists of 12 core clock periods, the maximum count rate is 1/12 of the core clock frequency.

In Counter function, the TLx register is incremented by a 1-to-0 transition at its corresponding external input pin, T0, T1, or T2. In this function, the external input is sampled during S5P2 of every machine cycle. When the samples show a high in one cycle and a low in the next cycle, the count is incremented. The new count value appears in the register during S3P1 of the cycle following the one in which the transition was detected. Since it takes two machine cycles (24 core clock periods) to recognize a 1-to-0 transition, the maximum count rate is 1/24 of the core clock frequency. There are no restrictions on the duty cycle of the external input signal, but to ensure that a given level is sampled at least once before it changes, it must be held for a minimum of one full machine cycle.

User configuration and control of all Timer operating modes is achieved via three SFRs:

| | |
|---|---|
| TMOD, TCON | Control and configuration for Timers 0 and 1. |
| T2CON | Control and configuration for Timer 2. |

**TMOD — Timer/Counter 0 and 1 Mode Register**

| | |
|---|---|
| SFR Address | 89H |
| Power-On Default Value | 00H |
| Bit Addressable | No |

| Gate | C/T | M1 | M0 | Gate | C/T | M1 | M0 |
|---|---|---|---|---|---|---|---|

**Table XV. TMOD SFR Bit Designations**

| Bit | Name | Description |
|---|---|---|
| 7 | Gate | Timer 1 Gating Control.<br>Set by software to enable Timer/Counter 1 only while $\overline{INT1}$ pin is high and TR1 control bit is set.<br>Cleared by software to enable Timer 1 whenever TR1 control bit is set. |
| 6 | C/T | Timer 1 Timer or Counter Select Bit.<br>Set by software to select counter operation (input from T1 pin).<br>Cleared by software to select timer operation (input from internal system clock). |
| 5 | M1 | Timer 1 Mode Select Bit 1 (used with M0 Bit). |
| 4 | M0 | Timer 1 Mode Select Bit 0.<br>M1 M0<br>0 0 TH1 operates as an 8-bit timer/counter. TL1 serves as 5-bit prescaler.<br>0 1 16-Bit Timer/Counter. TH1 and TL1 are cascaded; there is no prescaler.<br>1 0 8-Bit Autoreload Timer/Counter. TH1 holds a value that is to be reloaded into TL1 each time it overflows.<br>1 1 Timer/Counter 1 Stopped. |
| 3 | Gate | Timer 0 Gating Control.<br>Set by software to enable Timer/Counter 0 only while $\overline{INT0}$ pin is high and TR0 control bit is set.<br>Cleared by software to enable Timer 0 whenever TR0 control bit is set. |
| 2 | C/T | Timer 0 Timer or Counter Select Bit.<br>Set by software to select counter operation (input from T0 pin).<br>Cleared by software to select timer operation (input from internal system clock). |
| 1 | M1 | Timer 0 Mode Select Bit 1. |
| 0 | M0 | Timer 0 Mode Select Bit 0.<br>M1 M0<br>0 0 TH0 operates as an 8-bit timer/counter. TL0 serves as 5-bit prescaler.<br>0 1 16-Bit Timer/Counter. TH0 and TL0 are cascaded; there is no prescaler.<br>1 0 8-Bit Autoreload Timer/Counter. TH0 holds a value that is to be reloaded into TL0 each time it overflows.<br>1 1 TL0 is an 8-bit timer/counter controlled by the standard timer 0 control bits. TH0 is an 8-bit timer only, controlled by Timer 1 control bits. |

| | |
|---|---|
| **TCON** | **Timer/Counter 0 and 1 Control Register** |
| SFR Address | 88H |
| Power-On Default Value | 00H |
| Bit Addressable | Yes |

| TF1 | TR1 | TF0 | TR0 | IE1* | IT1* | IE0* | IT0* |
|---|---|---|---|---|---|---|---|

*These bits are not used in the control of Timer/Counter 0 and 1, but are used instead in the control and monitoring of the external $\overline{INT0}$ and $\overline{INT1}$ interrupt pins.

**Table XVI. TCON SFR Bit Designations**

| Bit | Name | Description |
|---|---|---|
| 7 | TF1 | Timer 1 Overflow Flag.<br>Set by hardware on a Timer/Counter 1 overflow.<br>Cleared by hardware when the Program Counter (PC) vectors to the interrupt service routine. |
| 6 | TR1 | Timer 1 Run Control Bit.<br>Set by user to turn on Timer/Counter 1.<br>Cleared by user to turn off Timer/Counter 1. |
| 5 | TF0 | Timer 0 Overflow Flag.<br>Set by hardware on a Timer/Counter 0 overflow.<br>Cleared by hardware when the PC vectors to the interrupt service routine. |
| 4 | TR0 | Timer 0 Run Control Bit.<br>Set by user to turn on Timer/Counter 0.<br>Cleared by user to turn off Timer/Counter 0. |
| 3 | IE1 | External Interrupt 1 ($\overline{INT1}$) Flag.<br>Set by hardware by a falling edge or zero level being applied to external interrupt pin $\overline{INT1}$, depending on bit IT1 state.<br>Cleared by hardware when the when the PC vectors to the interrupt service routine only if the interrupt was transition-activated. If level-activated, the external requesting source controls the request flag, rather than the on-chip hardware. |
| 2 | IT1 | External Interrupt 1 (IE1) Trigger Type.<br>Set by software to specify edge-sensitive detection (i.e., 1-to-0 transition).<br>Cleared by software to specify level-sensitive detection (i.e., zero level). |
| 1 | IE0 | External Interrupt 0 ($\overline{INT0}$) Flag.<br>Set by hardware by a falling edge or zero level being applied to external interrupt pin $\overline{INT0}$, depending on bit IT0 state.<br>Cleared by hardware when the PC vectors to the interrupt service routine only if the interrupt was transition activated. If level activated, the external requesting source controls the request flag, rather than the on-chip hardware. |
| 0 | IT0 | External Interrupt 0 (IE0) Trigger Type.<br>Set by software to specify edge-sensitive detection (i.e., 1-to-0 transition).<br>Cleared by software to specify level-sensitive detection (i.e., zero level). |

**Timer/Counters 0 and 1 Data Registers**

Each timer consists of two 8-bit registers. These can be used as independent registers or combined to be a single 16-bit register depending on the timer mode configuration.

**TH0 and TL0**

Timer 0 high byte and low byte.
SFR Address = 8CH, 8AH, respectively.

**TH1 and TL1**

Timer 1 high byte and low byte.
SFR Address = 8DH, 8BH, respectively.

**Mode 0 (8-Bit Shift Register Mode)**
Mode 0 is selected by clearing both the SM0 and SM1 bits in the SFR SCON. Serial data enters and exits through RxD. TxD outputs the shift clock. Eight data bits are transmitted or received. Transmission is initiated by any instruction that writes to SBUF. The data is shifted out of the RxD line. The eight bits are transmitted with the least significant bit (LSB) first, as shown in Figure 32.

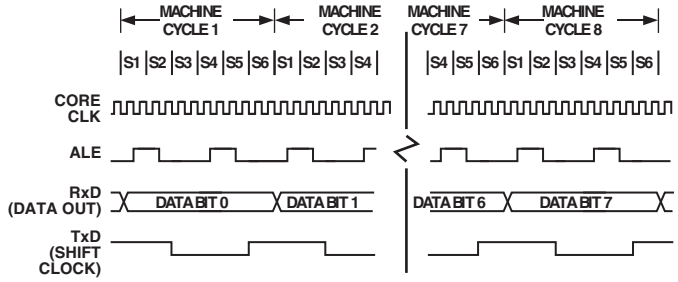



*Figure 32. UART Serial Port Transmission, Mode 0*

Reception is initiated when the receive enable bit (REN) is 1 and the receive interrupt bit (RI) is 0. When RI is cleared, the data is clocked into the RxD line and the clock pulses are output from the TxD line.

**Mode 1 (8-Bit UART, Variable Baud Rate)**
Mode 1 is selected by clearing SM0 and setting SM1. Each data byte (LSB first) is preceded by a start bit (0) and followed by a stop bit (1). Therefore 10 bits are transmitted on TxD or received on RxD. The baud rate is set by the Timer 1 or Timer 2 overflow rate, or a combination of the two (one for transmission and the other for reception).

Transmission is initiated by writing to SBUF. The "write to SBUF" signal also loads a 1 (stop bit) into the ninth bit position of the transmit shift register. The data is output bit by bit until the stop bit appears on TxD and the transmit interrupt flag (TI) is automatically set, as shown in Figure 33.

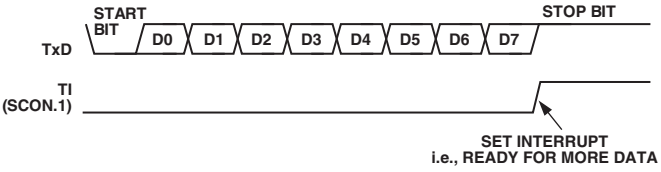



*Figure 33. UART Serial Port Transmission, Mode 0*

Reception is initiated when a 1-to-0 transition is detected on RxD. Assuming a valid start bit was detected, character reception continues. The start bit is skipped and the eight data bits are clocked into the serial port shift register. When all eight bits have been clocked in, the following events occur:

The eight bits in the receive shift register are latched into SBUF.

The ninth bit (Stop bit) is clocked into RB8 in SCON.

The Receiver interrupt flag (RI) is set.

This will be the case if, and only if, the following conditions are met at the time the final shift pulse is generated:

RI = 0, and

Either SM2 = 0 or SM2 = 1 and the received stop bit = 1.

If either of these conditions is not met, the received frame is irretrievably lost, and RI is not set.

**Mode 2 (9-Bit UART with Fixed Baud Rate)**
Mode 2 is selected by setting SM0 and clearing SM1. In this mode, the UART operates in 9-bit mode with a fixed baud rate. The baud rate is fixed at Core_Clk/64 by default, although by setting the SMOD bit in PCON, the frequency can be doubled to Core_Clk/32. Eleven bits are transmitted or received, a start bit (0), eight data bits, a programmable ninth bit, and a stop bit (1). The ninth bit is most often used as a parity bit, although it can be used for anything, including a ninth data bit if required.

To transmit, the eight data bits must be written into SBUF. The ninth bit must be written to TB8 in SCON. When transmission is initiated, the eight data bits (from SBUF) are loaded onto the transmit shift register (LSB first). The contents of TB8 are loaded into the ninth bit position of the transmit shift register. The transmission will start at the next valid baud rate clock. The TI flag is set as soon as the stop bit appears on TxD.

Reception for Mode 2 is similar to that of Mode 1. The eight data bytes are input at RxD (LSB first) and loaded onto the receive shift register. When all eight bits have been clocked in, the following events occur:

The eight bits in the receive shift register are latched into SBUF.

The ninth data bit is latched into RB8 in SCON.

The Receiver interrupt flag (RI) is set.

This will be the case if, and only if, the following conditions are met at the time the final shift pulse is generated:

RI = 0, and
Either SM2 = 0, or SM2 = 1 and the received stop bit = 1.

If either of these conditions is not met, the received frame is irretrievably lost, and RI is not set.

**Mode 3 (9-Bit UART with Variable Baud Rate)**
Mode 3 is selected by setting both SM0 and SM1. In this mode the 8051 UART serial port operates in 9-bit mode with a variable baud rate determined by either Timer 1 or Timer 2. The operation of the 9-bit UART is the same as for Mode 2, but the baud rate can be varied as for Mode 1.

In all four modes, transmission is initiated by any instruction that uses SBUF as a destination register. Reception is initiated in Mode 0 by the condition RI = 0 and REN = 1. Reception is initiated in the other modes by the incoming start bit if REN = 1.

**UART Serial Port Baud Rate Generation**
***Mode 0 Baud Rate Generation***
The baud rate in Mode 0 is fixed:

$$Mode\ 0\ Baud\ Rate = \left(Core\ Clock\ Frequency/12\right)$$

***Mode 2 Baud Rate Generation***
The baud rate in Mode 2 depends on the value of the SMOD bit in the PCON SFR. If SMOD = 0, the baud rate is 1/64 of the core clock. If SMOD = 1, the baud rate is 1/32 of the core clock:

$$Mode\ 2\ Baud\ Rate = \left(2^{SMOD}/64\right) \times \left(Core\ Clock\ Frequency\right)$$

***Mode 1 and 3 Baud Rate Generation***
The baud rates in Modes 1 and 3 are determined by the overflow rate in Timer 1 or Timer 2, or both (one for transmit and the other for receive).

**ADuC812 HARDWARE DESIGN CONSIDERATIONS**

This section outlines some of the key hardware design considerations that must be addressed when integrating the ADuC812 into any hardware system.

**Clock Oscillator**

The clock source for the ADuC812 can come either from an external source or from the internal clock oscillator. To use the internal clock oscillator, connect a parallel resonant crystal between Pins 32 and 33, and connect a capacitor from each pin to ground as shown below.

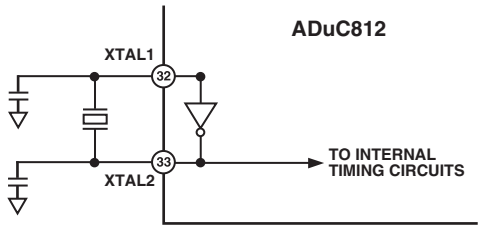



*Figure 35. External Parallel Resonant Crystal Connections*

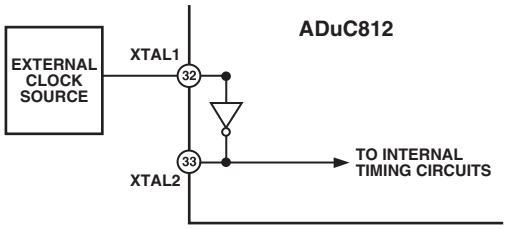



*Figure 36. Connecting an External Clock Source*

Whether using the internal oscillator or an external clock source, the ADuC812's specified operational clock speed range is 300 kHz to 16 MHz. The core is static, and will function all the way down to dc. But at clock speeds slower that 400 kHz the ADC will no longer function correctly. Therefore, to ensure specified operation, use a clock frequency of at least 400 kHz and no more than 16 MHz.

**External Memory Interface**

In addition to its internal program and data memories, the ADuC812 can access up to 64 K bytes of external program memory (ROM, PROM, etc.) and up to 16 M bytes of external data memory (SRAM).

To select from which code space (internal or external program memory) to begin executing instructions, tie the $\overline{EA}$ (external access) pin high or low, respectively. When $\overline{EA}$ is high (pulled up to $V_{DD}$), user program execution will start at address 0 of the internal 8 K bytes Flash/EE code space. When $\overline{EA}$ is low (tied to ground) user program execution will start at address 0 of the external code space. In either case, addresses above 1FFFH (8K) are mapped to the external space.

Note that a second very important function of the $\overline{EA}$ pin is described in the Single Pin Emulation Mode section.

External program memory (if used) must be connected to the ADuC812 as illustrated in Figure 37. Note that 16 I/O lines (Ports 0 and 2) are dedicated to bus functions during external program memory fetches. Port 0 (P0) serves as a multiplexed address/data bus. It emits the low byte of the program counter (PCL) as an address, and then goes into a float state awaiting the arrival of the code byte from the program memory. During the time that the low byte of the program counter is valid on P0, the signal ALE (Address Latch Enable) clocks this byte into an address latch. Meanwhile, Port 2 (P2) emits the high byte of the program counter (PCH), then $\overline{PSEN}$ strobes the EPROM and the code byte is read into the ADuC812.

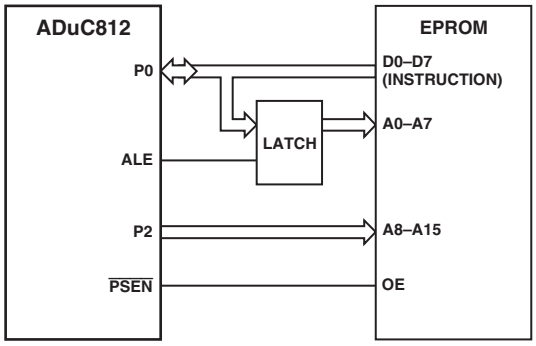



*Figure 37. External Program Memory Interface*

Note that program memory addresses are always 16 bits wide, even in cases where the actual amount of program memory used is less than 64 K bytes. External program execution sacrifices two of the 8-bit ports (P0 and P2) to the function of addressing the program memory. While executing from external program memory, Ports 0 and 2 can be used simultaneously for read/write access to external data memory, but not for general-purpose I/O.

Though both external program memory and external data memory are accessed by some of the same pins, the two are completely independent of each other from a software point of view. For example, the chip can read/write external data memory while executing from external program memory.

Figure 38 shows a hardware configuration for accessing up to 64 K bytes of external RAM. This interface is standard to any 8051 compatible MCU.

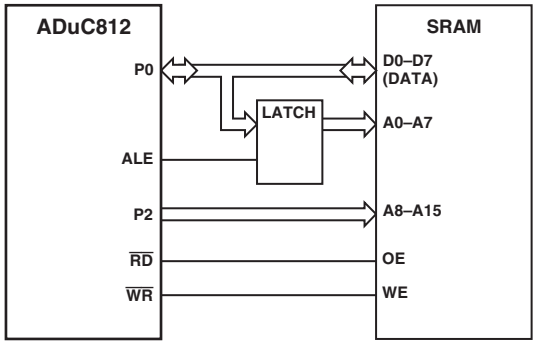



*Figure 38. External Data Memory Interface (64K Address Space)*

As an alternative to providing two separate power supplies, the user can help keep $AV_{DD}$ quiet by placing a small series resistor and/or ferrite bead between it and $DV_{DD}$, and then decoupling $AV_{DD}$ separately to ground. An example of this configuration is shown in Figure 44. With this configuration, other analog circuitry (such as op amps, voltage reference, and so on) can be powered from the $AV_{DD}$ supply line as well. The user will still want to include back-to-back Schottky diodes between $AV_{DD}$ and $DV_{DD}$ in order to protect from power-up and power-down transient conditions that could separate the two supply voltages momentarily.

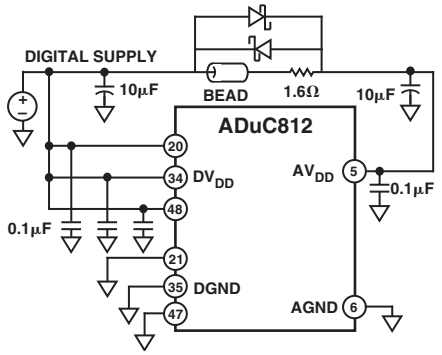



*Figure 44. External Single-Supply Connections*

Notice that in both Figure 43 and Figure 44, a large value (10 µF) reservoir capacitor sits on $DV_{DD}$ and a separate 10 µF capacitor sits on $AV_{DD}$. Also, local small value (0.1 µF) capacitors are located at each $V_{DD}$ pin of the chip. As per standard design practice, be sure to include all of these capacitors, and ensure the smaller capacitors are close to each $AV_{DD}$ pin with trace lengths as short as possible. Connect the ground terminal of each of these capacitors directly to the underlying ground plane. Finally, it should also be noted that, at all times, the analog and digital ground pins on the ADuC812 must be referenced to the same system ground reference point.

**Power Consumption**

The currents consumed by the various sections of the ADuC812 are shown in Table XXVII. The CORE values given represent the current drawn by $DV_{DD}$, while the rest (ADC, DAC, Voltage Reference) are pulled by the $AV_{DD}$ pin and can be disabled in software when not in use. The other on-chip peripherals (watchdog timer, power supply monitor, and so on) consume negligible current and are therefore lumped in with the CORE operating current here. Of course, the user must add any currents sourced by the DAC or the parallel and serial I/O pins, in order to determine the total current needed at the ADuC812's supply pins. Also, current drawn from the $DV_{DD}$ supply will increase by approximately 10 mA during Flash/EE erase and program cycles.

**Table XXVII. Typical $I_{DD}$ of Core and Peripherals**

| | $V_{DD}$ = 5 V | $V_{DD}$ = 3 V |
|---|---|---|
| CORE (Normal Mode) | (1.6 nAs × MCLK) + 6 mA | (0.8 nAs × MCLK) + 3 mA |
| CORE (Idle Mode) | (0.75 nAs × MCLK) + 5 mA | (0.25 nAs × MCLK) + 3 mA |
| ADC | 1.3 mA | 1.0 mA |
| DAC (Each) | 250 µA | 200 µA |
| Voltage Ref | 200 µA | 150 µA |

Since operating $DV_{DD}$ current is primarily a function of clock speed, the expressions for CORE supply current in Table XXVII are given as functions of MCLK, the oscillator frequency. Plug in a value for MCLK in hertz to determine the current consumed by the core at that oscillator frequency. Since the ADC and DACs can be enabled or disabled in software, add only the currents from the peripherals you expect to use. The internal voltage reference is automatically enabled whenever either the ADC or at least one DAC is enabled. And again, do not forget to include current sourced by I/O pins, serial port pins, DAC outputs, and so forth, plus the additional current drawn during Flash/EE erase and program cycles.

A software switch allows the chip to be switched from normal mode into idle mode, and also into full power-down mode. Below are brief descriptions of power-down and idle modes.

In idle mode, the oscillator continues to run but is gated off to the core only. The on-chip peripherals continue to receive the clock, and remain functional. Port pins and DAC output pins retain their states in this mode. The chip will recover from idle mode upon receiving any enabled interrupt, or upon receiving a hardware reset.

In full power-down mode, the on-chip oscillator stops, and all on-chip peripherals are shut down. Port pins retain their logic levels in this mode, but the DAC output goes to a high impedance state (three-state). The chip will only recover from power-down mode upon receiving a hardware reset or when power is cycled. During full power-down mode, the ADuC812 consumes a total of approximately 5 µA.

| Parameter | | 12 MHz Min | 12 MHz Max | Variable Clock Min | Variable Clock Max | Unit |
|---|---|---|---|---|---|---|
| EXTERNAL DATA MEMORY READ CYCLE | | | | | | |
| $t_{RLRH}$ | $\overline{RD}$ Pulsewidth | 400 | | $6t_{CK} - 100$ | | ns |
| $t_{AVLL}$ | Address Valid after ALE Low | 43 | | $t_{CK} - 40$ | | ns |
| $t_{LLAX}$ | Address Hold after ALE Low | 48 | | $t_{CK} - 35$ | | ns |
| $t_{RLDV}$ | $\overline{RD}$ Low to Valid Data In | | 252 | | $5t_{CK} - 165$ | ns |
| $t_{RHDX}$ | Data and Address Hold after $\overline{RD}$ | 0 | | 0 | | ns |
| $t_{RHDZ}$ | Data Float after $\overline{RD}$ | | 97 | | $2t_{CK} - 70$ | ns |
| $t_{LLDV}$ | ALE Low to Valid Data In | | 517 | | $8t_{CK} - 150$ | ns |
| $t_{AVDV}$ | Address to Valid Data In | | 585 | | $9t_{CK} - 165$ | ns |
| $t_{LLWL}$ | ALE Low to $\overline{RD}$ or $\overline{WR}$ Low | 200 | 300 | $3t_{CK} - 50$ | $3t_{CK} + 50$ | ns |
| $t_{AVWL}$ | Address Valid to $\overline{RD}$ or $\overline{WR}$ Low | 203 | | $4t_{CK} - 130$ | | ns |
| $t_{RLAZ}$ | $\overline{RD}$ Low to Address Float | | 0 | | 0 | ns |
| $t_{WHLH}$ | $\overline{RD}$ or $\overline{WR}$ High to ALE High | 43 | 123 | $t_{CK} - 40$ | $6t_{CK} - 100$ | ns |

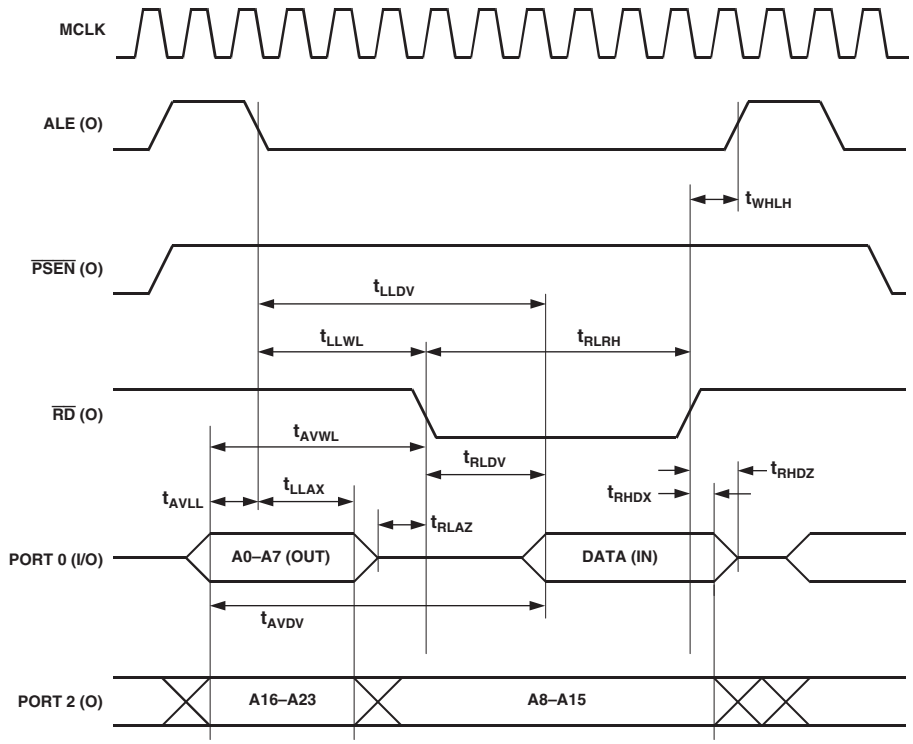



*Figure 52. External Data Memory Read Cycle*

| Parameter | | 12 MHz Min | 12 MHz Max | Variable Clock Min | Variable Clock Max | Unit |
|---|---|---|---|---|---|---|
| EXTERNAL DATA MEMORY WRITE CYCLE | | | | | | |
| $t_{WLWH}$ | $\overline{WR}$ Pulsewidth | 400 | | $6t_{CK} - 100$ | | ns |
| $t_{AVLL}$ | Address Valid after ALE Low | 43 | | $t_{CK} - 40$ | | ns |
| $t_{LLAX}$ | Address Hold after ALE Low | 48 | | $t_{CK} - 35$ | | ns |
| $t_{LLWL}$ | ALE Low to $\overline{RD}$ or $\overline{WR}$ Low | 200 | 300 | $3t_{CK} - 50$ | $3t_{CK} + 50$ | ns |
| $t_{AVWL}$ | Address Valid to $\overline{RD}$ or $\overline{WR}$ Low | 203 | | $4t_{CK} - 130$ | | ns |
| $t_{QVWX}$ | Data Valid to $\overline{WR}$ Transition | 33 | | $t_{CK} - 50$ | | ns |
| $t_{QVWH}$ | Data Setup before $\overline{WR}$ | 433 | | $7t_{CK} - 150$ | | ns |
| $t_{WHQX}$ | Data and Address Hold after $\overline{WR}$ | 33 | | $t_{CK} - 50$ | | ns |
| $t_{WHLH}$ | $\overline{RD}$ or $\overline{WR}$ High to ALE High | 43 | 123 | $t_{CK} - 40$ | $6t_{CK} - 100$ | ns |

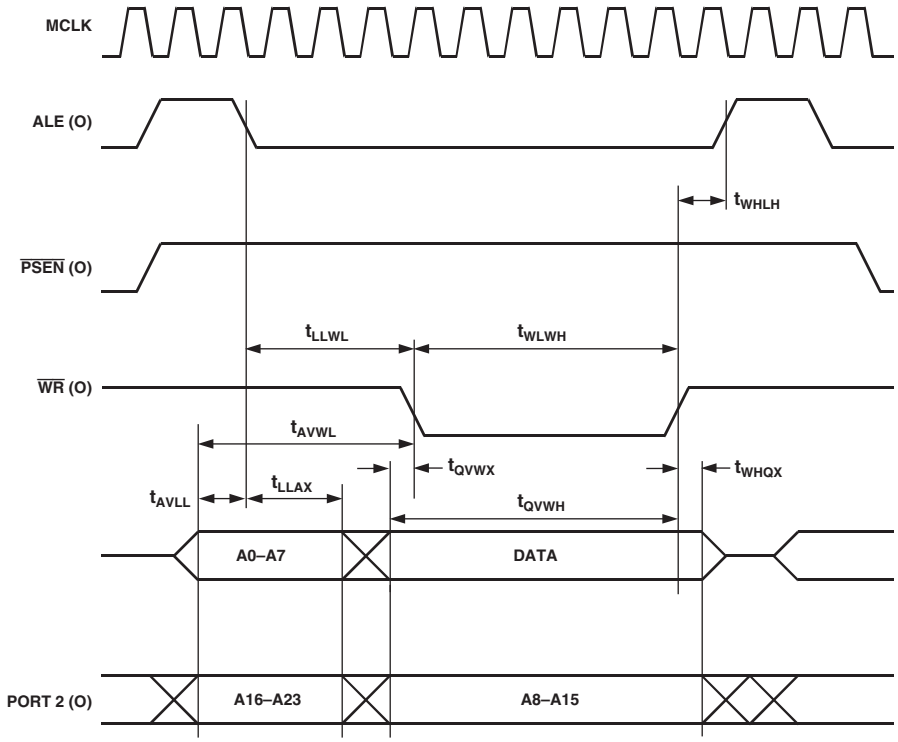



*Figure 53. External Data Memory Write Cycle*

| Parameter | | 12 MHz Min | 12 MHz Typ | 12 MHz Max | Variable Clock Min | Variable Clock Typ | Variable Clock Max | Unit |
|---|---|---|---|---|---|---|---|---|
| UART TIMING (Shift Register Mode) | | | | | | | | |
| $t_{XLXL}$ | Serial Port Clock Cycle Time | | 1.0 | | | $12t_{CK}$ | | μs |
| $t_{QVXH}$ | Output Data Setup to Clock | 700 | | | $10t_{CK} - 133$ | | | ns |
| $t_{DVXH}$ | Input Data Setup to Clock | 300 | | | $2t_{CK} + 133$ | | | ns |
| $t_{XHDX}$ | Input Data Hold after Clock | 0 | | | 0 | | | ns |
| $t_{XHQX}$ | Output Data Hold after Clock | 50 | | | $2t_{CK} - 117$ | | | ns |

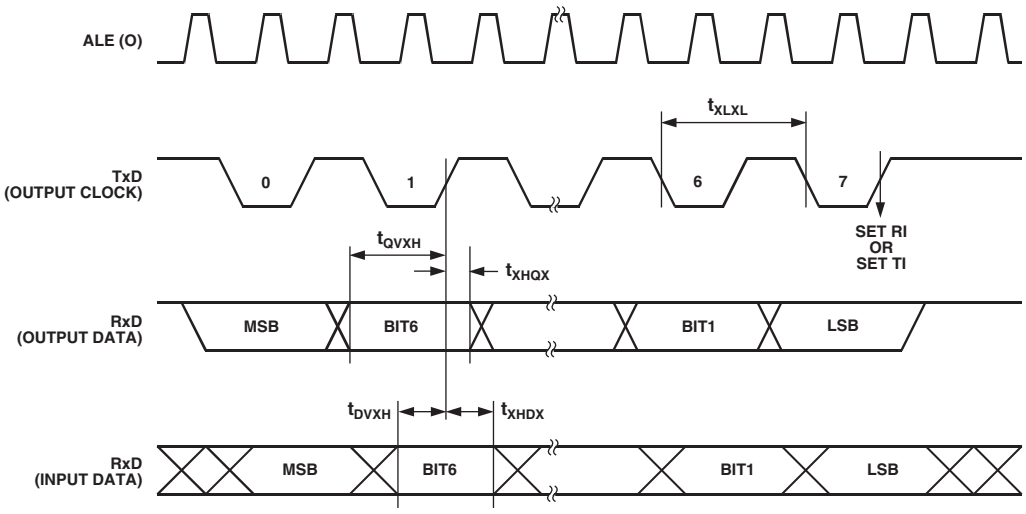
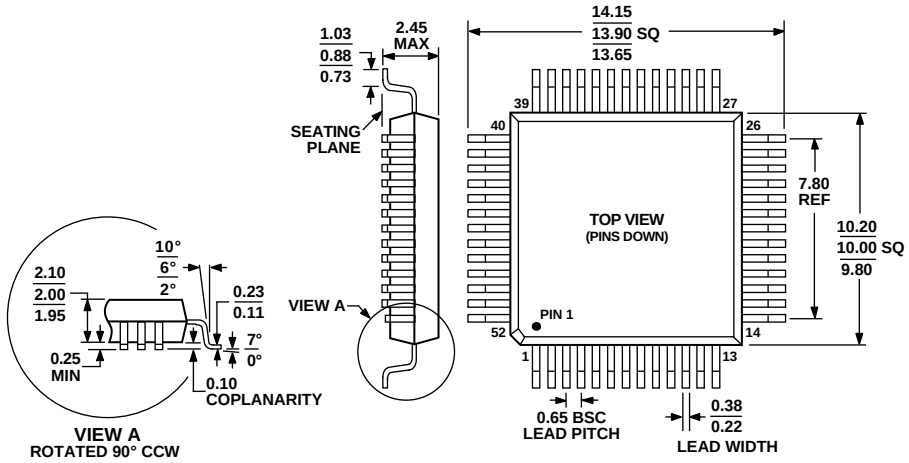


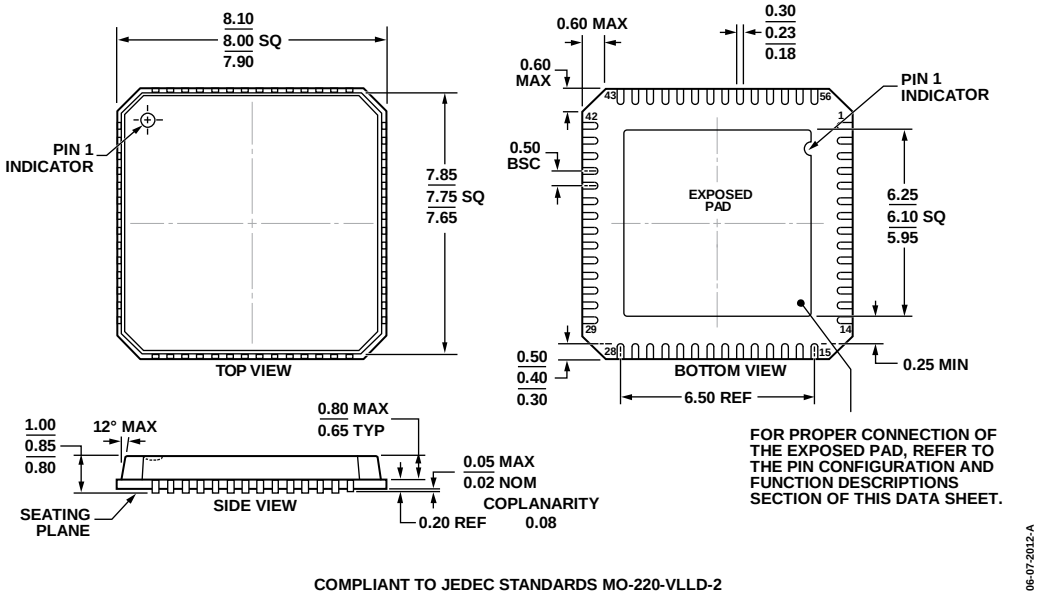

*Figure 54. UART Timing in Shift Register Mode*

# OUTLINE DIMENSIONS




COMPLIANT TO JEDEC STANDARDS MO-112-AC-1

*Figure 60. 52-Lead Metric Quad Flat Package [MQFP]*
*(S-52-2)*
*Dimensions shown in millimeters*




COMPLIANT TO JEDEC STANDARDS MO-220-VLLD-2

*Figure 61. 56-Lead Lead Frame Chip Scale Package [LFCSP_VQ]*
*8 x 8 mm Body, Very Thin Quad*
*(CP-56-1)*
*Dimensions shown in millimeters*

## ORDERING GUIDE

| Model[1] | Temperature Range | Package Description | Package Option |
|---|---|---|---|
| ADuC812BSZ | –40°C to +85°C | 52-Lead Metric Quad Flat Package [MQFP] | S-52-2 |
| ADuC812BSZ-REEL | –40°C to +85°C | 52-Lead Metric Quad Flat Package [MQFP] | S-52-2 |
| EVAL-ADuC812QSZ | | QuickStart Development System | |

[1] Z = RoHS Compliant Part.