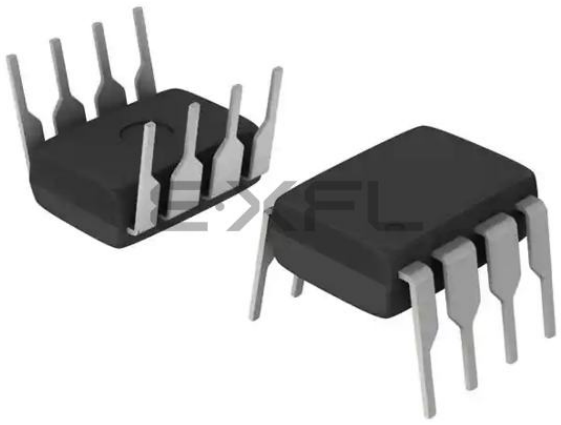

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	5
Program Memory Size	3.5KB (2K x 14)
Program Memory Type	OTP
EEPROM Size	16 x 8
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	A/D 4x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	8-DIP (0.300", 7.62mm)
Supplier Device Package	8-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic12lce674-04i-p

TABLE OF CONTENTS

Parameter	ADuC812BS V_{DD} = 5 V	ADuC812BS V_{DD} = 3 V	Unit	Test Conditions/Comments
DIGITAL OUTPUTS				
Output High Voltage (V_{OH})	2.4	2.4	V min	V_{DD} = 4.5 V to 5.5 V I_{SOURCE} = 80 μA
	4.0	2.6	V typ	V_{DD} = 2.7 V to 3.3 V I_{SOURCE} = 20 μA
Output Low Voltage (V_{OL})				
ALE, $\overline{PSEN}$, Ports 0 and 2	0.4	0.4	V max	I_{SINK} = 1.6 mA
	0.2	0.2	V typ	I_{SINK} = 1.6 mA
Port 3	0.4	0.4	V max	I_{SINK} = 8 mA
	0.2	0.2	V typ	I_{SINK} = 8 mA
Floating State Leakage Current	±10	±10	μA max	
	±1	±1	μA typ	
Floating State Output Capacitance	10	10	pF typ	
POWER REQUIREMENTS[14, 15, 16]				
I_{DD} Normal Mode[17]	43	25	mA max	MCLKIN = 16 MHz
	32	16	mA typ	MCLKIN = 16 MHz
	26	12	mA typ	MCLKIN = 12 MHz
	8	3	mA typ	MCLKIN = 1 MHz
I_{DD} Idle Mode	25	10	mA max	MCLKIN = 16 MHz
	18	6	mA typ	MCLKIN = 16 MHz
	15	6	mA typ	MCLKIN = 12 MHz
	7	2	mA typ	MCLKIN = 1 MHz
I_{DD} Power-Down Mode[18]	30	15	μA max	
	5	5	μA typ	

NOTES

[1]Specifications apply after calibration.

[2]Temperature range –40°C to +85°C.

[3]Linearity is guaranteed during normal MicroConverter core operation.

[4]Linearity may degrade when programming or erasing the 640 byte Flash/EE space during ADC conversion times due to on-chip charge pump activity.

[5]Measured in production at V_{DD} = 5 V after Software Calibration Routine at 25°C only.

[6]User may need to execute Software Calibration Routine to achieve these specifications, which are configuration dependent.

[7]The offset and gain calibration spans are defined as the voltage range of user system offset and gain errors that the ADuC812 can compensate.

[8]SNR calculation includes distortion and noise components.

[9]Specification is not production tested, but is supported by characterization data at initial product release.

[10]The temperature sensor will give a measure of the die temperature directly; air temperature can be inferred from this result.

[11]DAC linearity is calculated using:
Reduced code range of 48 to 4095, 0 to V_{REF} range
Reduced code range of 48 to 3995, 0 to V_{DD} range
DAC output load = 10 kΩ and 50 pF.

[12]Flash/EE Memory Performance Specifications are qualified as per JEDEC Specification (Data Retention) and JEDEC Draft Specification A117 (Endurance).

[13]Endurance Cycling is evaluated under the following conditions:
Mode = Byte Programming, Page Erase Cycling
Cycle Pattern = 00H to FFH
Erase Time = 20 ms
Program Time = 100 μs

[14]I_{DD} at other MCLKIN frequencies is typically given by:
Normal Mode (V_{DD} = 5 V): I_{DD} = (1.6 nAs × MCLKIN) + 6 mA
Normal Mode (V_{DD} = 3 V): I_{DD} = (0.8 nAs × MCLKIN) + 3 mA
Idle Mode (V_{DD} = 5 V): I_{DD} = (0.75 nAs × MCLKIN) + 6 mA
Idle Mode (V_{DD} = 3 V): I_{DD} = (0.25 nAs × MCLKIN) + 3 mA
where MCLKIN is the oscillator frequency in MHz and resultant I_{DD} values are in mA.

[15]I_{DD} currents are expressed as a summation of analog and digital power supply currents during normal MicroConverter operation.

[16]I_{DD} is not measured during Flash/EE program or erase cycles; I_{DD} will typically increase by 10 mA during these cycles.

[17]Analog I_{DD} = 2 mA (typ) in normal operation (internal V_{REF}, ADC, and DAC peripherals powered on).

[18]EA = Port0 = DV_{DD}, XTAL1 (Input) tied to DV_{DD}, during this measurement.

Typical specifications are not production tested, but are supported by characterization data at initial product release.

Timing Specifications—See Pages 46–55.

Specifications subject to change without notice.
Please refer to User Guide, Quick Reference Guide, Application Notes, and Silicon Errata Sheet at www.analog.com/microconverter for additional information.

PIN FUNCTION DESCRIPTIONS (continued)

Mnemonic	Type	Function
$\overline{\text{PSEN}}$	O	Program Store Enable, Logic Output. This output is a control signal that enables the external program memory to the bus during external fetch operations. It is active every six oscillator periods except during external data memory accesses. This pin remains high during internal program execution. $\overline{\text{PSEN}}$ can also be used to enable serial download mode when pulled low through a resistor on power-up or RESET.
ALE	O	Address Latch Enable, Logic Output. This output is used to latch the low byte (and page byte for 24-bit address space accesses) of the address into external memory during normal operation. It is activated every six oscillator periods except during an external data memory access.
$\overline{\text{EA}}$	I	External Access Enable, Logic Input. When held high, this input enables the device to fetch code from internal program memory locations 0000H to 1FFFH. When held low, this input enables the device to fetch all instructions from external program memory.
P0.7–P0.0 (A0–A7)	I/O	Port 0 is an 8-bit open-drain bidirectional I/O port. Port 0 pins that have 1s written to them float and in that state can be used as high impedance inputs. Port 0 is also the multiplexed low order address and data bus during accesses to external program or data memory. In this application, it uses strong internal pull-ups when emitting 1s.
EP		Exposed Pad. For the LFCSP, the exposed pad must be soldered and left unconnected.

TERMINOLOGY

ADC SPECIFICATIONS

Integral Nonlinearity

This is the maximum deviation of any code from a straight line passing through the endpoints of the ADC transfer function. The endpoints of the transfer function are zero scale, a point 1/2 LSB below the first code transition, and full scale, a point 1/2 LSB above the last code transition.

Differential Nonlinearity

This is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Offset Error

This is the deviation of the first code transition (0000 . . . 000) to (0000 . . . 001) from the ideal, i.e., +1/2 LSB.

Full-Scale Error

This is the deviation of the last code transition from the ideal AIN voltage (Full Scale – 1.5 LSB) after the offset error has been adjusted out.

Signal-to-(Noise + Distortion) Ratio

This is the measured ratio of signal-to-(noise + distortion) at the output of the ADC. The signal is the rms amplitude of the fundamental. Noise is the rms sum of all nonfundamental signals up to half the sampling frequency ($f_S/2$), excluding dc. The ratio is dependent upon the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal-to-(noise + distortion) ratio for an ideal N-bit converter with a sine wave input is given by:

$$\textit{Signal-to-(Noise + Distortion)} = (6.02N + 1.76)\ dB$$

Thus for a 12-bit converter, this is 74 dB.

Total Harmonic Distortion

Total Harmonic Distortion is the ratio of the rms sum of the harmonics to the fundamental.

DAC SPECIFICATIONS

Relative Accuracy

Relative accuracy or endpoint linearity is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for zero-scale error and full-scale error.

Voltage Output Settling Time

This is the amount of time it takes for the output to settle to a specified level for a full-scale input change.

Digital-to-Analog Glitch Impulse

This is the amount of charge injected into the analog output when the inputs change state. It is specified as the area of the glitch in nV sec.

OVERVIEW OF MCU-RELATED SFRs

Accumulator SFR

ACC is the Accumulator register and is used for math operations including addition, subtraction, integer multiplication and division, and Boolean bit manipulations. The mnemonics for accumulator-specific instructions refer to the Accumulator as A.

B SFR

The B register is used with the ACC for multiplication and division operations. For other instructions, it can be treated as a general-purpose scratch pad register.

Stack Pointer SFR

The SP register is the stack pointer and is used to hold an internal RAM address that is called the "top of the stack." The SP register is incremented before data is stored during PUSH and CALL executions. While the stack may reside anywhere in on-chip RAM, the SP register is initialized to 07H after a reset. This causes the stack to begin at location 08H.

Data Pointer

The Data Pointer is made up of three 8-bit registers: DPP (page byte), DPH (high byte), and DPL (low byte). These are used to provide memory addresses for internal and external code access and external data access. It may be manipulated as a 16-bit register (DPTR = DPH, DPL), although INC DPTR instructions will automatically carry over to DPP, or as three independent 8-bit registers (DPP, DPH, and DPL).

Program Status Word SFR

The PSW register is the Program Status Word that contains several bits reflecting the current status of the CPU as detailed in Table I.

SFR Address	D0H
Power-On Default Value	00H
Bit Addressable	Yes

CY	AC	F0	RS1	RS0	OV	F1	P

Table I. PSW SFR Bit Designations

Bit	Name	Description
7	CY	Carry Flag
6	AC	Auxiliary Carry Flag
5	F0	General-Purpose Flag
4	RS1	Register Bank Select Bits
3	RS0	RS1 RS0 Selected Bank 0 0 0 0 1 1 1 0 2 1 1 3
2	OV	Overflow Flag
1	F1	General-Purpose Flag
0	P	Parity Bit

Power Control SFR

The Power Control (PCON) register contains bits for power saving options and general-purpose status flags as shown in Table II.

SFR Address	87H
Power-On Default Value	00H
Bit Addressable	No

SMOD	———	———	ALEOFF	GF1	GF0	PD	IDL

Table II. PCON SFR Bit Designations

Bit	Name	Description
7	SMOD	Double UART Baud Rate
6	———	Reserved
5	———	Reserved
4	ALEOFF	Disable ALE Output
3	GF1	General-Purpose Flag Bit
2	GF0	General-Purpose Flag Bit
1	PD	Power-Down Mode Enable
0	IDL	Idle Mode Enable

ADCCON1—(ADC Control SFR #1)

The ADCCON1 register controls conversion and acquisition times, hardware conversion modes and power-down modes as detailed below.

SFR Address EFH
SFR Power-On Default Value 20H

MD1	MD0	CK1	CK0	AQ1	AQ0	T2C	EXC

Table III. ADCCON1 SFR Bit Designations

Bit	Name	Description
ADCCON1.7 ADCCON1.6	MD1 MD0	The mode bits (MD1, MD0) select the active operating mode of the ADC as follows: MD1 MD0 Active Mode 0 0 ADC powered down 0 1 ADC normal mode 1 0 ADC powered down if not executing a conversion cycle 1 1 ADC standby if not executing a conversion cycle Note: In power-down mode the ADC V_{REF} circuits are maintained on, whereas all ADC peripherals are powered down, thus minimizing current consumption.
ADCCON1.5 ADCCON1.4	CK1 CK0	The ADC clock divide bits (CK1, CK0) select the divide ratio for the master clock used to generate the ADC clock. A typical ADC conversion will require 17 ADC clocks. The divider ratio is selected as follows: CK1 CK0 MCLK Divider 0 0 1 0 1 2 1 0 4 1 1 8
ADCCON1.3 ADCCON1.2	AQ1 AQ0	The ADC acquisition select bits (AQ1, AQ0) select the time provided for the input track-and-hold amplifier to acquire the input signal, and are selected as follows: AQ1 AQ0 #ADC Clks 0 0 1 0 1 2 1 0 4 1 1 8
ADCCON1.1	T2C	The Timer 2 conversion bit (T2C) is set by the user to enable the Timer 2 overflow bit be used as the ADC convert start trigger input. ADC conversions are initiated on the second Timer 2 overflow.
ADCCON1.0	EXC	The external trigger enable bit (EXC) is set by the user to allow the external CONVST pin to be used as the active low convert start input. This input should be an active low pulse (minimum pulsewidth >100 ns) at the required sample rate.

and the gain calibration coefficient is divided into ADCGAINH (six bits) and ADCGAINL (eight bits). The offset calibration coefficient compensates for dc offset errors in both the ADC and the input signal.

Increasing the offset coefficient compensates for positive offset, and effectively pushes the ADC transfer function DOWN. Decreasing the offset coefficient compensates for negative offset, and effectively pushes the ADC transfer function UP. The maximum offset that can be compensated is typically ±5% of V_{REF}, which equates to typically ±125 mV with a 2.5 V reference.

Similarly, the gain calibration coefficient compensates for dc gain errors in both the ADC and the input signal.

Increasing the gain coefficient compensates for a smaller analog input signal range and scales the ADC transfer function UP, effectively increasing the slope of the transfer function. Decreasing the gain coefficient compensates for a larger analog input signal range and scales the ADC transfer function DOWN, effectively decreasing the slope of the transfer function. The maximum analog input signal range for which the gain coefficient can compensate is $1.025 \times V_{REF}$, and the minimum input range is $0.975 \times V_{REF}$, which equates to ±2.5% of the reference voltage.

Calibration

Each ADuC812 is calibrated in the factory prior to shipping, and the offset and gain calibration coefficients are stored in a hidden area of FLASH/EE memory. Each time the ADuC812 powers up, an internal power-on configuration routine copies these coefficients into the offset and gain calibration registers in the SFR area.

The MicroConverter ADC accuracy may vary from system to system due to board layout, grounding, clock speed, and so on. To get the best ADC accuracy in your system, perform the software calibration routine described in Application Note uC005, available from the MicroConverter homepage at www.analog.com/microconverter.

NONVOLATILE FLASH MEMORY

Flash Memory Overview

The ADuC812 incorporates Flash memory technology on-chip to provide the user with a nonvolatile, in-circuit reprogrammable code and data memory space.

Flash/EE memory is a relatively new type of nonvolatile memory technology based on a single transistor cell architecture.

This technology is basically an outgrowth of EPROM technology and was developed in the late 1980s. Flash/EE memory takes the flexible in-circuit reprogrammable features of EEPROM and combines them with the space efficient/density features of EPROM (see Figure 14).

Because Flash/EE technology is based on a single transistor cell architecture, a Flash memory array, like EPROM, can be implemented to achieve the space efficiencies or memory densities required by a given design.

Like EEPROM, Flash memory can be programmed in-system at a byte level, although it must first be erased in page blocks. Thus, Flash memory is often and more correctly referred to as Flash/EE memory.

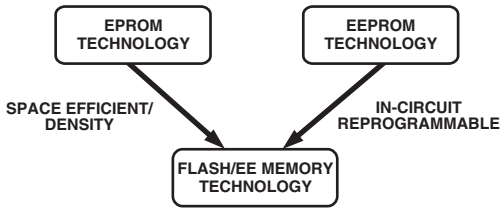

Figure 14. Flash Memory Development

Overall, Flash/EE memory represents a step closer to the ideal memory device that includes nonvolatility, in-circuit programmability, high density, and low cost. Incorporated in the ADuC812, Flash/EE memory technology allows the user to update program code space in-circuit without replacing one-time programmable (OTP) devices at remote operating nodes.

Flash/EE Memory and the ADuC812

The ADuC812 provides two arrays of Flash/EE memory for user applications. 8K bytes of Flash/EE program space are provided on-chip to facilitate code execution without any external discrete ROM device requirements. The program memory can be programmed using conventional third party memory programmers. This array can also be programmed in-circuit, using the serial download mode provided.

A 640 byte Flash/EE data memory space is also provided on-chip as a general-purpose nonvolatile scratchpad area. User access to this area is via a group of six SFRs.

ADuC812 Flash/EE Memory Reliability

The Flash/EE program and data memory arrays on the ADuC812 are fully qualified for two key Flash/EE memory characteristics: Flash/EE Memory Cycling Endurance and Flash/EE Memory Data Retention.

Endurance quantifies the ability of the Flash/EE memory to be cycled through many program, read, and erase cycles. In real terms, a single endurance cycle is composed of four independent sequential events:

a. Initial Page Erase Sequence
b. Read/Verify Sequence
c. Byte Program Sequence
d. Second Read/Verify Sequence

In reliability qualification, every byte in the program and data Flash/EE memory is cycled from 00H to FFH until the first fail is recorded, signifying the endurance limit of the on-chip Flash/EE memory.

As indicated in the Specification tables, the ADuC812 Flash/EE Memory Endurance qualification has been carried out in accordance with JEDEC Specification A117 over the industrial temperature ranges of –40°C, +25°C, and +85°C. The results allow the specification of a minimum endurance figure over supply and temperature of 10,000 cycles, with an endurance figure of 50,000 cycles being typical of operation at 25°C.

Retention quantifies the ability of the Flash/EE memory to retain its programmed data over time. Again, the ADuC812 has been qualified in accordance with the formal JEDEC Retention Lifetime Specification (A117) at a specific junction temperature (T_J = 55°C). As part of this qualification procedure, the Flash/EE memory is cycled to its specified endurance limit described above, before data retention is characterized. This means that the Flash/EE memory is guaranteed to retain its data for its full specified retention lifetime every time the Flash/EE memory is reprogrammed.

ECON—Flash/EE Memory Control SFR
This SFR acts as a command interpreter and may be written with one of five command modes to enable various read, program, and erase cycles as detailed in Table VII.

Table VII. ECON—Flash/EE Memory Control Register Command Modes

Command Byte	Command Mode
01H	READ COMMAND Results in four bytes being read into EDATA1–4 from memory page address contained in EADRL.
02H	PROGRAM COMMAND Results in four bytes (EDATA1–4) being written to memory page address in EADRL. This write command assumes the designated "write" page has been pre-erased.
03H	RESERVED FOR INTERNAL USE 03H should not be written to the ECON SFR.
04H	VERIFY COMMAND Allows the user to verify if data in EDATA1–4 is contained in page address designated by EADRL. A subsequent read of the ECON SFR will result in a zero being read if the verification is valid; a nonzero value will be read to indicate an invalid verification.
05H	ERASE COMMAND Results in an erase of the 4-byte page designated in EADRL.
06H	ERASE-ALL COMMAND Results in erase of the full Flash/EE data memory 160-page (640 bytes) array.
07H to FFH	RESERVED COMMANDS Commands reserved for future use.

Flash/EE Memory Timing
The typical program/erase times for the Flash/EE data memory are:

Erase Full Array (640 Bytes) – 20 ms
Erase Single Page (4 Bytes) – 20 ms
Program Page (4 Bytes) – 250 μs
Read Page (4 Bytes) – Within Single Instruction Cycle

Flash/EE erase and program timing is derived from the master clock. When using a master clock frequency of 11.0592 MHz, it is not necessary to write to the ETIM registers at all. However, when operating at other master clock frequencies (f_{CLK}), you must change the values of ETIM1 and ETIM2 to avoid degrading data Flash/EE endurance and retention. ETIM1 and ETIM2 form a 16-bit word, ETIM2 being the high byte and ETIM1 the low byte. The value of this 16-bit word must be set as follows to ensure optimum data Flash/EE endurance and retention.

$$ETIM2, ETIM1 = 100\ \mu s \times f_{CLK}$$

ETIM3 should always remain at its default value of 201 dec/C9 hex.

Using the Flash/EE Memory Interface
As with all Flash/EE memory architectures, the array can be programmed in system at a byte level, although it must be erased first, the erasure being performed in page blocks (4-byte pages in this case).

A typical access to the Flash/EE array will involve setting up the page address to be accessed in the EADRL SFR, configuring the EDATA1–4 with data to be programmed to the array (the EDATA SFRs will not be written for read accesses), and finally writing the ECON command word that initiates one of the six modes shown in Table VII. It should be noted that a given mode of operation is initiated as soon as the command word is written to the ECON SFR. The core microcontroller operation on the ADuC812 is idled until the requested Program/Read or Erase mode is completed.

In practice, this means that even though the Flash/EE memory mode of operation is typically initiated with a two-machine cycle MOV instruction (to write to the ECON SFR), the next instruction will not be executed until the Flash/EE operation is complete (250 μs or 20 ms later). This means that the core will not respond to Interrupt requests until the Flash/EE operation is complete, although the core peripheral functions like Counter/Timers will continue to count and time as configured throughout this pseudo-idle period.

Erase-All
Although the 640-byte user Flash/EE array is shipped from the factory pre-erased, i.e., byte locations set to FFH, it is nonetheless good programming practice to include an erase-all routine as part of any configuration/setup code running on the ADuC812. An ERASE-ALL command consists of writing 06H to the ECON SFR, which initiates an erase of all 640 byte locations in the Flash/EE array. This command coded in 8051 assembly would appear as:

```
MOV ECON, #06H      ; Erase all Command
                    ; 20 ms Duration
```

Program a Byte
In general terms, a byte in the Flash/EE array can only be programmed if it has previously been erased. To be more specific, a byte can only be programmed if it already holds the value FFH. Because of the Flash/EE architecture, this erasure must happen at a page level; therefore, a minimum of four bytes (1 page) will be erased when an erase command is initiated. A more specific example of the Program-Byte process is shown below. In this example, the user writes F3H into the second byte on Page 03H of the Flash/EE data memory space while preserving the other three bytes already in this page. As the user is only required to modify one of the page bytes, the full page must be first read so that this page can then be erased without the existing data being lost. This example, coded in 8051 assembly, would appear as:

```
MOV  EADRL, #03H    ; Set Page Address Pointer
MOV  ECON, #01H     ; Read Page
MOV  EDATA2, #0F3H  ; Write New Byte
MOV  ECON, #05H     ; Erase Page
MOV  ECON, #02H     ; Write Page (Program
                      Flash/EE)
```

Using the DAC

The on-chip DAC architecture consists of a resistor string DAC followed by an output buffer amplifier, the functional equivalent of which is illustrated in Figure 18. Details of the actual DAC architecture can be found in U.S. Patent Number 5969657 (www.uspto.gov). Features of this architecture include inherent guaranteed monotonicity and excellent differential linearity.

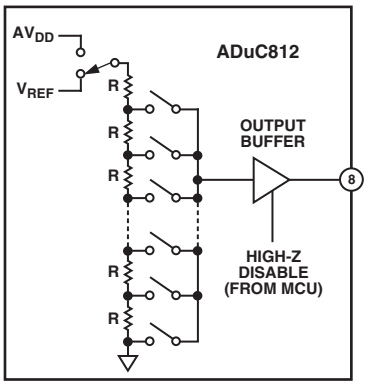

Figure 18. Resistor String DAC Functional Equivalent

As illustrated in Figure 18, the reference source for each DAC is user selectable in software. It can be either AV_{DD} or V_{REF}. In 0-to-AV_{DD} mode, the DAC output transfer function spans from 0 V to the voltage at the AV_{DD} pin. In 0-to-V_{REF} mode, the DAC output transfer function spans from 0 V to the internal V_{REF}, or if an external reference is applied, the voltage at the V_{REF} pin. The DAC output buffer amplifier features a true rail-to-rail output stage implementation. This means that unloaded, each output is capable of swinging to within less than 100 mV of both AV_{DD} and ground. Moreover, the DAC's linearity specification (when driving a 10 kΩ resistive load to ground) is guaranteed through the full transfer function *except* codes 0 to 48, and, in 0-to-AV_{DD} mode only, codes 3995 to 4095. Linearity degradation near ground and V_{DD} is caused by saturation of the output amplifier, and a general representation of its effects (neglecting offset and gain error) is illustrated in Figure 19. The dotted line in Figure 19 indicates the *ideal* transfer function, and the solid line represents what the transfer function might look like with endpoint nonlinearities due to saturation of the output amplifier. Note that Figure 19 represents a transfer function in 0-to-V_{DD} mode only. In 0-to-V_{REF} mode (with $V_{REF} < V_{DD}$) the lower nonlinearity would be similar, but the upper portion of the transfer function would follow the "ideal" line right to the end (V_{REF} in this case, not V_{DD}), showing no signs of endpoint linearity errors.

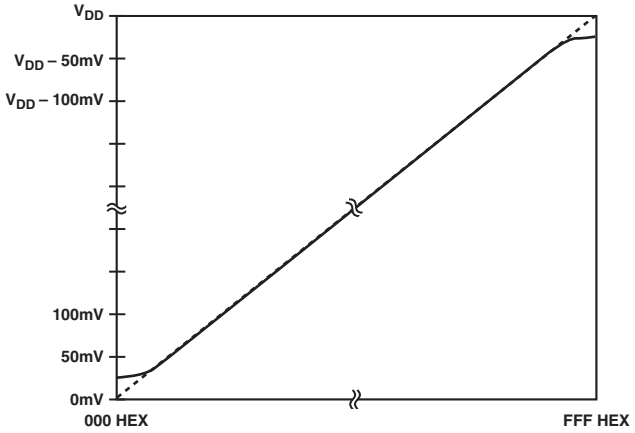

Figure 19. Endpoint Nonlinearities Due to Amplifier Saturation

The endpoint nonlinearities conceptually illustrated in Figure 19 get worse as a function of output loading. Most of the ADuC812's data sheet specifications assume a 10 kΩ resistive load to ground at the DAC output. As the output is forced to source or sink more current, the nonlinear regions at the top or bottom (respectively) of Figure 19 become larger. With larger current demands, this can significantly limit output voltage swing. Figure 20 and Figure 21 illustrate this behavior. It should be noted that the upper trace in each of these figures is only valid for an output range selection of 0-to-AV_{DD}. In 0-to-V_{REF} mode, DAC loading will not cause high-side voltage drops as long as the reference voltage remains below the upper trace in the corresponding figure. For example, if AV_{DD} = 3 V and V_{REF} = 2.5 V, the high-side voltage will not be affected by loads less than 5 mA. But somewhere around 7 mA the upper curve in Figure 21 drops below 2.5 V (V_{REF}), indicating that at these higher currents the output will not be capable of reaching V_{REF}.

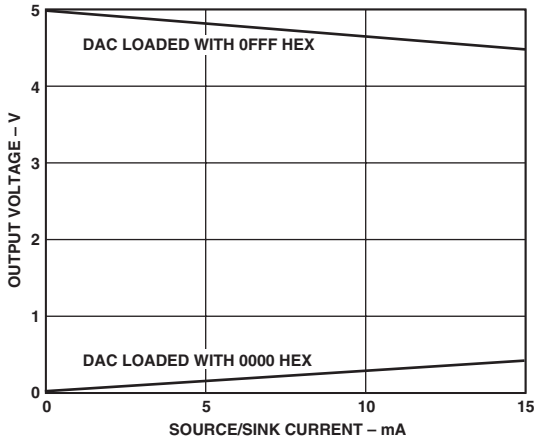

Figure 20. Source and Sink Current Capability with $V_{REF} = V_{DD} = 5$ V

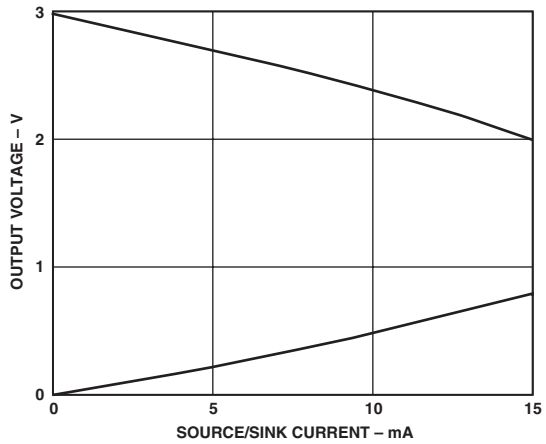

Figure 21. Source and Sink Current Capability with $V_{REF} = V_{DD} = 3$ V

To drive significant loads with the DAC outputs, external buffering may be required, as illustrated in Figure 22.

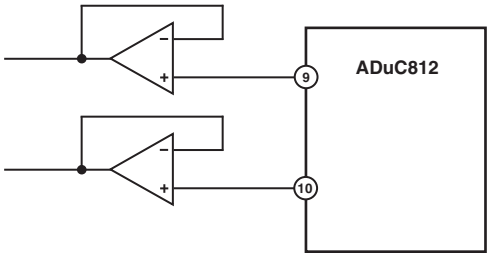

Figure 22. Buffering the DAC Outputs

The DAC output buffer also features a high impedance disable function. In the chip's default power-on state, both DACs are disabled, and their outputs are in a high impedance state (or "three-state") where they remain inactive until enabled in software. This means that if a zero output is desired during power-up or power-down transient conditions, then a pull-down resistor must be added to each DAC output. Assuming this resistor is in place, the DAC outputs will remain at ground potential whenever the DAC is disabled. However, each DAC output will still spike briefly when power is first applied to the chip, and again when each DAC is first enabled in software. Typical scope shots of these spikes are given in Figure 23 and Figure 24, respectively.

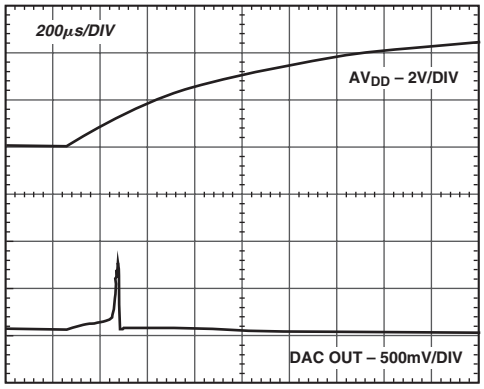

Figure 23. DAC Output Spike at Chip Power-Up

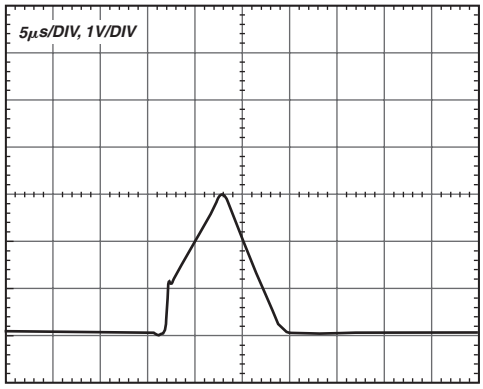

Figure 24. DAC Output Spike at DAC Enable

WATCHDOG TIMER

The purpose of the watchdog timer is to generate a device reset within a reasonable amount of time if the ADuC812 enters an erroneous state, possibly due to a programming error. The Watchdog function can be disabled by clearing the WDE (Watchdog Enable) bit in the Watchdog Control (WDCON) SFR. When enabled, the watchdog circuit will generate a system reset if the user program fails to set the watchdog timer refresh bits (WDR1, WDR2) within a predetermined amount of time (see PRE2–0 bits in WDCON). The watchdog timer itself is a 16-bit counter. The watchdog timeout interval can be adjusted via the PRE2–0 bits in WDCON. Full Control and Status of the watchdog timer function can be controlled via the watchdog timer control SFR (WDCON).

	Watchdog Timer
WDCON	**Control Register**
SFR Address	C0H
Power-On Default Value	00H
Bit Addressable	Yes

PRE2	PRE1	PRE0	—	WDR1	WDR2	WDS	WDE

Table IX. WDCON SFR Bit Designations

Bit	Name	Description
7	PRE2	Watchdog Timer Prescale Bits.
6	PRE1	
5	PRE0	PRE2 PRE1 PRE0 Timeout Period (ms) 0 0 0 16 0 0 1 32 0 1 0 64 0 1 1 128 1 0 0 256 1 0 1 512 1 1 0 1024 1 1 1 2048
4	—	Not Used.
3	WDR1	Watchdog Timer Refresh Bits. Set sequentially to refresh the watchdog timer.
2	WDR2	
1	WDS	Watchdog Status Bit. Set by the Watchdog Controller to indicate that a watchdog timeout has occurred. Cleared by writing a "0" or by an external hardware reset. It is not cleared by a watchdog reset.
0	WDE	Watchdog Enable Bit. Set by user to enable the watchdog and clear its counters.

Example

To set up the watchdog timer for a timeout period of 2048 ms, the following code would be used:

```
MOV     WDCON,#0E0h   ;2.048 second
                      ;timeout period
SETB    WDE           ;enable watchdog timer
```

To prevent the watchdog timer from timing out, the timer refresh bits need to be set before 2.048 seconds has elapsed.

```
SETB    WDR1        ;refresh watchdog timer..
SETB    WDR2        ; ..bits must be set in this
                    ;order
```

POWER SUPPLY MONITOR

As its name suggests, the Power Supply Monitor, once enabled, monitors both supplies (AV_{DD} and DV_{DD}) on the ADuC812. It will indicate when either power supply drops below one of five user selectable voltage trip points from 2.63 V to 4.63 V. For correct operation of the Power Supply Monitor function, AV_{DD} must be equal to or greater than 2.7 V. The Power Supply Monitor function is controlled via the PSMCON SFR. If enabled via the IE2 SFR, the Power Supply Monitor will interrupt the core using the PSMI bit in the PSMCON SFR. This bit will not be cleared until the failing power supply has returned above the trip point for at least 256 ms. This ensures that the power supply has fully settled before the bit is cleared. This monitor function allows the user to save working registers to avoid possible data loss due to the low supply condition, and also ensures that normal code execution will not resume until a safe supply level has been well established. The supply monitor is also protected against spurious glitches triggering the interrupt circuit.

MOSI (Master Out, Slave In Pin)
The MOSI (master out, slave in) pin is configured as an output line in master mode and an input line in slave mode. The MOSI line on the master (data out) should be connected to the MOSI line in the slave device (data in). The data is transferred as byte wide (8-bit) serial data, MSB first.

SCLOCK (Serial Clock I/O Pin)
The master serial clock (SCLOCK) is used to synchronize the data being transmitted and received through the MOSI and MISO data lines. A single data bit is transmitted and received in each SCLOCK period. Therefore, a byte is transmitted/received after eight SCLOCK periods. The SCLOCK pin is configured as an output in master mode and as an input in slave mode. In master mode, the bit rate, polarity, and phase of the clock are controlled by the CPOL, CPHA, SPR0, and SPR1 bits in the SPICON SFR (see Table XI). In slave mode, the SPICON register will have to be configured with the phase and polarity (CPHA and CPOL) of the expected input clock. In both master and slave modes, the data is transmitted on one edge of the SCLOCK signal and sampled on the other. It is important therefore that the CPHA and CPOL are configured the same for the master and slave devices.

$\overline{SS}$ (Slave Select Input Pin)
The Slave Select ($\overline{SS}$) input pin is shared with the ADC5 input. To configure this pin as a digital input, the bit must be cleared, e.g., CLR P1.5.

This line is active low. Data is only received or transmitted in slave mode when the $\overline{SS}$ pin is low, allowing the ADuC812 to be used in single master, multislave SPI configurations. If CPHA = 1, then the $\overline{SS}$ input may be permanently pulled low. With CPHA = 0, the $\overline{SS}$ input must be driven low before the first bit in a byte wide transmission or reception, and return high again after the last bit in that byte wide transmission or reception. In SPI Slave mode, the logic level on the external $\overline{SS}$ pin can be read via the SPR0 bit in the SPICON SFR. The following SFR registers are used to control the SPI interface.

SPICON	**SPI Control Register**
SFR Address	F8H
Power-On Default Value	OOH
Bit Addressable	Yes

ISPI	WCOL	SPE	SPIM	CPOL	CPHA	SPR1	SPR0

Table XI. SPICON SFR Bit Designations

Bit	Name	Description
7	ISPI	SPI Interrupt Bit. Set by MicroConverter at the end of each SPI transfer. Cleared directly by user code or indirectly by reading the SPIDAT SFR.
6	WCOL	Write Collision Error Bit. Set by MicroConverter if SPIDAT is written to while an SPI transfer is in progress. Cleared by user code.
5	SPE	SPI Interface Enable Bit. Set by user to enable the SPI interface. Cleared by user to enable I^2C interface.
4	SPIM	SPI Master/Slave Mode Select Bit. Set by user to enable Master mode operation (SCLOCK is an output). Cleared by user to enable Slave mode operation (SCLOCK is an input).
3	CPOL*	Clock Polarity Select Bit. Set by user if SCLOCK idles high. Cleared by user if SCLOCK idles low.
2	CPHA*	Clock Phase Select Bit. Set by user if leading SCLOCK edge is to transmit data. Cleared by user if trailing SCLOCK edge is to transmit data.
1	SPR1	SPI Bit Rate Select Bits.
0	SPR0	These bits select the SCLOCK rate (bit rate) in Master mode as follows: SPR1 SPR0 Selected Bit Rate 0 0 $f_{OSC}/4$ 0 1 $f_{OSC}/8$ 1 0 $f_{OSC}/32$ 1 1 $f_{OSC}/64$ In SPI Slave mode, i.e., SPIM = 0, the logic level on the external $\overline{SS}$ pin can be read via the SPR0 bit.

*The CPOL and CPHA bits should both contain the same values for master and slave devices.

I²C* COMPATIBLE INTERFACE

The ADuC812 supports a 2-wire serial interface mode that is I²C compatible. The I²C compatible interface shares its pins with the on-chip SPI interface and therefore the user can only enable one or the other interface at any given time (see SPE in Table IX). An application note describing the operation of this interface as implemented is available from the MicroConverter website at www.analog.com/microconverter. This interface can be configured as a software master or hardware slave, and uses two pins in the interface.

SDATA	Serial Data I/O Pin
SCLOCK	Serial Clock

Three SFRs are used to control the I²C compatible interface. These are described below:

I2CCON	**I²C Control Register**
SFR Address	E8H
Power-On Default Value	00H
Bit Addressable	Yes

MDO	MDE	MCO	MDI	I2CM	I2CRS	I2CTX	I2CI

Table XII. I2CCON SFR Bit Designations

Bit	Name	Description
7	MDO	I²C Software Master Data Output Bit (Master Mode Only). This data bit is used to implement a master I²C transmitter interface in software. Data written to this bit will be output on the SDATA pin if the data output enable (MDE) bit is set.
6	MDE	I²C Software Master Data Output Enable Bit (Master Mode Only). Set by the user to enable the SDATA pin as an output (Tx). Cleared by the user to enable SDATA pin as an input (Rx).
5	MCO	I²C Software Master Data Output Bit (Master Mode Only). This data bit is used to implement a master I²C transmitter interface in software. Data written to this bit will be output on the SCLOCK pin.
4	MDI	I²C Software Master Data Input Bit (Master Mode Only). This data bit is used to implement a master I²C receiver interface in software. Data on the SDATA pin is latched into this bit on SCLOCK if the Data Output Enable (MDE) = 0.
3	I2CM	I²C Master/Slave Mode Bit. Set by user to enable I²C software master mode. Cleared by user to enable I²C hardware slave mode.
2	I2CRS	I²C Reset Bit (Slave Mode Only). Set by user to reset the I²C interface. Cleared by user for normal I²C operation.
1	I2CTX	I²C Direction Transfer Bit (Slave Mode Only). Set by the MicroConverter if the interface is transmitting. Cleared by the MicroConverter if the interface is receiving.
0	I2CI	I²C Interrupt Bit (Slave Mode Only). Set by the MicroConverter after a byte has been transmitted or received. Cleared by user software.

I2CADD	**I²C Address Register**
Function	Holds the I²C peripheral address for the part. It may be overwritten by the user code. Application note uC001 at www.analog.com/microconverter describes the format of the I²C standard 7-bit address in detail.
SFR Address	9BH
Power-On Default Value	55H
Bit Addressable	No

I2CDAT	**I²C Data Register**
Function	The I2CDAT SFR is written by the user to transmit data over the I²C interface or read by user code to read data just received by the I²C interface. User software should only access I2CDAT once per interrupt cycle.
SFR Address	9AH
Power-On Default Value	00H
Bit Addressable	No

*Purchase of licensed I²C components of Analog Devices or one of its sublicensed Associated Companies conveys a license for the purchaser under the Philips I²C Patent Rights to use these components in an I²C system, provided that the system conforms to the I²C Standard Specification as defined by Philips.

8051 COMPATIBLE ON-CHIP PERIPHERALS

This section gives a brief overview of the various secondary peripheral circuits that are also available to the user on-chip. These remaining functions are fully 8051 compatible and are controlled via standard 8051 SFR bit definitions.

Parallel I/O Ports 0–3

The ADuC812 uses four input/output ports to exchange data with external devices. In addition to performing general-purpose I/O, some ports are capable of external memory operations; others are multiplexed with an alternate function for the peripheral features on the device. In general, when a peripheral is enabled, that pin may not be used as a general-purpose I/O pin.

Port 0 is an 8-bit, open-drain, bidirectional I/O port that is directly controlled via the P0 SFR (SFR address = 80H). Port 0 pins that have 1s written to them via the Port 0 SFR will be configured as open-drain and will therefore float. In that state, Port 0 pins can be used as high impedance inputs. An external pull-up resistor will be required on Port 0 outputs to force a valid logic high level externally. Port 0 is also the multiplexed low order address and data bus during accesses to external program or data memory. In this application, it uses strong internal pull-ups when emitting 1s.

Port 1 is also an 8-bit port directly controlled via the P1 SFR (SFR address = 90H). Port 1 is an input only port. Port 1 digital output capability is not supported on this device. Port 1 pins can be configured as digital inputs or analog inputs.

By (power-on) default these pins are configured as analog inputs, i.e., "1" written in the corresponding Port 1 register bit. To configure any of these pins as digital inputs, the user should write a "0" to these port bits to configure the corresponding pin as a high impedance digital input.

These pins also have various secondary functions described in Table XIII.

Table XIII. Port 1, Alternate Pin Functions

Pin	Alternate Function
P1.0	T2 (Timer/Counter 2 External Input)
P1.1	T2EX (Timer/Counter 2 Capture/Reload Trigger)
P1.5	$\overline{SS}$ (Slave Select for the SPI Interface)

Port 2 is a bidirectional port with internal pull-up resistors directly controlled via the P2 SFR (SFR address = A0H). Port 2 pins that have 1s written to them are pulled high by the internal pull-up resistors and, in that state, can be used as inputs. As inputs, Port 2 pins being pulled externally low will source current because of the internal pull-up resistors. Port 2 emits the high order address bytes during fetches from external program memory, and middle and high order address bytes during accesses to the 24-bit external data memory space.

Port 3 is a bidirectional port with internal pull-ups directly controlled via the P3 SFR (SFR address = B0H). Port 3 pins that have 1s written to them are pulled high by the internal pull-ups and, in that state, can be used as inputs. As inputs, Port 3 pins being pulled externally low will source current because of the internal pull-ups. Port 3 pins also have various secondary functions described in Table XIV.

Table XIV. Port 3, Alternate Pin Functions

Pin	Alternate Function
P3.0	RxD (UART Input Pin) (or Serial Data I/O in Mode 0)
P3.1	TxD (UART Output Pin) (or Serial Clock Output in Mode 0)
P3.2	$\overline{INT0}$ (External Interrupt 0)
P3.3	$\overline{INT1}$ (External Interrupt 1)
P3.4	T0 (Timer/Counter 0 External Input)
P3.5	T1 (Timer/Counter 1 External Input)
P3.6	$\overline{WR}$ (External Data Memory Write Strobe)
P3.7	$\overline{RD}$ (External Data Memory Read Strobe)

The alternate functions of P1.0, P1.1, P1.5, and Port 3 pins can be activated only if the corresponding bit latch in the P1 and P3 SFRs contains a 1. Otherwise, the port pin is stuck at 0.

Timers/Counters

The ADuC812 has three 16-bit Timer/Counters: Timer 0, Timer 1, and Timer 2. The Timer/Counter hardware has been included on-chip to relieve the processor core of the overhead inherent in implementing timer/counter functionality in software. Each Timer/Counter consists of two 8-bit registers, THx and TLx (x = 0, 1, and 2). All three can be configured to operate either as timers or event counters.

In Timer function, the TLx register is incremented every machine cycle. Thus, think of it as counting machine cycles. Since a machine cycle consists of 12 core clock periods, the maximum count rate is 1/12 of the core clock frequency.

In Counter function, the TLx register is incremented by a 1-to-0 transition at its corresponding external input pin, T0, T1, or T2. In this function, the external input is sampled during S5P2 of every machine cycle. When the samples show a high in one cycle and a low in the next cycle, the count is incremented. The new count value appears in the register during S3P1 of the cycle following the one in which the transition was detected. Since it takes two machine cycles (24 core clock periods) to recognize a 1-to-0 transition, the maximum count rate is 1/24 of the core clock frequency. There are no restrictions on the duty cycle of the external input signal, but to ensure that a given level is sampled at least once before it changes, it must be held for a minimum of one full machine cycle.

User configuration and control of all Timer operating modes is achieved via three SFRs:

TMOD, TCON	Control and configuration for Timers 0 and 1.
T2CON	Control and configuration for Timer 2.

TMOD — Timer/Counter 0 and 1 Mode Register

SFR Address	89H
Power-On Default Value	00H
Bit Addressable	No

Gate	C/T	M1	M0	Gate	C/T	M1	M0

Table XV. TMOD SFR Bit Designations

Bit	Name	Description
7	Gate	Timer 1 Gating Control. Set by software to enable Timer/Counter 1 only while $\overline{INT1}$ pin is high and TR1 control bit is set. Cleared by software to enable Timer 1 whenever TR1 control bit is set.
6	C/T	Timer 1 Timer or Counter Select Bit. Set by software to select counter operation (input from T1 pin). Cleared by software to select timer operation (input from internal system clock).
5	M1	Timer 1 Mode Select Bit 1 (used with M0 Bit).
4	M0	Timer 1 Mode Select Bit 0. M1 M0 0 0 TH1 operates as an 8-bit timer/counter. TL1 serves as 5-bit prescaler. 0 1 16-Bit Timer/Counter. TH1 and TL1 are cascaded; there is no prescaler. 1 0 8-Bit Autoreload Timer/Counter. TH1 holds a value that is to be reloaded into TL1 each time it overflows. 1 1 Timer/Counter 1 Stopped.
3	Gate	Timer 0 Gating Control. Set by software to enable Timer/Counter 0 only while $\overline{INT0}$ pin is high and TR0 control bit is set. Cleared by software to enable Timer 0 whenever TR0 control bit is set.
2	C/T	Timer 0 Timer or Counter Select Bit. Set by software to select counter operation (input from T0 pin). Cleared by software to select timer operation (input from internal system clock).
1	M1	Timer 0 Mode Select Bit 1.
0	M0	Timer 0 Mode Select Bit 0. M1 M0 0 0 TH0 operates as an 8-bit timer/counter. TL0 serves as 5-bit prescaler. 0 1 16-Bit Timer/Counter. TH0 and TL0 are cascaded; there is no prescaler. 1 0 8-Bit Autoreload Timer/Counter. TH0 holds a value that is to be reloaded into TL0 each time it overflows. 1 1 TL0 is an 8-bit timer/counter controlled by the standard timer 0 control bits. TH0 is an 8-bit timer only, controlled by Timer 1 control bits.

TCON	**Timer/Counter 0 and 1 Control Register**
SFR Address	88H
Power-On Default Value	00H
Bit Addressable	Yes

TF1	TR1	TF0	TR0	IE1*	IT1*	IE0*	IT0*

*These bits are not used in the control of Timer/Counter 0 and 1, but are used instead in the control and monitoring of the external $\overline{INT0}$ and $\overline{INT1}$ interrupt pins.

Table XVI. TCON SFR Bit Designations

Bit	Name	Description
7	TF1	Timer 1 Overflow Flag. Set by hardware on a Timer/Counter 1 overflow. Cleared by hardware when the Program Counter (PC) vectors to the interrupt service routine.
6	TR1	Timer 1 Run Control Bit. Set by user to turn on Timer/Counter 1. Cleared by user to turn off Timer/Counter 1.
5	TF0	Timer 0 Overflow Flag. Set by hardware on a Timer/Counter 0 overflow. Cleared by hardware when the PC vectors to the interrupt service routine.
4	TR0	Timer 0 Run Control Bit. Set by user to turn on Timer/Counter 0. Cleared by user to turn off Timer/Counter 0.
3	IE1	External Interrupt 1 ($\overline{INT1}$) Flag. Set by hardware by a falling edge or zero level being applied to external interrupt pin $\overline{INT1}$, depending on bit IT1 state. Cleared by hardware when the when the PC vectors to the interrupt service routine only if the interrupt was transition-activated. If level-activated, the external requesting source controls the request flag, rather than the on-chip hardware.
2	IT1	External Interrupt 1 (IE1) Trigger Type. Set by software to specify edge-sensitive detection (i.e., 1-to-0 transition). Cleared by software to specify level-sensitive detection (i.e., zero level).
1	IE0	External Interrupt 0 ($\overline{INT0}$) Flag. Set by hardware by a falling edge or zero level being applied to external interrupt pin $\overline{INT0}$, depending on bit IT0 state. Cleared by hardware when the PC vectors to the interrupt service routine only if the interrupt was transition activated. If level activated, the external requesting source controls the request flag, rather than the on-chip hardware.
0	IT0	External Interrupt 0 (IE0) Trigger Type. Set by software to specify edge-sensitive detection (i.e., 1-to-0 transition). Cleared by software to specify level-sensitive detection (i.e., zero level).

Timer/Counters 0 and 1 Data Registers

Each timer consists of two 8-bit registers. These can be used as independent registers or combined to be a single 16-bit register depending on the timer mode configuration.

TH0 and TL0

Timer 0 high byte and low byte.
SFR Address = 8CH, 8AH, respectively.

TH1 and TL1

Timer 1 high byte and low byte.
SFR Address = 8DH, 8BH, respectively.

Timer/Counter Operation Modes

The following paragraphs describe the operating modes for Timer/Counter 2. The operating modes are selected by bits in the T2CON SFR as shown in Table XVIII.

Table XVIII. TIMECON SFR Bit Designations

RCLK (or) TCLK	CAP2	TR2	MODE
0	0	1	16-Bit Autoreload
0	1	1	16-Bit Capture
1	X	1	Baud Rate
X	X	0	OFF

16-Bit Autoreload Mode

In Autoreload mode, there are two options, which are selected by bit EXEN2 in T2CON. If EXEN2 = 0, then when Timer 2 rolls over, it not only sets TF2 but also causes the Timer 2 registers to reload with the 16-bit value in registers RCAP2L and RCAP2H, which are preset by software. If EXEN2 = 1 then Timer 2 still performs the above, but with the added feature that a 1-to-0 transition at external input T2EX will also trigger the 16-bit reload and set EXF2. The Autoreload mode is illustrated in Figure 30.

16-Bit Capture Mode

In the Capture mode, there are again two options, which are selected by bit EXEN2 in T2CON. If EXEN2 = 0, then Timer 2 is a 16-bit timer or counter that, upon overflowing, sets bit TF2, the Timer 2 overflow bit, that can be used to generate an interrupt. If EXEN2 = 1, then Timer 2 still performs the above, but a l-to-0 transition on external input T2EX causes the current value in the Timer 2 registers, TL2 and TH2, to be captured into registers RCAP2L and RCAP2H, respectively. In addition, the transition at T2EX causes bit EXF2 in T2CON to be set, and EXF2, like TF2, can generate an interrupt. The Capture mode is illustrated in Figure 31.

The baud rate generator mode is selected by RCLK = 1 and/or TCLK = 1.

In either case, if Timer 2 is being used to generate the baud rate, the TF2 interrupt flag will not occur. Therefore Timer 2 interrupts will not occur, so they do not have to be disabled. In this mode however, the EXF2 flag can still cause interrupts and this can be used as a third external interrupt.

Baud rate generation will be described as part of the UART serial port operation in the following pages.

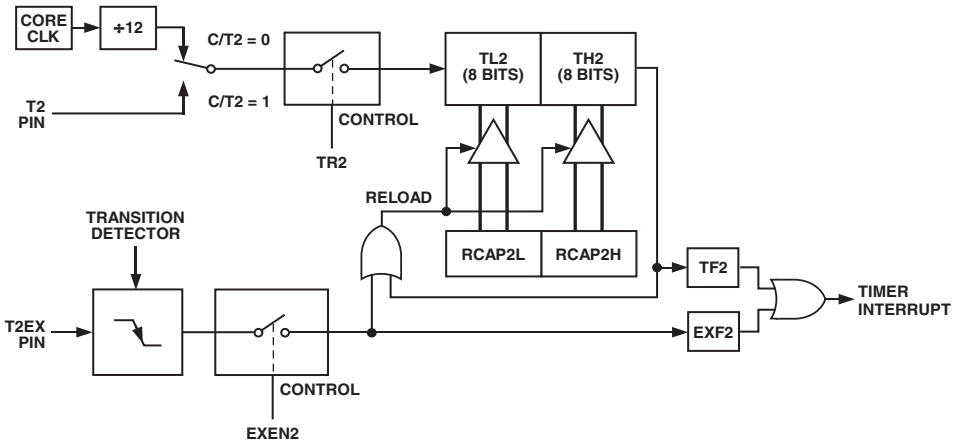

Figure 30. Timer/Counter 2, 16-Bit Autoreload Mode

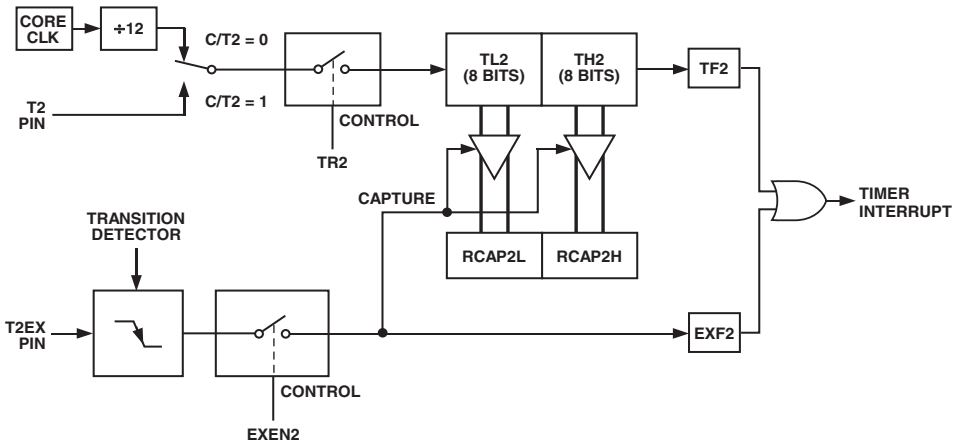

Figure 31. Timer/Counter 2, 16-Bit Capture Mode

UART SERIAL INTERFACE

The serial port is full-duplex, meaning it can transmit and receive simultaneously. It is also receive-buffered, meaning it can begin receiving a second byte before a previously received byte has been read from the receive register. However, if the first byte still has not been read by the time reception of the second byte is complete, the first byte will be lost. The physical interface to the serial data network is via Pins RXD(P3.0) and TXD(P3.1) while the SFR interface to the UART is comprised of SBUF and SCON, as described below.

SBUF

The serial port receive and transmit registers are both accessed through the SBUF SFR (SFR address = 99H). Writing to SBUF loads the transmit register and reading SBUF accesses a physically separate receive register.

SCON	**UART Serial Port Control Register**
SFR Address	98H
Power-On Default Value	00H
Bit Addressable	Yes

SM0	SM1	SM2	REN	TB8	RB8	TI	RI

Table XIX. SCON SFR Bit Designations

Bit	Name	Description
7	SM0	UART Serial Mode Select Bits.
6	SM1	These bits select the Serial Port operating mode as follows: SM0 SM1 Selected Operating Mode 0 0 Mode 0: Shift Register, fixed baud rate (Core_Clk/2) 0 1 Mode 1: 8-bit UART, variable baud rate 1 0 Mode 2: 9-bit UART, fixed baud rate (Core_Clk/64) or (Core_Clk/32) 1 1 Mode 3: 9-bit UART, variable baud rate
5	SM2	Multiprocessor Communication Enable Bit. Enables multiprocessor communication in Modes 2 and 3. In Mode 0, SM2 should be cleared. In Mode 1, if SM2 is set, RI will not be activated if a valid stop bit was not received. If SM2 is cleared, RI will be set as soon as the byte of data has been received. In Modes 2 or 3, if SM2 is set, RI will not be activated if the received ninth data bit in RB8 is 0. If SM2 is cleared, RI will be set as soon as the byte of data has been received.
4	REN	Serial Port Receive Enable Bit. Set by user software to enable serial port reception. Cleared by user software to disable serial port reception.
3	TB8	Serial Port Transmit (Bit 9). The data loaded into TB8 will be the ninth data bit that will be transmitted in Modes 2 and 3.
2	RB8	Serial Port Receiver Bit 9. The ninth data bit received in Modes 2 and 3 is latched into RB8. For Mode 1, the stop bit is latched into RB8.
1	TI	Serial Port Transmit Interrupt Flag. Set by hardware at the end of the eighth bit in Mode 0, or at the beginning of the stop bit in Modes 1, 2, and 3. TI must be cleared by user software.
0	RI	Serial Port Receive Interrupt Flag. Set by hardware at the end of the eighth bit in Mode 0, or halfway through the stop bit in Modes 1, 2, and 3. RI must be cleared by software.

As an alternative to providing two separate power supplies, the user can help keep AV_{DD} quiet by placing a small series resistor and/or ferrite bead between it and DV_{DD}, and then decoupling AV_{DD} separately to ground. An example of this configuration is shown in Figure 44. With this configuration, other analog circuitry (such as op amps, voltage reference, and so on) can be powered from the AV_{DD} supply line as well. The user will still want to include back-to-back Schottky diodes between AV_{DD} and DV_{DD} in order to protect from power-up and power-down transient conditions that could separate the two supply voltages momentarily.

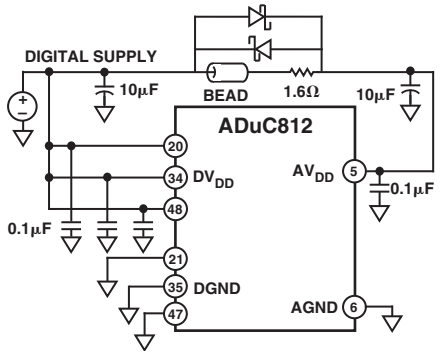

Figure 44. External Single-Supply Connections

Notice that in both Figure 43 and Figure 44, a large value (10 µF) reservoir capacitor sits on DV_{DD} and a separate 10 µF capacitor sits on AV_{DD}. Also, local small value (0.1 µF) capacitors are located at each V_{DD} pin of the chip. As per standard design practice, be sure to include all of these capacitors, and ensure the smaller capacitors are close to each AV_{DD} pin with trace lengths as short as possible. Connect the ground terminal of each of these capacitors directly to the underlying ground plane. Finally, it should also be noted that, at all times, the analog and digital ground pins on the ADuC812 must be referenced to the same system ground reference point.

Power Consumption

The currents consumed by the various sections of the ADuC812 are shown in Table XXVII. The CORE values given represent the current drawn by DV_{DD}, while the rest (ADC, DAC, Voltage Reference) are pulled by the AV_{DD} pin and can be disabled in software when not in use. The other on-chip peripherals (watchdog timer, power supply monitor, and so on) consume negligible current and are therefore lumped in with the CORE operating current here. Of course, the user must add any currents sourced by the DAC or the parallel and serial I/O pins, in order to determine the total current needed at the ADuC812's supply pins. Also, current drawn from the DV_{DD} supply will increase by approximately 10 mA during Flash/EE erase and program cycles.

Table XXVII. Typical I_{DD} of Core and Peripherals

	V_{DD} = 5 V	V_{DD} = 3 V
CORE (Normal Mode)	(1.6 nAs × MCLK) + 6 mA	(0.8 nAs × MCLK) + 3 mA
CORE (Idle Mode)	(0.75 nAs × MCLK) + 5 mA	(0.25 nAs × MCLK) + 3 mA
ADC	1.3 mA	1.0 mA
DAC (Each)	250 µA	200 µA
Voltage Ref	200 µA	150 µA

Since operating DV_{DD} current is primarily a function of clock speed, the expressions for CORE supply current in Table XXVII are given as functions of MCLK, the oscillator frequency. Plug in a value for MCLK in hertz to determine the current consumed by the core at that oscillator frequency. Since the ADC and DACs can be enabled or disabled in software, add only the currents from the peripherals you expect to use. The internal voltage reference is automatically enabled whenever either the ADC or at least one DAC is enabled. And again, do not forget to include current sourced by I/O pins, serial port pins, DAC outputs, and so forth, plus the additional current drawn during Flash/EE erase and program cycles.

A software switch allows the chip to be switched from normal mode into idle mode, and also into full power-down mode. Below are brief descriptions of power-down and idle modes.

In idle mode, the oscillator continues to run but is gated off to the core only. The on-chip peripherals continue to receive the clock, and remain functional. Port pins and DAC output pins retain their states in this mode. The chip will recover from idle mode upon receiving any enabled interrupt, or upon receiving a hardware reset.

In full power-down mode, the on-chip oscillator stops, and all on-chip peripherals are shut down. Port pins retain their logic levels in this mode, but the DAC output goes to a high impedance state (three-state). The chip will only recover from power-down mode upon receiving a hardware reset or when power is cycled. During full power-down mode, the ADuC812 consumes a total of approximately 5 µA.

Parameter		12 MHz Min	12 MHz Max	Variable Clock Min	Variable Clock Max	Unit
EXTERNAL DATA MEMORY WRITE CYCLE						
t_{WLWH}	$\overline{WR}$ Pulsewidth	400		$6t_{CK} - 100$		ns
t_{AVLL}	Address Valid after ALE Low	43		$t_{CK} - 40$		ns
t_{LLAX}	Address Hold after ALE Low	48		$t_{CK} - 35$		ns
t_{LLWL}	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	200	300	$3t_{CK} - 50$	$3t_{CK} + 50$	ns
t_{AVWL}	Address Valid to $\overline{RD}$ or $\overline{WR}$ Low	203		$4t_{CK} - 130$		ns
t_{QVWX}	Data Valid to $\overline{WR}$ Transition	33		$t_{CK} - 50$		ns
t_{QVWH}	Data Setup before $\overline{WR}$	433		$7t_{CK} - 150$		ns
t_{WHQX}	Data and Address Hold after $\overline{WR}$	33		$t_{CK} - 50$		ns
t_{WHLH}	$\overline{RD}$ or $\overline{WR}$ High to ALE High	43	123	$t_{CK} - 40$	$6t_{CK} - 100$	ns

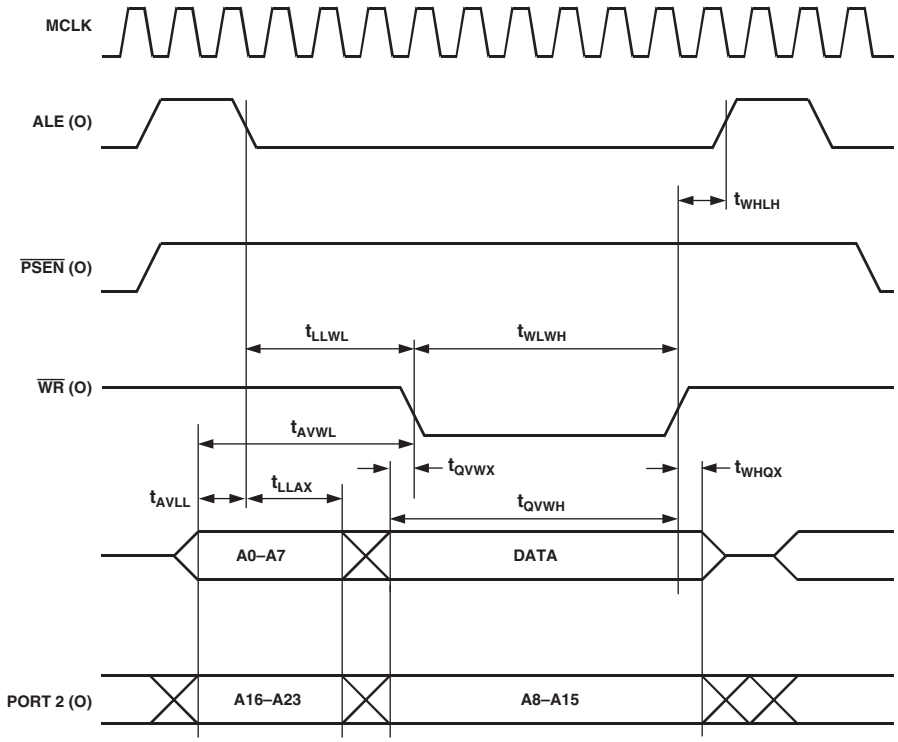

Figure 53. External Data Memory Write Cycle

REVISION HISTORY

3/13—Rev. E to Rev. F

Added EPAD Note to LFCSP Pin Configuration 6
Added EPAD Note to Pin Function Descriptions Table 8
Updated Outline Dimensions 56
Changes to Ordering Guide 56

4/03—Rev. D to Rev. E

Updated Outline Dimensions 56

2/03—Rev. C to Rev. D

Added CP-56 Package ..... Global
Edits to General Description 1
Added 56-Lead LFCSP Pin Configuration 6
Updated Ordering Guide 6
Added I2C Compatible Interface Timing Table 51
Added new Figure 55 51
Updated Outline Dimensions 56

03/02—Rev. B to Rev. C

Edits to Features 1
Edits to General Description 1
Edits to Functional Block Diagram 1
Edits to Specifications 3
Edits to Pin Configuration 6
Edits to Pin Function Descriptions 7
Edits to Figure 4 11
Edits to Serial Peripheral Interface Section 25
Edits to Table XI 26
Edits to Table XXIII 37
Edits to Tables XXIV, XXV, and XXVI 38

10/01—Data Sheet changed from Rev. A to Rev. B

Entire Data Sheet Revised ..... All