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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	DMA, I²S, POR, PWM, WDT
Number of I/O	38
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 13x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f091cct6

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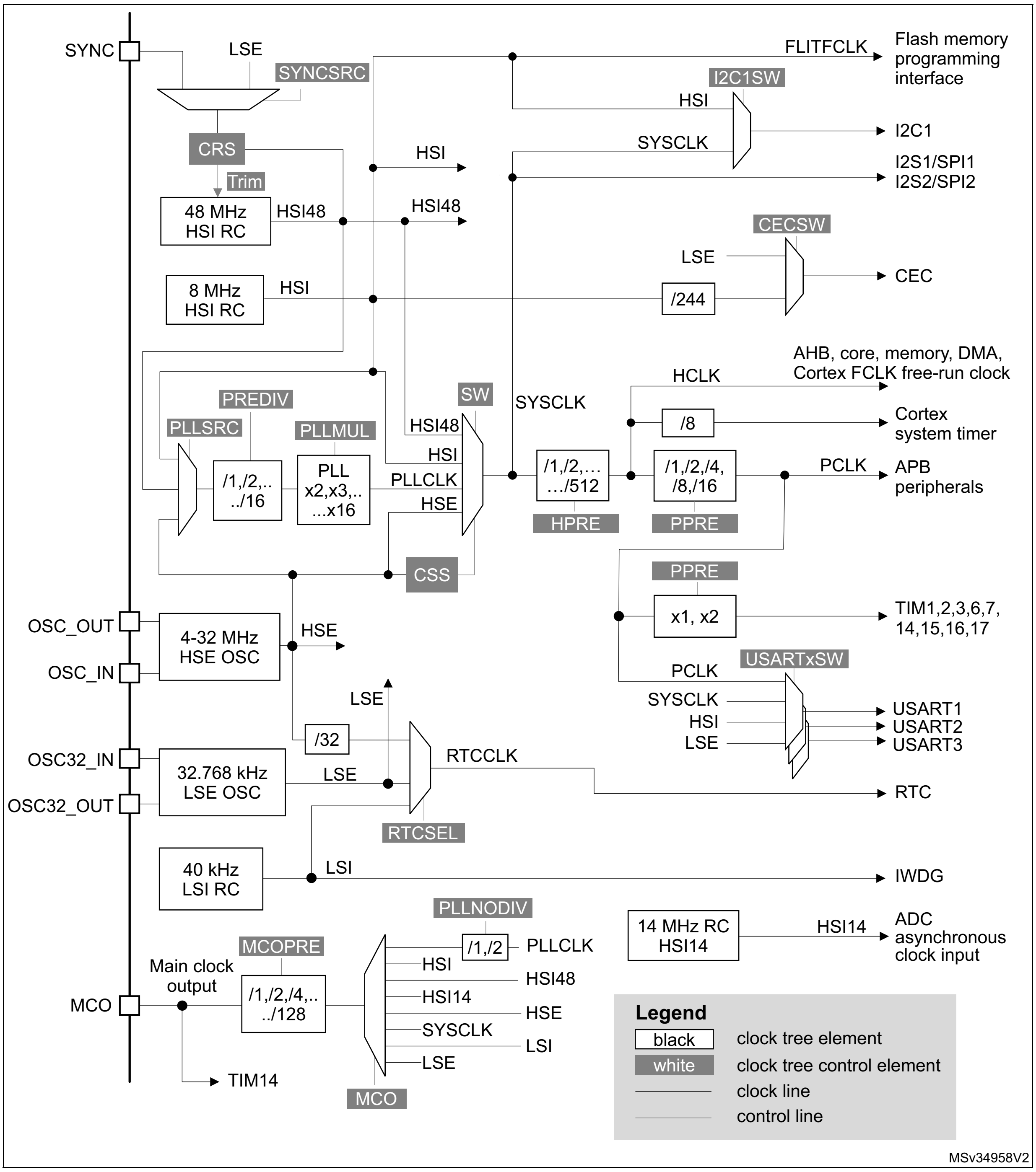
back to the internal RC oscillator. A software interrupt is generated if enabled. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example on failure of an indirectly used external crystal, resonator or oscillator).

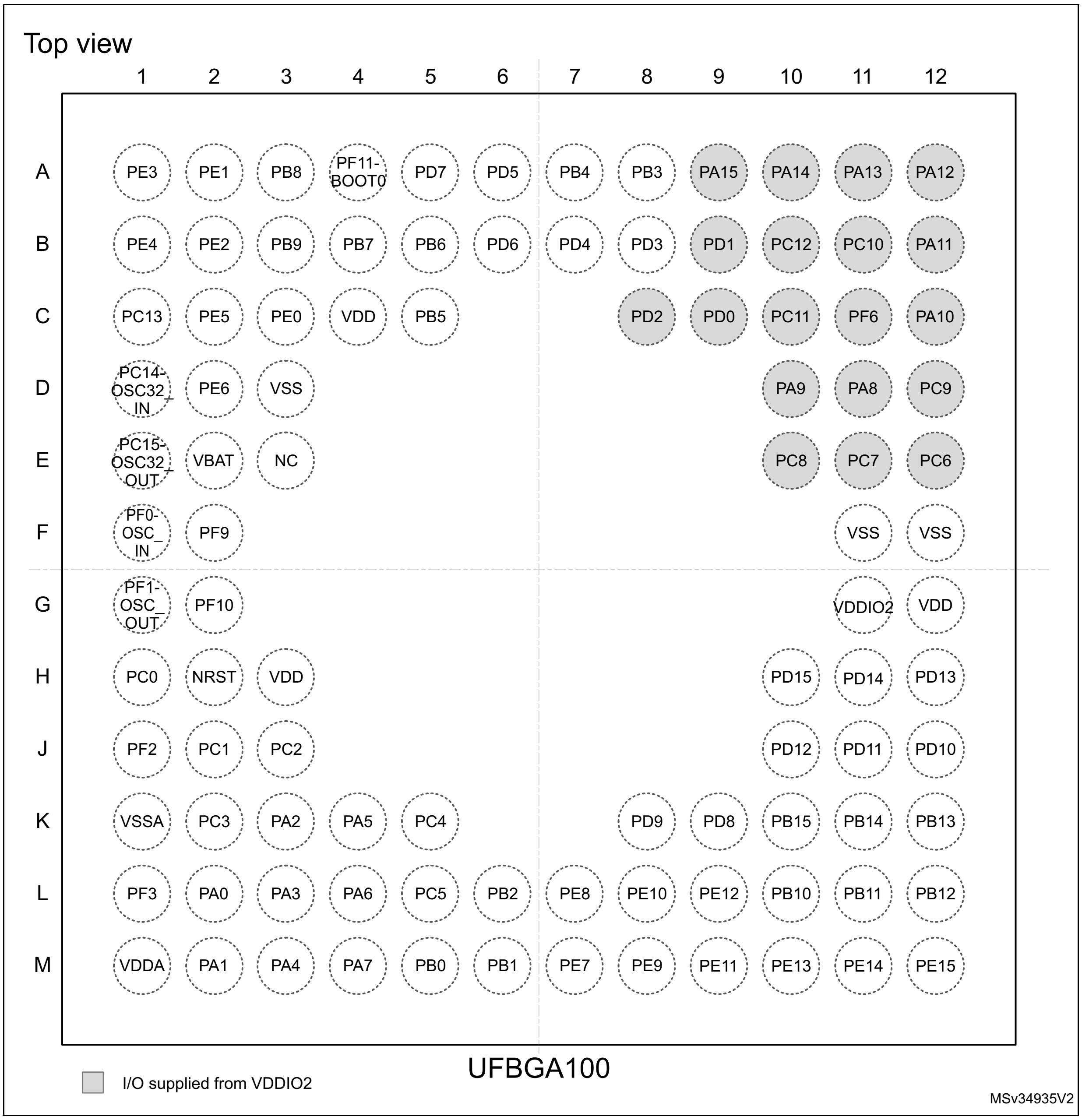
Figure 2. Clock tree



Several prescalers allow the application to configure the frequency of the AHB and the APB domains. The maximum frequency of the AHB and the APB domains is 48 MHz.

4 Pinouts and pin descriptions

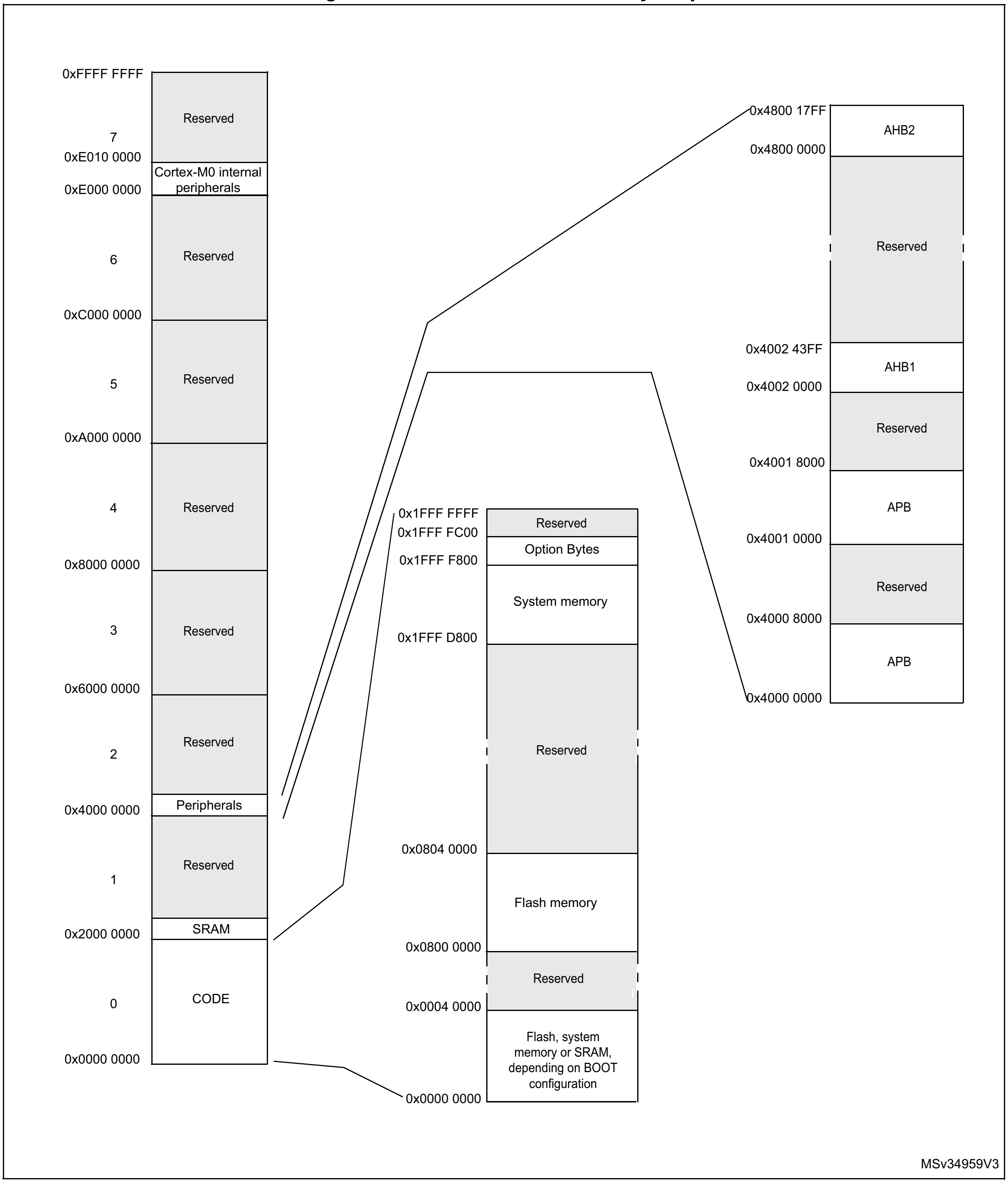
Figure 3. UFBGA100 package pinout



5 Memory mapping

To the difference of STM32F091xC memory map in *Figure 10*, the two bottom code memory spaces of STM32F091xB end at 0x0001 FFFF and 0x0801 FFFF, respectively.

Figure 10. STM32F091xC memory map



Typical and maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in analog input mode
- All peripherals are disabled except when explicitly mentioned
- The Flash memory access time is adjusted to the f_{HCLK} frequency:
  - 0 wait state and Prefetch OFF from 0 to 24 MHz
  - 1 wait state and Prefetch ON above 24 MHz
- When the peripherals are enabled $f_{PCLK} = f_{HCLK}$

The parameters given in *Table 29* to *Table 32* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 24: General operating conditions*.

Table 32. Typical and maximum current consumption from the V_{BAT} supply

Symbol	Parameter	Conditions	Typ @ V_{BAT}						Max(1)			Unit
			1.65 V	1.8 V	2.4 V	2.7 V	3.3 V	3.6 V	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD_VBAT}	RTC domain supply current	LSE & RTC ON; “Xtal mode”: lower driving capability; LSEDRV[1:0] = '00'	0.5	0.5	0.6	0.7	0.9	1.0	1.0	1.3	1.8	µA
		LSE & RTC ON; “Xtal mode” higher driving capability; LSEDRV[1:0] = '11'	0.8	0.8	0.9	1.0	1.2	1.3	1.4	1.7	2.2	

1. Data based on characterization results, not tested in production.

Typical current consumption

The MCU is placed under the following conditions:

- $V_{DD} = V_{DDA} = 3.3$ V
- All I/O pins are in analog input configuration
- The Flash memory access time is adjusted to f_{HCLK} frequency:
  - 0 wait state and Prefetch OFF from 0 to 24 MHz
  - 1 wait state and Prefetch ON above 24 MHz
- When the peripherals are enabled, $f_{PCLK} = f_{HCLK}$
- PLL is used for frequencies greater than 8 MHz
- AHB prescaler of 2, 4, 8 and 16 is used for the frequencies 4 MHz, 2 MHz, 1 MHz and 500 kHz respectively

trigger circuits used to discriminate the input value. Unless this specific configuration is required by the application, this supply current consumption can be avoided by configuring these I/Os in analog mode. This is notably the case of ADC input pins which should be configured as analog inputs.

Caution: Any floating input pin can also settle to an intermediate voltage level or switch inadvertently, as a result of external electromagnetic noise. To avoid current consumption related to floating pins, they must either be configured in analog mode, or forced internally to a definite digital value. This can be done either by using pull-up/down resistors or by configuring the pins in output mode.

I/O dynamic current consumption

In addition to the internal peripheral current consumption measured previously (see *Table 35: Peripheral current consumption*), the I/Os used by an application also contribute to the current consumption. When an I/O pin switches, it uses the current from the I/O supply voltage to supply the I/O pin circuitry and to charge/discharge the capacitive load (internal or external) connected to the pin:

$$I_{SW} = V_{DDIOx} \times f_{SW} \times C$$

where

I_{SW} is the current sunk by a switching I/O to charge/discharge the capacitive load

V_{DDIOx} is the I/O supply voltage

f_{SW} is the I/O switching frequency

C is the total capacitance seen by the I/O pin: $C = C_{INT} + C_{EXT} + C_S$

C_S is the PCB board capacitance including the pad pin.

The test pin is configured in push-pull output mode and is toggled by software at a fixed frequency.

High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 32 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in *Table 39*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 39. HSE oscillator characteristics

Symbol	Parameter	Conditions(1)	Min(2)	Typ	Max(2)	Unit
f_{OSC_IN}	Oscillator frequency	-	4	8	32	MHz
R_F	Feedback resistor	-	-	200	-	kΩ
I_{DD}	HSE current consumption	During startup(3)	-	-	8.5	mA
		V_{DD} = 3.3 V, Rm = 30 Ω, CL = 10 pF@8 MHz	-	0.4	-	
		V_{DD} = 3.3 V, Rm = 45 Ω, CL = 10 pF@8 MHz	-	0.5	-	
		V_{DD} = 3.3 V, Rm = 30 Ω, CL = 5 pF@32 MHz	-	0.8	-	
		V_{DD} = 3.3 V, Rm = 30 Ω, CL = 10 pF@32 MHz	-	1	-	
		V_{DD} = 3.3 V, Rm = 30 Ω, CL = 20 pF@32 MHz	-	1.5	-	
g_m	Oscillator transconductance	Startup	10	-	-	mA/V
$t_{SU(HSE)}$(4)	Startup time	V_{DD} is stabilized	-	2	-	ms

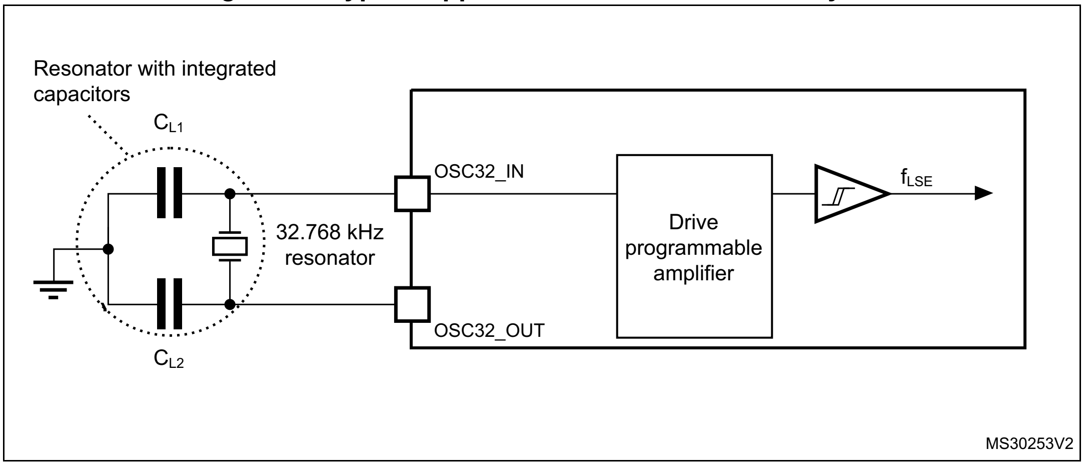
1. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
2. Guaranteed by design, not tested in production.
3. This consumption level occurs during the first 2/3 of the $t_{SU(HSE)}$ startup time
4. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 20 pF range (Typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see *Figure 17*). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}.

Note: For information on selecting the crystal, refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website www.st.com.

Note: For information on selecting the crystal, refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website www.st.com.

Figure 18. Typical application with a 32.768 kHz crystal



Note: An external resistor is not required between OSC32_IN and OSC32_OUT and it is forbidden to add one.

6.3.8 Internal clock source characteristics

The parameters given in *Table 41* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 24: General operating conditions*. The provided curves are characterization results, not tested in production.

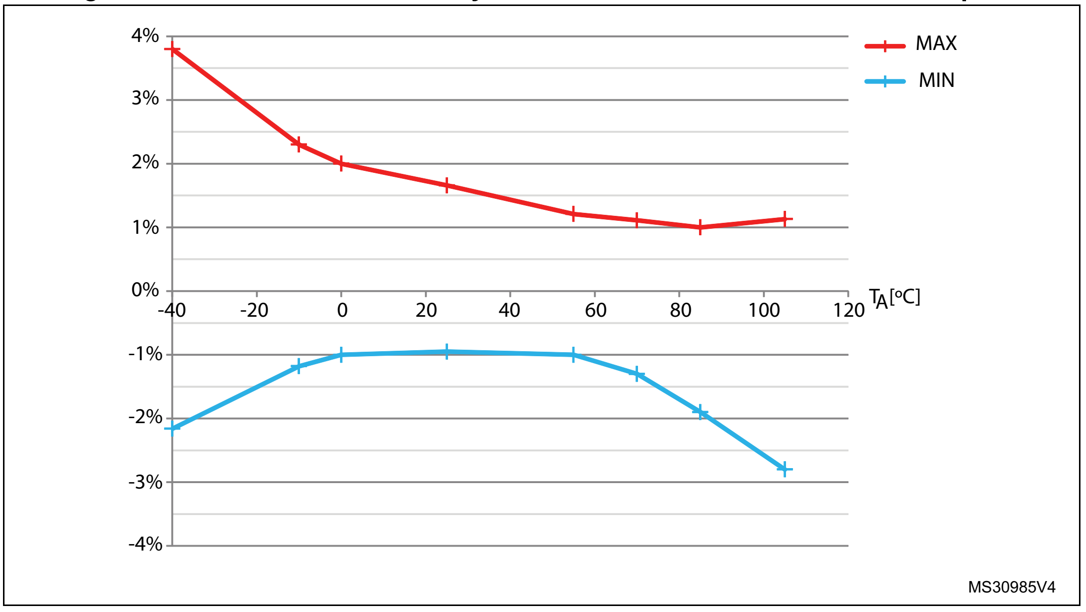
High-speed internal (HSI) RC oscillator

Table 41. HSI oscillator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	Frequency	-	-	8	-	MHz
TRIM	HSI user trimming step	-	-	-	1(2)	%
$DuCy_{(HSI)}$	Duty cycle	-	45(2)	-	55(2)	%
ACC_{HSI}	Accuracy of the HSI oscillator	T_A = -40 to 105°C	-2.8(3)	-	3.8(3)	%
		T_A = -10 to 85°C	-1.9(3)	-	2.3(3)	
		T_A = 0 to 85°C	-1.9(3)	-	2(3)	
		T_A = 0 to 70°C	-1.3(3)	-	2(3)	
		T_A = 0 to 55°C	-1(3)	-	2(3)	
		T_A = 25°C(4)	-1	-	1	
$t_{su(HSI)}$	HSI oscillator startup time	-	1(2)	-	2(2)	µs
$I_{DDA(HSI)}$	HSI oscillator power consumption	-	-	80	100(2)	µA

1. V_{DDA} = 3.3 V, T_A = -40 to 105°C unless otherwise specified.
2. Guaranteed by design, not tested in production.
3. Data based on characterization results, not tested in production.
4. Factory calibrated, parts not soldered.

Figure 19. HSI oscillator accuracy characterization results for soldered parts



Low-speed internal (LSI) RC oscillator

Table 44. LSI oscillator characteristics(1)

Symbol	Parameter	Min	Typ	Max	Unit
f_{LSI}	Frequency	30	40	50	kHz
$t_{su(LSI)}$(2)	LSI oscillator startup time	-	-	85	µs
$I_{DDA(LSI)}$(2)	LSI oscillator power consumption	-	0.75	1.2	µA

1. V_{DDA} = 3.3 V, T_A = –40 to 105 °C unless otherwise specified.
2. Guaranteed by design, not tested in production.

6.3.9 PLL characteristics

The parameters given in *Table 45* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 24: General operating conditions*.

Table 45. PLL characteristics

Symbol	Parameter	Value			Unit
		Min	Typ	Max	
f_{PLL_IN}	PLL input clock(1)	1(2)	8.0	24(2)	MHz
	PLL input clock duty cycle	40(2)	-	60(2)	%
f_{PLL_OUT}	PLL multiplier output clock	16(2)	-	48	MHz
t_{LOCK}	PLL lock time	-	-	200(2)	µs
$Jitter_{PLL}$	Cycle-to-cycle jitter	-	-	300(2)	ps

1. Take care to use the appropriate multiplier factors to obtain PLL input clock values compatible with the range defined by f_{PLL_OUT}.
2. Guaranteed by design, not tested in production.

6.3.10 Memory characteristics

Flash memory

The characteristics are given at T_A = –40 to 105 °C unless otherwise specified.

Table 46. Flash memory characteristics

Symbol	Parameter	Conditions	Min	Typ	Max(1)	Unit
t_{prog}	16-bit programming time	T_A = - 40 to +105 °C	40	53.5	60	µs
t_{ERASE}	Page (2 KB) erase time	T_A = - 40 to +105 °C	20	-	40	ms
t_{ME}	Mass erase time	T_A = - 40 to +105 °C	20	-	40	ms
I_{DD}	Supply current	Write mode	-	-	10	mA
		Erase mode	-	-	12	mA

1. Guaranteed by design, not tested in production.

Input/output AC characteristics

The definition and values of input/output AC characteristics are given in *Figure 24* and *Table 55*, respectively. Unless otherwise specified, the parameters given are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 24: General operating conditions*.

Table 55. I/O AC characteristics(1)(2)

OSPEEDRy [1:0] value(1)	Symbol	Parameter	Conditions	Min	Max	Unit
x0	$f_{max(IO)out}$	Maximum frequency(3)	C_L = 50 pF, $V_{DDIOx} \geq 2$ V	-	2	MHz
	$t_{f(IO)out}$	Output fall time		-	125	ns
	$t_{r(IO)out}$	Output rise time		-	125	
	$f_{max(IO)out}$	Maximum frequency(3)	C_L = 50 pF, $V_{DDIOx} < 2$ V	-	1	MHz
	$t_{f(IO)out}$	Output fall time		-	125	ns
	$t_{r(IO)out}$	Output rise time		-	125	
01	$f_{max(IO)out}$	Maximum frequency(3)	C_L = 50 pF, $V_{DDIOx} \geq 2$ V	-	10	MHz
	$t_{f(IO)out}$	Output fall time		-	25	ns
	$t_{r(IO)out}$	Output rise time		-	25	
	$f_{max(IO)out}$	Maximum frequency(3)	C_L = 50 pF, $V_{DDIOx} < 2$ V	-	4	MHz
	$t_{f(IO)out}$	Output fall time		-	62.5	ns
	$t_{r(IO)out}$	Output rise time		-	62.5	
11	$f_{max(IO)out}$	Maximum frequency(3)	C_L = 30 pF, $V_{DDIOx} \geq 2.7$ V	-	50	MHz
			C_L = 50 pF, $V_{DDIOx} \geq 2.7$ V	-	30	
			C_L = 50 pF, 2 V $\leq V_{DDIOx} < 2.7$ V	-	20	
			C_L = 50 pF, $V_{DDIOx} < 2$ V	-	10	
	$t_{f(IO)out}$	Output fall time	C_L = 30 pF, $V_{DDIOx} \geq 2.7$ V	-	5	ns
			C_L = 50 pF, $V_{DDIOx} \geq 2.7$ V	-	8	
			C_L = 50 pF, 2 V $\leq V_{DDIOx} < 2.7$ V	-	12	
			C_L = 50 pF, $V_{DDIOx} < 2$ V	-	25	
	$t_{r(IO)out}$	Output rise time	C_L = 30 pF, $V_{DDIOx} \geq 2.7$ V	-	5	
			C_L = 50 pF, $V_{DDIOx} \geq 2.7$ V	-	8	
			C_L = 50 pF, 2 V $\leq V_{DDIOx} < 2.7$ V	-	12	
			C_L = 50 pF, $V_{DDIOx} < 2$ V	-	25	

6.3.18 Comparator characteristics

Table 61. Comparator characteristics

Symbol	Parameter	Conditions		Min[(1)]	Typ	Max[(1)]	Unit
V_{DDA}	Analog supply voltage	-		V_{DD}	-	3.6	V
V_{IN}	Comparator input voltage range	-		0	-	V_{DDA}	-
V_{SC}	V_{REFINT} scaler offset voltage	-		-	±5	±10	mV
t_{S_SC}	V_{REFINT} scaler startup time from power down	-		-	-	0.2	ms
t_{START}	Comparator startup time	Startup time to reach propagation delay specification		-	-	60	µs
t_D	Propagation delay for 200 mV step with 100 mV overdrive	Ultra-low power mode		-	2	4.5	µs
		Low power mode		-	0.7	1.5	µs
		Medium power mode		-	0.3	0.6	µs
		High speed mode	$V_{DDA} \geq 2.7$ V	-	50	100	ns
			$V_{DDA} < 2.7$ V	-	100	240	ns
	Propagation delay for full range step with 100 mV overdrive	Ultra-low power mode		-	2	7	µs
		Low power mode		-	0.7	2.1	µs
		Medium power mode		-	0.3	1.2	µs
		High speed mode	$V_{DDA} \geq 2.7$ V	-	90	180	ns
			$V_{DDA} < 2.7$ V	-	110	300	ns
V_{offset}	Comparator offset error	-		-	±4	±10	mV
dV_{offset}/dT	Offset error temperature coefficient	-		-	18	-	µV/°C
$I_{DD(COMP)}$	COMP current consumption	Ultra-low power mode		-	1.2	1.5	µA
		Low power mode		-	3	5	µA
		Medium power mode		-	10	15	µA
		High speed mode		-	75	100	µA

Figure 28. SPI timing diagram - slave mode and CPHA = 0

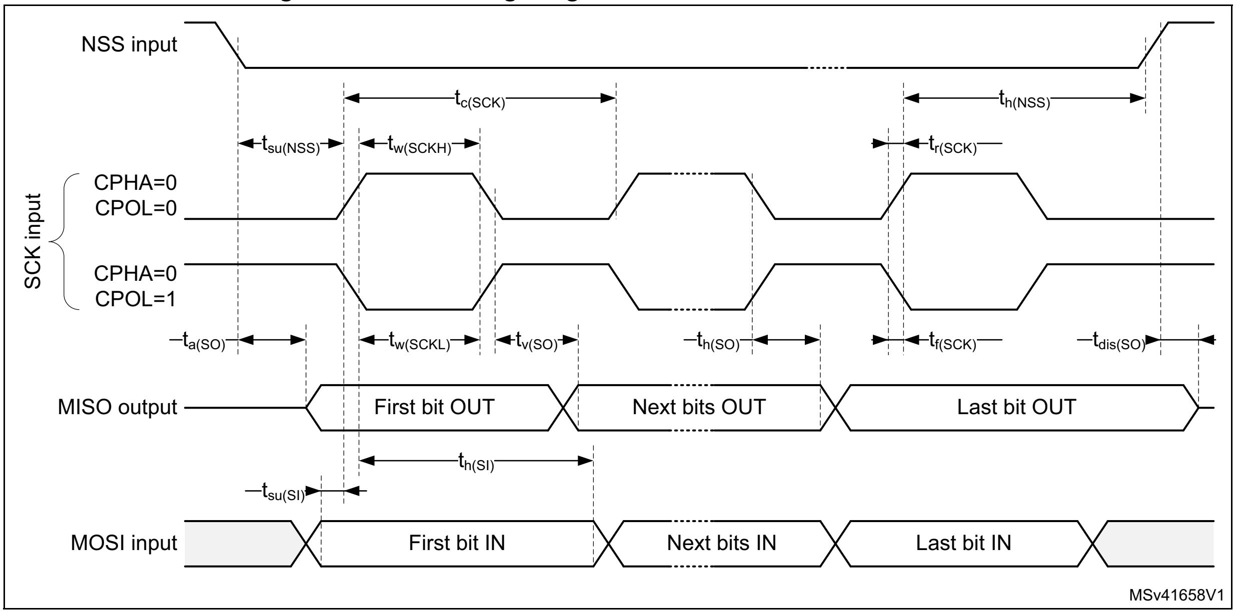
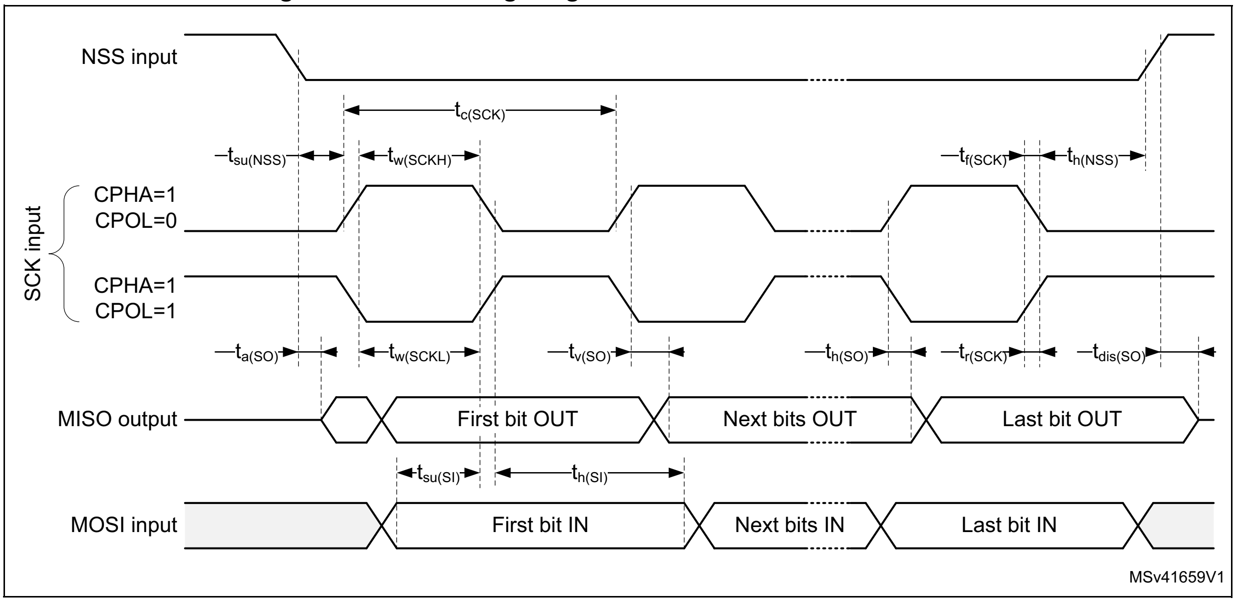


Figure 29. SPI timing diagram - slave mode and CPHA = 1



1. Measurement points are done at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.

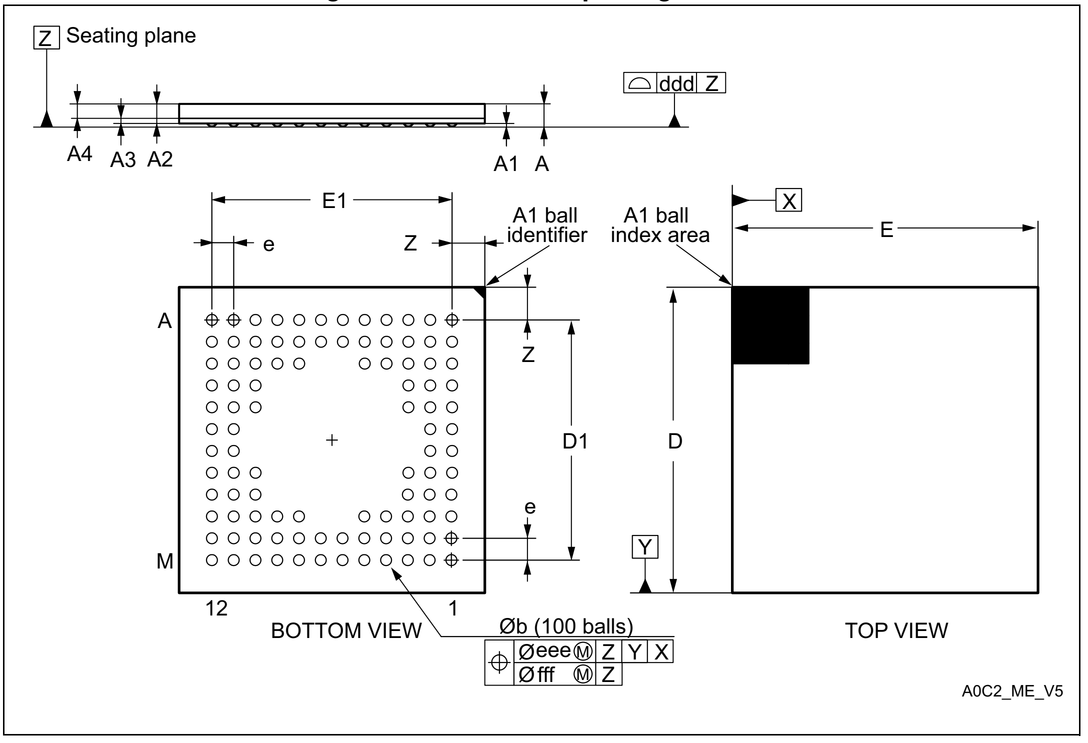
7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

7.1 UFBGA100 package information

UFBGA100 is a 100-ball, 7 x 7 mm, 0.50 mm pitch, ultra-fine-profile ball grid array package.

Figure 33. UFBGA100 package outline



1. Drawing is not to scale.

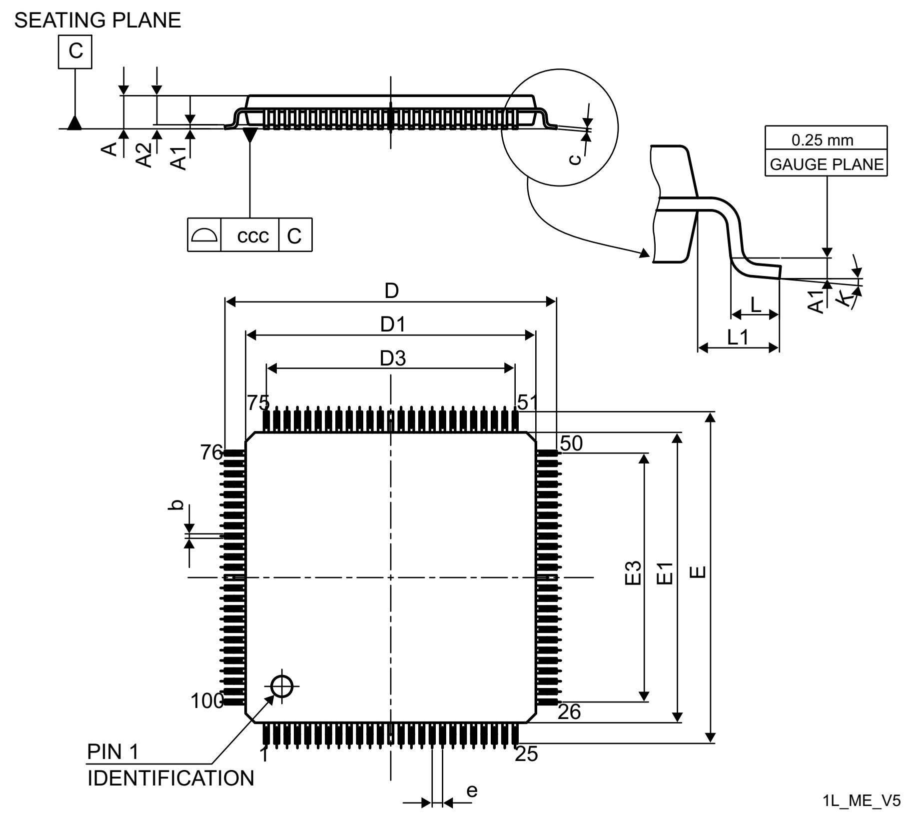
Table 70. UFBGA100 package mechanical data

Symbol	millimeters			inches(1)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	-	0.600	-	-	0.0236
A1	-	-	0.110	-	-	0.0043
A2	-	0.450	-	-	0.0177	-
A3	-	0.130	-	-	0.0051	0.0094
A4	-	0.320	-	-	0.0126	-

7.2 LQFP100 package information

LQFP100 is a100-pin, 14 x 14 mm low-profile quad flat package.

Figure 36. LQFP100 package outline



1. Drawing is not to scale.

Table 72. LQPF100 package mechanical data

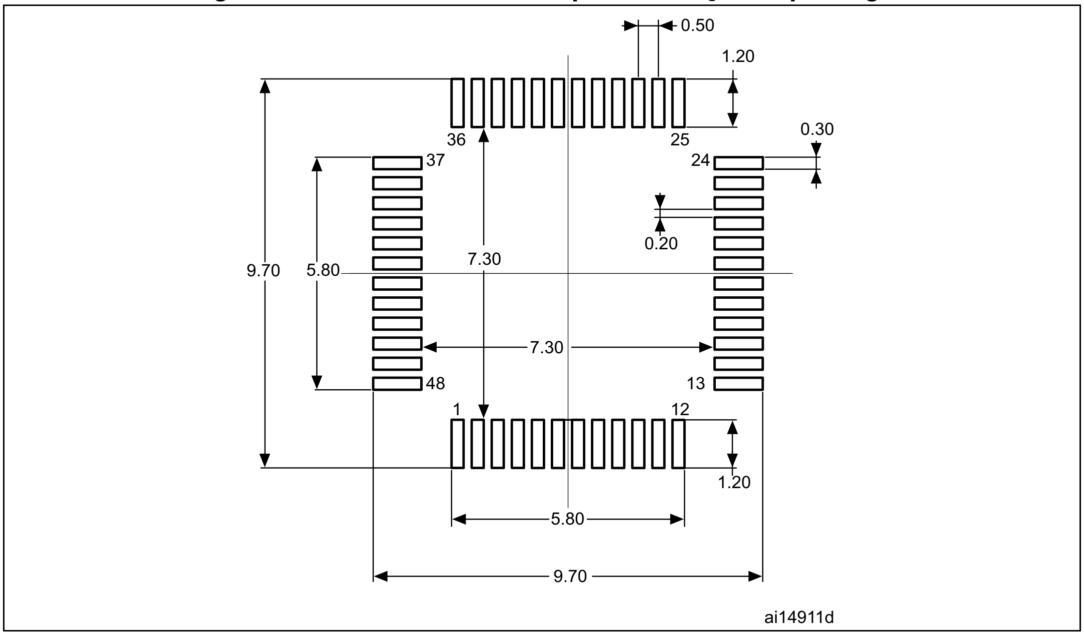
Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	15.800	16.000	16.200	0.6220	0.6299	0.6378
D1	13.800	14.000	14.200	0.5433	0.5512	0.5591
D3	-	12.000	-	-	0.4724	-
E	15.800	16.000	16.200	0.6220	0.6299	0.6378

Table 78. LQFP48 package mechanical data

Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3	-	5.500	-	-	0.2165	-
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	-	5.500	-	-	0.2165	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 49. Recommended footprint for LQFP48 package



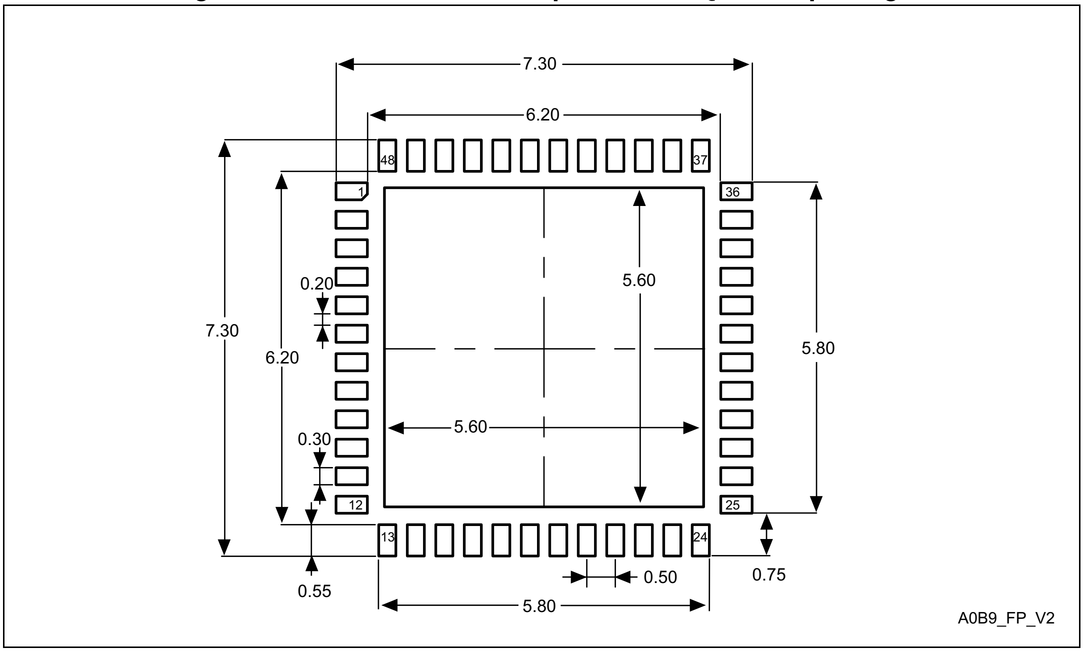
1. Dimensions are expressed in millimeters.

Table 79. UFQFPN48 package mechanical data

Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	0.000	0.020	0.050	0.0000	0.0008	0.0020
D	6.900	7.000	7.100	0.2717	0.2756	0.2795
E	6.900	7.000	7.100	0.2717	0.2756	0.2795
D2	5.500	5.600	5.700	0.2165	0.2205	0.2244
E2	5.500	5.600	5.700	0.2165	0.2205	0.2244
L	0.300	0.400	0.500	0.0118	0.0157	0.0197
T	-	0.152	-	-	0.0060	-
b	0.200	0.250	0.300	0.0079	0.0098	0.0118
e	-	0.500	-	-	0.0197	-
ddd	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 52. Recommended footprint for UFQFPN48 package



1. Dimensions are expressed in millimeters.

Using the values obtained in *Table 80* T_{Jmax} is calculated as follows:

– For LQFP64, 45 °C/W

T_{Jmax} = 100 °C + (45 °C/W × 134 mW) = 100 °C + 6.03 °C = 106.03 °C

This is above the range of the suffix 6 version parts (–40 < T_J < 105 °C).

In this case, parts must be ordered at least with the temperature range suffix 7 (see *Section 8: Ordering information*) unless we reduce the power dissipation in order to be able to use suffix 6 parts.

Refer to the figure below to select the required temperature range (suffix 6 or 7) according to your temperature or power requirements.

Figure 54. LQFP64 P_D max versus T_A