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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	CANbus, I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	DMA, I ² S, POR, PWM, WDT
Number of I/O	38
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 13x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f091cct6tr

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

3.4 Cyclic redundancy check calculation unit (CRC)

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code using a configurable generator polynomial value and size.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

3.5 **Power management**

3.5.1 Power supply schemes

- $V_{DD} = V_{DDIO1} = 2.0$ to 3.6 V: external power supply for I/Os (V_{DDIO1}) and the internal regulator. It is provided externally through VDD pins.
- V_{DDA} = from V_{DD} to 3.6 V: external analog power supply for ADC, DAC, Reset blocks, RCs and PLL (minimum voltage to be applied to V_{DDA} is 2.4 V when the ADC or DAC are used). It is provided externally through VDDA pin. The V_{DDA} voltage level must be always greater or equal to the V_{DD} voltage level and must be established first.
- V_{DDIO2} = 1.65 to 3.6 V: external power supply for marked I/Os. V_{DDIO2} is provided externally through the VDDIO2 pin. The V_{DDIO2} voltage level is completely independent from V_{DD} or V_{DDA}, but it must not be provided without a valid supply on V_{DD}. The V_{DDIO2} supply is monitored and compared with the internal reference voltage (V_{REFINT}). When the V_{DDIO2} is below this threshold, all the I/Os supplied from this rail are disabled by hardware. The output of this comparator is connected to EXTI line 31 and it can be used to generate an interrupt. Refer to the pinout diagrams or tables for concerned I/Os list.
- V_{BAT} = 1.65 to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.

For more details on how to connect power pins, refer to *Figure 13: Power supply scheme*.

3.5.2 Power supply supervisors

The device has integrated power-on reset (POR) and power-down reset (PDR) circuits. They are always active, and ensure proper operation above a threshold of 2 V. The device remains in reset mode when the monitored supply voltage is below a specified threshold, $V_{\text{POR/PDR}}$, without the need for an external reset circuit.

- The POR monitors only the V_{DD} supply voltage. During the startup phase it is required that V_{DDA} should arrive first and be greater than or equal to V_{DD}.
- The PDR monitors both the V_{DD} and V_{DDA} supply voltages, however the V_{DDA} power supply supervisor can be disabled (by programming a dedicated Option bit) to reduce the power consumption if the application design ensures that V_{DDA} is higher than or equal to V_{DD}.

The device features an embedded programmable voltage detector (PVD) that monitors the V_{DD} power supply and compares it to the V_{PVD} threshold. An interrupt can be generated when V_{DD} drops below the V_{PVD} threshold and/or when V_{DD} is higher than the V_{PVD}



Additionally, also the internal RC 48 MHz oscillator can be selected for system clock or PLL input source. This oscillator can be automatically fine-trimmed by the means of the CRS peripheral using the external synchronization.

3.7 General-purpose inputs/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions.

The I/O configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

3.8 Direct memory access controller (DMA)

The 12-channel general-purpose DMAs (seven channels for DMA1 and five channels for DMA2) manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers.

The DMAs support circular buffer management, removing the need for user code intervention when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with support for software trigger on each channel. Configuration is made by software and transfer sizes between source and destination are independent.

DMA can be used with the main peripherals: SPIx, I2Sx, I2Cx, USARTx, all TIMx timers (except TIM14), DAC and ADC.

3.9 Interrupts and events

3.9.1 Nested vectored interrupt controller (NVIC)

The STM32F0xx family embeds a nested vectored interrupt controller able to handle up to 32 maskable interrupt channels (not including the 16 interrupt lines of $Cortex^{\mathbb{R}}$ -M0) and 4 priority levels.

- Closely coupled NVIC gives low latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of late arriving higher priority interrupts
- Support for tail-chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimal interrupt latency.



precise voltage of V_{REFINT} is individually measured for each part by ST during production test and stored in the system memory area. It is accessible in read-only mode.

Calibration value name	Description	Memory address
VREFINT_CAL	Raw data acquired at a temperature of 30 °C (± 5 °C), V _{DDA} = 3.3 V (± 10 mV)	0x1FFF F7BA - 0x1FFF F7BB

Table 4. Internal voltage reference calibration values

3.10.3 V_{BAT} battery voltage monitoring

This embedded hardware feature allows the application to measure the V_{BAT} battery voltage using the internal ADC channel ADC_IN18. As the V_{BAT} voltage may be higher than V_{DDA}, and thus outside the ADC input range, the V_{BAT} pin is internally connected to a bridge divider by 2. As a consequence, the converted digital value is half the V_{BAT} voltage.

3.11 Digital-to-analog converter (DAC)

The two 12-bit buffered DAC channels can be used to convert digital signals into analog voltage signal outputs. The chosen design structure is composed of integrated resistor strings and an amplifier in non-inverting configuration.

This digital Interface supports the following features:

- 8-bit or 12-bit monotonic output
- Left or right data alignment in 12-bit mode
- Synchronized update capability
- Noise-wave generation
- Triangular-wave generation
- Dual DAC channel independent or simultaneous conversions
- DMA capability for each channel
- External triggers for conversion

Six DAC trigger inputs are used in the device. The DAC is triggered through the timer trigger outputs and the DAC interface is generating its own DMA requests.

3.12 Comparators (COMP)

The device embeds two fast rail-to-rail low-power comparators with programmable reference voltage (internal or external), hysteresis and speed (low speed for low power) and with selectable output polarity.

The reference voltage can be one of the following:

- External I/O
- DAC output pins
- Internal reference voltage or submultiple (1/4, 1/2, 3/4).Refer to *Table 28: Embedded internal reference voltage* for the value and precision of the internal reference voltage.



	Number of capacitive sensing channels						
Analog I/O group	STM32F091Vx	STM32F091Rx	STM32F091Cx				
G1	3	3	3				
G2	3	3	3				
G3	3	3	2				
G4	3	3	3				
G5	3	3	3				
G6	3	3	3				
G7	3	0	0				
G8	3	0	0				
Number of capacitive sensing channels	24	18	17				

Table 6. Number of capacitive sensing channels available on STM32F091xB/xC devices

3.14 Timers and watchdogs

The STM32F091xB/xC devices include up to six general-purpose timers, two basic timers and an advanced control timer.

Table 7 compares the features of the different timers.

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/compare channels	Complementary outputs
Advanced control	TIM1	16-bit	Up, down, up/down	integer from 1 to 65536	Yes	4	3
	TIM2	32-bit	Up, down, up/down	integer from 1 to 65536	Yes	4	-
	TIM3	16-bit	Up, down, up/down	integer from 1 to 65536	Yes	4	-
General purpose	TIM14	16-bit	Up	integer from 1 to 65536	No	1	-
	TIM15	16-bit	Up	integer from 1 to 65536	Yes	2	1
	TIM16 TIM17	16-bit	Up	integer from 1 to 65536	Yes	1	1
Basic	TIM6 TIM7	16-bit	Up	integer from 1 to 65536	Yes	-	-

Table 7. Timer feature comparison



	Pi	n nui	mber	S						Pin functions	
UFBGA100	LQFP100	UFBGA64	LQFP64	WLCSP64	LQFP48/UFQFPN48	Pin name (function upon reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
B2	1	-	-	-	-	PE2	I/O	FT		TSC_G7_IO1, TIM3_ETR	-
A1	2	-	-	-	-	PE3	I/O	FT		TSC_G7_IO2, TIM3_CH1	-
B1	3	-	-	-	-	PE4	I/O	FT		TSC_G7_IO3, TIM3_CH2	-
C2	4	-	-	-	-	PE5	I/O	FT		TSC_G7_IO4, TIM3_CH3	-
D2	5	-	-	-	-	PE6	I/O	FT		TIM3_CH4	WKUP3, RTC_TAMP3
E2	6	B2	1	B8	1	VBAT	S	-	-	Backup power s	upply
C1	7	A2	2	B7	2	PC13	I/O	тс	(1) (2)	-	WKUP2, RTC_TAMP1, RTC_TS, RTC_OUT
D1	8	A1	3	C8	3	PC14- OSC32_IN (PC14)	I/O	тс	(1) (2)	-	OSC32_IN
E1	9	B1	4	C7	4	PC15- OSC32_OUT (PC15)	I/O	тс	(1) (2)	-	OSC32_OUT
F2	10	-	-	-	-	PF9	I/O	FT		TIM15_CH1, USART6_TX	-
G2	11	-	-	-	-	PF10	I/O	FT		TIM15_CH2, USART6_RX	-
F1	12	C1	5	D8	5	PF0-OSC_IN (PF0)	I/O	FTf		CRS_SYNC, I2C1_SDA	OSC_IN
G1	13	D1	6	E8	6	PF1-OSC_OUT (PF1)	I/O	FTf		I2C1_SCL	OSC_OUT
H2	14	E1	7	D7	7	NRST	I/O	RST		Device reset input / intern (active low)	nal reset output)
H1	15	E3	8	E7	-	PC0	I/O	ТТа		EVENTOUT, USART6_TX, USART7_TX	ADC_IN10
J2	16	E2	9	F8	-	PC1	I/O	ТТа		EVENTOUT, USART6_RX, USART7_RX	ADC_IN11
J3	17	F2	10	D6	-	PC2	I/O	ТТа		SPI2_MISO, I2S2_MCK, EVENTOUT, USART8_TX	ADC_IN12
K2	18	G1	11	E6	-	PC3	I/O	ТТа		SPI2_MOSI, I2S2_SD, EVENTOUT, USART8_RX	ADC_IN13

Table 13. STM32F091xB/xC pin definitions



	Pi	in nu	mber	s						Pin functions		
UFBGA100	LQFP100	UFBGA64	LQFP64	WLCSP64	LQFP48/UFQFPN48	Pin name (function upon reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions	
M11	45	-	-	-	-	PE14	I/O	FT		SPI1_MISO, I2S1_MCK, TIM1_CH4	-	
M12	46	-	-	-	-	PE15	I/O	FT		SPI1_MOSI, I2S1_SD, TIM1_BKIN	-	
L10	47	G7	29	G3	21	PB10	I/O	FTf		SPI2_SCK, I2S2_CK, I2C2_SCL, USART3_TX, CEC, TSC_SYNC, TIM2_CH3	-	
L11	48	H7	30	H3	22	PB11	I/O	FTf		USART3_RX, TIM2_CH4, EVENTOUT, TSC_G6_IO1, I2C2_SDA	-	
F12	49	D5	31	H2	23	VSS	S	-		Ground		
G12	50	E5	32	H1	24	VDD	S	-		Digital power supply		
L12	51	H8	33	G2	25	PB12	I/O	FT		TIM1_BKIN, TIM15_BKIN, SPI2_NSS, I2S2_WS, USART3_CK, TSC_G6_IO2, EVENTOUT	-	
K12	52	G8	34	F2	26	PB13	I/O	FTf		SPI2_SCK, I2S2_CK, I2C2_SCL, USART3_CTS, TIM1_CH1N, TSC_G6_IO3	-	
K11	53	F8	35	G1	27	PB14	I/O	FTf		SPI2_MISO, I2S2_MCK, I2C2_SDA, USART3_RTS, TIM1_CH2N, TIM15_CH1, TSC_G6_IO4	-	
K10	54	F7	36	F1	28	PB15	I/O	FT		SPI2_MOSI, I2S2_SD, TIM1_CH3N, TIM15_CH1N, TIM15_CH2	WKUP7, RTC_REFIN	
K9	55	-	-	-	-	PD8	I/O	FT		USART3_TX	-	
K8	56	-	-	-	-	PD9	I/O	FT		USART3_RX	-	
J12	57	-	-	-	-	PD10	I/O	FT		USART3_CK	-	
J11	58	-	-	-	-	PD11	I/O	FT		USART3_CTS	-	

Table 13. STM32F091xB/xC pin definitions (continued)



6.1.6 Power supply scheme



Caution: Each power supply pair (V_{DD}/V_{SS}, V_{DDA}/V_{SSA} etc.) must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to, or below, the appropriate pins on the underside of the PCB to ensure the good functionality of the device.



6.1.7 Current consumption measurement



Figure 14. Current consumption measurement scheme



	Peripheral	Typical consumption at 25 °C	Unit
	APB-Bridge ⁽²⁾	3.6	
	ADC ⁽³⁾	4.3	
	CAN	12.4	
	CEC	0.4	
	CRS	0.0	
	DAC ⁽³⁾	4.2	
	DBG (MCU Debug Support)	0.2	
	I2C1	2.9	
	I2C2	2.4	
	PWR	0.6	
	SPI1	8.8	
	SPI2	7.8	
	SYSCFG and COMP	1.9	
	TIM1	15.2	
	TIM14	2.6	
	TIM15	8.7	
AFD	TIM16	5.8	μΑνινίτε
	TIM17	7.0	
	TIM2	16.2	
	TIM3	11.9	
	TIM6	11.8	
	TIM7	2.5	
	USART1	17.6	
	USART2	16.3	
	USART3	16.2	
	USART4	4.7	
	USART5	4.4	
	USART6	5.5	
	USART7	5.2	
	USART8	5.1	
	WWDG	1.1	
	All APB peripherals	207.2	

 Table 35. Peripheral current consumption (continued)

1. The BusMatrix is automatically active when at least one master is ON (CPU, DMA).

2. The APB Bridge is automatically active when at least one peripheral is ON on the Bus.

 The power consumption of the analog part (I_{DDA}) of peripherals such as ADC, DAC, comparators, is not included. Refer to the tables of characteristics in the subsequent sections.



High-speed internal (HSI) RC oscillator

Symbol	Parameter	Conditions	Min	Тур	Max	Unit	
f _{HSI}	Frequency	-	-	8	-	MHz	
TRIM	HSI user trimming step	-	-	-	1 ⁽²⁾	%	
DuCy _(HSI)	Duty cycle	-	45 ⁽²⁾	-	55 ⁽²⁾	%	
		T _A = -40 to 105°C	-2.8 ⁽³⁾	-	3.8 ⁽³⁾		
	Accuracy of the HSI oscillator	T _A = -10 to 85°C	-1.9 ⁽³⁾	-	2.3 ⁽³⁾		
100		T _A = 0 to 85°C	-1.9 ⁽³⁾	-	2 ⁽³⁾	0/	
ACCHSI		$T_A = 0$ to $70^{\circ}C$	-1.3 ⁽³⁾	-	2 ⁽³⁾	70	
		$T_A = 0$ to 55°C	-1 ⁽³⁾	-	2 ⁽³⁾		
		$T_A = 25^{\circ}C^{(4)}$	-1	-	1		
t _{su(HSI)}	HSI oscillator startup time	-	1 ⁽²⁾	-	2 ⁽²⁾	μs	
I _{DDA(HSI)}	HSI oscillator power consumption	-	-	80	100 ⁽²⁾	μA	

Table 41. HSI oscillator characteristics⁽¹⁾

1. V_{DDA} = 3.3 V, T_A = -40 to 105°C unless otherwise specified.

2. Guaranteed by design, not tested in production.

3. Data based on characterization results, not tested in production.

4. Factory calibrated, parts not soldered.



Figure 19. HSI oscillator accuracy characterization results for soldered parts



Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to +/-8 mA, and sink or source up to +/- 20 mA (with a relaxed V_{OL}/V_{OH}).

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in Section 6.2:

- The sum of the currents sourced by all the I/Os on V_{DDIOx}, plus the maximum consumption of the MCU sourced on V_{DD}, cannot exceed the absolute maximum rating ΣI_{VDD} (see *Table 21: Voltage characteristics*).
- The sum of the currents sunk by all the I/Os on V_{SS}, plus the maximum consumption of the MCU sunk on V_{SS}, cannot exceed the absolute maximum rating ΣI_{VSS} (see *Table 21: Voltage characteristics*).

Output voltage levels

Unless otherwise specified, the parameters given in the table below are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 24: General operating conditions*. All I/Os are CMOS- and TTL-compliant (FT, TTa or TC unless otherwise specified).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{OL}	Output low level voltage for an I/O pin	CMOS port ⁽²⁾	-	0.4	
V _{OH}	Output high level voltage for an I/O pin	I _{IO} = 8 mA V _{DDIOx} ≥ 2.7 V	V _{DDIOx} -0.4	-	V
V _{OL}	Output low level voltage for an I/O pin	TTL port ⁽²⁾	-	0.4	
V _{OH}	Output high level voltage for an I/O pin	I _{IO} = 8 mA V _{DDIOx} ≥ 2.7 V	2.4	-	V
V _{OL} ⁽³⁾	Output low level voltage for an I/O pin	I _{IO} = 20 mA	-	1.3	V
V _{OH} ⁽³⁾	Output high level voltage for an I/O pin	V _{DDIOx} ≥2.7 V	V _{DDIOx} -1.3	-	
V _{OL} ⁽³⁾	Output low level voltage for an I/O pin	I _{IO} = 6 mA	-	0.4	V
V _{OH} ⁽³⁾	Output high level voltage for an I/O pin	V _{DDIOx} ≥ 2 V	V _{DDIOx} -0.4	-	v
V _{OL} ⁽⁴⁾	Output low level voltage for an I/O pin	II I = 4 mA	-	0.4	V
V _{OH} ⁽⁴⁾	Output high level voltage for an I/O pin	1 ₀ – 4 mA	V _{DDIOx} -0.4	-	V
V _{OLFm+} ⁽³⁾	Output low level voltage for an FTf I/O pin in	I _{IO} = 20 mA V _{DDIOx} ≥ 2.7 V	-	0.4	V
		I _{IO} = 10 mA	-	0.4	V

Table 54. Output voltage characteristics⁽¹⁾

 The I_{IO} current sourced or sunk by the device must always respect the absolute maximum rating specified in Table 21: Voltage characteristics, and the sum of the currents sourced or sunk by all the I/Os (I/O ports and control pins) must always respect the absolute maximum ratings ΣI_{IO}.

2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.

3. Data based on characterization results. Not tested in production.

4. Data based on characterization results. Not tested in production.





OSPEEDRy [1:0] value ⁽¹⁾	Symbol	Parameter	Conditions	Min	Мах	Unit
	f _{max(IO)out}	Maximum frequency ⁽³⁾		-	2	MHz
Fm+ configuration (4)	t _{f(IO)out}	Output fall time	C _L = 50 pF, V _{DDIOx} ≥ 2 V	-	12	ns
	t _{r(IO)out}	Output rise time		-	34	
	f _{max(IO)out}	Maximum frequency ⁽³⁾		-	0.5	MHz
	t _{f(IO)out}	Output fall time	C _L = 50 pF, V _{DDIOx} < 2 V	-	16	200
	t _{r(IO)out}	Output rise time		-	44	115
-	t _{EXTIpw}	Pulse width of external signals detected by the EXTI controller	-	10	-	ns

Table 55. I/O AC characteristics⁽¹⁾⁽²⁾ (continued)

 The I/O speed is configured using the OSPEEDRx[1:0] bits. Refer to the STM32F0xxxx RM0091 reference manual for a description of GPIO Port configuration register.

2. Guaranteed by design, not tested in production.

- 3. The maximum frequency is defined in *Figure 24*.
- 4. When Fm+ configuration is set, the I/O speed control is bypassed. Refer to the STM32F0xxxx reference manual RM0091 for a detailed description of Fm+ I/O configuration.



Figure 24. I/O AC characteristics definition

6.3.15 NRST pin characteristics

The NRST pin input driver uses the CMOS technology. It is connected to a permanent pull-up resistor, $\mathsf{R}_{\mathsf{PU}}.$

Unless otherwise specified, the parameters given in the table below are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 24: General operating conditions*.

Symbol	Parameter	Conditions	Min	Тур	Мах	Unit
V _{IL(NRST)}	NRST input low level voltage	-	-	-	0.3 V _{DD} +0.07 ⁽¹⁾	V
V _{IH(NRST)}	NRST input high level voltage	-	0.445 V _{DD} +0.398 ⁽¹⁾	-	-	v

Table 56. NRST pin characteristics





Figure 28. SPI timing diagram - slave mode and CPHA = 0





1. Measurement points are done at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}



Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.





 Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.



Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.



Figure 50. LQFP48 package marking example

 Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.



7.7 UFQFPN48 package information

UFQFPN48 is a 48-lead, 7x7 mm, 0.5 mm pitch, ultra-thin fine-pitch quad flat package.





1. Drawing is not to scale.

- 2. All leads/pads should also be soldered to the PCB to improve the lead/pad solder joint life.
- 3. There is an exposed die pad on the underside of the UFQFPN package. It is recommended to connect and solder this back-side pad to PCB ground.



Symbol		millimeters		inches ⁽¹⁾			
Symbol	Min	Тур	Мах	Min	Тур	Мах	
А	0.500	0.550	0.600	0.0197	0.0217	0.0236	
A1	0.000	0.020	0.050	0.0000	0.0008	0.0020	
D	6.900	7.000	7.100	0.2717	0.2756	0.2795	
E	6.900	7.000	7.100	0.2717	0.2756	0.2795	
D2	5.500	5.600	5.700	0.2165	0.2205	0.2244	
E2	5.500	5.600	5.700	0.2165	0.2205	0.2244	
L	0.300	0.400	0.500	0.0118	0.0157	0.0197	
Т	-	0.152	-	-	0.0060	-	
b	0.200	0.250	0.300	0.0079	0.0098	0.0118	
е	-	0.500	-	-	0.0197	-	
ddd	-	-	0.080	-	-	0.0031	

Table 79. UFQFPN48 package mechanical data

1. Values in inches are converted from mm and rounded to 4 decimal digits.



Figure 52. Recommended footprint for UFQFPN48 package

1. Dimensions are expressed in millimeters.



Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.



Figure 53. UFQFPN48 package marking example

 Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.



Each temperature range suffix corresponds to a specific guaranteed ambient temperature at maximum dissipation and, to a specific maximum junction temperature.

As applications do not commonly use the STM32F091xB/xC at maximum dissipation, it is useful to calculate the exact power consumption and junction temperature to determine which temperature range will be best suited to the application.

The following examples show how to calculate the temperature range needed for a given application.

Example 1: High-performance application

Assuming the following application conditions:

Maximum temperature T_{Amax} = 82 °C (measured according to JESD51-2), I_{DDmax} = 50 mA, V_{DD} = 3.5 V, maximum 20 I/Os used at the same time in output at low level with I_{OL} = 8 mA, V_{OL} = 0.4 V and maximum 8 I/Os used at the same time in output at low level with I_{OL} = 20 mA, V_{OL} = 1.3 V

P_{INTmax} = 50 mA × 3.5 V= 175 mW

P_{IOmax} = 20 × 8 mA × 0.4 V + 8 × 20 mA × 1.3 V = 272 mW

This gives: P_{INTmax} = 175 mW and P_{IOmax} = 272 mW:

P_{Dmax} = 175 + 272 = 447 mW

Using the values obtained in *Table 80* T_{Jmax} is calculated as follows:

- For LQFP64, 45 °C/W

T_{Jmax} = 82 °C + (45 °C/W × 447 mW) = 82 °C + 20.115 °C = 102.115 °C

This is within the range of the suffix 6 version parts ($-40 < T_J < 105 \text{ °C}$).

In this case, parts must be ordered at least with the temperature range suffix 6 (see *Section 8: Ordering information*).

Note: With this given P_{Dmax} we can find the T_{Amax} allowed for a given device temperature range (order code suffix 6 or 7).

Suffix 6: $T_{Amax} = T_{Jmax} - (45^{\circ}C/W \times 447 \text{ mW}) = 105\text{-}20.115 = 84.885^{\circ}C$ Suffix 7: $T_{Amax} = T_{Jmax} - (45^{\circ}C/W \times 447 \text{ mW}) = 125\text{-}20.115 = 104.885^{\circ}C$

Example 2: High-temperature application

Using the same rules, it is possible to address applications that run at high temperatures with a low dissipation, as long as junction temperature T_J remains within the specified range.

Assuming the following application conditions:

Maximum temperature $T_{Amax} = 100$ °C (measured according to JESD51-2), $I_{DDmax} = 20$ mA, $V_{DD} = 3.5$ V, maximum 20 I/Os used at the same time in output at low level with $I_{OL} = 8$ mA, $V_{OL} = 0.4$ V $P_{INTmax} = 20$ mA × 3.5 V= 70 mW $P_{IOmax} = 20 \times 8$ mA × 0.4 V = 64 mW This gives: $P_{INTmax} = 70$ mW and $P_{IOmax} = 64$ mW: $P_{Dmax} = 70 + 64 = 134$ mW

Thus: P_{Dmax} = 134 mW

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Using the values obtained in *Table 80* T_{Jmax} is calculated as follows:

- For LQFP64, 45 °C/W
- T_{Jmax} = 100 °C + (45 °C/W × 134 mW) = 100 °C + 6.03 °C = 106.03 °C

This is above the range of the suffix 6 version parts ($-40 < T_J < 105 \text{ °C}$).

In this case, parts must be ordered at least with the temperature range suffix 7 (see *Section 8: Ordering information*) unless we reduce the power dissipation in order to be able to use suffix 6 parts.

Refer to the figure below to select the required temperature range (suffix 6 or 7) according to your temperature or power requirements.





