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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	DMA, I²S, POR, PWM, WDT
Number of I/O	38
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 13x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f091cct7

Figure 4. LQFP100 package pinout

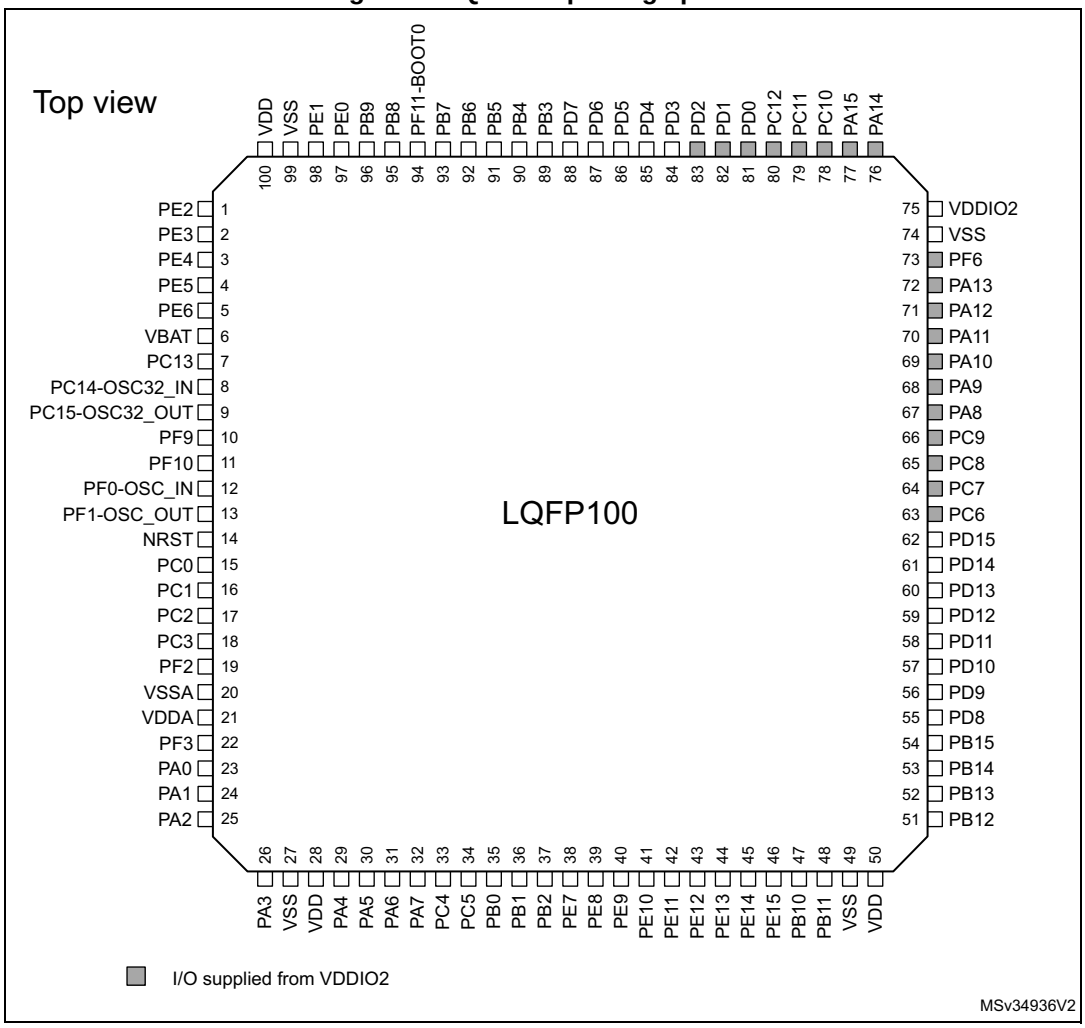


Table 13. STM32F091xB/xC pin definitions (continued)

Pin numbers						Pin name (function upon reset)	Pin type	I/O structure	Notes	Pin functions	
UFBGA100	LQFP100	UFBGA64	LQFP64	WLCSP64	LQFP48/UFQFPN48					Alternate functions	Additional functions
J1	19	-	-	-	-	PF2	I/O	FT		EVENTOUT, USART7_TX, USART7_CK_RTS	WKUP8
K1	20	F1	12	G8	8	VSSA	S	-		Analog ground	
M1	21	H1	13	H8	9	VDDA	S	-		Analog power supply	
L1	22	-	-	-	-	PF3	I/O	FT		EVENTOUT, USART7_RX, USART6_CK_RTS	
L2	23	G2	14	F7	10	PA0	I/O	TTa		USART2_CTS, TIM2_CH1_ETR, TSC_G1_IO1, USART4_TX COMP1_OUT	RTC_ TAMP2, WKUP1, ADC_IN0, COMP1_INM6
M2	24	H2	15	F6	11	PA1	I/O	TTa		USART2_RTS, TIM2_CH2, TIM15_CH1N, TSC_G1_IO2, USART4_RX, EVENTOUT	ADC_IN1, COMP1_INP
K3	25	F3	16	E5	12	PA2	I/O	TTa		USART2_TX, TIM2_CH3, TIM15_CH1, TSC_G1_IO3 COMP2_OUT	ADC_IN2, WKUP4, COMP2_INM6
L3	26	G3	17	H7	13	PA3	I/O	TTa		USART2_RX,TIM2_CH4, TIM15_CH2, TSC_G1_IO4	ADC_IN3, COMP2_INP
D3	27	C2	18	G7	-	VSS	S	-		Ground	
H3	28	D2	19	G6	-	VDD	S	-		Digital power supply	
M3	29	H3	20	H6	14	PA4	I/O	TTa		SPI1_NSS, I2S1_WS, TIM14_CH1, TSC_G2_IO1, USART2_CK, USART6_TX	COMP1_INM4, COMP2_INM4, ADC_IN4, DAC_OUT1
K4	30	F4	21	F5	15	PA5	I/O	TTa		SPI1_SCK, I2S1_CK, CEC, TIM2_CH1_ETR, TSC_G2_IO2, USART6_RX	COMP1_INM5, COMP2_INM5, ADC_IN5, DAC_OUT2

Table 13. STM32F091xB/xC pin definitions (continued)

Pin numbers						Pin name (function upon reset)	Pin type	I/O structure	Notes	Pin functions	
UFBGA100	LQFP100	UFBGA64	LQFP64	WLCSP64	LQFP48/UFQFPN48					Alternate functions	Additional functions
L4	31	G4	22	G5	16	PA6	I/O	TTa		SPI1_MISO, I2S1_MCK, TIM3_CH1, TIM1_BKIN, TIM16_CH1, COMP1_OUT, TSC_G2_IO3, EVENTOUT, USART3_CTS	ADC_IN6
M4	32	H4	23	E4	17	PA7	I/O	TTa		SPI1_MOSI, I2S1_SD, TIM3_CH2, TIM14_CH1, TIM1_CH1N, TIM17_CH1, COMP2_OUT, TSC_G2_IO4, EVENTOUT	ADC_IN7
K5	33	H5	24	H5	-	PC4	I/O	TTa		EVENTOUT, USART3_TX	ADC_IN14
L5	34	H6	25	F4	-	PC5	I/O	TTa		TSC_G3_IO1, USART3_RX	ADC_IN15, WKUP5
M5	35	F5	26	G4	18	PB0	I/O	TTa		TIM3_CH3, TIM1_CH2N, TSC_G3_IO2, EVENTOUT, USART3_CK	ADC_IN8
M6	36	G5	27	F3	19	PB1	I/O	TTa		TIM3_CH4, USART3_RTS, TIM14_CH1, TIM1_CH3N, TSC_G3_IO3	ADC_IN9
L6	37	G6	28	H4	20	PB2	I/O	FT		TSC_G3_IO4	-
M7	38	-	-	-	-	PE7	I/O	FT		TIM1_ETR, USART5_CK_RTS	-
L7	39	-	-	-	-	PE8	I/O	FT		TIM1_CH1N, USART4_TX	-
M8	40	-	-	-	-	PE9	I/O	FT		TIM1_CH1, USART4_RX	-
L8	41	-	-	-	-	PE10	I/O	FT		TIM1_CH2N, USART5_TX	-
M9	42	-	-	-	-	PE11	I/O	FT		TIM1_CH2, USART5_RX	-
L9	43	-	-	-	-	PE12	I/O	FT		SPI1_NSS, I2S1_WS, TIM1_CH3N	-
M10	44	-	-	-	-	PE13	I/O	FT		SPI1_SCK, I2S1_CK, TIM1_CH3	-

Table 18. Alternate functions selected through GPIOE_AFR registers for port E

Pin name	AF0	AF1
PE0	TIM16_CH1	EVENTOUT
PE1	TIM17_CH1	EVENTOUT
PE2	TIM3_ETR	TSC_G7_IO1
PE3	TIM3_CH1	TSC_G7_IO2
PE4	TIM3_CH2	TSC_G7_IO3
PE5	TIM3_CH3	TSC_G7_IO4
PE6	TIM3_CH4	-
PE7	TIM1_ETR	USART5_CK_RTS
PE8	TIM1_CH1N	USART4_TX
PE9	TIM1_CH1	USART4_RX
PE10	TIM1_CH2N	USART5_TX
PE11	TIM1_CH2	USART5_RX
PE12	TIM1_CH3N	SPI1_NSS, I2S1_WS
PE13	TIM1_CH3	SPI1_SCK, I2S1_CK
PE14	TIM1_CH4	SPI1_MISO, I2S1_MCK
PE15	TIM1_BKIN	SPI1_MOSI, I2S1_SD

Table 19. Alternate functions selected through GPIOF_AFR registers for port F

Pin name	AF0	AF1	AF2
PF0	CRS_SYNC	I2C1_SDA	-
PF1	-	I2C1_SCL	-
PF2	EVENTOUT	USART7_TX	USART7_CK_RTS
PF3	EVENTOUT	USART7_RX	USART6_CK_RTS
PF6	-	-	-
PF9	TIM15_CH1	USART6_TX	-
PF10	TIM15_CH2	USART6_RX	-

Table 22. Current characteristics

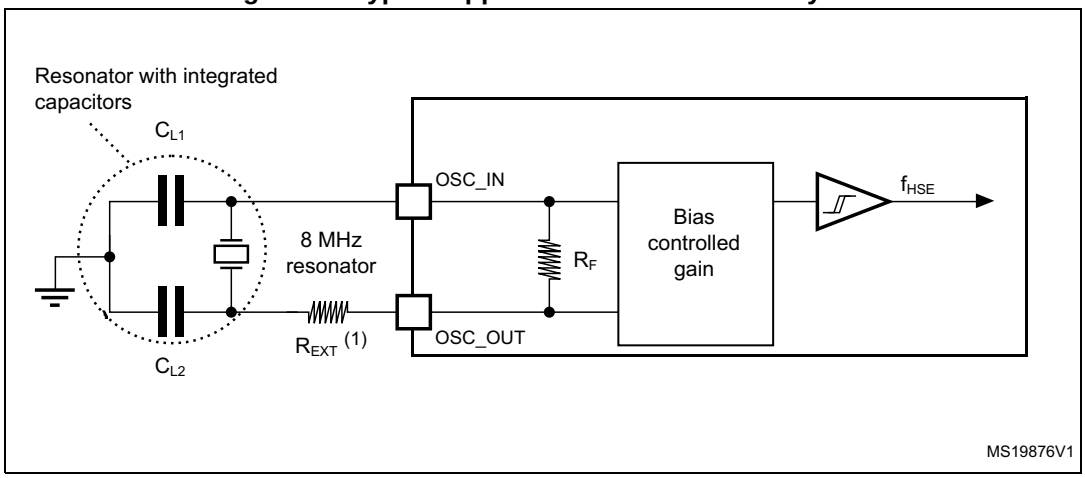
Symbol	Ratings	Max.	Unit
ΣI_{VDD}	Total current into sum of all VDD power lines (source)(1)	120	mA
ΣI_{VSS}	Total current out of sum of all VSS ground lines (sink)(1)	-120	
$I_{VDD(PIN)}$	Maximum current into each VDD power pin (source)(1)	100	
$I_{VSS(PIN)}$	Maximum current out of each VSS ground pin (sink)(1)	-100	
$I_{IO(PIN)}$	Output current sunk by any I/O and control pin	25	
	Output current source by any I/O and control pin	-25	
$\Sigma I_{IO(PIN)}$	Total output current sunk by sum of all I/Os and control pins(2)	80	
	Total output current sourced by sum of all I/Os and control pins(2)	-80	
	Total output current sourced by sum of all I/Os supplied by VDDIO2	-40	
$I_{INJ(PIN)}$(3)	Injected current on FT and FTf pins	-5/+0(4)	
	Injected current on TC and RST pin	± 5	
	Injected current on TTa pins(5)	± 5	
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/O and control pins)(6)	± 25	

1. All main power (VDD, VDDA) and ground (VSS, VSSA) pins must always be connected to the external power supply, in the permitted range.
2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count QFP packages.
3. A positive injection is induced by $V_{IN} > V_{DDIOx}$ while a negative injection is induced by $V_{IN} < V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 21: Voltage characteristics* for the maximum allowed input voltage values.
4. Positive injection is not possible on these I/Os and does not occur for input voltages lower than the specified maximum value.
5. On these I/Os, a positive injection is induced by $V_{IN} > V_{DDA}$. Negative injection disturbs the analog performance of the device. See note (2) below *Table 59: ADC accuracy*.
6. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

Table 23. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	150	°C

Figure 17. Typical application with an 8 MHz crystal



1. R_{EXT} value depends on the crystal characteristics.

Low-speed external clock generated from a crystal resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in *Table 40*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 40. LSE oscillator characteristics (f_{LSE} = 32.768 kHz)

Symbol	Parameter	Conditions(1)	Min(2)	Typ	Max(2)	Unit
I_{DD}	LSE current consumption	low drive capability	-	0.5	0.9	µA
		medium-low drive capability	-	-	1	
		medium-high drive capability	-	-	1.3	
		high drive capability	-	-	1.6	
g_m	Oscillator transconductance	low drive capability	5	-	-	µA/V
		medium-low drive capability	8	-	-	
		medium-high drive capability	15	-	-	
		high drive capability	25	-	-	
$t_{SU(LSE)}$(3)	Startup time	V_{DDIOx} is stabilized	-	2	-	s

1. Refer to the note and caution paragraphs below the table, and to the application note AN2867 “Oscillator design guide for ST microcontrollers”.
2. Guaranteed by design, not tested in production.
3. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal and it can vary significantly with the crystal manufacturer

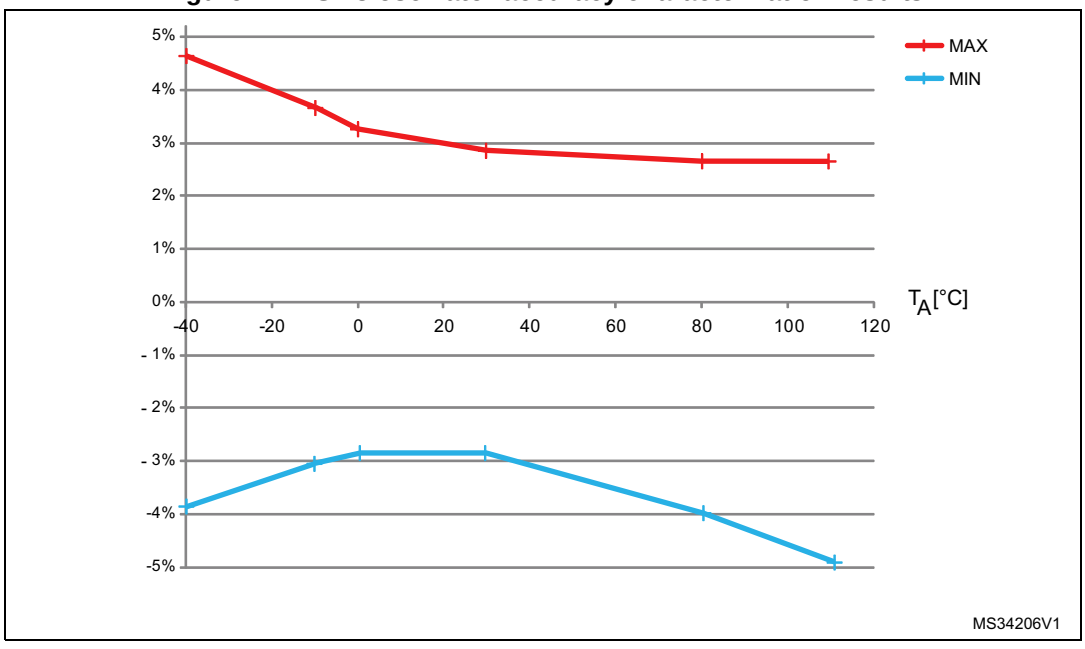
High-speed internal 48 MHz (HSI48) RC oscillator

Table 43. HSI48 oscillator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI48}	Frequency	-	-	48	-	MHz
TRIM	HSI48 user-trimming step	-	0.09(2)	0.14	0.2(2)	%
$DuCy_{(HSI48)}$	Duty cycle	-	45(2)	-	55(2)	%
ACC_{HSI48}	Accuracy of the HSI48 oscillator (factory calibrated)	T_A = –40 to 105 °C	-4.9(3)	-	4.7(3)	%
		T_A = –10 to 85 °C	-4.1(3)	-	3.7(3)	%
		T_A = 0 to 70 °C	-3.8(3)	-	3.4(3)	%
		T_A = 25 °C	-2.8	-	2.9	%
$t_{su(HSI48)}$	HSI48 oscillator startup time	-	-	-	6(2)	µs
$I_{DDA(HSI48)}$	HSI48 oscillator power consumption	-	-	312	350(2)	µA

1. V_{DDA} = 3.3 V, T_A = –40 to 105 °C unless otherwise specified.
2. Guaranteed by design, not tested in production.
3. Data based on characterization results, not tested in production.

Figure 21. HSI48 oscillator accuracy characterization results



Low-speed internal (LSI) RC oscillator

Table 44. LSI oscillator characteristics(1)

Symbol	Parameter	Min	Typ	Max	Unit
f_{LSI}	Frequency	30	40	50	kHz
$t_{su(LSI)}$(2)	LSI oscillator startup time	-	-	85	µs
$I_{DDA(LSI)}$(2)	LSI oscillator power consumption	-	0.75	1.2	µA

1. V_{DDA} = 3.3 V, T_A = –40 to 105 °C unless otherwise specified.
2. Guaranteed by design, not tested in production.

6.3.9 PLL characteristics

The parameters given in *Table 45* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 24: General operating conditions*.

Table 45. PLL characteristics

Symbol	Parameter	Value			Unit
		Min	Typ	Max	
f_{PLL_IN}	PLL input clock(1)	1(2)	8.0	24(2)	MHz
	PLL input clock duty cycle	40(2)	-	60(2)	%
f_{PLL_OUT}	PLL multiplier output clock	16(2)	-	48	MHz
t_{LOCK}	PLL lock time	-	-	200(2)	µs
$Jitter_{PLL}$	Cycle-to-cycle jitter	-	-	300(2)	ps

1. Take care to use the appropriate multiplier factors to obtain PLL input clock values compatible with the range defined by f_{PLL_OUT}.
2. Guaranteed by design, not tested in production.

6.3.10 Memory characteristics

Flash memory

The characteristics are given at T_A = –40 to 105 °C unless otherwise specified.

Table 46. Flash memory characteristics

Symbol	Parameter	Conditions	Min	Typ	Max(1)	Unit
t_{prog}	16-bit programming time	T_A = - 40 to +105 °C	40	53.5	60	µs
t_{ERASE}	Page (2 KB) erase time	T_A = - 40 to +105 °C	20	-	40	ms
t_{ME}	Mass erase time	T_A = - 40 to +105 °C	20	-	40	ms
I_{DD}	Supply current	Write mode	-	-	10	mA
		Erase mode	-	-	12	mA

1. Guaranteed by design, not tested in production.

Table 52. I/O current injection susceptibility

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}	Injected current on BOOT0	-0	NA	mA
	Injected current on PF1 pin (FTf pin)	-0	NA	
	Injected current on PC0 pin (TTA pin)	-0	+5	
	Injected current on PA4, PA5 pins with induced leakage current on adjacent pins less than -20 µA	-5	NA	
	Injected current on other FT and FTf pins	-5	NA	
	Injected current on all other TC, TTa and RST pins	-5	+5	

6.3.14 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in *Table 53* are derived from tests performed under the conditions summarized in *Table 24: General operating conditions*. All I/Os are designed as CMOS- and TTL-compliant.

Table 53. I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Low level input voltage	TC and TTa I/O	-	-	$0.3\ V_{DDIOx}+0.07$(1)	V
		FT and FTf I/O	-	-	$0.475\ V_{DDIOx}-0.2$(1)	
		All I/Os	-	-	$0.3\ V_{DDIOx}$	
V_{IH}	High level input voltage	TC and TTa I/O	$0.445\ V_{DDIOx}+0.398$(1)	-	-	V
		FT and FTf I/O	$0.5\ V_{DDIOx}+0.2$(1)	-	-	
		All I/Os	$0.7\ V_{DDIOx}$	-	-	
V_{hys}	Schmitt trigger hysteresis	TC and TTa I/O	-	200(1)	-	mV
		FT and FTf I/O	-	100(1)	-	
I_{lkg}	Input leakage current(2)	TC, FT and FTf I/O TTa in digital mode $V_{SS} \le V_{IN} \le V_{DDIOx}$	-	-	± 0.1	µA
		TTa in digital mode $V_{DDIOx} \le V_{IN} \le V_{DDA}$	-	-	1	
		TTa in analog mode $V_{SS} \le V_{IN} \le V_{DDA}$	-	-	± 0.2	
		FT and FTf I/O $V_{DDIOx} \le V_{IN} \le 5$ V	-	-	10	

Figure 22. TC and TTa I/O input characteristics

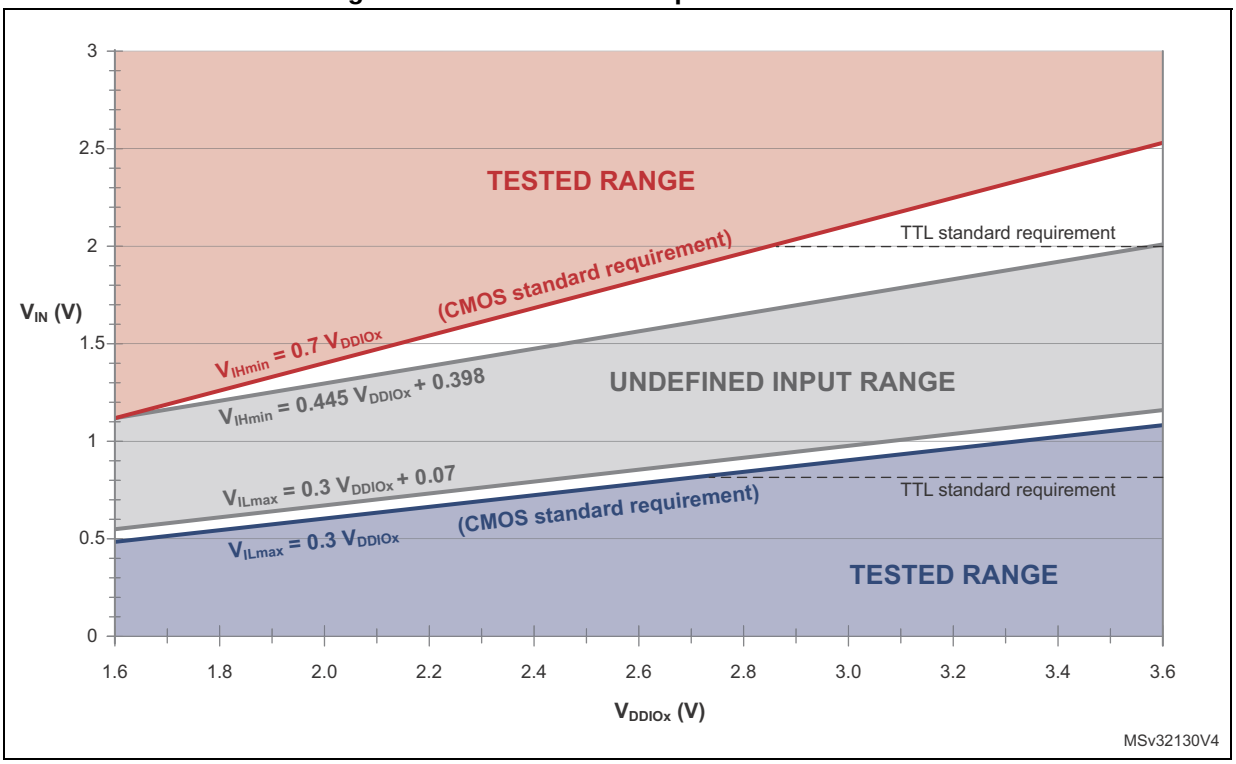


Figure 23. Five volt tolerant (FT and FTf) I/O input characteristics

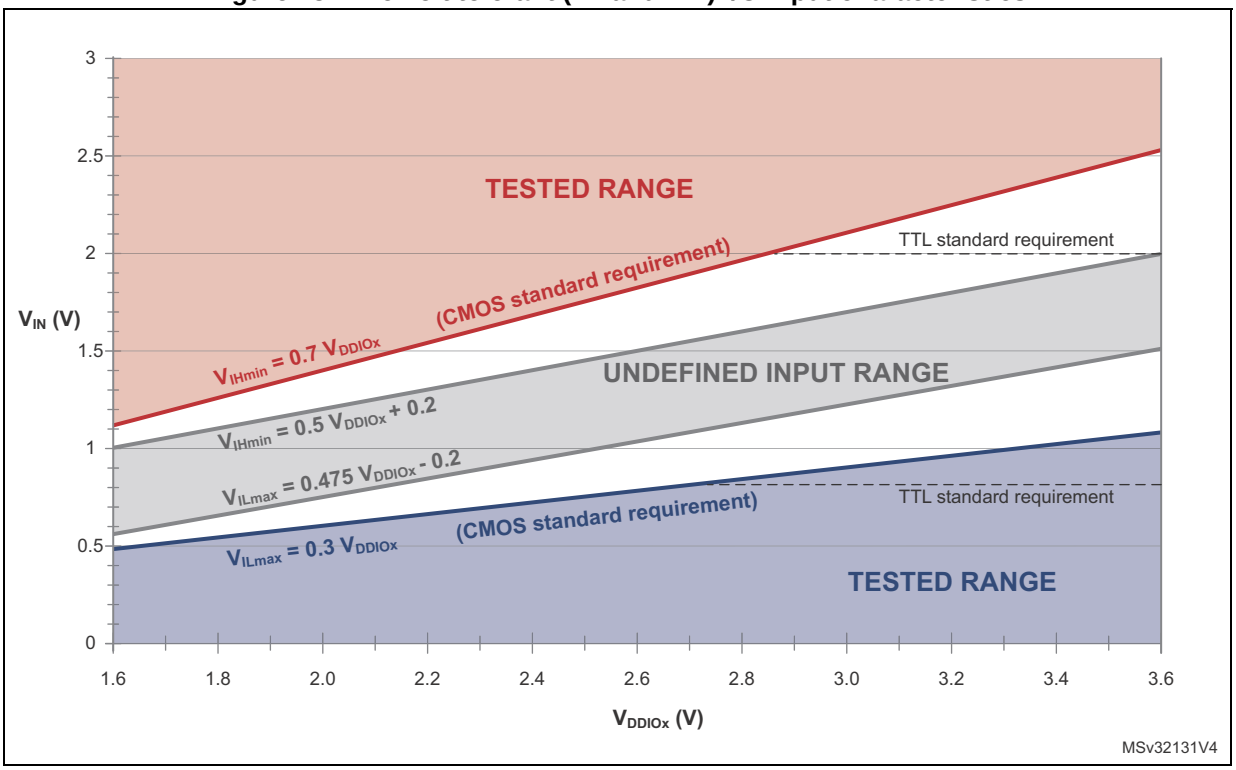


Table 57. ADC characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{TRIG} (2)	External trigger frequency	f_{ADC} = 14 MHz, 12-bit resolution	-	-	823	kHz
		12-bit resolution	-	-	17	$1/f_{ADC}$
V_{AIN}	Conversion voltage range	-	0	-	V_{DDA}	V
R_{AIN} (2)	External input impedance	See *Equation 1* and *Table 58* for details	-	-	50	kΩ
R_{ADC} (2)	Sampling switch resistance	-	-	-	1	kΩ
C_{ADC} (2)	Internal sample and hold capacitor	-	-	-	8	pF
t_{CAL} (2)(3)	Calibration time	f_{ADC} = 14 MHz	5.9			µs
		-	83			$1/f_{ADC}$
$W_{LATENCY}$ (2)(4)	ADC_DR register ready latency	ADC clock = HSI14	1.5 ADC cycles + 2 f_{PCLK} cycles	-	1.5 ADC cycles + 3 f_{PCLK} cycles	-
		ADC clock = PCLK/2	-	4.5	-	f_{PCLK} cycle
		ADC clock = PCLK/4	-	8.5	-	f_{PCLK} cycle
t_{latr} (2)	Trigger conversion latency	$f_{ADC} = f_{PCLK}/2 = 14$ MHz	0.196			µs
		$f_{ADC} = f_{PCLK}/2$	5.5			$1/f_{PCLK}$
		$f_{ADC} = f_{PCLK}/4 = 12$ MHz	0.219			µs
		$f_{ADC} = f_{PCLK}/4$	10.5			$1/f_{PCLK}$
		$f_{ADC} = f_{HSI14}$ = 14 MHz	0.179	-	0.250	µs
$Jitter_{ADC}$	ADC jitter on trigger conversion	$f_{ADC} = f_{HSI14}$	-	1	-	$1/f_{HSI14}$
t_S (2)	Sampling time	f_{ADC} = 14 MHz	0.107	-	17.1	µs
		-	1.5	-	239.5	$1/f_{ADC}$
t_{STAB} (2)	Stabilization time	-	14			$1/f_{ADC}$
t_{CONV} (2)	Total conversion time (including sampling time)	f_{ADC} = 14 MHz, 12-bit resolution	1	-	18	µs
		12-bit resolution	14 to 252 (t_S for sampling +12.5 for successive approximation)			$1/f_{ADC}$

1. During conversion of the sampled value (12.5 x ADC clock period), an additional consumption of 100 µA on I_{DDA} and 60 µA on I_{DD} should be taken into account.
2. Guaranteed by design, not tested in production.
3. Specified value includes only ADC timing. It does not include the latency of the register access.
4. This parameter specify latency for transfer of the conversion result to the ADC_DR register. EOC flag is set at this time.

Equation 1: R_{AIN} max formula

$$R_{AIN} < \frac{T_S}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The formula above (*Equation 1*) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N = 12 (from 12-bit resolution).

Table 58. R_{AIN} max for f_{ADC} = 14 MHz

T_S (cycles)	t_S (µs)	R_{AIN} max (kΩ)(1)
1.5	0.11	0.4
7.5	0.54	5.9
13.5	0.96	11.4
28.5	2.04	25.2
41.5	2.96	37.2
55.5	3.96	50
71.5	5.11	NA
239.5	17.1	NA

1. Guaranteed by design, not tested in production.

Table 59. ADC accuracy(1)(2)(3)

Symbol	Parameter	Test conditions	Typ	Max(4)	Unit
ET	Total unadjusted error	f_{PCLK} = 48 MHz, f_{ADC} = 14 MHz, R_{AIN} < 10 kΩ V_{DDA} = 3 V to 3.6 V T_A = 25 °C	±1.3	±2	LSB
EO	Offset error		±1	±1.5	
EG	Gain error		±0.5	±1.5	
ED	Differential linearity error		±0.7	±1	
EL	Integral linearity error		±0.8	±1.5	
ET	Total unadjusted error	f_{PCLK} = 48 MHz, f_{ADC} = 14 MHz, R_{AIN} < 10 kΩ V_{DDA} = 2.7 V to 3.6 V T_A = - 40 to 105 °C	±3.3	±4	LSB
EO	Offset error		±1.9	±2.8	
EG	Gain error		±2.8	±3	
ED	Differential linearity error		±0.7	±1.3	
EL	Integral linearity error		±1.2	±1.7	
ET	Total unadjusted error	f_{PCLK} = 48 MHz, f_{ADC} = 14 MHz, R_{AIN} < 10 kΩ V_{DDA} = 2.4 V to 3.6 V T_A = 25 °C	±3.3	±4	LSB
EO	Offset error		±1.9	±2.8	
EG	Gain error		±2.8	±3	
ED	Differential linearity error		±0.7	±1.3	
EL	Integral linearity error		±1.2	±1.7	

1. ADC DC accuracy values are measured after internal calibration.

Table 67. I²C analog filter characteristics(1)

Symbol	Parameter	Min	Max	Unit
t_{AF}	Maximum width of spikes that are suppressed by the analog filter	50(2)	260(3)	ns

1. Guaranteed by design, not tested in production.
2. Spikes with widths below $t_{AF(min)}$ are filtered.
3. Spikes with widths above $t_{AF(max)}$ are not filtered

SPI/I²S characteristics

Unless otherwise specified, the parameters given in *Table 68* for SPI or in *Table 69* for I²S are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and supply voltage conditions summarized in *Table 24: General operating conditions*.

Refer to *Section 6.3.14: I/O port characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI and WS, CK, SD for I²S).

Table 68. SPI characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	-	18	MHz
		Slave mode	-	18	
$t_{r(SCK)}$ $t_{f(SCK)}$	SPI clock rise and fall time	Capacitive load: C = 15 pF	-	6	ns
$t_{su(NSS)}$	NSS setup time	Slave mode	4Tpclk	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode	2Tpclk + 10	-	
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low time	Master mode, f_{PCLK} = 36 MHz, presc = 4	Tpclk/2 -2	Tpclk/2 + 1	
$t_{su(MI)}$ $t_{su(SI)}$	Data input setup time	Master mode	4	-	
		Slave mode	5	-	
$t_{h(MI)}$	Data input hold time	Master mode	4	-	
$t_{h(SI)}$		Slave mode	5	-	
$t_{a(SO)}$(2)	Data output access time	Slave mode, f_{PCLK} = 20 MHz	0	3Tpclk	
$t_{dis(SO)}$(3)	Data output disable time	Slave mode	0	18	
$t_{v(SO)}$	Data output valid time	Slave mode (after enable edge)	-	22.5	
$t_{v(MO)}$	Data output valid time	Master mode (after enable edge)	-	6	
$t_{h(SO)}$	Data output hold time	Slave mode (after enable edge)	11.5	-	
$t_{h(MO)}$		Master mode (after enable edge)	2	-	
DuCy(SCK)	SPI slave input clock duty cycle	Slave mode	25	75	%

1. Data based on characterization results, not tested in production.
2. Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.
3. Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z

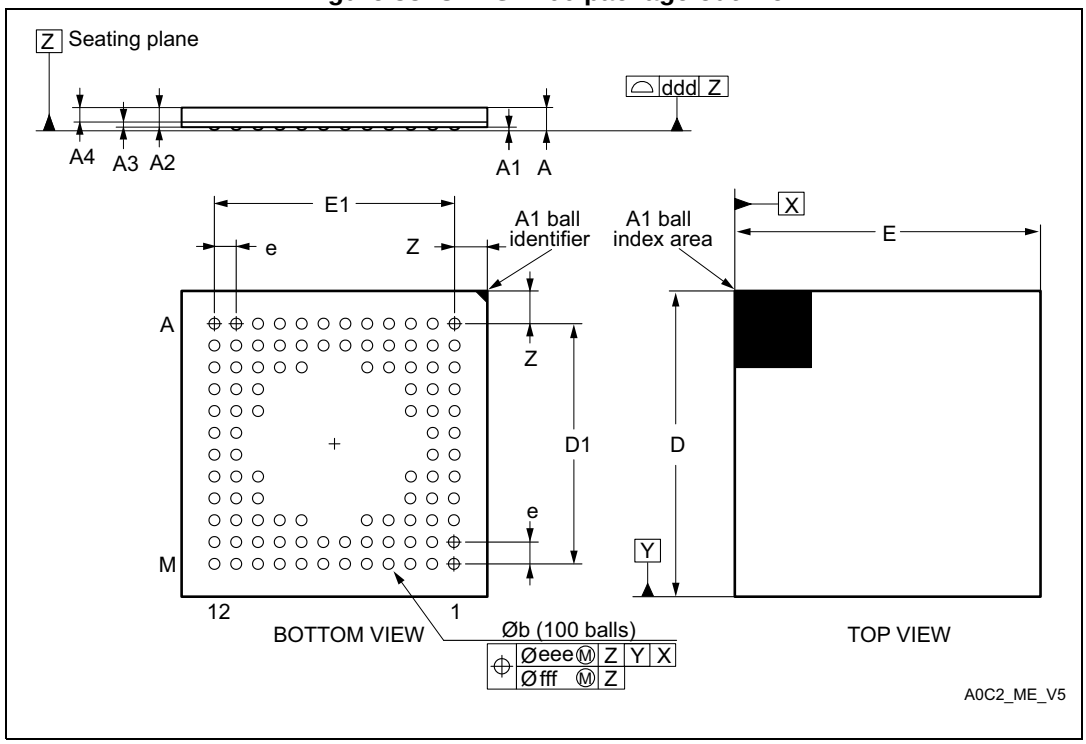
7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

7.1 UFBGA100 package information

UFBGA100 is a 100-ball, 7 x 7 mm, 0.50 mm pitch, ultra-fine-profile ball grid array package.

Figure 33. UFBGA100 package outline



1. Drawing is not to scale.

Table 70. UFBGA100 package mechanical data

Symbol	millimeters			inches(1)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	-	0.600	-	-	0.0236
A1	-	-	0.110	-	-	0.0043
A2	-	0.450	-	-	0.0177	-
A3	-	0.130	-	-	0.0051	0.0094
A4	-	0.320	-	-	0.0126	-

Table 70. UFBGA100 package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
b	0.240	0.290	0.340	0.0094	0.0114	0.0134
D	6.850	7.000	7.150	0.2697	0.2756	0.2815
D1	-	5.500	-	-	0.2165	-
E	6.850	7.000	7.150	0.2697	0.2756	0.2815
E1	-	5.500	-	-	0.2165	-
e	-	0.500	-	-	0.0197	-
Z	-	0.750	-	-	0.0295	-
ddd	-	-	0.080	-	-	0.0031
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 34. Recommended footprint for UFBGA100 package

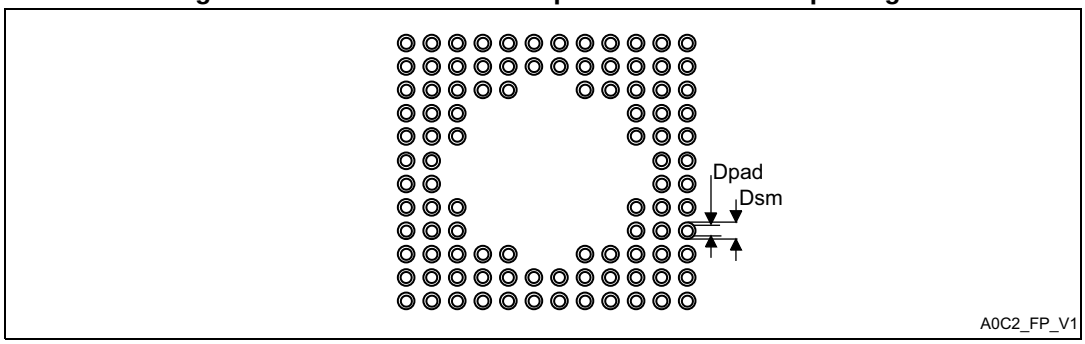


Table 71. UFBGA100 recommended PCB design rules

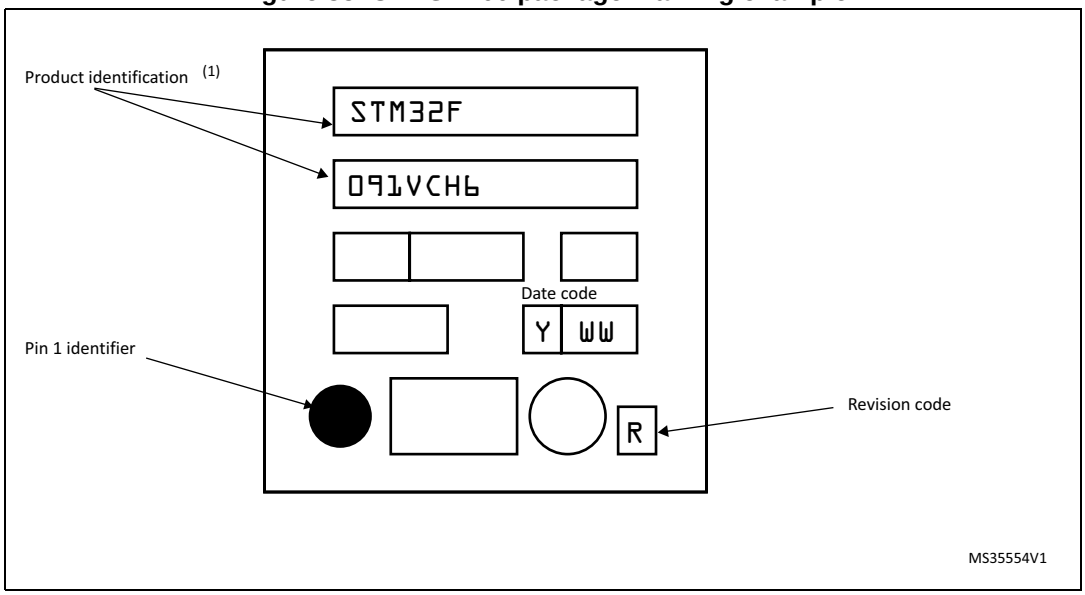
Dimension	Recommended values
Pitch	0.5
Dpad	0.280 mm
Dsm	0.370 mm typ. (depends on the solder mask registration tolerance)
Stencil opening	0.280 mm
Stencil thickness	Between 0.100 mm and 0.125 mm

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 35. UFBGA100 package marking example

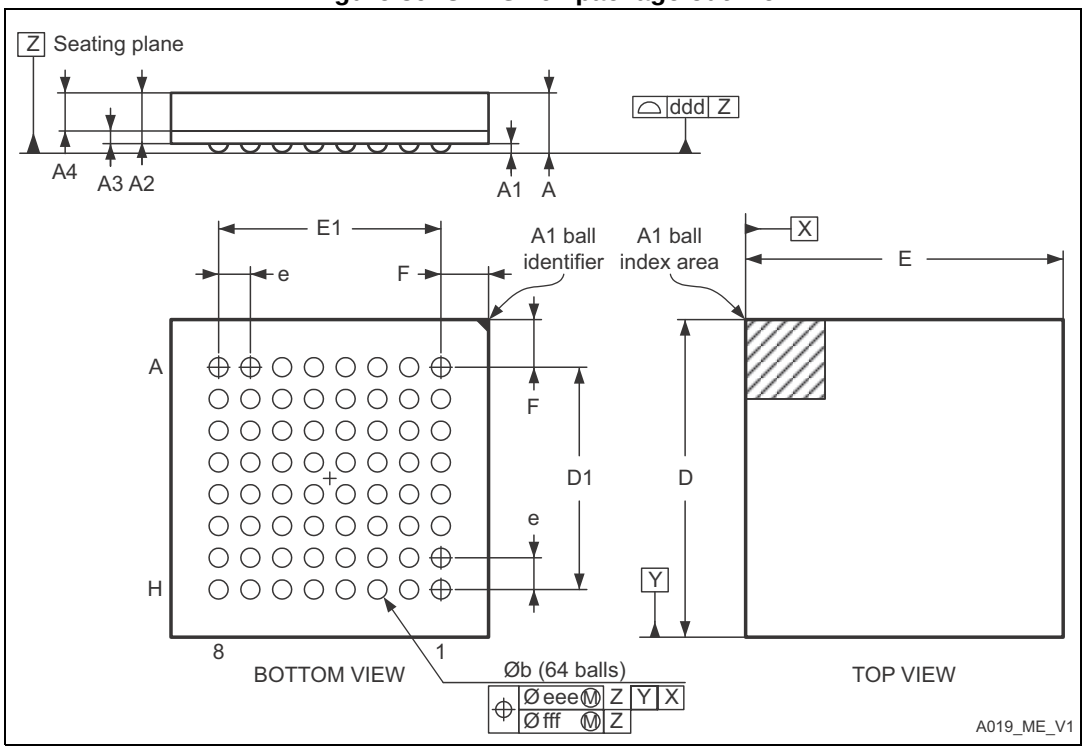


1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

7.3 UFBGA64 package information

UFBGA64 is a 64-ball, 5 x 5 mm, 0.5 mm pitch ultra-fine-profile ball grid array package.

Figure 39. UFBGA64 package outline



1. Drawing is not to scale.

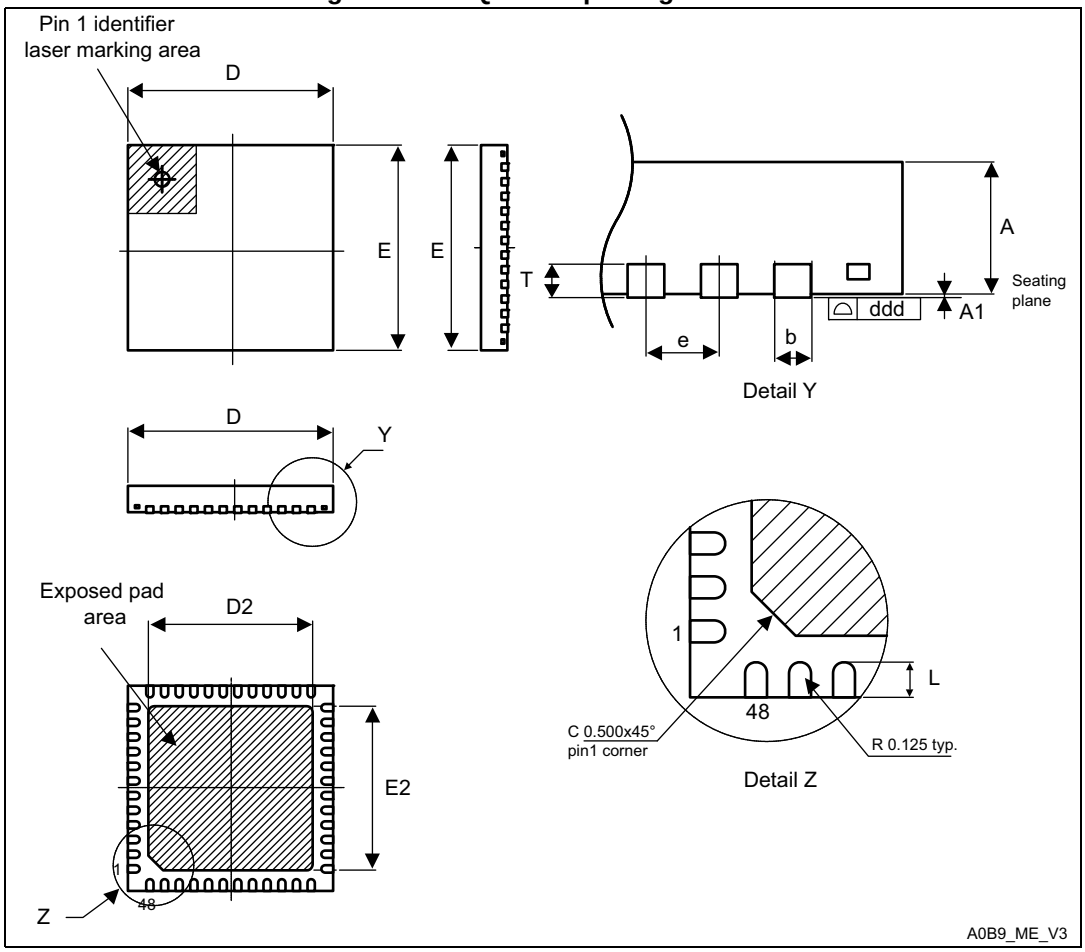
Table 73. UFBGA64 package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.460	0.530	0.600	0.0181	0.0209	0.0236
A1	0.050	0.080	0.110	0.0020	0.0031	0.0043
A2	0.400	0.450	0.500	0.0157	0.0177	0.0197
A3	0.080	0.130	0.180	0.0031	0.0051	0.0071
A4	0.270	0.320	0.370	0.0106	0.0126	0.0146
b	0.170	0.280	0.330	0.0067	0.0110	0.0130
D	4.850	5.000	5.150	0.1909	0.1969	0.2028
D1	3.450	3.500	3.550	0.1358	0.1378	0.1398
E	4.850	5.000	5.150	0.1909	0.1969	0.2028
E1	3.450	3.500	3.550	0.1358	0.1378	0.1398
e	-	0.500	-	-	0.0197	-
F	0.700	0.750	0.800	0.0276	0.0295	0.0315

7.7 UFQFPN48 package information

UFQFPN48 is a 48-lead, 7x7 mm, 0.5 mm pitch, ultra-thin fine-pitch quad flat package.

Figure 51. UFQFPN48 package outline



1. Drawing is not to scale.
2. All leads/pads should also be soldered to the PCB to improve the lead/pad solder joint life.
3. There is an exposed die pad on the underside of the UFQFPN package. It is recommended to connect and solder this back-side pad to PCB ground.

Each temperature range suffix corresponds to a specific guaranteed ambient temperature at maximum dissipation and, to a specific maximum junction temperature.

As applications do not commonly use the STM32F091xB/xC at maximum dissipation, it is useful to calculate the exact power consumption and junction temperature to determine which temperature range will be best suited to the application.

The following examples show how to calculate the temperature range needed for a given application.

Example 1: High-performance application

Assuming the following application conditions:

Maximum temperature T_{Amax} = 82 °C (measured according to JESD51-2), I_{DDmax} = 50 mA, V_{DD} = 3.5 V, maximum 20 I/Os used at the same time in output at low level with I_{OL} = 8 mA, V_{OL}= 0.4 V and maximum 8 I/Os used at the same time in output at low level with I_{OL} = 20 mA, V_{OL}= 1.3 V

P_{INTmax} = 50 mA × 3.5 V= 175 mW

P_{IOmax} = 20 × 8 mA × 0.4 V + 8 × 20 mA × 1.3 V = 272 mW

This gives: P_{INTmax} = 175 mW and P_{IOmax} = 272 mW:

P_{Dmax} = 175 + 272 = 447 mW

Using the values obtained in *Table 80* T_{Jmax} is calculated as follows:

– For LQFP64, 45 °C/W

T_{Jmax} = 82 °C + (45 °C/W × 447 mW) = 82 °C + 20.115 °C = 102.115 °C

This is within the range of the suffix 6 version parts (–40 < T_J < 105 °C).

In this case, parts must be ordered at least with the temperature range suffix 6 (see *Section 8: Ordering information*).

Note: With this given P_{Dmax} we can find the T_{Amax} allowed for a given device temperature range (order code suffix 6 or 7).

Suffix 6: $T_{Amax} = T_{Jmax}$ - (45°C/W × 447 mW) = 105-20.115 = 84.885 °C

Suffix 7: $T_{Amax} = T_{Jmax}$ - (45°C/W × 447 mW) = 125-20.115 = 104.885 °C

Example 2: High-temperature application

Using the same rules, it is possible to address applications that run at high temperatures with a low dissipation, as long as junction temperature T_J remains within the specified range.

Assuming the following application conditions:

Maximum temperature T_{Amax} = 100 °C (measured according to JESD51-2), I_{DDmax} = 20 mA, V_{DD} = 3.5 V, maximum 20 I/Os used at the same time in output at low level with I_{OL} = 8 mA, V_{OL}= 0.4 V

P_{INTmax} = 20 mA × 3.5 V= 70 mW

P_{IOmax} = 20 × 8 mA × 0.4 V = 64 mW

This gives: P_{INTmax} = 70 mW and P_{IOmax} = 64 mW:

P_{Dmax} = 70 + 64 = 134 mW

Thus: P_{Dmax} = 134 mW

8 Ordering information

For a list of available options (memory, package, and so on) or for further information on any aspect of this device, please contact your nearest ST sales office.

Table 81. Ordering information scheme

Example: STM32 F 091 R C T 6 x

Device family

STM32 = ARM-based 32-bit microcontroller

Product type

F = General-purpose

Sub-family

091= STM32F091xx

Pin count

C = 48 pins
R = 64 pins
V = 100 pins

User code memory size

B = 128 Kbyte
C = 256 Kbyte

Package

H = UFBGA
T = LQFP
U = UFQFPN
Y = WLCSP

Temperature range

6 = –40 to 85 °C
7 = –40 to 105 °C

Options

xxx = code ID of programmed parts (includes packing type)
TR = tape and reel packing
blank = tray packing