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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	CANbus, I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	DMA, I ² S, POR, PWM, WDT
Number of I/O	38
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 13x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-UFQFN Exposed Pad
Supplier Device Package	48-UFQFPN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f091ccu7

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3.4 Cyclic redundancy check calculation unit (CRC)

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code using a configurable generator polynomial value and size.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

3.5 **Power management**

3.5.1 Power supply schemes

- $V_{DD} = V_{DDIO1} = 2.0$ to 3.6 V: external power supply for I/Os (V_{DDIO1}) and the internal regulator. It is provided externally through VDD pins.
- V_{DDA} = from V_{DD} to 3.6 V: external analog power supply for ADC, DAC, Reset blocks, RCs and PLL (minimum voltage to be applied to V_{DDA} is 2.4 V when the ADC or DAC are used). It is provided externally through VDDA pin. The V_{DDA} voltage level must be always greater or equal to the V_{DD} voltage level and must be established first.
- V_{DDIO2} = 1.65 to 3.6 V: external power supply for marked I/Os. V_{DDIO2} is provided externally through the VDDIO2 pin. The V_{DDIO2} voltage level is completely independent from V_{DD} or V_{DDA}, but it must not be provided without a valid supply on V_{DD}. The V_{DDIO2} supply is monitored and compared with the internal reference voltage (V_{REFINT}). When the V_{DDIO2} is below this threshold, all the I/Os supplied from this rail are disabled by hardware. The output of this comparator is connected to EXTI line 31 and it can be used to generate an interrupt. Refer to the pinout diagrams or tables for concerned I/Os list.
- V_{BAT} = 1.65 to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.

For more details on how to connect power pins, refer to *Figure 13: Power supply scheme*.

3.5.2 Power supply supervisors

The device has integrated power-on reset (POR) and power-down reset (PDR) circuits. They are always active, and ensure proper operation above a threshold of 2 V. The device remains in reset mode when the monitored supply voltage is below a specified threshold, $V_{\text{POR/PDR}}$, without the need for an external reset circuit.

- The POR monitors only the V_{DD} supply voltage. During the startup phase it is required that V_{DDA} should arrive first and be greater than or equal to V_{DD}.
- The PDR monitors both the V_{DD} and V_{DDA} supply voltages, however the V_{DDA} power supply supervisor can be disabled (by programming a dedicated Option bit) to reduce the power consumption if the application design ensures that V_{DDA} is higher than or equal to V_{DD}.

The device features an embedded programmable voltage detector (PVD) that monitors the V_{DD} power supply and compares it to the V_{PVD} threshold. An interrupt can be generated when V_{DD} drops below the V_{PVD} threshold and/or when V_{DD} is higher than the V_{PVD}



Additionally, also the internal RC 48 MHz oscillator can be selected for system clock or PLL input source. This oscillator can be automatically fine-trimmed by the means of the CRS peripheral using the external synchronization.

3.7 General-purpose inputs/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions.

The I/O configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

3.8 Direct memory access controller (DMA)

The 12-channel general-purpose DMAs (seven channels for DMA1 and five channels for DMA2) manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers.

The DMAs support circular buffer management, removing the need for user code intervention when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with support for software trigger on each channel. Configuration is made by software and transfer sizes between source and destination are independent.

DMA can be used with the main peripherals: SPIx, I2Sx, I2Cx, USARTx, all TIMx timers (except TIM14), DAC and ADC.

3.9 Interrupts and events

3.9.1 Nested vectored interrupt controller (NVIC)

The STM32F0xx family embeds a nested vectored interrupt controller able to handle up to 32 maskable interrupt channels (not including the 16 interrupt lines of $Cortex^{\mathbb{R}}$ -M0) and 4 priority levels.

- Closely coupled NVIC gives low latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of late arriving higher priority interrupts
- Support for tail-chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimal interrupt latency.



3.19 High-definition multimedia interface (HDMI) - consumer electronics control (CEC)

The device embeds a HDMI-CEC controller that provides hardware support for the Consumer Electronics Control (CEC) protocol (Supplement 1 to the HDMI standard).

This protocol provides high-level control functions between all audiovisual products in an environment. It is specified to operate at low speeds with minimum processing and memory overhead. It has a clock domain independent from the CPU clock, allowing the HDMI_CEC controller to wakeup the MCU from Stop mode on data reception.

3.20 Controller area network (CAN)

The CAN is compliant with specifications 2.0A and B (active) with a bit rate up to 1 Mbit/s. It can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. It has three transmit mailboxes, two receive FIFOs with 3 stages and 14 scalable filter banks.

3.21 Clock recovery system (CRS)

The STM32F091xB/xC embeds a special block which allows automatic trimming of the internal 48 MHz oscillator to guarantee its optimal accuracy over the whole device operational range. This automatic trimming is based on the external synchronization signal, which could be either derived from LSE oscillator, from an external signal on CRS_SYNC pin or generated by user software. For faster lock-in during startup it is also possible to combine automatic trimming with manual trimming action.

3.22 Serial wire debug port (SW-DP)

An ARM SW-DP interface is provided to allow a serial wire debugging tool to be connected to the MCU.



	Pi	n nui	mber	s				-		Pin functions		
UFBGA100	LQFP100	UFBGA64	LQFP64	WLCSP64	LQFP48/UFQFPN48	Pin name (function upon reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions	
L4	31	G4	22	G5	16	PA6	I/O	ТТа		SPI1_MISO, I2S1_MCK, TIM3_CH1, TIM1_BKIN, TIM16_CH1, COMP1_OUT, TSC_G2_IO3, EVENTOUT, USART3_CTS	ADC_IN6	
M4	32	H4	23	E4	17	PA7	I/O	ТТа	Ta SPI1_MOSI, I2S1 TIM3_CH2, TIM14_ TIM1_CH1N, TIM17 COMP2_OUT TSC_G2_IO4 EVENTOUT		ADC_IN7	
K5	33	H5	24	H5	1	PC4	I/O	TTa		EVENTOUT, USART3_TX	ADC_IN14	
L5	34	H6	25	F4	-	PC5	I/O	ТТа		TSC_G3_IO1, USART3_RX	ADC_IN15, WKUP5	
M5	35	F5	26	G4	18	PB0	I/O	ТТа		TIM3_CH3, TIM1_CH2N, TSC_G3_IO2, EVENTOUT, USART3_CK	ADC_IN8	
M6	36	G5	27	F3	19	PB1	I/O	ТТа		TIM3_CH4, USART3_RTS, TIM14_CH1, TIM1_CH3N, TSC_G3_IO3	ADC_IN9	
L6	37	G6	28	H4	20	PB2	I/O	FT		TSC_G3_IO4	-	
M7	38	-	-	-	-	PE7	I/O	FT		TIM1_ETR, USART5_CK_RTS	-	
L7	39	-	-	-	-	PE8	I/O	FT		TIM1_CH1N, USART4_TX	-	
M8	40	-	-	-	-	PE9	I/O	FT		TIM1_CH1, USART4_RX	-	
L8	41	-	-	-	-	PE10	I/O	FT		TIM1_CH2N, USART5_TX	-	
M9	42	-	-	-	-	PE11	I/O	FT		TIM1_CH2, USART5_RX	-	
L9	43	-	-	-	-	PE12	I/O	FT		SPI1_NSS, I2S1_WS, TIM1_CH3N	-	
M10	44	-	-	-	-	PE13	I/O	FT		SPI1_SCK, I2S1_CK, TIM1_CH3	-	

			, ,, n
Table 13. STM32	2F091xB/xC pin	definitions	(continued)



5 Memory mapping

To the difference of STM32F091xC memory map in *Figure 10*, the two bottom code memory spaces of STM32F091xB end at 0x0001 FFFF and 0x0801 FFFF, respectively.







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Bus	Boundary address	Size	Peripheral
	0x4001 5C00 - 0x4001 7FFF	9 KB	Reserved
	0x4001 5800 - 0x4001 5BFF	1 KB	DBGMCU
	0x4001 4C00 - 0x4001 57FF	3 KB	Reserved
	0x4001 4800 - 0x4001 4BFF	1 KB	TIM17
	0x4001 4400 - 0x4001 47FF	1 KB	TIM16
	0x4001 4000 - 0x4001 43FF	1 KB	TIM15
	0x4001 3C00 - 0x4001 3FFF	1 KB	Reserved
	0x4001 3800 - 0x4001 3BFF	1 KB	USART1
	0x4001 3400 - 0x4001 37FF	1 KB	Reserved
	0x4001 3000 - 0x4001 33FF	1 KB	SPI1/I2S1
APB	0x4001 2C00 - 0x4001 2FFF	1 KB	TIM1
	0x4001 2800 - 0x4001 2BFF	1 KB	Reserved
	0x4001 2400 - 0x4001 27FF	1 KB	ADC
	0x4001 2000 - 0x4001 23FF	1 KB	Reserved
	0x4001 1C00 – 0x4001 1FFF	1 KB	USART8
	0x4001 1800 – 0x4001 1BFF	1 KB	USART7
	0x4001 1400 – 0x4001 17FF	1 KB	USART6
	0x4001 0800 - 0x4001 13FF	3 KB	Reserved
	0x4001 0400 - 0x4001 07FF	1 KB	EXTI
	0x4001 0000 - 0x4001 03FF	1 KB	SYSCFG + COMP
	0x4000 8000 - 0x4000 FFFF	32 KB	Reserved

Table 20. STM32F091xB/xC peripheral register boundary addresses (continued)



Bus	Boundary address	Size	Peripheral
	0x4000 7C00 - 0x4000 7FFF	1 KB	Reserved
	0x4000 7800 - 0x4000 7BFF	1 KB	CEC
	0x4000 7400 - 0x4000 77FF	1 KB	DAC
	0x4000 7000 - 0x4000 73FF	1 KB	PWR
	0x4000 6C00 - 0x4000 6FFF	1 KB	CRS
	0x4000 6800 - 0x4000 6BFF	1 KB	Reserved
	0x4000 6400 - 0x4000 67FF	1 KB	BxCAN
	0x4000 6100 - 0x4000 63FF	768 B	Reserved
	0x4000 6000 - 0x4000 60FF	256 B	CAN RAM
	0x4000 5C00 - 0x4000 5FFF	1 KB	Reserved
	0x4000 5800 - 0x4000 5BFF	1 KB	I2C2
	0x4000 5400 - 0x4000 57FF	1 KB	I2C1
	0x4000 5000 - 0x4000 53FF	1 KB	USART5
	0x4000 4C00 - 0x4000 4FFF	1 KB	USART4
	0x4000 4800 - 0x4000 4BFF	1 KB	USART3
	0x4000 4400 - 0x4000 47FF	1 KB	USART2
	0x4000 3C00 - 0x4000 43FF	2 KB	Reserved
APB	0x4000 3800 - 0x4000 3BFF	1 KB	SPI2
	0x4000 3400 - 0x4000 37FF	1 KB	Reserved
	0x4000 3000 - 0x4000 33FF	1 KB	IWDG
	0x4000 2C00 - 0x4000 2FFF	1 KB	WWDG
	0x4000 2800 - 0x4000 2BFF	1 KB	RTC
	0x4000 2400 - 0x4000 27FF	1 KB	Reserved
	0x4000 2000 - 0x4000 23FF	1 KB	TIM14
	0x4000 1800 - 0x4000 1FFF	2 KB	Reserved
	0x4000 1400 - 0x4000 17FF	1 KB	TIM7
	0x4000 1000 - 0x4000 13FF	1 KB	TIM6
	0x4000 0800 - 0x4000 0FFF	2 KB	Reserved
	0x4000 0400 - 0x4000 07FF	1 KB	TIM3
	0x4000 0000 - 0x4000 03FF	1 KB	TIM2

Table 20. STM32F091xB/xC peripheral register boundary addresses (continued)



6 Electrical characteristics

6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

6.1.1 Minimum and maximum values

Unless otherwise specified, the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at $T_A = 25$ °C and $T_A = T_A max$ (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean $\pm 3\sigma$).

6.1.2 Typical values

Unless otherwise specified, typical data are based on $T_A = 25$ °C, $V_{DD} = V_{DDA} = 3.3$ V. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean $\pm 2\sigma$).

6.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 11*.

6.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 12*.





		Conditions	Typ @ V _{BAT}									
Symbol	Parameter		1.65 V	1.8 V	2.4 V	2.7 V	3.3 V	3.6 V	T _A = 25 °C	T _A = 85 °C	T _A = 105 °C	Unit
I _{DD_VBAT}	RTC domain supply current	LSE & RTC ON; "Xtal mode": lower driving capability; LSEDRV[1:0] = '00'	0.5	0.5	0.6	0.7	0.9	1.0	1.0	1.3	1.8	
		LSE & RTC ON; "Xtal mode" higher driving capability; LSEDRV[1:0] = '11'	0.8	0.8	0.9	1.0	1.2	1.3	1.4	1.7	2.2	

Table 32. Typical and maximum current consumption from the $\rm V_{BAT}$ supply

1. Data based on characterization results, not tested in production.

Typical current consumption

The MCU is placed under the following conditions:

- V_{DD} = V_{DDA} = 3.3 V
- All I/O pins are in analog input configuration
- The Flash memory access time is adjusted to f_{HCLK} frequency:
 - 0 wait state and Prefetch OFF from 0 to 24 MHz
 - 1 wait state and Prefetch ON above 24 MHz
- When the peripherals are enabled, f_{PCLK} = f_{HCLK}
- PLL is used for frequencies greater than 8 MHz
- AHB prescaler of 2, 4, 8 and 16 is used for the frequencies 4 MHz, 2 MHz, 1 MHz and 500 kHz respectively



High-speed internal 14 MHz (HSI14) RC oscillator (dedicated to ADC)

Symbol	Parameter	Conditions	Min	Тур	Max	Unit			
f _{HSI14}	Frequency	-	-	14	-	MHz			
TRIM	HSI14 user-trimming step	-	-	-	1 ⁽²⁾	%			
DuCy _(HSI14)	Duty cycle	-	45 ⁽²⁾	-	55 ⁽²⁾	%			
		$T_A = -40$ to 105 °C	-4.2 ⁽³⁾	-	5.1 ⁽³⁾	%			
ACC	Accuracy of the HSI14 oscillator (factory calibrated)	T _A = −10 to 85 °C	-3.2 ⁽³⁾	-	3.1 ⁽³⁾	%			
ACC _{HSI14}		T _A = 0 to 70 °C	-2.5 ⁽³⁾	-	2.3 ⁽³⁾	%			
		T _A = 25 °C	-1	-	1	%			
t _{su(HSI14)}	HSI14 oscillator startup time	-	1 ⁽²⁾	-	2 ⁽²⁾	μs			
I _{DDA(HSI14)}	HSI14 oscillator power consumption	-	_	100	150 ⁽²⁾	μA			

Table 42. HSI14 oscillator characteristics⁽¹⁾

1. V_{DDA} = 3.3 V, T_A = -40 to 105 °C unless otherwise specified.

2. Guaranteed by design, not tested in production.

3. Data based on characterization results, not tested in production.



Figure 20. HSI14 oscillator accuracy characterization results



Input/output AC characteristics

The definition and values of input/output AC characteristics are given in *Figure 24* and *Table 55*, respectively. Unless otherwise specified, the parameters given are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 24: General operating conditions*.

OSPEEDRy [1:0] value ⁽¹⁾	Symbol	Parameter	Conditions	Min	Max	Unit			
	f _{max(IO)out}	Maximum frequency ⁽³⁾		-	2	MHz			
	t _{f(IO)out}	Output fall time	C _L = 50 pF, V _{DDIOx} ≥ 2 V	-	125	ns			
x0	t _{r(IO)out}	Output rise time		-	125				
×0	f _{max(IO)out}	Maximum frequency ⁽³⁾		-	1	MHz			
	t _{f(IO)out}	Output fall time	C _L = 50 pF, V _{DDIOx} < 2 V	-	125	ne			
	t _{r(IO)out}	Output rise time		-	125	115			
01	f _{max(IO)out}	Maximum frequency ⁽³⁾		-	10	MHz			
	t _{f(IO)out}	Output fall time	$C_L = 50 \text{ pF}, V_{DDIOx} \ge 2 \text{ V}$	-	25	00			
	t _{r(IO)out}	Output rise time		-	25	ns			
	f _{max(IO)out}	Maximum frequency ⁽³⁾		-	4	MHz			
	t _{f(IO)out}	Output fall time	C_L = 50 pF, V_{DDIOx} < 2 V	-	62.5	ns			
	t _{r(IO)out}	Output rise time		-	62.5	115			
	f		C_L = 30 pF, $V_{DDIOx} \ge 2.7 V$		50				
		Maximum frequency ⁽³⁾	$C_L = 50 \text{ pF}, V_{\text{DDIOx}} \ge 2.7 \text{ V}$						
	'max(IO)out		C_L = 50 pF, 2 V ≤ V_{DDIOx} < 2.7 V	-	20				
			C_L = 50 pF, V_{DDIOx} < 2 V	-	10				
			C_L = 30 pF, $V_{DDIOx} \ge 2.7 V$	-	5				
11	town	Output fall time	$C_L = 50 \text{ pF}, V_{DDIOx} \ge 2.7 \text{ V}$	-	8				
	۲(IO)out		C_L = 50 pF, 2 V \leq V _{DDIOx} $<$ 2.7 V	-	12				
			C _L = 50 pF, V _{DDIOx} < 2 V	-	25	ne			
			C_L = 30 pF, $V_{DDIOx} \ge 2.7 V$	-	5	115			
	+	Output rise time	$C_L = 50 \text{ pF}, V_{DDIOx} \ge 2.7 \text{ V}$	-	8				
	чr(IO)out		$C_{L} = 50 \text{ pF}, 2 \text{ V} \le \text{V}_{\text{DDIOx}} < 2.7 \text{ V}$	-	12				
			$C_L = 50 \text{ pF}, V_{DDIOx} < 2 \text{ V}$	-	25	1			

Table 55. I/O AC characteristics⁽¹⁾⁽²⁾



Symbol	Parameter	Min	Тур	Мах	Unit	Comments
Gain error ⁽³⁾	Gain error	-	-	±0.5	%	Given for the DAC in 12-bit configuration
t _{SETTLING} ⁽³⁾	Settling time (full scale: for a 10-bit input code transition between the lowest and the highest input codes when DAC_OUT reaches final value ±1LSB			C _{LOAD} ≤ 50 pF, R _{LOAD} ≥ 5 kΩ		
Update rate ⁽³⁾	Max frequency for a correct DAC_OUT change when small variation in the input code (from code i to i+1LSB)		-	1	MS/s	C _{LOAD} ≤ 50 pF, R _{LOAD} ≥ 5 kΩ
t _{WAKEUP} ⁽³⁾	³⁾ Wakeup time from off state (Setting the ENx bit in the DAC Control register)		6.5	10	μs	$C_{LOAD} \le 50 \text{ pF}, R_{LOAD} \ge 5 \text{ k}\Omega$ input code between lowest and highest possible ones.
PSRR+ ⁽¹⁾	Power supply rejection ratio (to V _{DDA}) (static DC measurement	-	-67	-40	dB	No R _{LOAD} , C _{LOAD} = 50 pF

Table 60.	DAC	characteristics	(continued)
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1. Guaranteed by design, not tested in production.

2. The DAC is in "quiescent mode" when it keeps the value steady on the output so no dynamic consumption is involved.

3. Data based on characterization results, not tested in production.



Prescaler divider PR[2:0] bits		Min timeout RL[11:0]= 0x000	Max timeout RL[11:0]= 0xFFF	Unit				
/4	0	0.1	409.6					
/8	1	0.2	819.2					
/16	2	0.4	1638.4					
/32	3	0.8	3276.8	ms				
/64	4	1.6	6553.6					
/128	5	3.2	13107.2					
/256	6 or 7	6.4	26214.4					

Table 65. IWDG min/max timeout period at 40 kHz (LSI)⁽¹⁾

1. These timings are given for a 40 kHz clock but the microcontroller internal RC frequency can vary from 30 to 60 kHz. Moreover, given an exact RC oscillator frequency, the exact timings still depend on the phasing of the APB interface clock versus the LSI clock so that there is always a full RC period of uncertainty.

Prescaler	WDGTB	Min timeout value	Max timeout value	Unit
1	0	0.0853	5.4613	
2	1	0.1706	10.9226	me
4	2	0.3413	21.8453	1115
8	3	0.6826	43.6906	

Table 66. WWDG min/max timeout value at 48 MHz (PCLK)

6.3.22 Communication interfaces

I²C interface characteristics

The I^2C interface meets the timings requirements of the I^2C -bus specification and user manual rev. 03 for:

- Standard-mode (Sm): with a bit rate up to 100 kbit/s
- Fast-mode (Fm): with a bit rate up to 400 kbit/s
- Fast-mode Plus (Fm+): with a bit rate up to 1 Mbit/s.

The I²C timings requirements are guaranteed by design when the I2Cx peripheral is properly configured (refer to Reference manual).

The SDA and SCL I/O requirements are met with the following restrictions: the SDA and SCL I/O pins are not "true" open-drain. When configured as open-drain, the PMOS connected between the I/O pin and V_{DDIOx} is disabled, but is still present. Only FTf I/O pins support Fm+ low level output current maximum requirement. Refer to Section 6.3.14: I/O port characteristics for the I²C I/Os characteristics.

All I²C SDA and SCL I/Os embed an analog filter. Refer to the table below for the analog filter characteristics:



7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK[®] is an ST trademark.

7.1 UFBGA100 package information

UFBGA100 is a 100-ball, 7 x 7 mm, 0.50 mm pitch, ultra-fine-profile ball grid array package.



Figure 33. UFBGA100 package outline

1. Drawing is not to scale.

Table 70. UFBGA100	package mechanical data
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Symbol	millimeters			inches ⁽¹⁾		
	Min.	Тур.	Max.	Min.	Тур.	Max.
А	-	-	0.600	-	-	0.0236
A1	-	-	0.110	-	-	0.0043
A2	-	0.450	-	-	0.0177	-
A3	-	0.130	-	-	0.0051	0.0094
A4	-	0.320	-	-	0.0126	-



Device marking

The following figure gives an example of topside marking orientation versus ball A1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.





 Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.



7.5 LQFP64 package information

LQFP64 is a 64-pin, 10 x 10 mm low-profile quad flat package.



Figure 45. LQFP64 package outline

1. Drawing is not to scale.

Table 77. LQFP64	package	mechanical	data
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Symbol	millimeters			inches ⁽¹⁾		
	Min	Тур	Max	Min	Тур	Max
А	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
С	0.090	-	0.200	0.0035	-	0.0079
D	-	12.000	-	-	0.4724	-
D1	-	10.000	-	-	0.3937	-
D3	-	7.500	-	-	0.2953	-
E	-	12.000	-	-	0.4724	-
E1	-	10.000	-	-	0.3937	-



7.8 Thermal characteristics

The maximum chip junction temperature (T_J max) must never exceed the values given in *Table 24: General operating conditions*.

The maximum chip-junction temperature, $T_{\rm J}$ max, in degrees Celsius, may be calculated using the following equation:

$$T_J max = T_A max + (P_D max x \Theta_{JA})$$

Where:

- T_A max is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- P_D max is the sum of P_{INT} max and P_{I/O} max (P_D max = P_{INT} max + P_{I/O}max),
- P_{INT} max is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.

 $\mathsf{P}_{\mathsf{I}\!/\!\mathsf{O}}$ max represents the maximum power dissipation on output pins where:

 $\mathsf{P}_{\mathsf{I}/\mathsf{O}} \max = \Sigma \; (\mathsf{V}_{\mathsf{OL}} \times \mathsf{I}_{\mathsf{OL}}) + \Sigma \; ((\mathsf{V}_{\mathsf{DDIOx}} - \mathsf{V}_{\mathsf{OH}}) \times \mathsf{I}_{\mathsf{OH}}),$

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Symbol	Parameter	Value	Unit
ΘjA	Thermal resistance junction-ambient UFBGA100 - 7 × 7 mm	55	
	Thermal resistance junction-ambient LQFP100 - 14 × 14 mm	42	
	Thermal resistance junction-ambient UFBGA64 - 5 × 5 mm / 0.5 mm pitch	65	
	Thermal resistance junction-ambient LQFP64 - 10 × 10 mm / 0.5 mm pitch	44	°C/W
	Thermal resistance junction-ambient WLCSP64 - 0.4 mm pitch	53	
	Thermal resistance junction-ambient LQFP48 - 7 × 7 mm	54	
	Thermal resistance junction-ambient UFQFPN48 - 7 × 7 mm	32	

Table 80. Package thermal characteristics

7.8.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org

7.8.2 Selecting the product temperature range

When ordering the microcontroller, the temperature range is specified in the ordering information scheme shown in *Section 8: Ordering information*.



Using the values obtained in *Table 80* T_{Jmax} is calculated as follows:

- For LQFP64, 45 °C/W
- T_{Jmax} = 100 °C + (45 °C/W × 134 mW) = 100 °C + 6.03 °C = 106.03 °C

This is above the range of the suffix 6 version parts ($-40 < T_J < 105 \text{ °C}$).

In this case, parts must be ordered at least with the temperature range suffix 7 (see *Section 8: Ordering information*) unless we reduce the power dissipation in order to be able to use suffix 6 parts.

Refer to the figure below to select the required temperature range (suffix 6 or 7) according to your temperature or power requirements.





