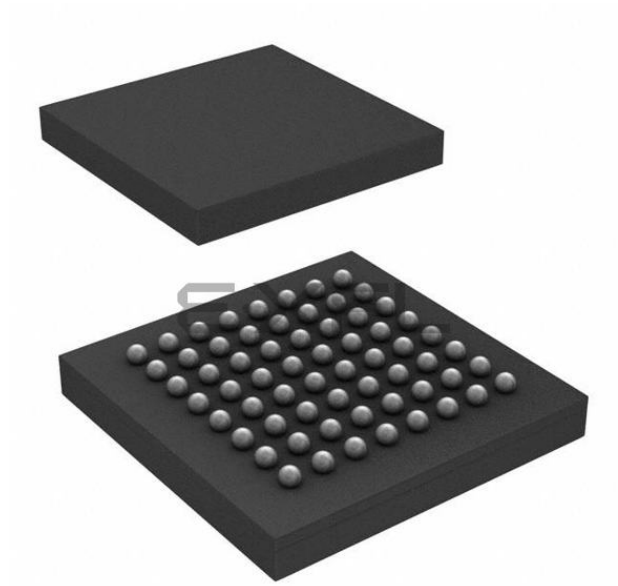

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	DMA, I²S, POR, PWM, WDT
Number of I/O	52
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 19x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-UFBGA, WLCSP
Supplier Device Package	64-WLCSP (3.35x3.59)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f091rcy6tr

Contents

Table 10. STM32F091xB/xC USART implementation (continued)

USART modes/features(1)	USART1 USART2 USART3	USART4	USART5 USART6 USART7 USART8
Single-wire half-duplex communication	X	X	X
IrDA SIR ENDEC block	X	-	-
LIN mode	X	-	-
Dual clock domain and wakeup from Stop mode	X	-	-
Receiver timeout interrupt	X	-	-
Modbus communication	X	-	-
Auto baud rate detection	X	-	-
Driver Enable	X	X	X

1. X = supported.

3.18 Serial peripheral interface (SPI) / Inter-integrated sound interface (I^2S)

Two SPIs are able to communicate up to 18 Mbit/s in slave and master modes in full-duplex and half-duplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame size is configurable from 4 bits to 16 bits.

Two standard I^2S interfaces (multiplexed with SPI1 and SPI2 respectively) supporting four different audio standards can operate as master or slave at half-duplex communication mode. They can be configured to transfer 16 and 24 or 32 bits with 16-bit or 32-bit data resolution and synchronized by a specific signal. Audio sampling frequency from 8 kHz up to 192 kHz can be set by an 8-bit programmable linear prescaler. When operating in master mode, they can output a clock for an external audio component at 256 times the sampling frequency.

Table 11. STM32F091xB/xC SPI/I^2S implementation

SPI features(1)	SPI1 and SPI2
Hardware CRC calculation	X
Rx/Tx FIFO	X
NSS pulse mode	X
I^2S mode	X
TI mode	X

1. X = supported.

Table 13. STM32F091xB/xC pin definitions (continued)

Pin numbers						Pin name (function upon reset)	Pin type	I/O structure	Notes	Pin functions	
UFBGA100	LQFP100	UFBGA64	LQFP64	WLCSP64	LQFP48/UFQFPN48					Alternate functions	Additional functions
L4	31	G4	22	G5	16	PA6	I/O	TTa		SPI1_MISO, I2S1_MCK, TIM3_CH1, TIM1_BKIN, TIM16_CH1, COMP1_OUT, TSC_G2_IO3, EVENTOUT, USART3_CTS	ADC_IN6
M4	32	H4	23	E4	17	PA7	I/O	TTa		SPI1_MOSI, I2S1_SD, TIM3_CH2, TIM14_CH1, TIM1_CH1N, TIM17_CH1, COMP2_OUT, TSC_G2_IO4, EVENTOUT	ADC_IN7
K5	33	H5	24	H5	-	PC4	I/O	TTa		EVENTOUT, USART3_TX	ADC_IN14
L5	34	H6	25	F4	-	PC5	I/O	TTa		TSC_G3_IO1, USART3_RX	ADC_IN15, WKUP5
M5	35	F5	26	G4	18	PB0	I/O	TTa		TIM3_CH3, TIM1_CH2N, TSC_G3_IO2, EVENTOUT, USART3_CK	ADC_IN8
M6	36	G5	27	F3	19	PB1	I/O	TTa		TIM3_CH4, USART3_RTS, TIM14_CH1, TIM1_CH3N, TSC_G3_IO3	ADC_IN9
L6	37	G6	28	H4	20	PB2	I/O	FT		TSC_G3_IO4	-
M7	38	-	-	-	-	PE7	I/O	FT		TIM1_ETR, USART5_CK_RTS	-
L7	39	-	-	-	-	PE8	I/O	FT		TIM1_CH1N, USART4_TX	-
M8	40	-	-	-	-	PE9	I/O	FT		TIM1_CH1, USART4_RX	-
L8	41	-	-	-	-	PE10	I/O	FT		TIM1_CH2N, USART5_TX	-
M9	42	-	-	-	-	PE11	I/O	FT		TIM1_CH2, USART5_RX	-
L9	43	-	-	-	-	PE12	I/O	FT		SPI1_NSS, I2S1_WS, TIM1_CH3N	-
M10	44	-	-	-	-	PE13	I/O	FT		SPI1_SCK, I2S1_CK, TIM1_CH3	-

Table 13. STM32F091xB/xC pin definitions (continued)

Pin numbers						Pin name (function upon reset)	Pin type	I/O structure	Notes	Pin functions	
UFBGA100	LQFP100	UFBGA64	LQFP64	WLCSP64	LQFP48/UFQFPN48					Alternate functions	Additional functions
C5	91	C4	57	C5	41	PB5	I/O	FT		SPI1_MOSI, I2S1_SD, I2C1_SMBA, TIM16_BKIN, TIM3_CH2, USART5_CK_RTS	WKUP6
B5	92	D3	58	A5	42	PB6	I/O	FTf		I2C1_SCL, USART1_TX, TIM16_CH1N, TSC_G5_I03	-
B4	93	C3	59	B5	43	PB7	I/O	FTf		I2C1_SDA, USART1_RX, USART4_CTS, TIM17_CH1N, TSC_G5_IO4	-
A4	94	B4	60	C6	44	PF11-BOOT0	I/O	FT		-	Boot memory selection
A3	95	B3	61	A6	45	PB8	I/O	FTf		I2C1_SCL, CEC, TIM16_CH1, TSC_SYNC, CAN_RX	-
B3	96	A3	62	B6	46	PB9	I/O	FTf		SPI2_NSS, I2S2_WS, I2C1_SDA, IR_OUT, TIM17_CH1, EVENTOUT, CAN_TX	-
C3	97	-	-	-	-	PE0	I/O	FT		EVENTOUT, TIM16_CH1	-
A2	98	-	-	-	-	PE1	I/O	FT		EVENTOUT, TIM17_CH1	-
D3	99	D4	63	A7	47	VSS	S	-		Ground	
C4	100	E4	64	A8	48	VDD	S	-		Digital power supply	

1. PC13, PC14 and PC15 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 in output mode is limited:
   - The speed should not exceed 2 MHz with a maximum load of 30 pF.
   - These GPIOs must not be used as current sources (e.g. to drive an LED).
2. After the first RTC domain power-up, PC13, PC14 and PC15 operate as GPIOs. Their function then depends on the content of the RTC registers which are not reset by the system reset. For details on how to manage these GPIOs, refer to the RTC domain and RTC register descriptions in the reference manual.
3. PC6, PC7, PC8, PC9, PA8, PA9, PA10, PA11, PA12, PA13, PF6, PA14, PA15, PC10, PC11, PC12, PD0, PD1 and PD2 I/Os are supplied by VDDIO2
4. After reset, these pins are configured as SWDIO and SWCLK alternate functions, and the internal pull-up on the SWDIO pin and the internal pull-down on the SWCLK pin are activated.

Table 16. Alternate functions selected through GPIOC_AFR registers for port C

Pin name	AF0	AF1	AF2
PC0	EVENTOUT	USART7_TX	USART6_TX
PC1	EVENTOUT	USART7_RX	USART6_RX
PC2	EVENTOUT	SPI2_MISO, I2S2_MCK	USART8_TX
PC3	EVENTOUT	SPI2_MOSI, I2S2_SD	USART8_RX
PC4	EVENTOUT	USART3_TX	-
PC5	TSC_G3_IO1	USART3_RX	-
PC6	TIM3_CH1	USART7_TX	-
PC7	TIM3_CH2	USART7_RX	-
PC8	TIM3_CH3	USART8_TX	-
PC9	TIM3_CH4	USART8_RX	-
PC10	USART4_TX	USART3_TX	-
PC11	USART4_RX	USART3_RX	-
PC12	USART4_CK	USART3_CK	USART5_TX
PC13	-	-	-
PC14	-	-	-
PC15	-	-	-

Table 17. Alternate functions selected through GPIOD_AFR registers for port D

Pin name	AF0	AF1	AF2
PD0	CAN_RX	SPI2_NSS, I2S2_WS	-
PD1	CAN_TX	SPI2_SCK, I2S2_CK	-
PD2	TIM3_ETR	USART3_RTS	USART5_RX
PD3	USART2_CTS	SPI2_MISO, I2S2_MCK	-
PD4	USART2_RTS	SPI2_MOSI, I2S2_SD	-
PD5	USART2_TX	-	-
PD6	USART2_RX	-	-
PD7	USART2_CK	-	-
PD8	USART3_TX	-	-
PD9	USART3_RX	-	-
PD10	USART3_CK	-	-
PD11	USART3_CTS	-	-
PD12	USART3_RTS	TSC_G8_IO1	USART8_CK_RTS
PD13	USART8_TX	TSC_G8_IO2	-
PD14	USART8_RX	TSC_G8_IO3	-
PD15	CRS_SYNC	TSC_G8_IO4	USART7_CK_RTS

Table 18. Alternate functions selected through GPIOE_AFR registers for port E

Pin name	AF0	AF1
PE0	TIM16_CH1	EVENTOUT
PE1	TIM17_CH1	EVENTOUT
PE2	TIM3_ETR	TSC_G7_IO1
PE3	TIM3_CH1	TSC_G7_IO2
PE4	TIM3_CH2	TSC_G7_IO3
PE5	TIM3_CH3	TSC_G7_IO4
PE6	TIM3_CH4	-
PE7	TIM1_ETR	USART5_CK_RTS
PE8	TIM1_CH1N	USART4_TX
PE9	TIM1_CH1	USART4_RX
PE10	TIM1_CH2N	USART5_TX
PE11	TIM1_CH2	USART5_RX
PE12	TIM1_CH3N	SPI1_NSS, I2S1_WS
PE13	TIM1_CH3	SPI1_SCK, I2S1_CK
PE14	TIM1_CH4	SPI1_MISO, I2S1_MCK
PE15	TIM1_BKIN	SPI1_MOSI, I2S1_SD

Table 19. Alternate functions selected through GPIOF_AFR registers for port F

Pin name	AF0	AF1	AF2
PF0	CRS_SYNC	I2C1_SDA	-
PF1	-	I2C1_SCL	-
PF2	EVENTOUT	USART7_TX	USART7_CK_RTS
PF3	EVENTOUT	USART7_RX	USART6_CK_RTS
PF6	-	-	-
PF9	TIM15_CH1	USART6_TX	-
PF10	TIM15_CH2	USART6_RX	-

Table 20. STM32F091xB/xC peripheral register boundary addresses (continued)

Bus	Boundary address	Size	Peripheral
APB	0x4000 7C00 - 0x4000 7FFF	1 KB	Reserved
	0x4000 7800 - 0x4000 7BFF	1 KB	CEC
	0x4000 7400 - 0x4000 77FF	1 KB	DAC
	0x4000 7000 - 0x4000 73FF	1 KB	PWR
	0x4000 6C00 - 0x4000 6FFF	1 KB	CRS
	0x4000 6800 - 0x4000 6BFF	1 KB	Reserved
	0x4000 6400 - 0x4000 67FF	1 KB	BxCAN
	0x4000 6100 - 0x4000 63FF	768 B	Reserved
	0x4000 6000 - 0x4000 60FF	256 B	CAN RAM
	0x4000 5C00 - 0x4000 5FFF	1 KB	Reserved
	0x4000 5800 - 0x4000 5BFF	1 KB	I2C2
	0x4000 5400 - 0x4000 57FF	1 KB	I2C1
	0x4000 5000 - 0x4000 53FF	1 KB	USART5
	0x4000 4C00 - 0x4000 4FFF	1 KB	USART4
	0x4000 4800 - 0x4000 4BFF	1 KB	USART3
	0x4000 4400 - 0x4000 47FF	1 KB	USART2
	0x4000 3C00 - 0x4000 43FF	2 KB	Reserved
	0x4000 3800 - 0x4000 3BFF	1 KB	SPI2
	0x4000 3400 - 0x4000 37FF	1 KB	Reserved
	0x4000 3000 - 0x4000 33FF	1 KB	IWDG
	0x4000 2C00 - 0x4000 2FFF	1 KB	WWDG
	0x4000 2800 - 0x4000 2BFF	1 KB	RTC
	0x4000 2400 - 0x4000 27FF	1 KB	Reserved
	0x4000 2000 - 0x4000 23FF	1 KB	TIM14
	0x4000 1800 - 0x4000 1FFF	2 KB	Reserved
	0x4000 1400 - 0x4000 17FF	1 KB	TIM7
	0x4000 1000 - 0x4000 13FF	1 KB	TIM6
	0x4000 0800 - 0x4000 0FFF	2 KB	Reserved
	0x4000 0400 - 0x4000 07FF	1 KB	TIM3
	0x4000 0000 - 0x4000 03FF	1 KB	TIM2

trigger circuits used to discriminate the input value. Unless this specific configuration is required by the application, this supply current consumption can be avoided by configuring these I/Os in analog mode. This is notably the case of ADC input pins which should be configured as analog inputs.

Caution: Any floating input pin can also settle to an intermediate voltage level or switch inadvertently, as a result of external electromagnetic noise. To avoid current consumption related to floating pins, they must either be configured in analog mode, or forced internally to a definite digital value. This can be done either by using pull-up/down resistors or by configuring the pins in output mode.

I/O dynamic current consumption

In addition to the internal peripheral current consumption measured previously (see *Table 35: Peripheral current consumption*), the I/Os used by an application also contribute to the current consumption. When an I/O pin switches, it uses the current from the I/O supply voltage to supply the I/O pin circuitry and to charge/discharge the capacitive load (internal or external) connected to the pin:

$$I_{SW} = V_{DDIOx} \times f_{SW} \times C$$

where

I_{SW} is the current sunk by a switching I/O to charge/discharge the capacitive load

V_{DDIOx} is the I/O supply voltage

f_{SW} is the I/O switching frequency

C is the total capacitance seen by the I/O pin: $C = C_{INT} + C_{EXT} + C_S$

C_S is the PCB board capacitance including the pad pin.

The test pin is configured in push-pull output mode and is toggled by software at a fixed frequency.

6.3.6 Wakeup time from low-power mode

The wakeup times given in *Table 36* are the latency between the event and the execution of the first user instruction. The device goes in low-power mode after the WFE (Wait For Event) instruction, in the case of a WFI (Wait For Interruption) instruction, 16 CPU cycles must be added to the following timings due to the interrupt latency in the Cortex M0 architecture.

The SYSCLK clock source setting is kept unchanged after wakeup from Sleep mode. During wakeup from Stop or Standby mode, SYSCLK takes the default setting: HSI 8 MHz.

The wakeup source from Sleep and Stop mode is an EXTI line configured in event mode. The wakeup source from Standby mode is the WKUP1 pin (PA0).

All timings are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 24: General operating conditions*.

Table 36. Low-power mode wakeup timings

Symbol	Parameter	Conditions	Typ @V_{DD} = V_{DDA}					Max	Unit
			= 2.0 V	= 2.4 V	= 2.7 V	= 3 V	= 3.3 V		
t_{WUSTOP}	Wakeup from Stop mode	Regulator in run mode	3.2	3.1	2.9	2.9	2.8	5	µs
		Regulator in low power mode	7.0	5.8	5.2	4.9	4.6	9	
$t_{WUSTANDBY}$	Wakeup from Standby mode	-	60.4	55.6	53.5	52	51	-	
$t_{WUSLEEP}$	Wakeup from Sleep mode	-	4 SYSCLK cycles					-	

6.3.7 External clock source characteristics

High-speed external user clock generated from an external source

In bypass mode the HSE oscillator is switched off and the input pin is a standard GPIO.

The external clock signal has to respect the I/O characteristics in *Section 6.3.14*. However, the recommended clock input waveform is shown in *Figure 15: High-speed external clock source AC timing diagram*.

Table 37. High-speed external user clock characteristics

Symbol	Parameter[1]	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency	-	8	32	MHz
V_{HSEH}	OSC_IN input pin high level voltage	0.7 V_{DDIOx}	-	V_{DDIOx}	V
V_{HSEL}	OSC_IN input pin low level voltage	V_{SS}	-	0.3 V_{DDIOx}	
$t_{w(HSEH)}$ $t_{w(HSEL)}$	OSC_IN high or low time	15	-	-	ns
$t_{r(HSE)}$ $t_{f(HSE)}$	OSC_IN rise or fall time	-	-	20	

Figure 22. TC and TTa I/O input characteristics

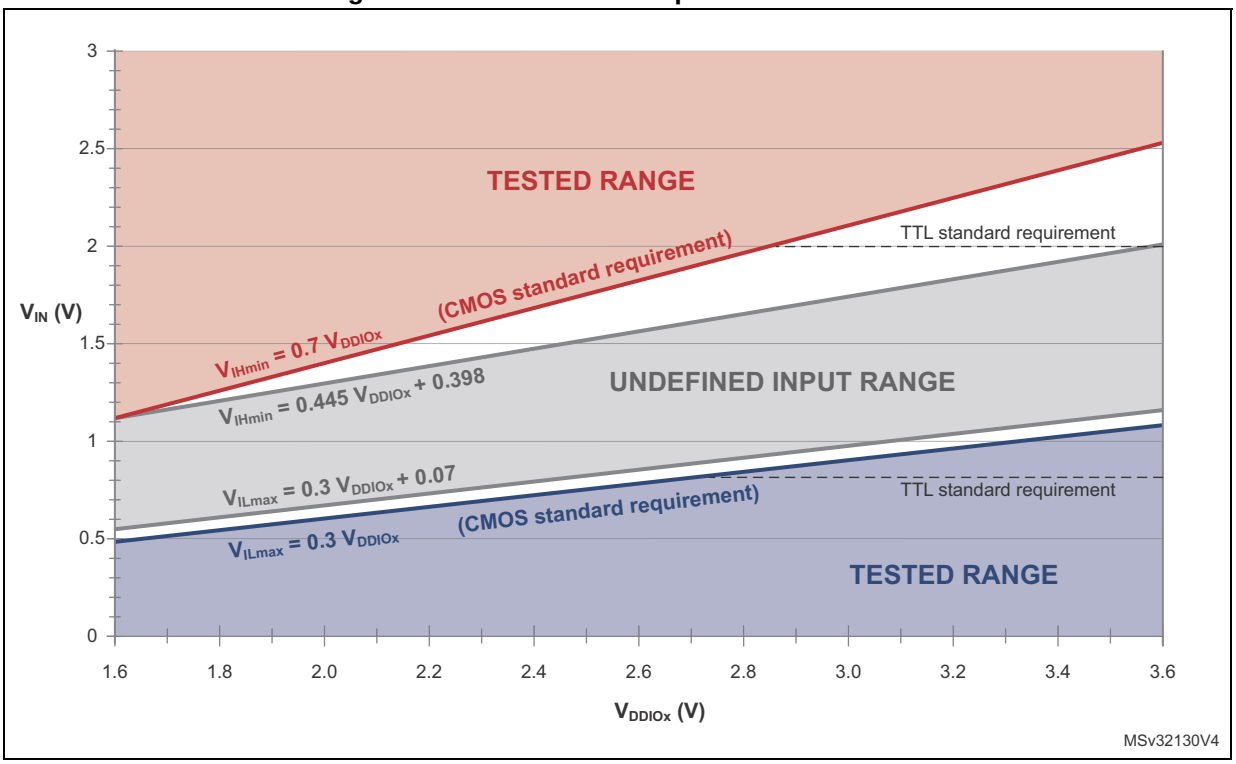


Figure 23. Five volt tolerant (FT and FTf) I/O input characteristics

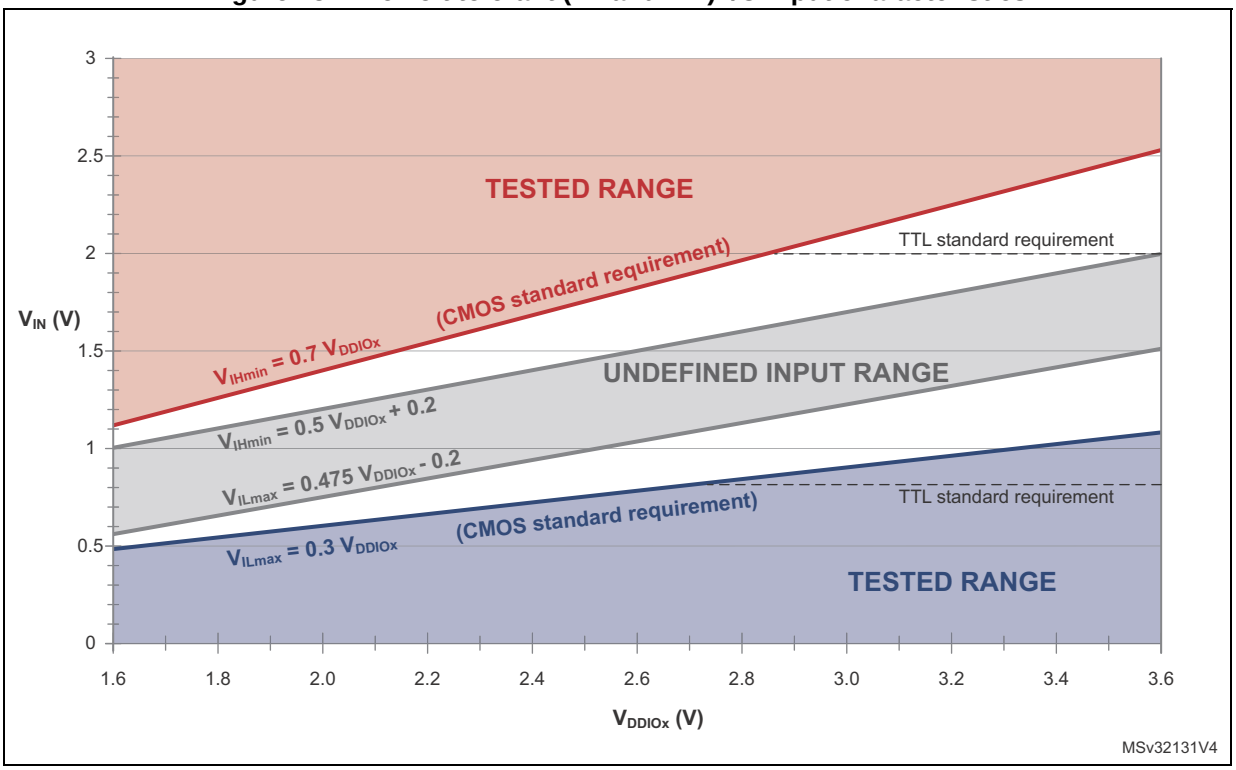


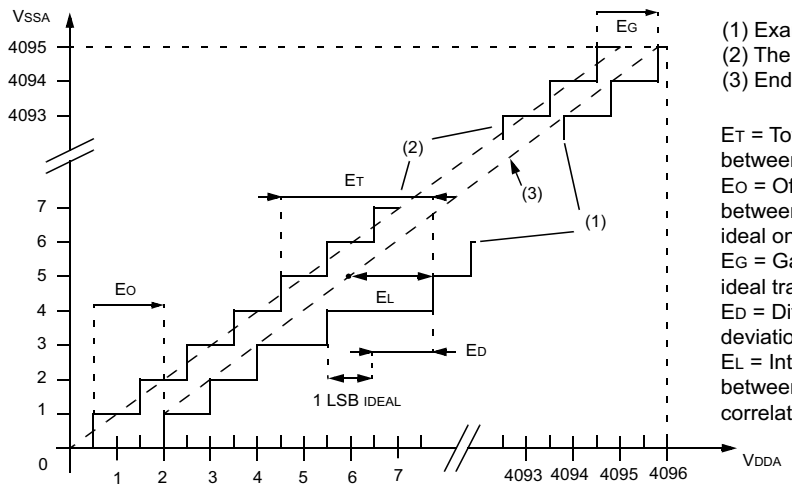
Table 57. ADC characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{TRIG} (2)	External trigger frequency	f_{ADC} = 14 MHz, 12-bit resolution	-	-	823	kHz
		12-bit resolution	-	-	17	$1/f_{ADC}$
V_{AIN}	Conversion voltage range	-	0	-	V_{DDA}	V
R_{AIN} (2)	External input impedance	See *Equation 1* and *Table 58* for details	-	-	50	kΩ
R_{ADC} (2)	Sampling switch resistance	-	-	-	1	kΩ
C_{ADC} (2)	Internal sample and hold capacitor	-	-	-	8	pF
t_{CAL} (2)(3)	Calibration time	f_{ADC} = 14 MHz	5.9			µs
		-	83			$1/f_{ADC}$
$W_{LATENCY}$ (2)(4)	ADC_DR register ready latency	ADC clock = HSI14	1.5 ADC cycles + 2 f_{PCLK} cycles	-	1.5 ADC cycles + 3 f_{PCLK} cycles	-
		ADC clock = PCLK/2	-	4.5	-	f_{PCLK} cycle
		ADC clock = PCLK/4	-	8.5	-	f_{PCLK} cycle
t_{latr} (2)	Trigger conversion latency	$f_{ADC} = f_{PCLK}/2 = 14$ MHz	0.196			µs
		$f_{ADC} = f_{PCLK}/2$	5.5			$1/f_{PCLK}$
		$f_{ADC} = f_{PCLK}/4 = 12$ MHz	0.219			µs
		$f_{ADC} = f_{PCLK}/4$	10.5			$1/f_{PCLK}$
		$f_{ADC} = f_{HSI14}$ = 14 MHz	0.179	-	0.250	µs
$Jitter_{ADC}$	ADC jitter on trigger conversion	$f_{ADC} = f_{HSI14}$	-	1	-	$1/f_{HSI14}$
t_S (2)	Sampling time	f_{ADC} = 14 MHz	0.107	-	17.1	µs
		-	1.5	-	239.5	$1/f_{ADC}$
t_{STAB} (2)	Stabilization time	-	14			$1/f_{ADC}$
t_{CONV} (2)	Total conversion time (including sampling time)	f_{ADC} = 14 MHz, 12-bit resolution	1	-	18	µs
		12-bit resolution	14 to 252 (t_S for sampling +12.5 for successive approximation)			$1/f_{ADC}$

1. During conversion of the sampled value (12.5 x ADC clock period), an additional consumption of 100 µA on I_{DDA} and 60 µA on I_{DD} should be taken into account.
2. Guaranteed by design, not tested in production.
3. Specified value includes only ADC timing. It does not include the latency of the register access.
4. This parameter specify latency for transfer of the conversion result to the ADC_DR register. EOC flag is set at this time.

2. ADC Accuracy vs. Negative Injection Current: Injecting negative current on any of the standard (non-robust) analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current.
Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 6.3.14* does not affect the ADC accuracy.
3. Better performance may be achieved in restricted V_{DDA}, frequency and temperature ranges.
4. Data based on characterization results, not tested in production.

Figure 26. ADC accuracy characteristics



(1) Example of an actual transfer curve
(2) The ideal transfer curve
(3) End point correlation line

E_T = Total Unajusted Error: maximum deviation between the actual and ideal transfer curves.
E_O = Offset Error: maximum deviation between the first actual transition and the first ideal one.
E_G = Gain Error: deviation between the last ideal transition and the last actual one.
E_D = Differential Linearity Error: maximum deviation between actual steps and the ideal ones.
E_L = Integral Linearity Error: maximum deviation between any actual transition and the end point correlation line.

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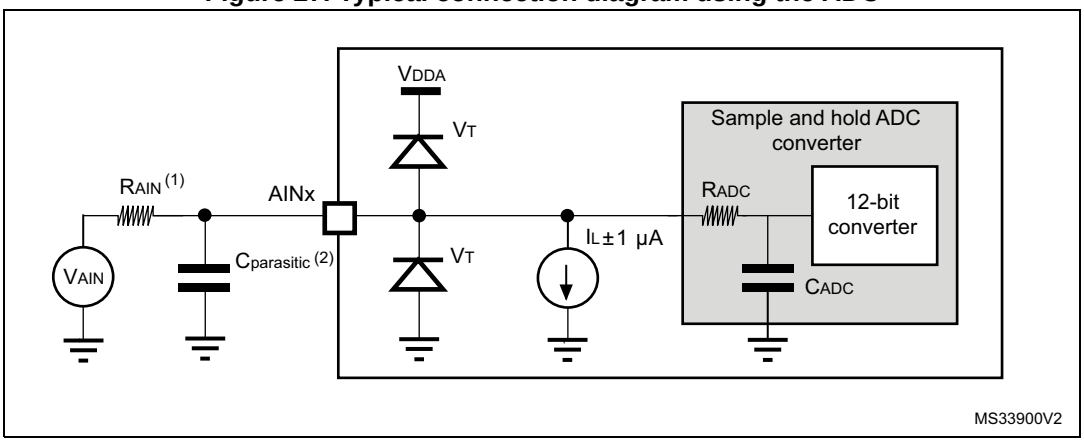
Figure 27. Typical connection diagram using the ADC



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1. Refer to *Table 57: ADC characteristics* for the values of R_{AIN}, R_{ADC} and C_{ADC}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.

General PCB design guidelines

Power supply decoupling should be performed as shown in *Figure 13: Power supply scheme*. The 10 nF capacitor should be ceramic (good quality) and it should be placed as close as possible to the chip.

Table 67. I²C analog filter characteristics(1)

Symbol	Parameter	Min	Max	Unit
t_{AF}	Maximum width of spikes that are suppressed by the analog filter	50(2)	260(3)	ns

1. Guaranteed by design, not tested in production.
2. Spikes with widths below $t_{AF(min)}$ are filtered.
3. Spikes with widths above $t_{AF(max)}$ are not filtered

SPI/I²S characteristics

Unless otherwise specified, the parameters given in *Table 68* for SPI or in *Table 69* for I²S are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and supply voltage conditions summarized in *Table 24: General operating conditions*.

Refer to *Section 6.3.14: I/O port characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI and WS, CK, SD for I²S).

Table 68. SPI characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	-	18	MHz
		Slave mode	-	18	
$t_{r(SCK)}$ $t_{f(SCK)}$	SPI clock rise and fall time	Capacitive load: C = 15 pF	-	6	ns
$t_{su(NSS)}$	NSS setup time	Slave mode	4Tpclk	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode	2Tpclk + 10	-	
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low time	Master mode, f_{PCLK} = 36 MHz, presc = 4	Tpclk/2 -2	Tpclk/2 + 1	
$t_{su(MI)}$ $t_{su(SI)}$	Data input setup time	Master mode	4	-	
		Slave mode	5	-	
$t_{h(MI)}$	Data input hold time	Master mode	4	-	
$t_{h(SI)}$		Slave mode	5	-	
$t_{a(SO)}$(2)	Data output access time	Slave mode, f_{PCLK} = 20 MHz	0	3Tpclk	
$t_{dis(SO)}$(3)	Data output disable time	Slave mode	0	18	
$t_{v(SO)}$	Data output valid time	Slave mode (after enable edge)	-	22.5	
$t_{v(MO)}$	Data output valid time	Master mode (after enable edge)	-	6	
$t_{h(SO)}$	Data output hold time	Slave mode (after enable edge)	11.5	-	
$t_{h(MO)}$		Master mode (after enable edge)	2	-	
DuCy(SCK)	SPI slave input clock duty cycle	Slave mode	25	75	%

1. Data based on characterization results, not tested in production.
2. Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.
3. Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z

Figure 28. SPI timing diagram - slave mode and CPHA = 0

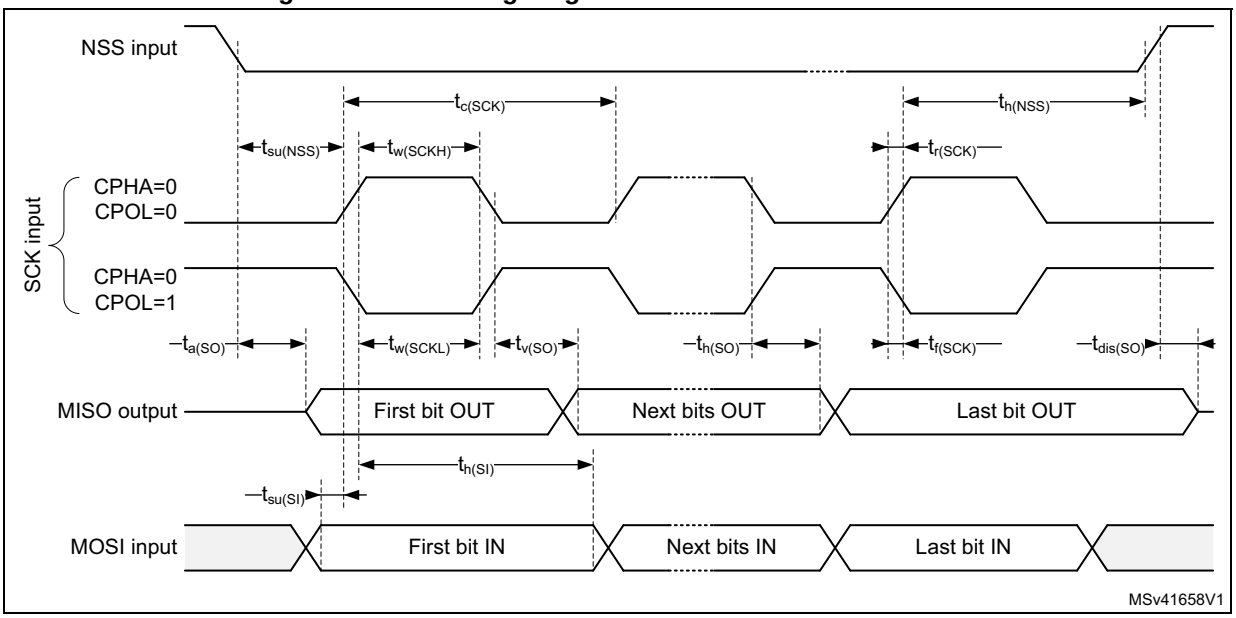
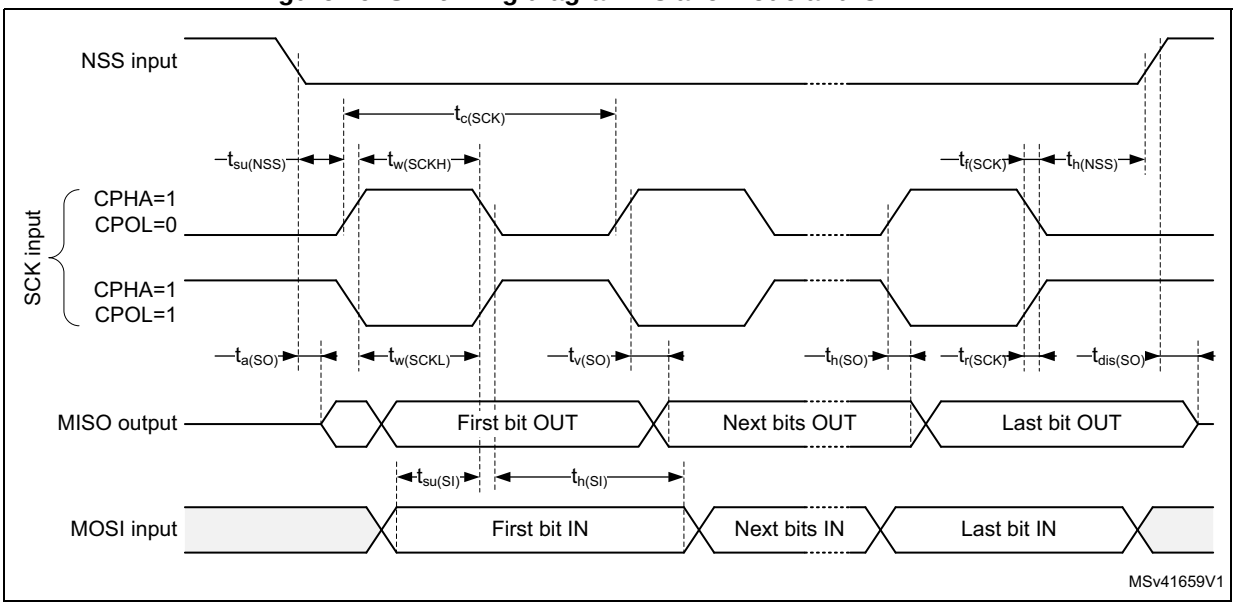
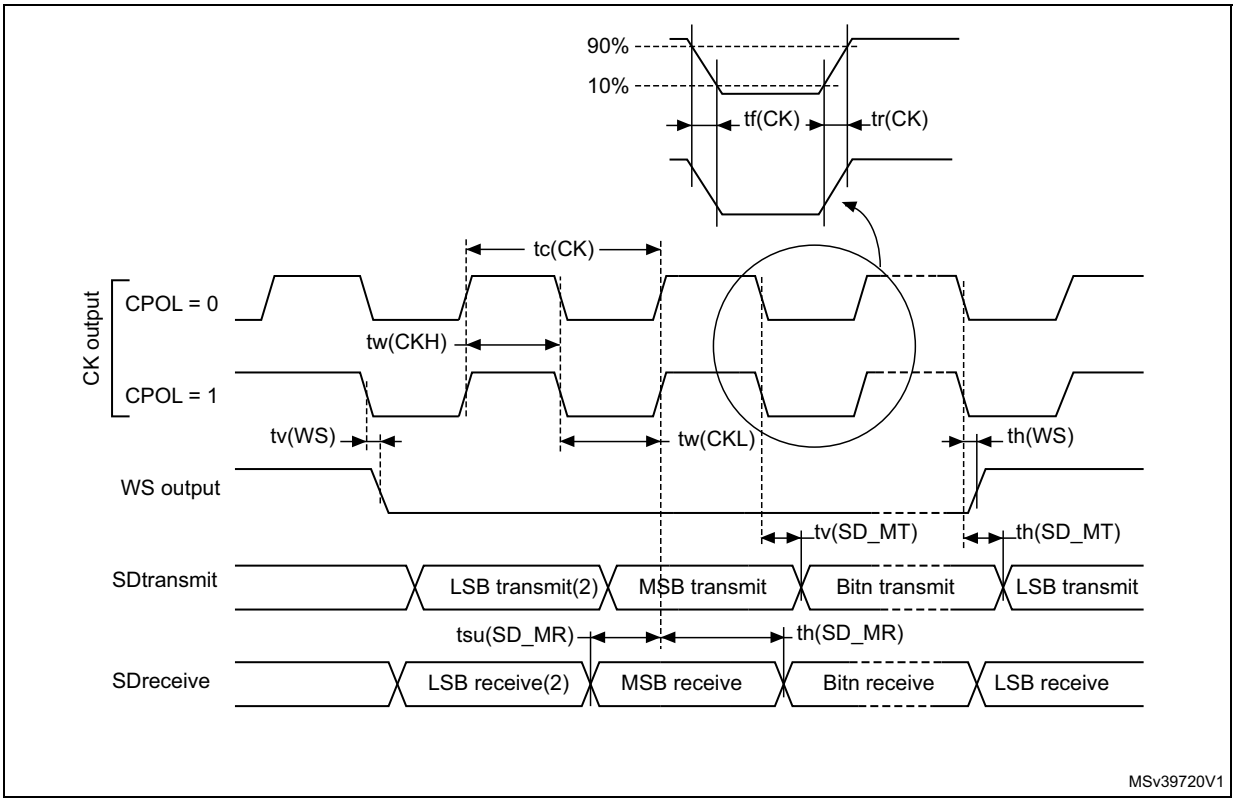


Figure 29. SPI timing diagram - slave mode and CPHA = 1



1. Measurement points are done at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.

Figure 32. I²S master timing diagram (Philips protocol)



1. Data based on characterization results, not tested in production.
2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

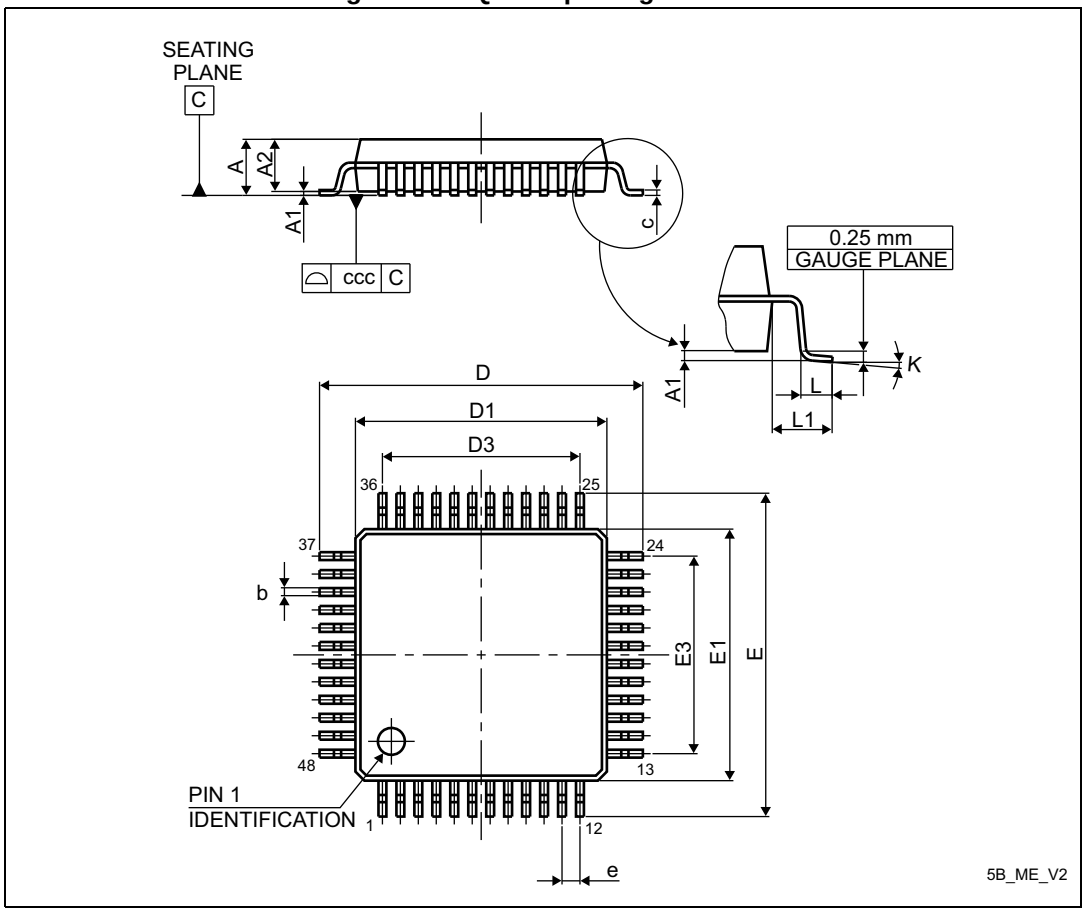
CAN (controller area network) interface

Refer to *Section 6.3.14: I/O port characteristics* for more details on the input/output alternate function characteristics (CAN_TX and CAN_RX).

7.6 LQFP48 package information

LQFP48 is a 48-pin, 7 x 7 mm low-profile quad flat package.

Figure 48. LQFP48 package outline



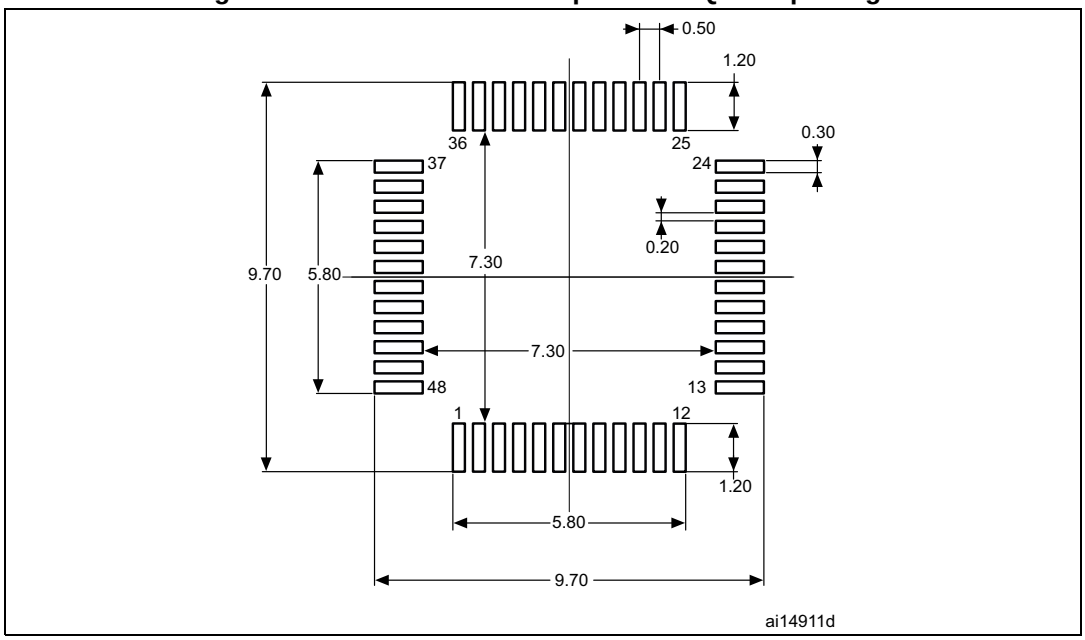
1. Drawing is not to scale.

Table 78. LQFP48 package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3	-	5.500	-	-	0.2165	-
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	-	5.500	-	-	0.2165	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 49. Recommended footprint for LQFP48 package



1. Dimensions are expressed in millimeters.

9 Revision history

Table 82. Document revision history

Date	Revision	Changes
30-Oct-2014	1	Initial release.
09-Feb-2015	2	Updated: – *Table: HSI oscillator characteristics,* – *Figure : HSI oscillator accuracy characterization results for soldered parts,* – *Figure: WLCSP64 wafer level chip size package mechanical drawing,* – *Table: WLCSP64 - 64-pin, 3.347 x 3.585 mm, 0.4 mm pitch wafer level chip scale package mechanical data,.* Added: – *Figure: WLCSP64 - 64-pin, 3.347 x 3.585 mm, 0.4 mm pitch wafer level chip scale recommended footprint.*
17-Dec-2015	3	***Section 2: Description*:** – *Table 2: STM32F091xB/xC family device features and peripheral counts*- I/O and capacitive channel numbers corrected ***Section 3: Functional overview*:** – updated *Figure 1: Block diagram* (number of AF) and *Figure 2: Clock tree* – *Section 3.5.4: Low-power modes* - added info. on comm. peripherals configurable to operate with HSI – *Section 3.13: Touch sensing controller (TSC)* - number of channels corrected – added number of complementary outputs for the general purpose and for the advance control timers in *Table 7: Timer feature comparison* – *Table 9: STM32F091xB/xC I^2C implementation* - added 20mA value to Fast Mode Plus output drive ***Section 4: Pinouts and pin descriptions*:** – Package pinout figures updated (look and feel) – *Figure 7: WLCSP64 package pinout* - **now presented in top view** – *Table 13: STM32F091xB/xC pin definitions* - MCO moved from additional to alternate functions column – *Table 19: Alternate functions selected through GPIOF_AFR registers for port F*- lines PF4 and PF5 removed – ***Section 5: Memory mapping*:** – added information on STM32F091xB difference versus STM32F091xC map in *Figure 10*