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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	DMA, I²S, POR, PWM, WDT
Number of I/O	88
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 19x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f091vct6

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2 Description

The STM32F091xB/xC microcontrollers incorporate the high-performance ARM® Cortex®-M0 32-bit RISC core operating at up to 48 MHz frequency, high-speed embedded memories (up to 256 Kbytes of Flash memory and 32 Kbytes of SRAM), and an extensive range of enhanced peripherals and I/Os. The device offers standard communication interfaces (two I^2Cs, two SPIs/one I^2S, one HDMI CEC and up to eight USARTs), one CAN, one 12-bit ADC, one 12-bit DAC with two channels, seven 16-bit timers, one 32-bit timer and an advanced-control PWM timer.

The STM32F091xB/xC microcontrollers operate in the -40 to +85 °C and -40 to +105 °C temperature ranges, from a 2.0 to 3.6 V power supply. A comprehensive set of power-saving modes allows the design of low-power applications.

The STM32F091xB/xC microcontrollers include devices in seven different packages ranging from 48 pins to 100 pins with a die form also available upon request. Depending on the device chosen, different sets of peripherals are included.

These features make the STM32F091xB/xC microcontrollers suitable for a wide range of applications such as application control and user interfaces, hand-held equipment, A/V receivers and digital TV, PC peripherals, gaming and GPS platforms, industrial applications, PLCs, inverters, printers, scanners, alarm systems, video intercoms and HVACs.

Table 13. STM32F091xB/xC pin definitions (continued)

Pin numbers						Pin name (function upon reset)	Pin type	I/O structure	Notes	Pin functions	
UFBGA100	LQFP100	UFBGA64	LQFP64	WLCSP64	LQFP48/UFQFPN48					Alternate functions	Additional functions
L4	31	G4	22	G5	16	PA6	I/O	TTa		SPI1_MISO, I2S1_MCK, TIM3_CH1, TIM1_BKIN, TIM16_CH1, COMP1_OUT, TSC_G2_IO3, EVENTOUT, USART3_CTS	ADC_IN6
M4	32	H4	23	E4	17	PA7	I/O	TTa		SPI1_MOSI, I2S1_SD, TIM3_CH2, TIM14_CH1, TIM1_CH1N, TIM17_CH1, COMP2_OUT, TSC_G2_IO4, EVENTOUT	ADC_IN7
K5	33	H5	24	H5	-	PC4	I/O	TTa		EVENTOUT, USART3_TX	ADC_IN14
L5	34	H6	25	F4	-	PC5	I/O	TTa		TSC_G3_IO1, USART3_RX	ADC_IN15, WKUP5
M5	35	F5	26	G4	18	PB0	I/O	TTa		TIM3_CH3, TIM1_CH2N, TSC_G3_IO2, EVENTOUT, USART3_CK	ADC_IN8
M6	36	G5	27	F3	19	PB1	I/O	TTa		TIM3_CH4, USART3_RTS, TIM14_CH1, TIM1_CH3N, TSC_G3_IO3	ADC_IN9
L6	37	G6	28	H4	20	PB2	I/O	FT		TSC_G3_IO4	-
M7	38	-	-	-	-	PE7	I/O	FT		TIM1_ETR, USART5_CK_RTS	-
L7	39	-	-	-	-	PE8	I/O	FT		TIM1_CH1N, USART4_TX	-
M8	40	-	-	-	-	PE9	I/O	FT		TIM1_CH1, USART4_RX	-
L8	41	-	-	-	-	PE10	I/O	FT		TIM1_CH2N, USART5_TX	-
M9	42	-	-	-	-	PE11	I/O	FT		TIM1_CH2, USART5_RX	-
L9	43	-	-	-	-	PE12	I/O	FT		SPI1_NSS, I2S1_WS, TIM1_CH3N	-
M10	44	-	-	-	-	PE13	I/O	FT		SPI1_SCK, I2S1_CK, TIM1_CH3	-

Table 13. STM32F091xB/xC pin definitions (continued)

Pin numbers						Pin name (function upon reset)	Pin type	I/O structure	Notes	Pin functions	
UFBGA100	LQFP100	UFBGA64	LQFP64	WLCSP64	LQFP48/UFQFPN48					Alternate functions	Additional functions
A10	76	A7	49	B3	37	PA14	I/O	FT	(3) (4)	USART2_TX, SWCLK	-
A9	77	A6	50	A2	38	PA15	I/O	FT	(3)	SPI1_NSS, I2S1_WS, USART2_RX, USART4_RTS, TIM2_CH1_ETR, EVENTOUT	-
B11	78	B7	51	A3	-	PC10	I/O	FT	(3)	USART3_TX, USART4_TX	-
C10	79	B6	52	C4	-	PC11	I/O	FT	(3)	USART3_RX, USART4_RX	-
B10	80	C5	53	B4	-	PC12	I/O	FT	(3)	USART3_CK, USART4_CK, USART5_TX	-
C9	81	-	-	-	-	PD0	I/O	FT	(3)	SPI2_NSS, I2S2_WS, CAN_RX	-
B9	82	-	-	-	-	PD1	I/O	FT	(3)	SPI2_SCK, I2S2_CK CAN_TX	-
C8	83	B5	54	A4	-	PD2	I/O	FT	(3)	USART3_RTS, TIM3_ETR, USART5_RX	-
B8	84	-	-	-	-	PD3	I/O	FT		SPI2_MISO, I2S2_MCK, USART2_CTS	-
B7	85	-	-	-	-	PD4	I/O	FT		SPI2_MOSI, I2S2_SD, USART2_RTS	-
A6	86	-	-	-	-	PD5	I/O	FT		USART2_TX	-
B6	87	-	-	-	-	PD6	I/O	FT		USART2_RX	-
A5	88	-	-	-	-	PD7	I/O	FT		USART2_CK	-
A8	89	A5	55	D4	39	PB3	I/O	FT		SPI1_SCK, I2S1_CK, TIM2_CH2, TSC_G5_IO1, EVENTOUT, USART5_TX	-
A7	90	A4	56	D5	40	PB4	I/O	FT		SPI1_MISO, I2S1_MCK, TIM17_BKIN, TIM3_CH1, TSC_G5_IO2, EVENTOUT, USART5_RX	-

Table 16. Alternate functions selected through GPIOC_AFR registers for port C

Pin name	AF0	AF1	AF2
PC0	EVENTOUT	USART7_TX	USART6_TX
PC1	EVENTOUT	USART7_RX	USART6_RX
PC2	EVENTOUT	SPI2_MISO, I2S2_MCK	USART8_TX
PC3	EVENTOUT	SPI2_MOSI, I2S2_SD	USART8_RX
PC4	EVENTOUT	USART3_TX	-
PC5	TSC_G3_IO1	USART3_RX	-
PC6	TIM3_CH1	USART7_TX	-
PC7	TIM3_CH2	USART7_RX	-
PC8	TIM3_CH3	USART8_TX	-
PC9	TIM3_CH4	USART8_RX	-
PC10	USART4_TX	USART3_TX	-
PC11	USART4_RX	USART3_RX	-
PC12	USART4_CK	USART3_CK	USART5_TX
PC13	-	-	-
PC14	-	-	-
PC15	-	-	-

Table 17. Alternate functions selected through GPIOD_AFR registers for port D

Pin name	AF0	AF1	AF2
PD0	CAN_RX	SPI2_NSS, I2S2_WS	-
PD1	CAN_TX	SPI2_SCK, I2S2_CK	-
PD2	TIM3_ETR	USART3_RTS	USART5_RX
PD3	USART2_CTS	SPI2_MISO, I2S2_MCK	-
PD4	USART2_RTS	SPI2_MOSI, I2S2_SD	-
PD5	USART2_TX	-	-
PD6	USART2_RX	-	-
PD7	USART2_CK	-	-
PD8	USART3_TX	-	-
PD9	USART3_RX	-	-
PD10	USART3_CK	-	-
PD11	USART3_CTS	-	-
PD12	USART3_RTS	TSC_G8_IO1	USART8_CK_RTS
PD13	USART8_TX	TSC_G8_IO2	-
PD14	USART8_RX	TSC_G8_IO3	-
PD15	CRS_SYNC	TSC_G8_IO4	USART7_CK_RTS

Table 18. Alternate functions selected through GPIOE_AFR registers for port E

Pin name	AF0	AF1
PE0	TIM16_CH1	EVENTOUT
PE1	TIM17_CH1	EVENTOUT
PE2	TIM3_ETR	TSC_G7_IO1
PE3	TIM3_CH1	TSC_G7_IO2
PE4	TIM3_CH2	TSC_G7_IO3
PE5	TIM3_CH3	TSC_G7_IO4
PE6	TIM3_CH4	-
PE7	TIM1_ETR	USART5_CK_RTS
PE8	TIM1_CH1N	USART4_TX
PE9	TIM1_CH1	USART4_RX
PE10	TIM1_CH2N	USART5_TX
PE11	TIM1_CH2	USART5_RX
PE12	TIM1_CH3N	SPI1_NSS, I2S1_WS
PE13	TIM1_CH3	SPI1_SCK, I2S1_CK
PE14	TIM1_CH4	SPI1_MISO, I2S1_MCK
PE15	TIM1_BKIN	SPI1_MOSI, I2S1_SD

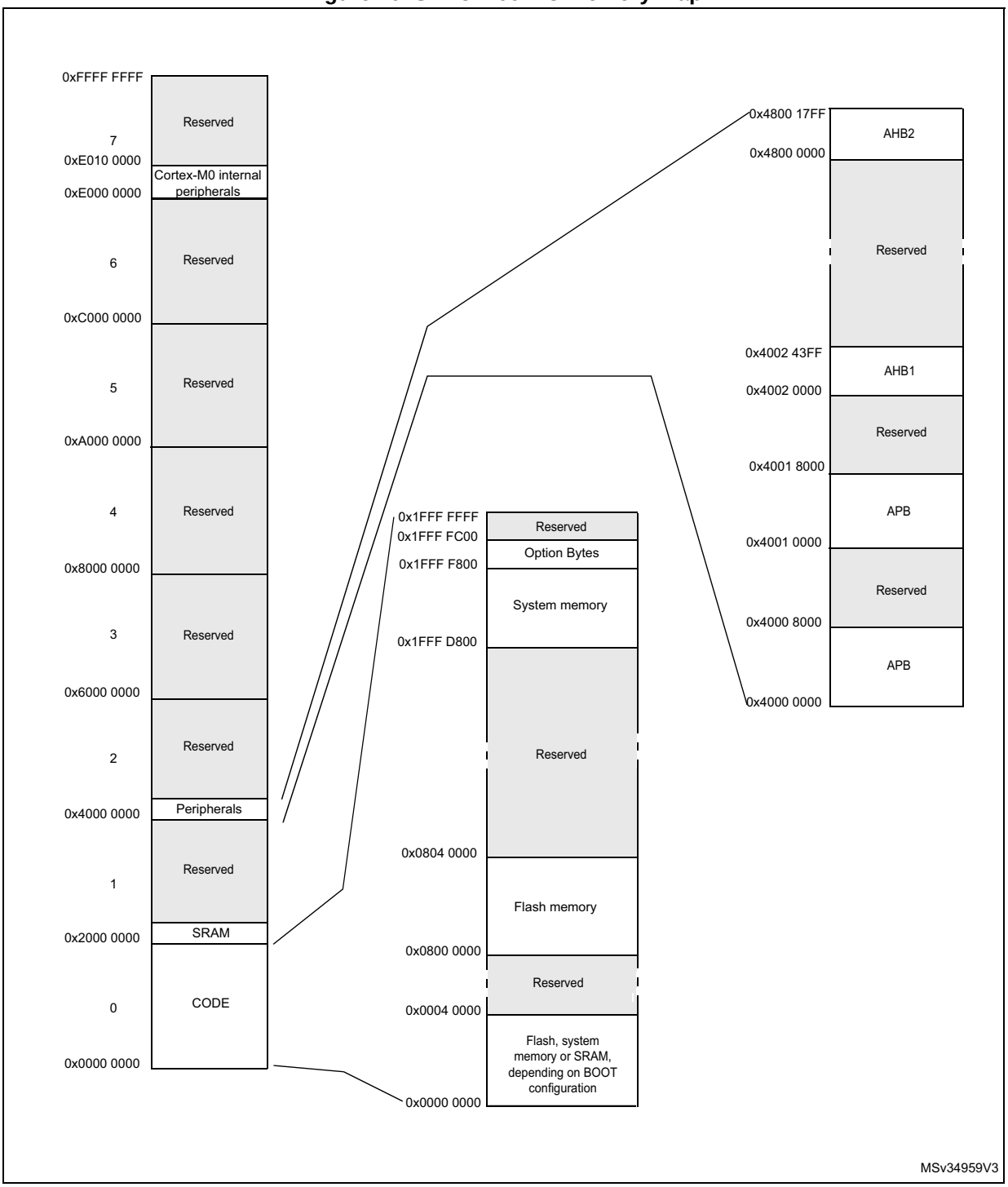
Table 19. Alternate functions selected through GPIOF_AFR registers for port F

Pin name	AF0	AF1	AF2
PF0	CRS_SYNC	I2C1_SDA	-
PF1	-	I2C1_SCL	-
PF2	EVENTOUT	USART7_TX	USART7_CK_RTS
PF3	EVENTOUT	USART7_RX	USART6_CK_RTS
PF6	-	-	-
PF9	TIM15_CH1	USART6_TX	-
PF10	TIM15_CH2	USART6_RX	-

5 Memory mapping

To the difference of STM32F091xC memory map in *Figure 10*, the two bottom code memory spaces of STM32F091xB end at 0x0001 FFFF and 0x0801 FFFF, respectively.

Figure 10. STM32F091xC memory map



1. Data based on characterization results, not tested in production unless otherwise specified.

Table 30. Typical and maximum current consumption from the V_{DDA} supply

Symbol	Para-meter	Conditions (1)	f_{HCLK}	V_{DDA} = 2.4 V				V_{DDA} = 3.6 V				Unit
				Typ	Max @ T_A(2)			Typ	Max @ T_A(2)			
					25 °C	85 °C	105 °C		25 °C	85 °C	105 °C	
I_{DDA}	Supply current in Run or Sleep mode, code executing from Flash memory or RAM	HSI48	48 MHz	312	333	338	347	316	334	341	350	µA
		HSE bypass, PLL on	48 MHz	147	168	178	181	160	181	192	197	
			32 MHz	101	119	125	127	109	127	135	138	
			24 MHz	80	96	98	100	87	101	106	109	
		HSE bypass, PLL off	8 MHz	2.8	3.5	3.7	3.9	3.7	4.3	4.6	4.7	
			1 MHz	2.7	3.2	3.5	3.8	3.3	3.9	4.4	4.7	
		HSI clock, PLL on	48 MHz	214	243	254	259	235	262	275	281	
			32 MHz	166	193	203	204	185	207	216	220	
			24 MHz	144	171	177	178	161	180	187	190	
		HSI clock, PLL off	8 MHz	65	83	85	86	77	90	92	93	

1. Current consumption from the V_{DDA} supply is independent of whether the digital peripherals are enabled or disabled, being in Run or Sleep mode or executing from Flash memory or RAM. Furthermore, when the PLL is off, I_{DDA} is independent from the frequency.
2. Data based on characterization results, not tested in production unless otherwise specified.

Table 31. Typical and maximum consumption in Stop and Standby modes

Sym-bol	Para-meter	Conditions		Typ @V_{DD} (V_{DD} = V_{DDA})						Max(1)			Unit
				2.0 V	2.4 V	2.7 V	3.0 V	3.3 V	3.6 V	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in Stop mode	Regulator in run mode, all oscillators OFF		14.6	14.8	14.9	15.1	15.4	15.8	18	51	97	µA
		Regulator in low-power mode, all oscillators OFF		3.3	3.4	3.6	3.8	4.1	4.4	11	53	106	
	Supply current in Standby mode	LSI ON and IWDG ON		0.9	1.0	1.1	1.2	1.3	1.4	2.3	2.7	3.6	
		LSI OFF and IWDG OFF		0.6	0.7	0.8	0.9	1.0	1.1	1.9	2.3	3.0	
I_{DDA}	Supply current in Stop mode	V_{DDA} monitoring ON	Regulator in run mode, all oscillators OFF	1.9	2.0	2.2	2.3	2.4	2.6	3.8	4.2	4.6	
			Regulator in low-power mode, all oscillators OFF	1.9	2.0	2.2	2.3	2.4	2.6	3.8	4.2	4.6	
	Supply current in Standby mode		LSI ON and IWDG ON	2.3	2.5	2.7	2.8	3.0	3.3	3.8	4.2	4.8	
			LSI OFF and IWDG OFF	1.8	1.9	2.0	2.2	2.3	2.5	3.6	3.9	4.2	
	Supply current in Stop mode	V_{DDA} monitoring OFF	Regulator in run mode, all oscillators OFF	1.2	1.2	1.3	1.3	1.4	1.4	-	-	-	
			Regulator in low-power mode, all oscillators OFF	1.2	1.2	1.3	1.3	1.4	1.4	-	-	-	
	Supply current in Standby mode		LSI ON and IWDG ON	1.6	1.7	1.8	1.9	2.0	2.1	-	-	-	
			LSI OFF and IWDG OFF	1.1	1.1	1.1	1.2	1.3	1.3	-	-	-	

1. Data based on characterization results, not tested in production unless otherwise specified.

trigger circuits used to discriminate the input value. Unless this specific configuration is required by the application, this supply current consumption can be avoided by configuring these I/Os in analog mode. This is notably the case of ADC input pins which should be configured as analog inputs.

Caution: Any floating input pin can also settle to an intermediate voltage level or switch inadvertently, as a result of external electromagnetic noise. To avoid current consumption related to floating pins, they must either be configured in analog mode, or forced internally to a definite digital value. This can be done either by using pull-up/down resistors or by configuring the pins in output mode.

I/O dynamic current consumption

In addition to the internal peripheral current consumption measured previously (see *Table 35: Peripheral current consumption*), the I/Os used by an application also contribute to the current consumption. When an I/O pin switches, it uses the current from the I/O supply voltage to supply the I/O pin circuitry and to charge/discharge the capacitive load (internal or external) connected to the pin:

$$I_{SW} = V_{DDIOx} \times f_{SW} \times C$$

where

I_{SW} is the current sunk by a switching I/O to charge/discharge the capacitive load

V_{DDIOx} is the I/O supply voltage

f_{SW} is the I/O switching frequency

C is the total capacitance seen by the I/O pin: $C = C_{INT} + C_{EXT} + C_S$

C_S is the PCB board capacitance including the pad pin.

The test pin is configured in push-pull output mode and is toggled by software at a fixed frequency.

Table 35. Peripheral current consumption (continued)

Peripheral		Typical consumption at 25 °C	Unit
APB	APB-Bridge(2)	3.6	µA/MHz
	ADC(3)	4.3	
	CAN	12.4	
	CEC	0.4	
	CRS	0.0	
	DAC(3)	4.2	
	DBG (MCU Debug Support)	0.2	
	I2C1	2.9	
	I2C2	2.4	
	PWR	0.6	
	SPI1	8.8	
	SPI2	7.8	
	SYSCFG and COMP	1.9	
	TIM1	15.2	
	TIM14	2.6	
	TIM15	8.7	
	TIM16	5.8	
	TIM17	7.0	
	TIM2	16.2	
	TIM3	11.9	
	TIM6	11.8	
	TIM7	2.5	
	USART1	17.6	
	USART2	16.3	
	USART3	16.2	
	USART4	4.7	
	USART5	4.4	
	USART6	5.5	
	USART7	5.2	
	USART8	5.1	
	WWDG	1.1	
	All APB peripherals	**207.2**	

1. The BusMatrix is automatically active when at least one master is ON (CPU, DMA).
2. The APB Bridge is automatically active when at least one peripheral is ON on the Bus.
3. The power consumption of the analog part (I_{DDA}) of peripherals such as ADC, DAC, comparators, is not included. Refer to the tables of characteristics in the subsequent sections.

Table 53. I/O static characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{PU}	Weak pull-up equivalent resistor (3)	$V_{IN} = V_{SS}$	25	40	55	kΩ
R_{PD}	Weak pull-down equivalent resistor(3)	$V_{IN} = - V_{DDIOx}$	25	40	55	kΩ
C_{IO}	I/O pin capacitance	-	-	5	-	pF

1. Data based on design simulation only. Not tested in production.
2. The leakage could be higher than the maximum value, if negative current is injected on adjacent pins. Refer to *Table 52: I/O current injection susceptibility*.
3. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS contribution to the series resistance is minimal (~10% order).

All I/Os are CMOS- and TTL-compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements is shown in *Figure 22* for standard I/Os, and in *Figure 23* for 5 V-tolerant I/Os. The following curves are design simulation results, not tested in production.

Input/output AC characteristics

The definition and values of input/output AC characteristics are given in *Figure 24* and *Table 55*, respectively. Unless otherwise specified, the parameters given are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 24: General operating conditions*.

Table 55. I/O AC characteristics(1)(2)

OSPEEDRy [1:0] value(1)	Symbol	Parameter	Conditions	Min	Max	Unit
x0	$f_{max(IO)out}$	Maximum frequency(3)	C_L = 50 pF, $V_{DDIOx} \geq 2$ V	-	2	MHz
	$t_{f(IO)out}$	Output fall time		-	125	ns
	$t_{r(IO)out}$	Output rise time		-	125	
	$f_{max(IO)out}$	Maximum frequency(3)	C_L = 50 pF, $V_{DDIOx} < 2$ V	-	1	MHz
	$t_{f(IO)out}$	Output fall time		-	125	ns
	$t_{r(IO)out}$	Output rise time		-	125	
01	$f_{max(IO)out}$	Maximum frequency(3)	C_L = 50 pF, $V_{DDIOx} \geq 2$ V	-	10	MHz
	$t_{f(IO)out}$	Output fall time		-	25	ns
	$t_{r(IO)out}$	Output rise time		-	25	
	$f_{max(IO)out}$	Maximum frequency(3)	C_L = 50 pF, $V_{DDIOx} < 2$ V	-	4	MHz
	$t_{f(IO)out}$	Output fall time		-	62.5	ns
	$t_{r(IO)out}$	Output rise time		-	62.5	
11	$f_{max(IO)out}$	Maximum frequency(3)	C_L = 30 pF, $V_{DDIOx} \geq 2.7$ V	-	50	MHz
			C_L = 50 pF, $V_{DDIOx} \geq 2.7$ V	-	30	
			C_L = 50 pF, 2 V ≤ V_{DDIOx} < 2.7 V	-	20	
			C_L = 50 pF, $V_{DDIOx} < 2$ V	-	10	
	$t_{f(IO)out}$	Output fall time	C_L = 30 pF, $V_{DDIOx} \geq 2.7$ V	-	5	ns
			C_L = 50 pF, $V_{DDIOx} \geq 2.7$ V	-	8	
			C_L = 50 pF, 2 V ≤ V_{DDIOx} < 2.7 V	-	12	
			C_L = 50 pF, $V_{DDIOx} < 2$ V	-	25	
	$t_{r(IO)out}$	Output rise time	C_L = 30 pF, $V_{DDIOx} \geq 2.7$ V	-	5	
			C_L = 50 pF, $V_{DDIOx} \geq 2.7$ V	-	8	
			C_L = 50 pF, 2 V ≤ V_{DDIOx} < 2.7 V	-	12	
			C_L = 50 pF, $V_{DDIOx} < 2$ V	-	25	

Table 65. IWDG min/max timeout period at 40 kHz (LSI)(1)

Prescaler divider	PR[2:0] bits	Min timeout RL[11:0]= 0x000	Max timeout RL[11:0]= 0xFFF	Unit
/4	0	0.1	409.6	ms
/8	1	0.2	819.2	
/16	2	0.4	1638.4	
/32	3	0.8	3276.8	
/64	4	1.6	6553.6	
/128	5	3.2	13107.2	
/256	6 or 7	6.4	26214.4	

1. These timings are given for a 40 kHz clock but the microcontroller internal RC frequency can vary from 30 to 60 kHz. Moreover, given an exact RC oscillator frequency, the exact timings still depend on the phasing of the APB interface clock versus the LSI clock so that there is always a full RC period of uncertainty.

Table 66. WWDG min/max timeout value at 48 MHz (PCLK)

Prescaler	WDGTB	Min timeout value	Max timeout value	Unit
1	0	0.0853	5.4613	ms
2	1	0.1706	10.9226	
4	2	0.3413	21.8453	
8	3	0.6826	43.6906	

6.3.22 Communication interfaces

I^2C interface characteristics

The I^2C interface meets the timings requirements of the I^2C-bus specification and user manual rev. 03 for:

- Standard-mode (Sm): with a bit rate up to 100 kbit/s
- Fast-mode (Fm): with a bit rate up to 400 kbit/s
- Fast-mode Plus (Fm+): with a bit rate up to 1 Mbit/s.

The I^2C timings requirements are guaranteed by design when the I2Cx peripheral is properly configured (refer to Reference manual).

The SDA and SCL I/O requirements are met with the following restrictions: the SDA and SCL I/O pins are not “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and V_{DDIOx} is disabled, but is still present. Only FTf I/O pins support Fm+ low level output current maximum requirement. Refer to *Section 6.3.14: I/O port characteristics* for the I^2C I/Os characteristics.

All I^2C SDA and SCL I/Os embed an analog filter. Refer to the table below for the analog filter characteristics:

7.8 Thermal characteristics

The maximum chip junction temperature ($T_J$max) must never exceed the values given in *Table 24: General operating conditions*.

The maximum chip-junction temperature, T_J max, in degrees Celsius, may be calculated using the following equation:

$$T_J \text{ max} = T_A \text{ max} + (P_D \text{ max} \times \Theta_{JA})$$

Where:

- T_A max is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- P_D max is the sum of P_{INT} max and $P_{I/O}$ max (P_D max = P_{INT} max + $P_{I/O}$max),
- P_{INT} max is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins where:

$$P_{I/O} \text{ max} = \Sigma (V_{OL} \times I_{OL}) + \Sigma ((V_{DDIOx} - V_{OH}) \times I_{OH}),$$

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 80. Package thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	**Thermal resistance junction-ambient** UFBGA100 - 7 × 7 mm	55	°C/W
	Thermal resistance junction-ambient LQFP100 - 14 × 14 mm	42	
	Thermal resistance junction-ambient UFBGA64 - 5 × 5 mm / 0.5 mm pitch	65	
	Thermal resistance junction-ambient LQFP64 - 10 × 10 mm / 0.5 mm pitch	44	
	Thermal resistance junction-ambient WLCSP64 - 0.4 mm pitch	53	
	Thermal resistance junction-ambient LQFP48 - 7 × 7 mm	54	
	Thermal resistance junction-ambient UFQFPN48 - 7 × 7 mm	32	

7.8.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org

7.8.2 Selecting the product temperature range

When ordering the microcontroller, the temperature range is specified in the ordering information scheme shown in *Section 8: Ordering information*.

8 Ordering information

For a list of available options (memory, package, and so on) or for further information on any aspect of this device, please contact your nearest ST sales office.

Table 81. Ordering information scheme

Example: STM32 F 091 R C T 6 x

Device family

STM32 = ARM-based 32-bit microcontroller

Product type

F = General-purpose

Sub-family

091= STM32F091xx

Pin count

C = 48 pins
R = 64 pins
V = 100 pins

User code memory size

B = 128 Kbyte
C = 256 Kbyte

Package

H = UFBGA
T = LQFP
U = UFQFPN
Y = WLCSP

Temperature range

6 = –40 to 85 °C
7 = –40 to 105 °C

Options

xxx = code ID of programmed parts (includes packing type)
TR = tape and reel packing
blank = tray packing

Table 82. Document revision history (continued)

Date	Revision	Changes
10-Jan-2017	4	***Section 6: Electrical characteristics*:** – *Table 40: LSE oscillator characteristics (f_{LSE} = 32.768 kHz)* - information on configuring different drive capabilities removed. See the corresponding reference manual. – *Table 28: Embedded internal reference voltage* - V_{REFINT} values – *Table 60: DAC characteristics* - min. R_{LOAD} to V_{DDA} defined – *Figure 28: SPI timing diagram - slave mode and CPHA = 0* and *Figure 29: SPI timing diagram - slave mode and CPHA = 1* enhanced and corrected ***Section 8: Ordering information*:** – The name of the section changed from the previous “Part numbering”