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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	V850ES
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	CSI, EBI/EMI, I²C, UART/USART
Peripherals	DMA, LVD, PWM, WDT
Number of I/O	128
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.85V ~ 3.6V
Data Converters	A/D 16x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd70f3743gj-gae-ax

Related Documents

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

Documents related to V850ES/JJ3

Document Name	Document No.
V850ES Architecture User's Manual	U15943E
V850ES/JJ3 Hardware User's Manual	This manual

Documents related to development tools

Document Name		Document No.
QB-V850ESSX2 In-Circuit Emulator		U17091E
QB-V850MINI On-Chip Debug Emulator		U17638E
QB-MINI2 On-Chip Debug Emulator with Programming Function		U18371E
CA850 Ver. 3.00 C Compiler Package	Operation	U17293E
	C Language	U17291E
	Assembly Language	U17292E
	Link Directives	U17294E
PM+ Ver. 6.20 Project Manager		U17990E
ID850QB Ver. 3.20 Integrated Debugger	Operation	U17964E
SM850 Ver. 2.50 System Simulator	Operation	U16218E
SM850 Ver. 2.00 or Later System Simulator	External Part User Open Interface Specification	U14873E
SM+ System Simulator	Operation	U17246E
	User Open Interface	U17247E
RX850 Ver. 3.20 Real-Time OS	Basics	U13430E
	Installation	U17419E
	Technical	U13431E
	Task Debugger	U17420E
RX850 Pro Ver. 3.20 Real-Time OS	Basics	U13773E
	Installation	U17421E
	Technical	U13772E
	Task Debugger	U17422E
AZ850 Ver. 3.30 System Performance Analyzer		U17423E
PG-FP4 Flash Memory Programmer		U15260E

CHAPTER 2 PIN FUNCTIONS

2.1 List of Pin Functions

The names and functions of the pins of the V850ES/JJ3 are described below.

There are three types of pin I/O buffer power supplies: AV_{REF0}, AV_{REF1}, and EV_{DD}. The relationship between these power supplies and the pins is described below.

Table 2-1. Pin I/O Buffer Power Supplies

Power Supply	Corresponding Pins
AV_{REF0}	Port 7
AV_{REF1}	Port 1
EV_{DD}	$\overline{\text{RESET}}$, ports 0, 3 to 6, 8, 9, CD, CM, CS, CT, DH, DL

CHAPTER 3 CPU FUNCTION

The CPU of the V850ES/JJ3 is based on RISC architecture and executes almost all instructions with one clock by using a 5-stage pipeline.

3.1 Features

○ Minimum instruction execution time: 31.25 ns (at 32 MHz operation)
30.5 μs (with subclock (f_{XT}) = 32.768 kHz operation)

○ Memory space Program (physical address) space: 64 MB linear
Data (logical address) space: 4 GB linear

○ General-purpose registers: 32 bits × 32 registers

○ Internal 32-bit architecture

○ 5-stage pipeline control

○ Multiplication/division instruction

○ Saturation operation instruction

○ 32-bit shift instruction: 1 clock

○ Load/store instruction with long/short format

○ Four types of bit manipulation instructions

- SET1
- CLR1
- NOT1
- TST1

(5) Port 5 function control expansion register (PFCE5)

After reset: 00H R/W Address: FFFFF70AH

	7	6	5	4	3	2	1	0
PFCE5	0	0	PFCE55	PFCE54	PFCE53	PFCE52	PFCE51	PFCE50

Remark For details of alternate function specification, see **4.3.5 (6) Port 5 alternate function specifications**.

(6) Port 5 alternate function specifications

PFCE55	PFC55	Specification of P55 pin alternate function
0	0	$\overline{\text{SCKB2}}$ I/O
0	1	KR5 input
1	0	Setting prohibited
1	1	RTP05 output

PFCE54	PFC54	Specification of P54 pin alternate function
0	0	SOB2 output
0	1	KR4 input
1	0	Setting prohibited
1	1	RTP04 output

PFCE53	PFC53	Specification of P53 pin alternate function
0	0	SIB2 input
0	1	TIQ00 input/KR3[Note] input
1	0	TOQ00 output
1	1	RTP03 output

PFCE52	PFC52	Specification of P52 pin alternate function
0	0	Setting prohibited
0	1	TIQ03 input/KR2[Note] input
1	0	TOQ03 output
1	1	RTP02 output

PFCE51	PFC51	Specification of P51 pin alternate function
0	0	Setting prohibited
0	1	TIQ02 input/KR1[Note] input
1	0	TOQ02 output
1	1	RTP01 output

(4) Port 6 function control register H (PFC6H)

After reset: 00H R/W Address: FFFFF46DH

	15	14	13	12	11	10	9	8
PFC6H	0	0	PFC613	PFC612	0	0	PFC69	0

PFC613	Specification of P613 pin alternate function
0	TIP81 input
1	TOP81 output

PFC612	Specification of P612 pin alternate function
0	TIP80 input
1	TOP80 output

PFC69	Specification of P69 pin alternate function
0	TIP70 input
1	TOP70 output

(5) Port 6 function register (PF6)

After reset: 0000H R/W Address: PF6 FFFFFC6CH
PF6L FFFFFC6CH, PF6H FFFFFC6DH

	15	14	13	12	11	10	9	8
PF6 (PF6H)	PF615	PF614	PF613	PF612	PF611	PF610	PF69	PF68

	7	6	5	4	3	2	1	0
(PF6L)	PF67	PF66	PF65	PF64	PF63	PF62	PF61	PF60

PF6n	Normal output/N-ch open-drain output control (n = 0 to 15)
0	Normal output (CMOS output)
1	N-ch open-drain output

Caution When an output pin is pulled up at EV_{DD} or higher, be sure to set the PF6n bit to 1.

Remarks 1. The PF6 register can be read or written in 16-bit units.
However, when using the higher 8 bits of the PF6 register as the PF6H register and the lower 8 bits as the PF6L register, PF6 can be read or written in 8-bit and 1-bit units.

2. To read/write bits 8 to 15 of the PF6 register in 8-bit or 1-bit units, specify them as bits 0 to 7 of the PF6H register.

4.3.8 Port 8

Port 8 is a 2-bit port for which I/O settings can be controlled in 1-bit units.

Port 8 includes the following alternate-function pins.

Table 4-11. Port 8 Alternate-Function Pins

Pin Name	Pin No.	Alternate-Function Pin Name	I/O	Remark	Block Type
P80	59	RXDA3/INTP8	Input	Selectable as N-ch open-drain output	L-2
P81	60	TXDA3	Output		E-2

Caution The P80 pin has hysteresis characteristics in the input mode of the alternate-function pin, but does not have the hysteresis characteristics in the port mode.

(1) Port 8 register (P8)

After reset: 00H (output latch) R/W Address: FFFFF410H

	7	6	5	4	3	2	1	0
P8	0	0	0	0	0	0	P81	P80

P8n	Output data control (n = 0, 1)
0	Outputs 0
1	Outputs 1

(2) Port 8 mode register (PM8)

After reset: FFH R/W Address: FFFFF430H

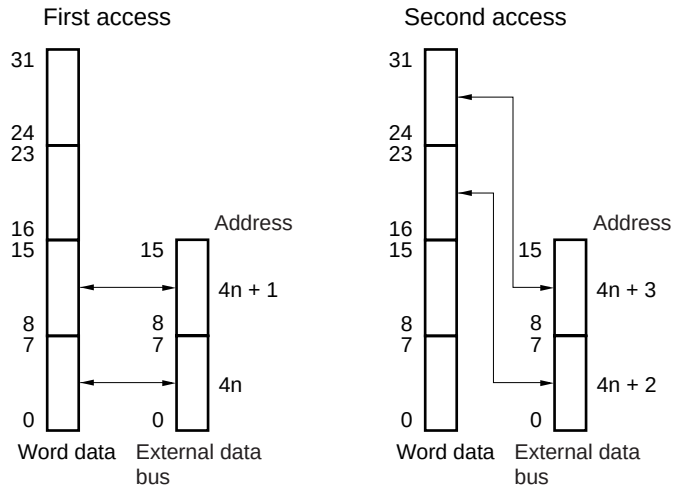
	7	6	5	4	3	2	1	0
PM8	1	1	1	1	1	1	PM81	PM80

PM8n	I/O mode control (n = 0, 1)
0	Output mode
1	Input mode

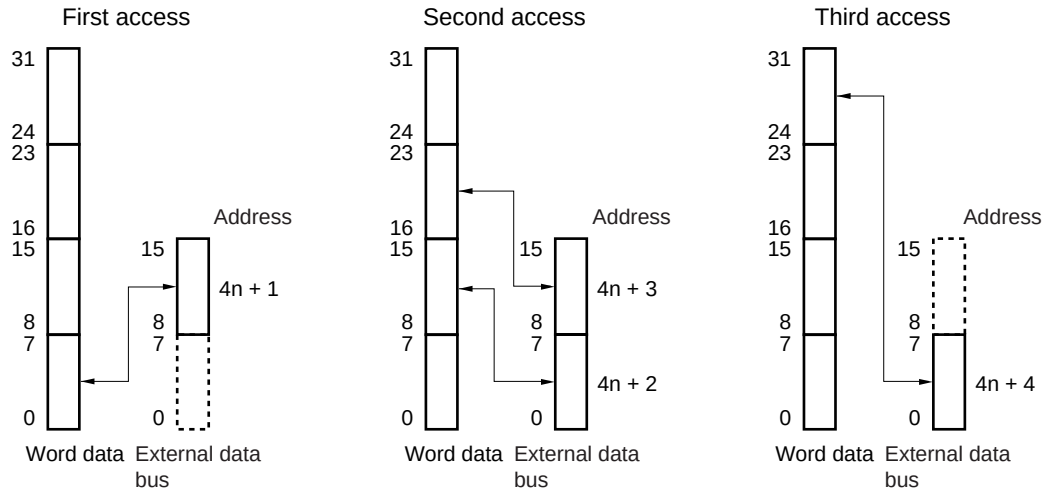
(4) Word access (32 bits)

(a) 16-bit data bus width (1/2)

<1> Access to address (4n)



<2> Access to address (4n + 1)



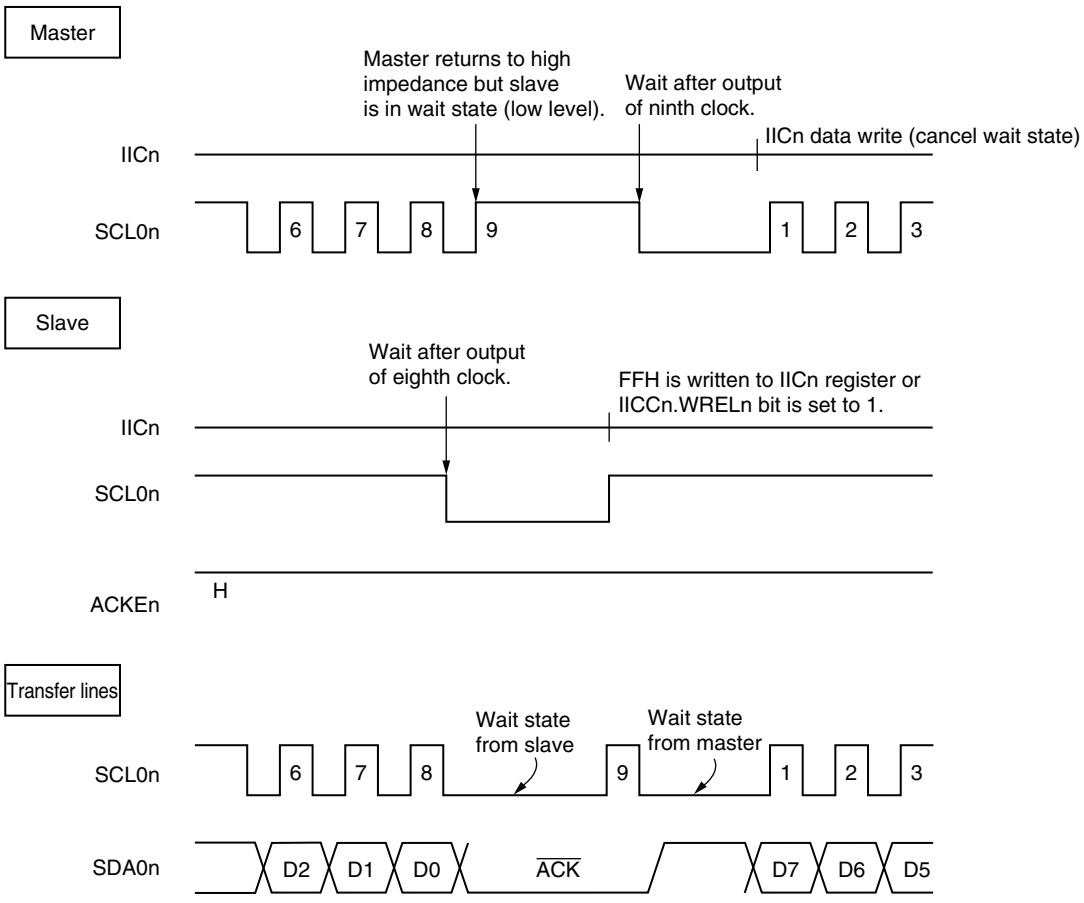
17.6.6 Wait state

A wait state is used to notify the communication partner that a device (master or slave) is preparing to transmit or receive data (i.e., is in a wait state).

Setting the SCL0n pin to low level notifies the communication partner of the wait state. When the wait state has been canceled for both the master and slave devices, the next data transfer can begin (n = 0 to 2).

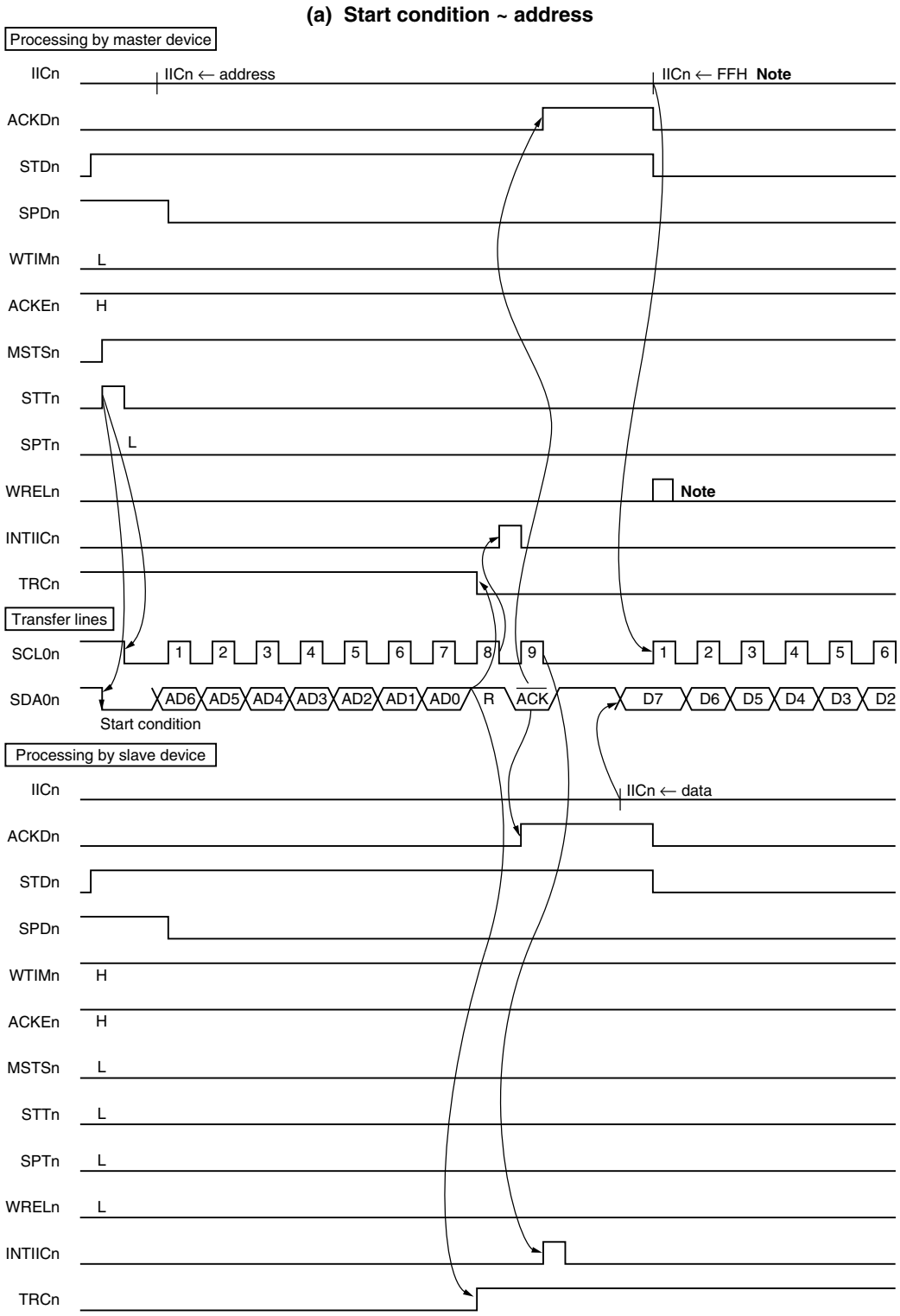
Figure 17-13. Wait State (1/2)

(a) When master device has a nine-clock wait and slave device has an eight-clock wait (master: transmission, slave: reception, and IICCn.ACKEn bit = 1)



Remark n = 0 to 2

Figure 17-24. Example of Slave to Master Communication
(When 8-Clock Wait for Master and 9-Clock Wait for Slave Are Selected) (1/3)



Note To cancel master wait, write FFH to IICn or set WRELn.

Remark n = 0 to 2

(2) DMA destination address registers 0 to 3 (DDA0 to DDA3)

The DDA0 to DDA3 registers set the DMA destination address (26 bits each) for DMA channel n (n = 0 to 3). These registers are divided into two 16-bit registers, DDAnH and DDAnL.

These registers can be read or written in 16-bit units.

After reset: Undefined R/W Address: DDA0H FFFFF086H, DDA1H FFFFF08EH, DDA2H FFFFF096H, DDA3H FFFFF09EH, DDA0L FFFFF084H, DDA1L FFFFF08CH, DDA2L FFFFF094H, DDA3L FFFFF09CH

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DDAnH (n = 0 to 3)	IR	0	0	0	0	0	DA25	DA24	DA23	DA22	DA21	DA20	DA19	DA18	DA17	DA16
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DDAnL (n = 0 to 3)	DA15	DA14	DA13	DA12	DA11	DA10	DA9	DA8	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0

IR	Specification of DMA transfer destination
0	External memory or on-chip peripheral I/O
1	Internal RAM

DA25 to DA16	Set an address (A25 to A16) of DMA transfer destination (default value is undefined). During DMA transfer, the next DMA transfer destination address is held. When DMA transfer is completed, the DMA transfer source address set first is held.

DA15 to DA0	Set an address (A15 to A0) of DMA transfer destination (default value is undefined). During DMA transfer, the next DMA transfer destination address is held. When DMA transfer is completed, the DMA transfer source address set first is held.

Cautions 1. Be sure to clear bits 14 to 10 of the DDAnH register to 0.

2. Set the DDAnH and DDAnL registers at the following timing when DMA transfer is disabled (DCHCn.Enn bit = 0).

- **Period from after reset to start of first DMA transfer**
- **Period from after channel initialization by DCHCn.INITn bit to start of DMA transfer**
- **Period from after completion of DMA transfer (DCHCn.TCn bit = 1) to start of the next DMA transfer**

3. When the value of the DDAn register is read, two 16-bit registers, DDAnH and DDAnL, are read. If reading and updating conflict, a value being updated may be read (see 18.13 Cautions).

4. Following reset, set the DSAnH, DSAnL, DDAnH, DDAnL, and DBCn registers before starting DMA transfer. If these registers are not set, the operation when DMA transfer is started is not guaranteed.

CHAPTER 19 INTERRUPT/EXCEPTION PROCESSING FUNCTION

The V850ES/JJ3 is provided with a dedicated interrupt controller (INTC) for interrupt servicing and can process a total of 71 interrupt requests.

An interrupt is an event that occurs independently of program execution, and an exception is an event whose occurrence is dependent on program execution.

The V850ES/JJ3 can process interrupt request signals from the on-chip peripheral hardware and external sources. Moreover, exception processing can be started by the TRAP instruction (software exception) or by generation of an exception event (i.e. fetching of an illegal opcode) (exception trap).

19.1 Features

○ Interrupts
- Non-maskable interrupts: 2 sources
- Maskable interrupts: External: 9, Internal: 60 sources
- 8 levels of programmable priorities (maskable interrupts)
- Multiple interrupt control according to priority
- Masks can be specified for each maskable interrupt request.
- Noise elimination, edge detection, and valid edge specification for external interrupt request signals.

○ Exceptions
- Software exceptions: 32 sources
- Exception trap: 2 sources (illegal opcode exception, debug trap)

Interrupt/exception sources are listed in Table 19-1.

28.3.2 Setting

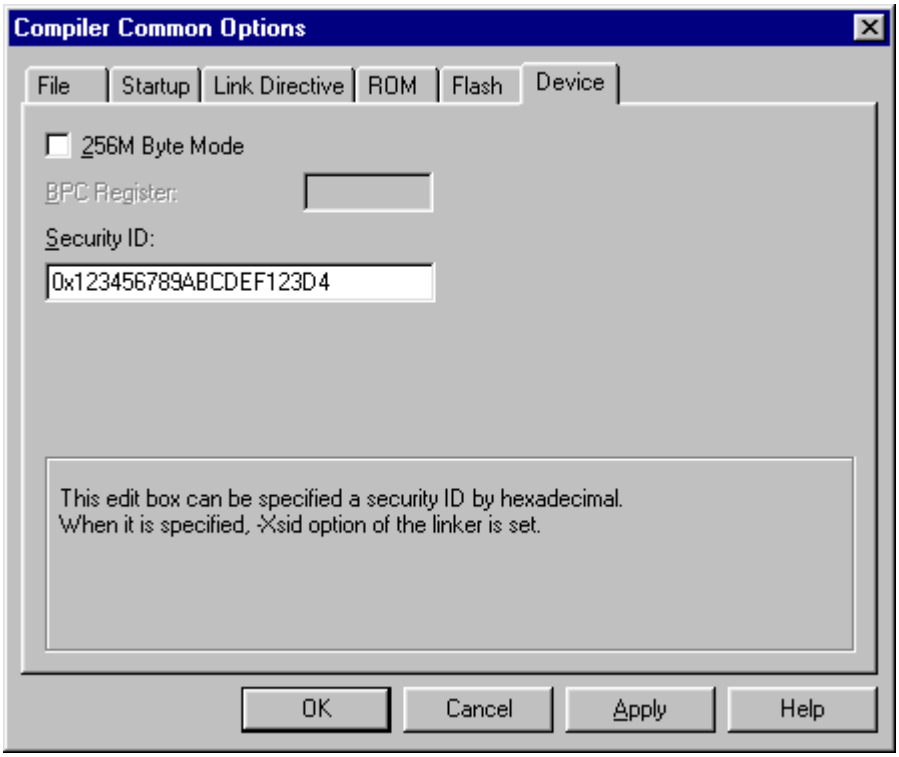
The following shows how to set the ID code as shown in Table 28-5.

When the ID code is set as shown in Table 28-5, the ID code input in the configuration dialog box of the ID850QB is “123456789ABCDEF123D4” (the ID code is case-insensitive).

Table 28-5. ID Code

Address	Value
0x70	0x12
0x71	0x34
0x72	0x56
0x73	0x78
0x74	0x9A
0x75	0xBC
0x76	0xDE
0x77	0XF1
0x78	0x23
0x79	0xD4

The ID code can be specified for the device file that supports CA850 Ver. 3.10 or later and the security ID using the PM+ compiler common option setting.



(7/37)

Chapter	Classification	Function	Details of Function	Cautions	Page
Chapter 5	Soft	Bus control functions	DWC0 register	Write to the DWC0 register after reset, and then do not change the set values. Also, do not access an external memory area until the initial settings of the DWC0 register are complete.	p. 178 ☐
				When V850ES/JJ3 is used in separate bus mode and operated at f_{XX} > 20 MHz, be sure to insert one or more wait.	p. 178 ☐
				Be sure to clear bits 15, 11, 7, and 3 to “0”.	p. 178 ☐
			AWC register	Address setup wait and address hold wait cycles are not inserted when the internal ROM area, internal RAM area, and on-chip peripheral I/O areas are accessed.	p. 181 ☐
				Write to the AWC register after reset, and then do not change the set values. Also, do not access an external memory area until the initial settings of the AWC register are complete.	p. 181 ☐
				When V850ES/JJ3 is operated at f_{XX} > 20 MHz, be sure to insert the address hold wait and the address setup wait.	p. 181 ☐
				Be sure to set bits 15 to 8 to “1”.	p. 181 ☐
			BCC register	The internal ROM, internal RAM, and on-chip peripheral I/O areas are not subject to idle state insertion.	p. 182 ☐
				Write to the BCC register after reset, and then do not change the set values. Also, do not access an external memory area until the initial settings of the BCC register are complete.	p. 182 ☐
				Be sure to set bits 15, 13, 11, and 9 to “1”, and clear bits 14, 12, 10, 8, 6, 4, 2, and 0 to “0”.	p. 182 ☐
Chapter 6	Soft	Clock generation function	PCC register	Do not change the CPU clock (by using the CK3 to CK0 bits) while CLKOUT is being output.	p. 196 ☐
				Use a bit manipulation instruction to manipulate the CK3 bit. When using an 8-bit manipulation instruction, do not change the set values of the CK2 to CK0 bits.	p. 196 ☐
				When stopping the main clock, stop the PLL. Also stop the operations of the on-chip peripheral functions operating with the main clock.	p. 197 ☐
				If the following conditions are not satisfied, change the CK2 to CK0 bits so that the conditions are satisfied, then change to the subclock operation mode. Internal system clock (f_{CLK}) > Subclock (f_{XT}: 32.768 kHz) × 4	p. 197 ☐
				Enable operation of the on-chip peripheral functions operating with the main clock only after the oscillation of the main clock stabilizes. If their operations are enabled before the lapse of the oscillation stabilization time, a malfunction may occur.	p. 198 ☐
			RCM register	The internal oscillator cannot be stopped while the CPU is operating on the internal oscillation clock (CCLS.CCLSF bit = 1). Do not set the RSTOP bit to 1.	p. 199 ☐
				The internal oscillator oscillates if the CCLS.CCLSF bit is set to 1 (when WDT overflow occurs during oscillation stabilization) even when the RSTOP bit is set to 1. At this time, the RSTOP bit remains being set to 1.	p. 199 ☐
			PLLCTL register	When the PLLON bit is cleared to 0, the SELPLL bit is automatically cleared to 0 (clockthrough mode).	p. 201 ☐
				The SELPLL bit can be set to 1 only when the PLL clock frequency is stabilized. If not (unlocked), “0” is written to the SELPLL bit if data is written to it.	p. 201 ☐
			CKC register	The PLL mode cannot be used at f_X = 5.0 to 10.0 MHz.	p. 202 ☐
				Before changing the multiplication factor between 4 and 8 by using the CKC register, set the clock-through mode and stop the PLL.	p. 202 ☐
				Be sure to set bits 3 and 1 to “1” and clear bits 7 to 4 and 2 to “0”.	p. 202 ☐