Renesas Electronics America Inc - UPD70F3744GJ-GAE-AX Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	V850ES
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	CSI, EBI/EMI, I²C, UART/USART
Peripherals	DMA, LVD, PWM, WDT
Number of I/O	128
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	40K x 8
Voltage - Supply (Vcc/Vdd)	2.85V ~ 3.6V
Data Converters	A/D 16x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd70f3744gj-gae-ax

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Pin Name	Pin No.	I/O	Function	Alternate Function
P90	61	I/O	Port 9 16-bit I/O port Input/output can be specified in 1-bit units. N-ch open-drain output can be specified in 1-bit units. 5 V tolerant.	A0/KR6/TXDA1/SDA02
P91	62			A1/KR7/RXDA1/SCL02
P92	63			A2/TIP41/TOP41
P93	64			A3/TIP40/TOP40
P94	65			A4/TIP31/TOP31
P95	66			A5/TIP30/TOP30
P96	67			A6/TIP21/TOP21
P97	68			A7/SIB1/TIP20/TOP20
P98	69			A8/SOB1
P99	70			A9/$\overline{\text{SCKB1}}$
P910	71			A10/SIB3
P911	72			A11/SOB3
P912	73			A12/$\overline{\text{SCKB3}}$
P913	74			A13/INTP4
P914	75			A14/INTP5/TIP51/TOP51
P915	76			A15/INTP6/TIP50/TOP50
PCD0	77	I/O	Port CD 4-bit I/O port Input/output can be specified in 1-bit units.	–
PCD1	78			–
PCD2	79			–
PCD3	80			–
PCM0	85	I/O	Port CM 6-bit I/O port Input/output can be specified in 1-bit units.	$\overline{\text{WAIT}}$
PCM1	86			CLKOUT
PCM2	87			$\overline{\text{HLDAK}}$
PCM3	88			$\overline{\text{HLDRQ}}$
PCM4	89			–
PCM5	90			–
PCS0	81	I/O	Port CS 8-bit I/O port Input/output can be specified in 1-bit units.	$\overline{\text{CS0}}$
PCS1	82			$\overline{\text{CS1}}$
PCS2	83			$\overline{\text{CS2}}$
PCS3	84			$\overline{\text{CS3}}$
PCS4	91			–
PCS5	92			–
PCS6	93			–
PCS7	94			–

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Address	Function Register Name	Symbol	R/W	Manipulatable Bits			Default Value
				1	8	16	
FFFFF0C2H	DMA transfer count register 1	DBC1	R/W			√	Undefined
FFFFF0C4H	DMA transfer count register 2	DBC2				√	Undefined
FFFFF0C6H	DMA transfer count register 3	DBC3				√	Undefined
FFFFF0D0H	DMA addressing control register 0	DADC0				√	0000H
FFFFF0D2H	DMA addressing control register 1	DADC1				√	0000H
FFFFF0D4H	DMA addressing control register 2	DADC2				√	0000H
FFFFF0D6H	DMA addressing control register 3	DADC3				√	0000H
FFFFF0E0H	DMA channel control register 0	DCHC0		√	√		00H
FFFFF0E2H	DMA channel control register 1	DCHC1		√	√		00H
FFFFF0E4H	DMA channel control register 2	DCHC2		√	√		00H
FFFFF0E6H	DMA channel control register 3	DCHC3		√	√		00H
FFFFF100H	Interrupt mask register 0	IMR0				√	FFFFH
FFFFF100H	Interrupt mask register 0L	IMR0L		√	√		FFH
FFFFF101H	Interrupt mask register 0H	IMR0H		√	√		FFH
FFFFF102H	Interrupt mask register 1	IMR1				√	FFFFH
FFFFF102H	Interrupt mask register 1L	IMR1L		√	√		FFH
FFFFF103H	Interrupt mask register 1H	IMR1H		√	√		FFH
FFFFF104H	Interrupt mask register 2	IMR2				√	FFFFH
FFFFF104H	Interrupt mask register 2L	IMR2L		√	√		FFH
FFFFF105H	Interrupt mask register 2H	IMR2H		√	√		FFH
FFFFF106H	Interrupt mask register 3	IMR3				√	FFFFH
FFFFF106H	Interrupt mask register 3L	IMR3L		√	√		FFH
FFFFF107H	Interrupt mask register 3H	IMR3H		√	√		FFH
FFFFF108H	Interrupt mask register 4	IMR4				√	FFFFH
FFFFF108H	Interrupt mask register 4L	IMR4L		√	√		FFH
FFFFF109H	Interrupt mask register 4H	IMR4H		√	√		FFH
FFFFF110H	Interrupt control register	LVIIC		√	√		47H
FFFFF112H	Interrupt control register	PIC0		√	√		47H
FFFFF114H	Interrupt control register	PIC1		√	√		47H
FFFFF116H	Interrupt control register	PIC2		√	√		47H
FFFFF118H	Interrupt control register	PIC3		√	√		47H
FFFFF11AH	Interrupt control register	PIC4		√	√		47H
FFFFF11CH	Interrupt control register	PIC5		√	√		47H
FFFFF11EH	Interrupt control register	PIC6		√	√		47H
FFFFF120H	Interrupt control register	PIC7		√	√		47H
FFFFF122H	Interrupt control register	TQ0OVIC		√	√		47H
FFFFF124H	Interrupt control register	TQ0CCIC0		√	√		47H
FFFFF126H	Interrupt control register	TQ0CCIC1		√	√		47H
FFFFF128H	Interrupt control register	TQ0CCIC2		√	√		47H
FFFFF12AH	Interrupt control register	TQ0CCIC3		√	√		47H
FFFFF12CH	Interrupt control register	TP0OVIC		√	√		47H
FFFFF12EH	Interrupt control register	TP0CCIC0		√	√		47H
FFFFF130H	Interrupt control register	TP0CCIC1		√	√		47H

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Address	Function Register Name	Symbol	R/W	Manipulatable Bits			Default Value
				1	8	16	
FFFFF5C5H	TMP3 option register 0	TP3OPT0	R/W	√	√		00H
FFFFF5C6H	TMP3 capture/compare register 0	TP3CCR0				√	0000H
FFFFF5C8H	TMP3 capture/compare register 1	TP3CCR1				√	0000H
FFFFF5CAH	TMP3 counter read buffer register	TP3CNT	R			√	0000H
FFFFF5D0H	TMP4 control register 0	TP4CTL0	R/W	√	√		00H
FFFFF5D1H	TMP4 control register 1	TP4CTL1		√	√		00H
FFFFF5D2H	TMP4 I/O control register 0	TP4IOC0		√	√		00H
FFFFF5D3H	TMP4 I/O control register 1	TP4IOC1		√	√		00H
FFFFF5D4H	TMP4 I/O control register 2	TP4IOC2		√	√		00H
FFFFF5D5H	TMP4 option register 0	TP4OPT0		√	√		00H
FFFFF5D6H	TMP4 capture/compare register 0	TP4CCR0				√	0000H
FFFFF5D8H	TMP4 capture/compare register 1	TP4CCR1				√	0000H
FFFFF5DAH	TMP4 counter read buffer register	TP4CNT	R			√	0000H
FFFFF5E0H	TMP5 control register 0	TP5CTL0	R/W	√	√		00H
FFFFF5E1H	TMP5 control register 1	TP5CTL1		√	√		00H
FFFFF5E2H	TMP5 I/O control register 0	TP5IOC0		√	√		00H
FFFFF5E3H	TMP5 I/O control register 1	TP5IOC1		√	√		00H
FFFFF5E4H	TMP5 I/O control register 2	TP5IOC2		√	√		00H
FFFFF5E5H	TMP5 option register 0	TP5OPT0		√	√		00H
FFFFF5E6H	TMP5 capture/compare register 0	TP5CCR0				√	0000H
FFFFF5E8H	TMP5 capture/compare register 1	TP5CCR1				√	0000H
FFFFF5EAH	TMP5 counter read buffer register	TP5CNT	R			√	0000H
FFFFF5F0H	TMP6 control register 0	TP6CTL0	R/W	√	√		00H
FFFFF5F1H	TMP6 control register 1	TP6CTL1		√	√		00H
FFFFF5F2H	TMP6 I/O control register 0	TP6IOC0		√	√		00H
FFFFF5F3H	TMP6 I/O control register 1	TP6IOC1		√	√		00H
FFFFF5F4H	TMP6 I/O control register 2	TP6IOC2		√	√		00H
FFFFF5F5H	TMP6 option register 0	TP6OPT0		√	√		00H
FFFFF5F6H	TMP6 capture/compare register 0	TP6CCR0				√	0000H
FFFFF5F8H	TMP6 capture/compare register 1	TP6CCR1				√	0000H
FFFFF5FAH	TMP6 counter read buffer register	TP6CNT	R			√	0000H
FFFFF600H	TMP7 control register 0	TP7CTL0	R/W	√	√		00H
FFFFF601H	TMP7 control register 1	TP7CTL1		√	√		00H
FFFFF602H	TMP7 I/O control register 0	TP7IOC0		√	√		00H
FFFFF603H	TMP7 I/O control register 1	TP7IOC1		√	√		00H
FFFFF604H	TMP7 I/O control register 2	TP7IOC2		√	√		00H
FFFFF605H	TMP7 option register 0	TP7OPT0		√	√		00H
FFFFF606H	TMP7 capture/compare register 0	TP7CCR0				√	0000H
FFFFF608H	TMP7 capture/compare register 1	TP7CCR1				√	0000H
FFFFF60AH	TMP7 counter read buffer register	TP7CNT	R			√	0000H
FFFFF610H	TMP8 control register 0	TP8CTL0	R/W	√	√		00H
FFFFF611H	TMP8 control register 1	TP8CTL1		√	√		00H

CHAPTER 4 PORT FUNCTIONS

4.1 Features

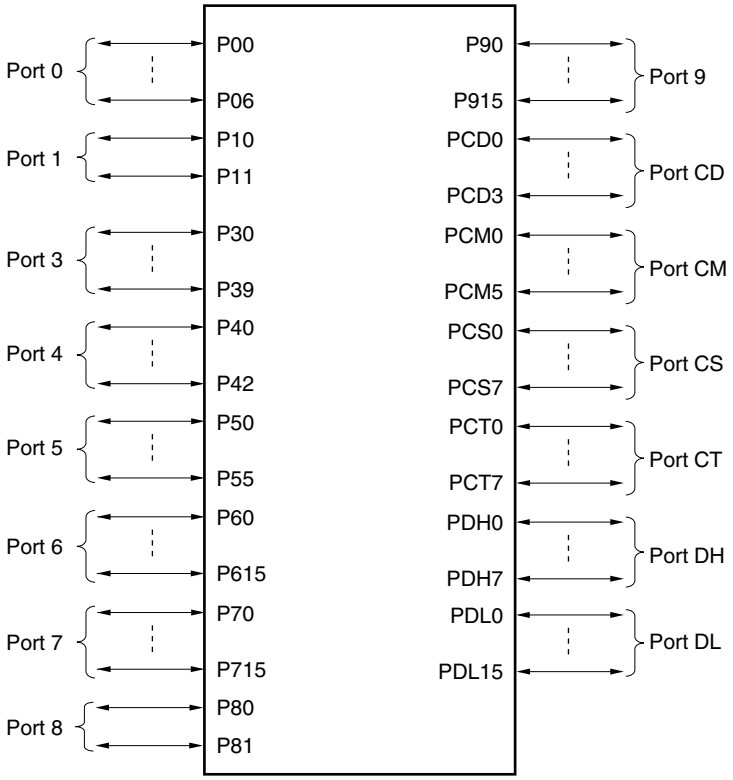
○ I/O ports: 128
- 5 V tolerant/N-ch open-drain output switchable: 60 (ports 0, 3 to 6, 8, 9)

○ Input/output specifiable in 1-bit units

4.2 Basic Port Configuration

The V850ES/JJ3 features a total of 128 I/O ports consisting of ports 0, 1, 3 to 9, CD, CM, CS, CT, DH, and DL. The port configuration is shown below.

Figure 4-1. Port Configuration Diagram



Caution Ports 0, 3 to 6, 8, and 9 are 5 V tolerant.

Table 4-1. I/O Buffer Power Supplies for Pins

Power Supply	Corresponding Pins
AV_{REF0}	Port 7
AV_{REF1}	Port 1
EV_{DD}	$\overline{RESET}$, ports 0, 3 to 6, 8, 9, CD, CM, CS, CT, DH, DL

(4) Port n function control register (PFCn)

The PFCn register specifies the alternate function of a port pin to be used if the pin has two alternate functions.

Each bit of this register corresponds to one pin of port n, and the alternate function of a port pin can be specified in 1-bit units.

After reset: 00H R/W

	7	6	5	4	3	2	1	0
PFCn	PFCn7	PFCn6	PFCn5	PFCn4	PFCn3	PFCn2	PFCn1	PFCn0

PFCnm	Specification of alternate function
0	Alternate function 1
1	Alternate function 2

(5) Port n function control expansion register (PFCEn)

The PFCEn register specifies the alternate function of a port pin to be used if the pin has three or more alternate functions.

Each bit of this register corresponds to one pin of port n, and the alternate function of a port pin can be specified in 1-bit units.

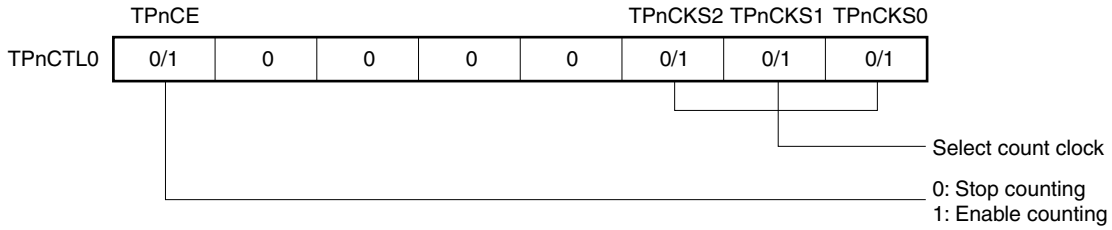
After reset: 00H R/W

	7	6	5	4	3	2	1	0
PFCEn	PFCEn7	PFCEn6	PFCEn5	PFCEn4	PFCEn3	PFCEn2	PFCEn1	PFCEn0
PFCn	PFCn7	PFCn6	PFCn5	PFCn4	PFCn3	PFCn2	PFCn1	PFCn0

PFCEnm	PFCnm	Specification of alternate function
0	0	Alternate function 1
0	1	Alternate function 2
1	0	Alternate function 3
1	1	Alternate function 4

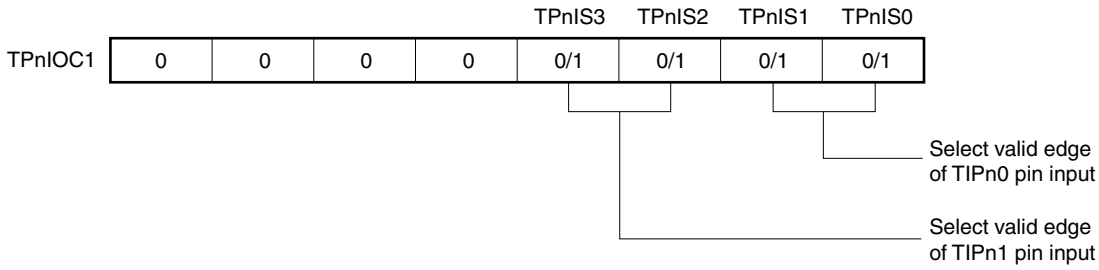
Figure 7-36. Register Setting in Pulse Width Measurement Mode (1/2)

(a) TMPn control register 0 (TPnCTL0)

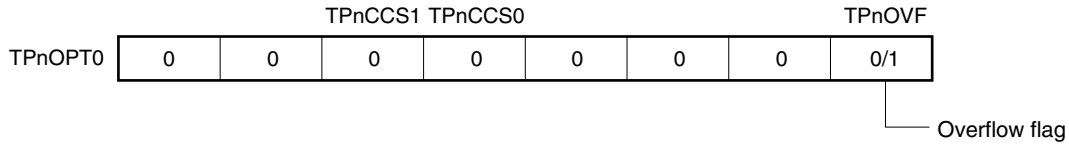


(b) TMPn control register 1 (TPnCTL1)

(c) TMPn I/O control register 1 (TPnIOC1)



(d) TMPn option register 0 (TPnOPT0)



7.5.8 Timer output operations

The following table shows the operations and output levels of the TOPn0 and TOPn1 pins.

Table 7-4. Timer Output Control in Each Mode

Operation Mode	TOPn1 Pin	TOPn0 Pin
Interval timer mode	Square wave output	
External event count mode	Square wave output	–
External trigger pulse output mode	External trigger pulse output	Square wave output
One-shot pulse output mode	One-shot pulse output	
PWM output mode	PWM output	
Free-running timer mode	Square wave output (only when compare function is used)	
Pulse width measurement mode	–	

Remark n = 0 to 8

Table 7-5. Truth Table of TOPn0 and TOPn1 Pins Under Control of Timer Output Control Bits

TPnIOC0.TPnOLm Bit	TPnIOC0.TPnOEm Bit	TPnCTL0.TPnCE Bit	Level of TOPnm Pin
0	0	×	Low-level output
	1	0	Low-level output
		1	Low level immediately before counting, high level after counting is started
1	0	×	High-level output
	1	0	High-level output
		1	High level immediately before counting, low level after counting is started

Remark n = 0 to 8
m = 0, 1

(5) TMQ0 I/O control register 2 (TQ0IOC2)

The TQ0IOC2 register is an 8-bit register that controls the valid edge of the external event count input signal (TIQ00 pin) and external trigger input signal (TIQ00 pin).

This register can be read or written in 8-bit or 1-bit units.

Reset sets this register to 00H.

After reset: 00H R/W Address: FFFFF544H

	7	6	5	4	3	2	1	0
TQ0IOC2	0	0	0	0	TQ0EES1	TQ0EES0	TQ0ETS1	TQ0ETS0

TQ0EES1	TQ0EES0	External event count input signal (TIQ00 pin) valid edge setting
0	0	No edge detection (external event count invalid)
0	1	Detection of rising edge
1	0	Detection of falling edge
1	1	Detection of both edges

TQ0ETS1	TQ0ETS0	External trigger input signal (TIQ00 pin) valid edge setting
0	0	No edge detection (external trigger invalid)
0	1	Detection of rising edge
1	0	Detection of falling edge
1	1	Detection of both edges

Cautions

1. **Rewrite the TQ0EES1, TQ0EES0, TQ0ETS1, and TQ0ETS0 bits when the TQ0CTL0.TQ0CE bit = 0. (The same value can be written when the TQ0CE bit = 1.) If rewriting was mistakenly performed, clear the TQ0CE bit to 0 and then set the bits again.**
2. **The TQ0EES1 and TQ0EES0 bits are valid only when the TQ0CTL1.TQ0EEE bit = 1 or when the external event count mode (TQ0CTL1.TQ0MD2 to TQ0CTL1.TQ0MD0 bits = 001) has been set.**
3. **The TQ0ETS1 and TQ0ETS0 bits are valid only when the external trigger pulse output mode (TQ0CTL1.TQ0MD2 to TQ0CTL1.TQ0MD0 bits = 010) or the one-shot pulse output mode (TQ0CTL1.TQ0MD2 to TQ0CTL1.TQ0MD0 = 011) is set.**

When the TQ0CE bit is set to 1, 16-bit timer/event counter Q waits for a trigger. When the trigger is generated, the 16-bit counter is cleared from FFFFH to 0000H, starts counting, and outputs a one-shot pulse from the TOQ0k pin. After the one-shot pulse is output, the 16-bit counter is set to FFFFH, stops counting, and waits for a trigger. If a trigger is generated again while the one-shot pulse is being output, it is ignored.

The output delay period and active level width of the one-shot pulse can be calculated as follows.

Output delay period = (Set value of TQ0CCRk register) × Count clock cycle

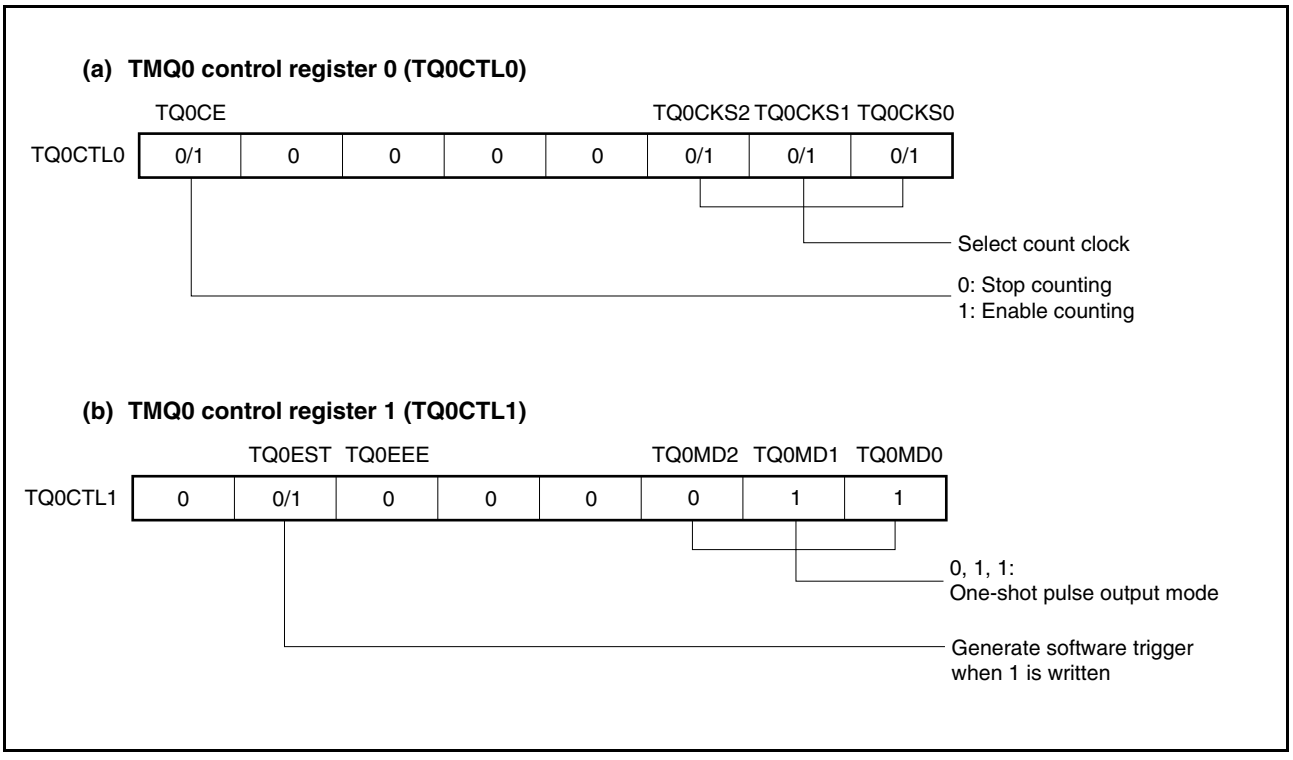
Active level width = (Set value of TQ0CCR0 register − Set value of TQ0CCRk register + 1) × Count clock cycle

The compare match interrupt request signal INTTQ0CC0 is generated when the 16-bit counter counts after its count value matches the value of the CCR0 buffer register. The compare match interrupt request signal INTTQ0CCk is generated when the count value of the 16-bit counter matches the value of the CCRk buffer register.

The valid edge of an external trigger input or setting the software trigger (TQ0CTL1.TQ0EST bit) to 1 is used as the trigger.

Remark k = 1 to 3

Figure 8-22. Register Setting for Operation in One-Shot Pulse Output Mode (1/3)



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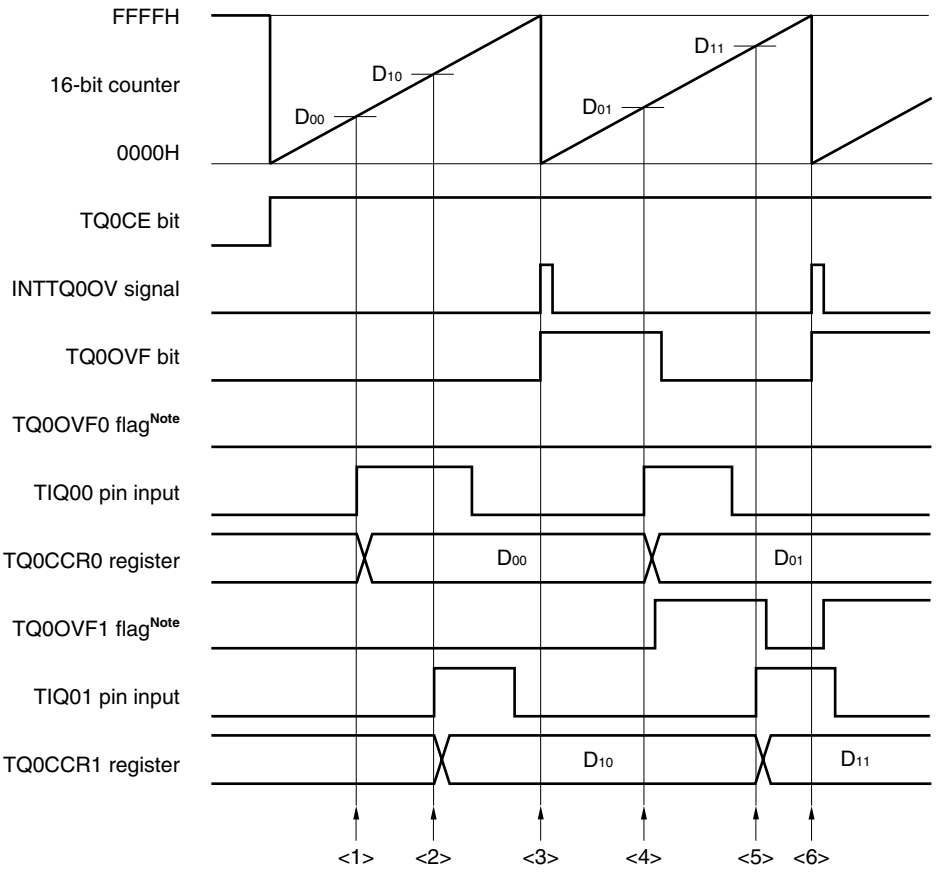
Example when two capture registers are used (without using overflow interrupt)



Note The TQ0OVF0 and TQ0OVF1 flags are set on the internal RAM by software.

<1> Read the TQ0CCR0 register (setting of the default value of the TIQ00 pin input).
<2> Read the TQ0CCR1 register (setting of the default value of the TIQ01 pin input).
<3> An overflow occurs. Nothing is done by software.
<4> Read the TQ0CCR0 register.
Read the overflow flag. If the overflow flag is 1, set only the TQ0OVF1 flag to 1, and clear the overflow flag to 0.
Because the overflow flag is 1, the pulse width can be calculated by (10000H + D_{01} − D_{00}).
<5> Read the TQ0CCR1 register.
Read the overflow flag. Because the overflow flag is cleared in <4>, 0 is read.
Read the TQ0OVF1 flag. If the TQ0OVF1 flag is 1, clear it to 0.
Because the TQ0OVF1 flag is 1, the pulse width can be calculated by (10000H + D_{11} − D_{10}) (correct).
<6> Same as <3>

(2) D/A conversion value setting registers 0, 1 (DA0CS0, DA0CS1)

The DA0CS0 and DA0CS1 registers set the analog voltage value output to the ANO0 and ANO1 pins.

These registers can be read or written in 8-bit units.

Reset sets these registers to 00H.

After reset: 00H R/W Address: DA0CS0 FFFFF280H, DA0CS1 FFFFF281H

	7	6	5	4	3	2	1	0
DA0CSn	DA0CSn7	DA0CSn6	DA0CSn5	DA0CSn4	DA0CSn3	DA0CSn2	DA0CSn1	DA0CSn0

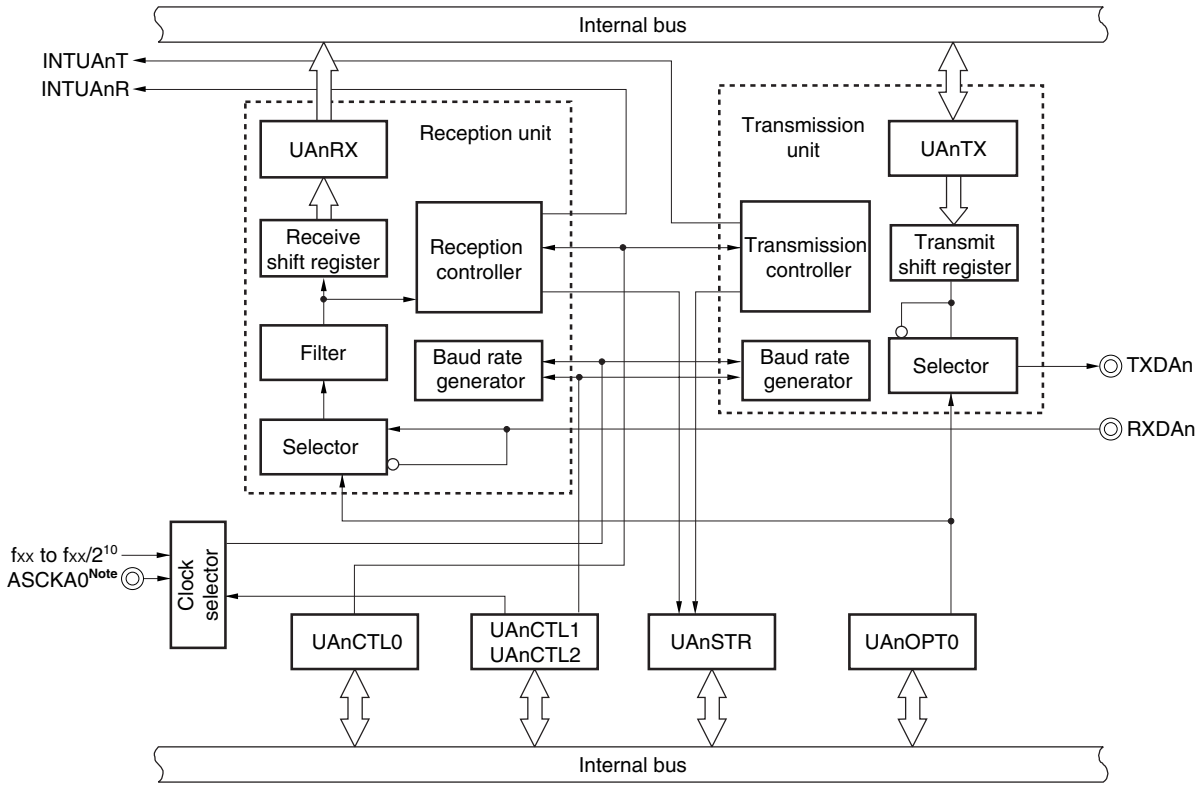
Caution In the real-time output mode (DA0M.DA0MDn bit = 1), set the DA0CSn register before the INTTP2CC0/INTTP3CC0 signals are generated. D/A conversion starts when the INTTP2CC0/INTTP3CC0 signals are generated.

Remark n = 0, 1

15.3 Configuration

The block diagram of the UARTAn is shown below.

Figure 15-4. Block Diagram of Asynchronous Serial Interface An



Note UARTA0 only

Remarks 1. n = 0 to 3

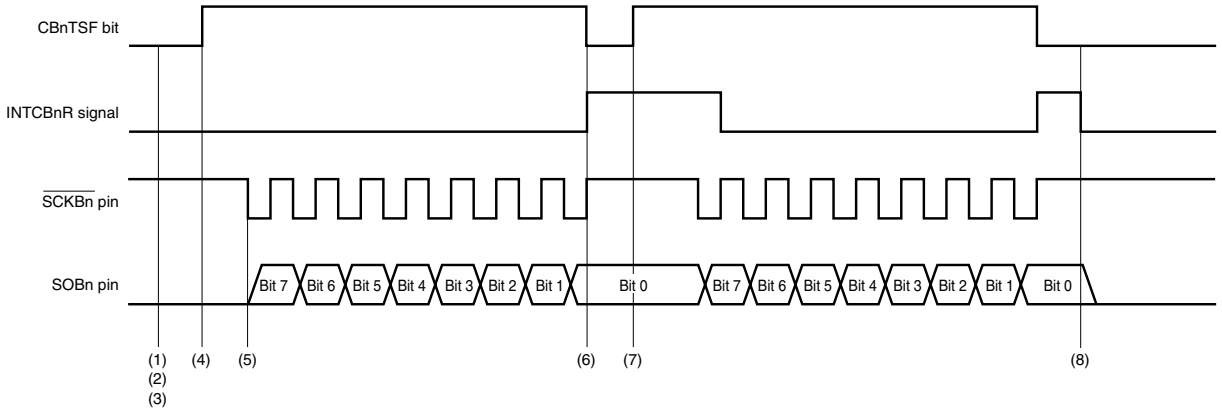
2. For the configuration of the baud rate generator, see **Figure 15-16**.

UARTAn includes the following hardware.

Table 15-1. Configuration of UARTAn

Item	Configuration
Registers	UARTAn control register 0 (UAnCTL0) UARTAn control register 1 (UAnCTL1) UARTAn control register 2 (UAnCTL2) UARTAn option control register 0 (UAnOPT0) UARTAn status register (UAnSTR) UARTAn receive shift register UARTAn receive data register (UAnRX) UARTAn transmit shift register UARTAn transmit data register (UAnTX)

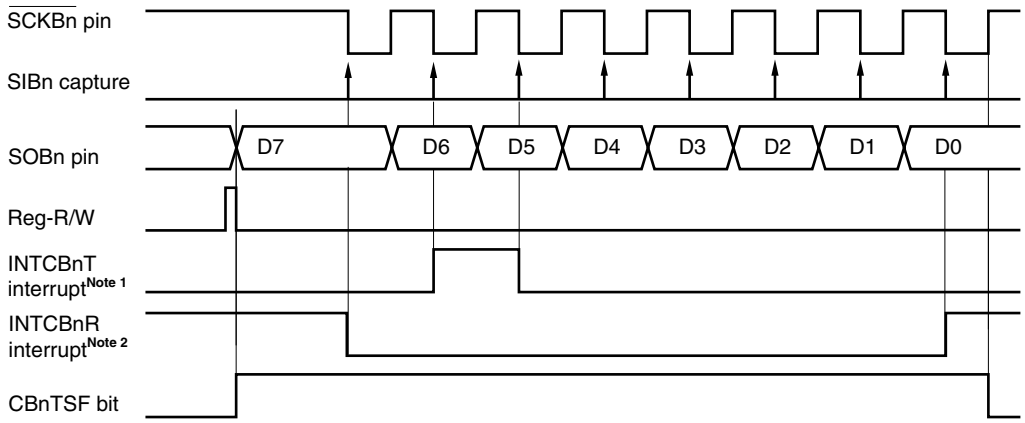
(2) Operation timing



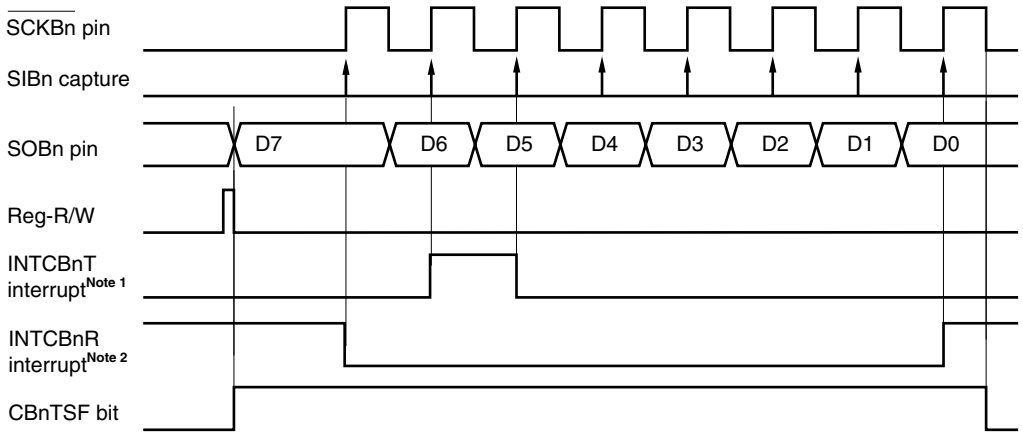
(1) Write 07H to the CBnCTL1 register, and select communication type 1, communication clock (f_{CCLK}) = external clock ($\overline{SCKBn}$), and slave mode.
(2) Write 00H to the CBnCTL2 register, and set the transfer data length to 8 bits.
(3) Write C1H to the CBnCTL0 register, and select the transmission mode and MSB first at the same time as enabling the operation of the communication clock (f_{CCLK}).
(4) The CBnSTR.CBnTSF bit is set to 1 by writing the transmit data to the CBnTX register, and the device waits for a serial clock input.
(5) When a serial clock is input, output the transmit data from the SOBn pin in synchronization with the serial clock.
(6) When transmission of the transfer data length set with the CBnCTL2 register is completed, stop the serial clock input and transmit data output, generate the reception completion interrupt request signal (INTCBnR) at the last edge of the serial clock, and clear the CBnTSF bit to 0.
(7) To continue transmission, write the transmit data to the CBnTX register again after the INTCBnR signal is generated, and wait for a serial clock input.
(8) To end transmission, write the CBnCTL0.CBnPWR bit = 0 and the CBnCTL0.CBnTXE bit = 0.

Remark n = 0 to 5

(iii) Communication type 2 (CBnCKP and CBnDAP bits = 01)



(iv) Communication type 4 (CBnCKP and CBnDAP bits = 11)



Notes 1. The INTCBnT interrupt is set when the data written to the CBnTX register is transferred to the data shift register in the continuous transmission or continuous transmission/reception modes. In the single transmission or single transmission/reception modes, the INTCBnT interrupt request signal is not generated, but the INTCBnR interrupt request signal is generated upon end of communication.

2. The INTCBnR interrupt occurs if reception is correctly ended and receive data is ready in the CBnRX register while reception is enabled. In the single mode, the INTCBnR interrupt request signal is generated even in the transmission mode, upon end of communication.

Caution In single transfer mode, writing to the CBnTX register with the CBnTSF bit set to 1 is ignored. This has no influence on the operation during transfer.
For example, if the next data is written to the CBnTX register when DMA is started by generating the INTCBnR signal, the written data is not transferred because the CBnTSF bit is set to 1.
Use the continuous transfer mode, not the single transfer mode, for such applications.

17.14.2 When communication reservation function is disabled (IICFn.IICRSVn bit = 1)

When the IICCn.STTn bit is set when the bus is not used in a communication during bus communication, this request is rejected and a start condition is not generated. There are two modes in which the bus is not used.

- When arbitration results in neither master nor slave operation
- When an extension code is received and slave operation is disabled ($\overline{ACK}$ is not returned and the bus was released when the IICCn.LRELn bit was set to 1) (n = 0 to 2).

To confirm whether the start condition was generated or request was rejected, check the IICFn.STCFn flag. The time shown in Table 17-7 is required until the STCFn flag is set after setting the STTn bit to 1. Therefore, secure the time by software.

Table 17-7. Wait Periods

OCKSENm	OCKSm1	OCKSm0	CLn1	CLn0	Wait Period
1	0	0	0	×	10 clocks
1	0	1	0	×	15 clocks
1	1	0	0	×	20 clocks
1	1	1	0	×	25 clocks
0	0	0	1	0	5 clocks

Remarks 1. ×: don't care

2. n = 0 to 2
m = 0, 1

19.4.3 EP flag

The EP flag is a status flag used to indicate that exception processing is in progress. It is set when an exception occurs.

After reset: 00000020H

	31	8	7	6	5	4	3	2	1	0
PSW	0		NP	**EP**	ID	SAT	CY	OV	S	Z

EP	Exception processing status
0	Exception processing not in progress.
1	Exception processing in progress.

24.4 Operation

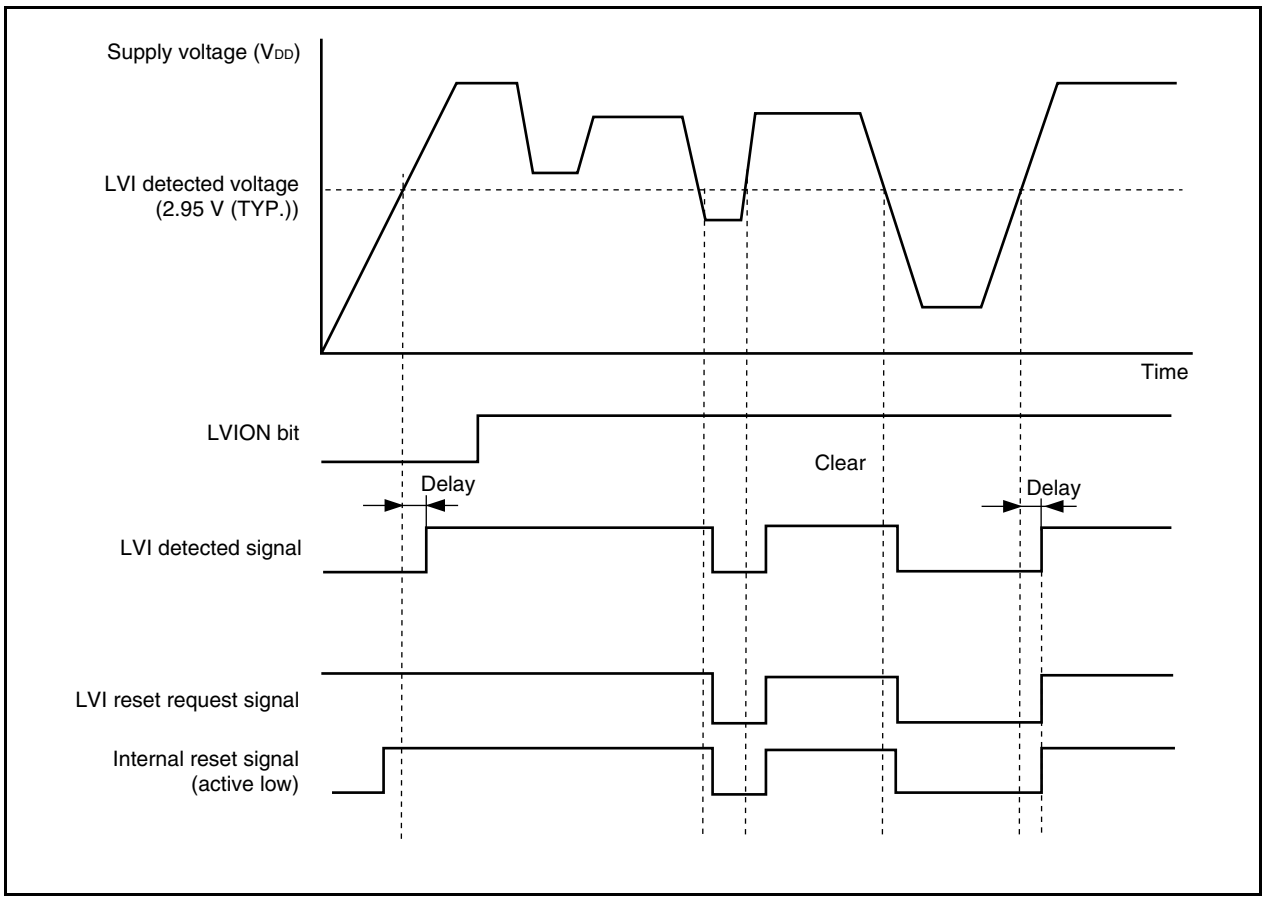
Depending on the setting of the LVIM.VIMD bit, an interrupt signal (INTLVI) or an internal reset signal is generated. How to specify each operation is described below, together with timing charts.

24.4.1 To use for internal reset signal

<To start operation>
<1> Mask the interrupt of LVI.
<2> Select the voltage to be detected by using the LVIS.LVIS0 bit.
<3> Set the LVIM.LVION bit to 1 (to enable operation).
<4> Insert a wait cycle of 0.2 ms (max.) or more by software.
<5> By using the LVIM.LVIF bit, check if the supply voltage > detected voltage.
<6> Set the LVIMD bit to 1 (to generate an internal reset signal).

Caution If the LVIMD bit is set to 1, the contents of the LVIM and LVIS registers cannot be changed until a reset request other than LVI is generated.

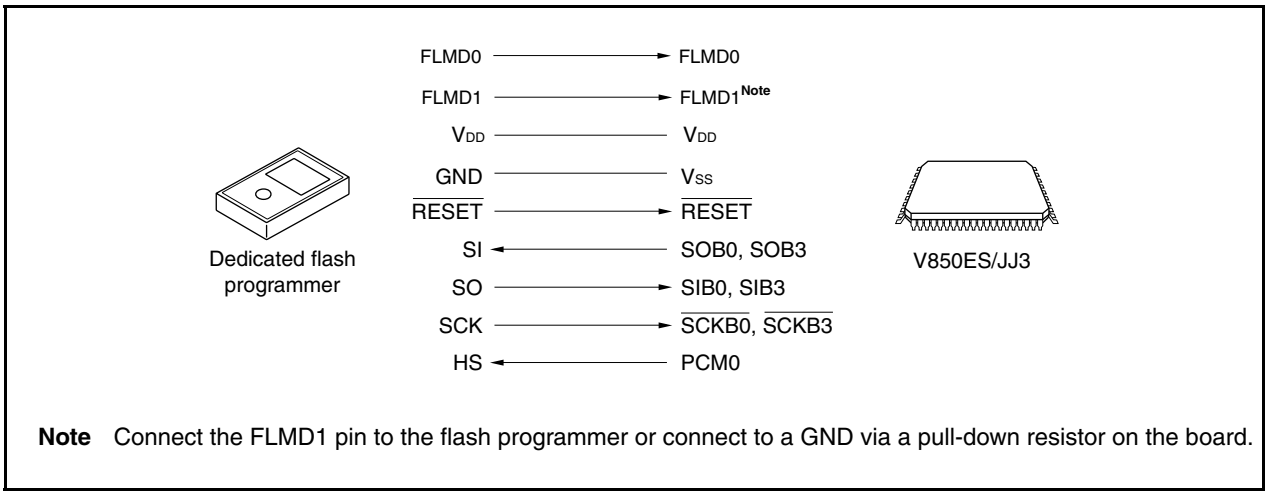
Figure 24-2. Operation Timing of Low-Voltage Detector (LVIMD Bit = 1)



(3) CSIB0 + HS, CSIB3 + HS

Serial clock: 2.4 kHz to 2.5 MHz (MSB first)

Figure 27-5. Communication with Dedicated Flash Programmer (CSIB0 + HS, CSIB3 + HS)



Note Connect the FLMD1 pin to the flash programmer or connect to a GND via a pull-down resistor on the board.

The dedicated flash programmer outputs the transfer clock, and the V850ES/JJ3 operates as a slave.

When the PG-FP4 is used as the dedicated flash programmer, it generates the following signals to the V850ES/JJ3. For details, refer to the **PG-FP4 User's Manual (U15260E)**.

Table 27-5. Signal Connections of Dedicated Flash Programmer (PG-FP4)

PG-FP4			V850ES/JJ3	Processing for Connection		
Signal Name	I/O	Pin Function	Pin Name	UARTA0	CSIB0, CSIB3	CSIB0 + HS, CSIB3 + HS
FLMD0	Output	Write enable/disable	FLMD0	◎	◎	◎
FLMD1	Output	Write enable/disable	FLMD1	◎Note 1	◎Note 1	◎Note 1
VDD	–	VDD voltage generation/voltage monitor	VDD	◎	◎	◎
GND	–	Ground	VSS	◎	◎	◎
CLK	Output	Clock output to V850ES/JJ3	X1, X2	×Note 2	×Note 2	×Note 2
RESET	Output	Reset signal	RESET	◎	◎	◎
SI/RxD	Input	Receive signal	SOB0, SOB3/ TXDA0	◎	◎	◎
SO/TxD	Output	Transmit signal	SIB0, SIB3/ RXDA0	◎	◎	◎
SCK	Output	Transfer clock	SCKB0, SCKB3	×	◎	◎
HS	Input	Handshake signal for CSIB0 + HS, CSIB3 + HS communication	PCM0	×	×	◎

Notes 1. Wire these pins as shown in Figure 27-6, or connect then to GND via pull-down resistor on board.

2. Clock cannot be supplied via the CLK pin of the flash programmer. Create an oscillator on board and supply the clock.

Remark ◎: Must be connected.

×: Does not have to be connected.

- Port registers when UARTA0 is used

  When UARTA0 is used, port registers are set to make the TXDA0 and RXDA0 pins valid by the debug monitor program. Do not change the following register settings with the user program during debugging. (The same value can be overwritten.)

	7	6	5	4	3	2	1	0
PFC3	×	×	×	×	×	×	0	0

	7	6	5	4	3	2	1	0
PMC3L	×	×	×	×	×	×	1	1

Remark ×: don't care

- Port registers when CSIB0 is used

  When CSIB0 is used, port registers are set to make the SIB0, SOB0, $\overline{\text{SCKB0}}$, and HS (PMC0) pins valid by the debug monitor program. Do not change the following register settings with the user program during debugging. (The same value can be overwritten.)

(a) SIB0, SOB0, and $\overline{\text{SCKB0}}$ settings

	7	6	5	4	3	2	1	0
PMC4	×	×	×	×	×	1	1	1

	7	6	5	4	3	2	1	0
PFC4	×	×	×	×	×	×	0	0

(b) HS (PMC0 pin) settings

	7	6	5	4	3	2	1	0
PMCM	×	×	×	×	×	×	×	0

	7	6	5	4	3	2	1	0
PCM	×	×	×	×	×	×	×	**Note**

Note Writing to this bit is prohibited.
The port values corresponding to the HS pin are changed by the monitor program according to the debugger status. To perform port register settings in 8-bit units, the user program can usually use read-modify-write. If an interrupt for debugging occurs before writing, however, an unexpected operation may be performed.

Remark ×: don't care

(14/37)

Chapter	Classification	Function	Details of Function	Cautions	Page
Chapter 11	Soft	Watchdog timer 2 function	WDTM2 register	To stop the operation of watchdog timer 2, set the RCM.RSTOP bit to 1 (to stop the internal oscillator) and write 00H in the WDTM2 register. If the RCM.RSTOP bit cannot be set to 1, set the WDCS23 bit to 1 (2^n/f_{XX} is selected and the clock can be stopped in the IDLE1, IDLW2, sub-IDLE, and subclock operation modes).	p. 413 ☐
			WDTE register	When a value other than “ACH” is written to the WDTE register, an overflow signal is forcibly output.	p. 414 ☐
				When a 1-bit memory manipulation instruction is executed for the WDTE register, an overflow signal is forcibly output.	p. 414 ☐
				To intentionally generate an overflow signal, write a value other than “ACH” to the WDTE register only once, or write data to the WDTM2 register only twice. However, when the watchdog timer 2 is set to stop operation, an overflow signal is not generated even if data is written to the WDTM2 register only twice, or a value other than “ACH” is written to the WDTE register only once.	p. 414 ☐
				The read value of the WDTE register is “9AH” (which differs from written value “ACH”).	p. 414 ☐
Chapter 12	Soft	Real-time output function (RTO)	RTBLn, RTBHn registers	When writing to bits 6 and 7 of the RTBHn register, always write 0.	p. 418 ☐
				Accessing the RTBLn and RTBHn registers is prohibited in the following statuses. For details, see **3.4.8 (2) Accessing specific on-chip peripheral I/O registers**. • When the CPU operates with the subclock and the main clock oscillation is stopped • When the CPU operates with the internal oscillation clock	p. 418 ☐
				After setting the real-time output port, set output data to the RTBLn and RTBHn registers by the time a realtime output trigger is generated.	p. 418 ☐
			RTPMn register	By enabling the real-time output operation (RTPCn.RTPOEn bit = 1), the bits enabled to real-time output among the RTPn0 to RTPn5 signals perform realtime output, and the bits set to port mode output 0.	p. 419 ☐
				If real-time output is disabled (RTPOEn bit = 0), the real-time output pins (RTPn0 to RTPn5) all output 0, regardless of the RTPMn register setting.	p. 419 ☐
				In order to use this register as the real-time output pins (RTPn0 to RTPn5), set these pins as real-time output port pins using the PMC and PFC registers.	p. 419 ☐
			RTPCn register	Set the RTPEGn, BYTEn, and EXTRn bits only when RTPOEn bit = 0.	p. 420 ☐
			Realtime output operation	Prevent the following conflicts by software. • Conflict between real-time output disable/enable switching (RTPOEn bit) and selected real-time output trigger. • Conflict between writing to the RTBHn and RTBLn registers in the real-time output enabled status and the selected real-time output trigger.	p. 422 ☐
			Initialization	Before performing initialization, disable real-time output (RTPOEn bit = 0).	p. 422 ☐
			RTBHn, RTBLn registers	Once real-time output has been disabled (RTPOEn bit = 0), be sure to initialize the RTBHn and RTBLn registers before enabling real-time output again (RTPOEn bit = 0 → 1).	p. 422 ☐
Chapter 13	Hard	A/D converter	ANI0 to ANI15 pins	Make sure that the voltages input to the ANI0 to ANI15 pins do not exceed the rated values. In particular if a voltage of AV_{REF0} or higher is input to a channel, the conversion value of that channel becomes undefined, and the conversion values of the other channels may also be affected.	p. 426 ☐
	Soft		ADA0M0 register	Accessing the ADA0M0 register is prohibited in the following statuses. For details, see **3.4.8 (2) Accessing specific on-chip peripheral I/O registers**. • When the CPU operates with the subclock and the main clock oscillation is stopped • When the CPU operates with the internal oscillation clock	p. 428 ☐