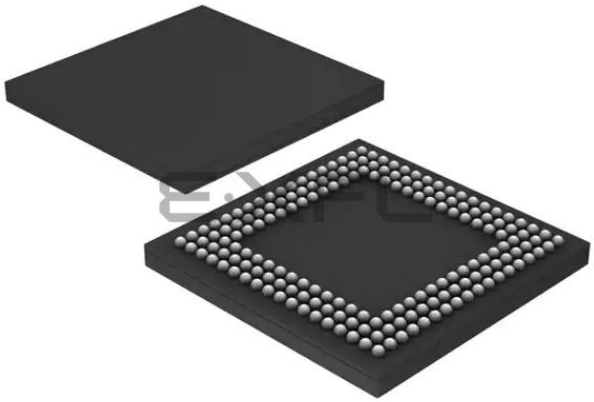

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM926EJ-S
Core Size	16/32-Bit
Speed	270MHz
Connectivity	EBI/EMI, I²C, IrDA, Memory Card, PCM, SPI, UART/USART, USB OTG
Peripherals	DMA, I²S, LCD, PWM, WDT
Number of I/O	20
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	192K x 8
Voltage - Supply (Vcc/Vdd)	1.1V ~ 3.6V
Data Converters	A/D 4x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	180-TFBGA
Supplier Device Package	180-TFBGA (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc3141fet180-551

Table 4. Pin description *…continued*

Pin names with prefix m are multiplexed pins. See Table 10 for pin function selection of multiplexed pins.

Pin name	BGA Ball	Digital I/O level [1]	Application function	Pin state after reset[2]	Cell type [3]	Description
VSSE_IOC	B12; D6; D8; D9; G11; L9; L13	-	Ground	-	PG1	-
LCD interface						
mLCD_CSB[4]	K8	SUP8	DO	O	DIO4	LCD chip select (active LOW).
mLCD_E_RD[4]	L8	SUP8	DO	O	DIO4	LCD 6800 enable or 8080 read enable (active HIGH).
mLCD_RS[4]	P8	SUP8	DO	O	DIO4	LCD instruction register (LOW)/data register (HIGH) select.
mLCD_RW_WR[4]	N9	SUP8	DO	O	DIO4	LCD 6800 read/write select or 8080 write enable (active HIGH).
mLCD_DB_0[4]	N8	SUP8	DIO	O	DIO4	LCD data 0.
mLCD_DB_1[4]	P9	SUP8	DIO	O	DIO4	LCD data 1.
mLCD_DB_2[4]	N6	SUP8	DIO	O	DIO4	LCD data 2.
mLCD_DB_3[4]	P6	SUP8	DIO	O	DIO4	LCD data 3.
mLCD_DB_4[4]	N7	SUP8	DIO	O	DIO4	LCD data 4.
mLCD_DB_5[4]	P7	SUP8	DIO	O	DIO4	LCD data 5.
mLCD_DB_6[4]	K6	SUP8	DIO	O	DIO4	LCD data 6.
mLCD_DB_7[4]	P5	SUP8	DIO	O	DIO4	LCD data 7.
mLCD_DB_8[4]	N5	SUP8	DIO	O	DIO4	LCD data 8/8-bit data 0.
mLCD_DB_9[4]	L5	SUP8	DIO	O	DIO4	LCD data 9/8-bit data 1.
mLCD_DB_10[4]	K7	SUP8	DIO	O	DIO4	LCD data 10/8-bit data 2.
mLCD_DB_11[4]	N4	SUP8	DIO	O	DIO4	LCD data 11/8-bit data 3.
mLCD_DB_12[4]	K5	SUP8	DIO	O	DIO4	LCD data 12/8-bit data 4/4-bit data 0.
mLCD_DB_13[4]	P4	SUP8	DIO	O	DIO4	LCD data 13/8-bit data 5/4-bit data 1/serial clock output.
mLCD_DB_14[4]	P3	SUP8	DIO	O	DIO4	LCD data 14/8-bit data 6/4-bit data 2/serial data input.
mLCD_DB_15[4]	N3	SUP8	DIO	O	DIO4	LCD data 15/8-bit data 7/4-bit data 3/serial data output.
I^2S/digital audio input						
I2SRX_DATA0[4]	M10	SUP3	DI/GPIO	I	DIO1	I^2S serial data receive input.
I2SRX_DATA1[4]	G14	SUP3	DI/GPIO	I	DIO1	I^2S serial data receive input.
I2SRX_BCK0[4]	N10	SUP3	DIO/GPIO	I	DIO1	I^2S bit clock.
I2SRX_BCK1[4]	F14	SUP3	DIO/GPIO	I	DIO1	I^2S bit clock.
I2SRX_WS0[4]	P11	SUP3	DIO/GPIO	I	DIO1	I^2S word select.
I2SRX_WS1[4]	F13	SUP3	DIO/GPIO	I	DIO1	I^2S word select.

Table 9: Peripherals that support DMA *…continued*

Peripheral name	Supported transfer types
$I^2S0/1$ receive	Peripheral to Memory
$I^2S0/1$ transmit	Memory to peripheral
PCM interface	Memory to peripheral and peripheral to memory

[1] AES decryption engine is available on LPC3143 only.

6.12 Interrupt controller

The interrupt controller collects interrupt requests from multiple devices, masks interrupt requests, and forwards the combined requests to the processor. The interrupt controller also provides facilities to identify the interrupt requesting devices to be served.

This module has the following features:

- The interrupt controller decodes all the interrupt requests issued by the on-chip peripherals.
- Two interrupt lines (Fast Interrupt Request (FIQ), Interrupt Request (IRQ)) to the ARM core. The ARM core supports two distinct levels of priority on all interrupt sources, FIQ for high priority interrupts and IRQ for normal priority interrupts.
- Software interrupt request capability associated with each request input.
- Visibility of interrupts request state before masking.
- Support for nesting of interrupt service routines.
- Interrupts routed to IRQ and to FIQ are vectored.
- Level interrupt support.

The following blocks can generate interrupts:

- NAND flash controller
- USB 2.0 HS OTG
- Event router
- 10 bit ADC
- UART
- LCD interface
- MCI
- SPI
- I^2C0-bus and I^2C1-bus controllers
- Timer 0, timer 1, timer 2, and timer 3
- I^2S transmit: I2STX_0 and I2STX_1
- I^2S receive: I2SRX_0 and I2SRX_1
- DMA

6.13 Multi-layer AHB

The multi-layer AHB is an interconnection scheme based on the AHB protocol that enables parallel access paths between multiple masters and slaves in a system.

Multiple masters can have access to different slaves at the same time.

Figure 5 gives an overview of the multi-layer AHB configuration in the LPC3141/3143. AHB masters and slaves are numbered according to their AHB port number.

This module has the following features:

- Supports all combinations of 32-bit masters and slaves (fully connected interconnect matrix).
- Round-Robin priority mechanism for bus arbitration: all masters have the same priority and get bus access in their natural order.
- Four devices on a master port (listed in their natural order for bus arbitration):
  - DMA
  - ARM926 instruction port
  - ARM926 data port
  - USB OTG
- Devices on a slave port (some ports are shared between multiple devices):
  - AHB to APB bridge 0
  - AHB to APB bridge 1
  - AHB to APB bridge 2
  - AHB to APB bridge 3
  - AHB to APB bridge 4
  - Interrupt controller
  - NAND flash controller
  - MCI SD/SDIO
  - USB 2.0 HS OTG
  - 96 kB ISRAM
  - 96 kB ISRAM
  - 128 kB ROM
  - MPMC (Multi-Purpose Memory Controller)

6.14 APB bridge

The APB bridge is a bus bridge between AMBA Advanced High-performance Bus (AHB) and the ARM Peripheral Bus (APB) interface.

The module supports two different architectures:

- Single-clock architecture, synchronous bridge. The same clock is used at the AHB side and at the APB side of the bridge. The AHB-to-APB4 bridge uses this architecture.
- Dual-clock architecture, asynchronous bridge. Different clocks are used at the AHB side and at the APB side of the bridge. The AHB-to-APB0, AHB-to-APB1, AHB-to-APB2, and AHB-to-APB3 bridges use this architecture.

6.15 Clock Generation Unit (CGU)

The clock generation unit generates all clock signals in the system and controls the reset signals for all modules. The structure of the CGU is shown in Figure 6. Each output clock generated by the CGU belongs to one of the domains. Each clock domain is fed by a single base clock that originates from one of the available clock sources. Within a clock domain, fractional dividers are available to divide the base clock to a lower frequency.

Within most clock domains, the output clocks are again grouped into one or more subdomains. All output clocks within one subdomain are either all generated by the same fractional divider or they are connected directly to the base clock. Therefore all output clocks within one subdomain have the same frequency and all output clocks within one clock domain are synchronous because they originate from the same base clock.

The CGU reference clock is generated by the external crystal. Furthermore the CGU has several Phase Locked Loop (PLL) circuits to generate clock signals that can be used for system clocks and/or audio clocks. All clock sources, except the output of the PLLs, can be used as reference input for the PLLs.

This module has the following features:

- Advanced features to optimize the system for low power:
  - All output clocks can be disabled individually for flexible power optimization.
  - Some modules have automatic clock gating: they are only active when (bus) access to the module is required.
  - Variable clock scaling for automatic power optimization of the AHB bus (high clock frequency when the bus is active, low clock frequency when the bus is idle).
  - Clock wake-up feature: module clocks can be programmed to be activated automatically on the basis of an event detected by the event router (see also Section 6.19). For example, all clocks (including the core/bus clocks) are off and activated automatically when a button is pressed.
- Supports five clock sources:
  - Reference clock generated by the oscillator with an external crystal.
  - Pins I2SRX_BCK0, I2SRX_WS0, I2SRX_BCK1 and I2SRX_WS1 are used to input external clock signals (used for generating audio frequencies in I2SRX slave mode, see also Section 6.4).
- Supports two PLLs:
  - System PLL generates programmable system clock frequency from its reference input.
  - I^2S/Audio PLL generates programmable audio clock frequency (typically 256 $\times$ fs) from its reference input.

    Remark: Both the System PLL and the I^2S/Audio PLL generate their frequencies based on their (individual) reference clocks. The reference clocks can be programmed to the oscillator clock or one of the external clock signals.
- Highly flexible switchbox to distribute the signals from the clock sources to the module clocks.
  - Each clock generated by the CGU is derived from one of the base clocks and optionally divided by a fractional divider.

- After a reset, a register will indicate whether a reset has occurred because of a watchdog generated reset.
- Watchdog timer can also be used as a normal timer in addition to the watchdog functionality (output m0).

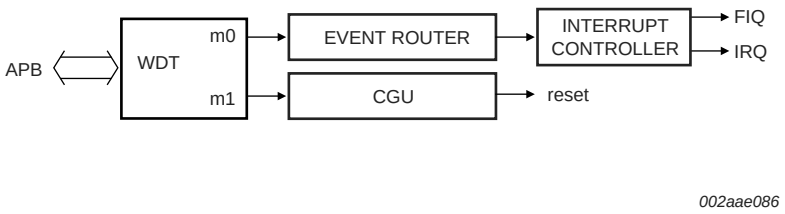


Fig 7. Block diagram of the Watchdog Timer

6.17 Input/Output Configuration module (IOCONFIG)

The General Purpose Input/Output (GPIO) pins can be controlled through the register interface provided by the IOCONFIG module. Next to several dedicated GPIO pins, most digital IO pins can also be used as GPIO if they are not required for their normal, dedicated function.

This module has the following features:

- Provides control for the digital pins that can double as GPIO (next to their normal function). The pinning list in Table 4 indicates which pins can double as GPIO.
- Each controlled pin can be configured for 4 operational modes:
  - Normal operation (i.e. controlled by a function block)
  - Driven LOW
  - Driven HIGH
  - High impedance/input
- A GPIO pin can be observed (read) in any mode.
- The register interface provides ‘set’ and ‘clear’ access methods for choosing the operational mode.

6.18 10-bit Analog-to-Digital Converter (ADC10B)

This module is a 10-bit successive approximation ADC with an input multiplexer to allow for multiple analog signals on its input. A common use of this module is to read out multiple keys on one input from a resistor network.

This module has the following features:

- Four analog input channels, selected by an analog multiplexer.
- Programmable ADC resolution from 2 bit to 10 bit.
- The maximum conversion rate is 400 kSamples/s for 10 bit resolution and 1500 kSamples/s for 2 bit resolution.
- Single and continuous analog-to-digital conversion scan modes.
- Power-down mode.

- MP PCM: Multi-Protocol PCM. Configurable directional per slot.
- IOM-2: Extended ISDN-Oriented modular. Double clocking physical format.

- Twelve 8-bit slots in a frame with enabling control per slot.
- Internal frame clock generation in master mode.
- Receive and transmit DMA handshaking using a request/clear protocol.
- Interrupt generation per frame.

PCM (Pulse Code Modulation) is a very common method used for transmitting analog data in digital format. Most common applications of PCM are Digital audio as in Audio CD and computers, digital telephony and digital videos.

The IOM (ISDN Oriented Modular) interface is primarily used to interconnect telecommunications ICs providing ISDN compatibility. It delivers a symmetrical full-duplex communication link containing user data, control/programming lines, and status channels.

6.26 LCD interface

The dedicated LCD interface contains logic to interface to a 6800 (Motorola) or a 8080 (Intel) compatible LCD controller which support 4/8/16 bit modes. This module also supports a serial interface mode. The speed of the interface can be adjusted in software to match the speed of the connected LCD display.

This module has the following features:

- 4/8/16 bit parallel interface mode: 6800-series, 8080-series.
- Serial interface mode.
- Supports multiple frequencies for the 6800/8080 bus to support high- and low-speed controllers.
- Supports polling the busy flag from LCD controller to off-load the CPU from polling.
- Contains a 16 byte FIFO for sending control and data information to the LCD controller.
- Supports maskable interrupts.
- Supports DMA transfers.

6.27 I^2C-bus master/slave interface

The LPC3141/3143 contains two I^2C master/slave interfaces.

This module has the following features:

- **I2C0 interface**: The I^2C0-bus interface is a standard I^2C-compliant bus interface with open-drain pins. This interface supports functions described in the I^2C-bus specification for speeds up to 400 kHz. This includes multi-master operation and allows powering off this device in a working system while leaving the I^2C-bus functional.
- **I2C1 interface**: The I^2C1-bus interface uses standard I/O pins and is intended for use with a single-master I^2C-bus and does not support powering off this device. Standard I/Os also do not support multi-master I^2C implementations.
- Supports normal mode (100 kHz SCL).

7. Limiting values

Table 11. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
All digital I/O pins							
V_i	input voltage			–0.5	-	+3.6	V
V_o	output voltage			–0.5	-	+3.6	V
I_o	output current	VDDE_IOC = 3.3 V		-	4	-	mA
Temperature values							
T_j	junction temperature			–40	25	+125	°C
T_{stg}	storage temperature		[2]	–65	-	+150	°C
T_{amb}	ambient temperature			–40	+25	+85	°C
Electrostatic handling							
V_{ESD}	electrostatic discharge voltage	human body model	[3]	–500	-	+500	V
		machine model		–100	-	+100	V
		charged device model		-	500	-	V

[1] The following applies to the limiting values:

a) This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.

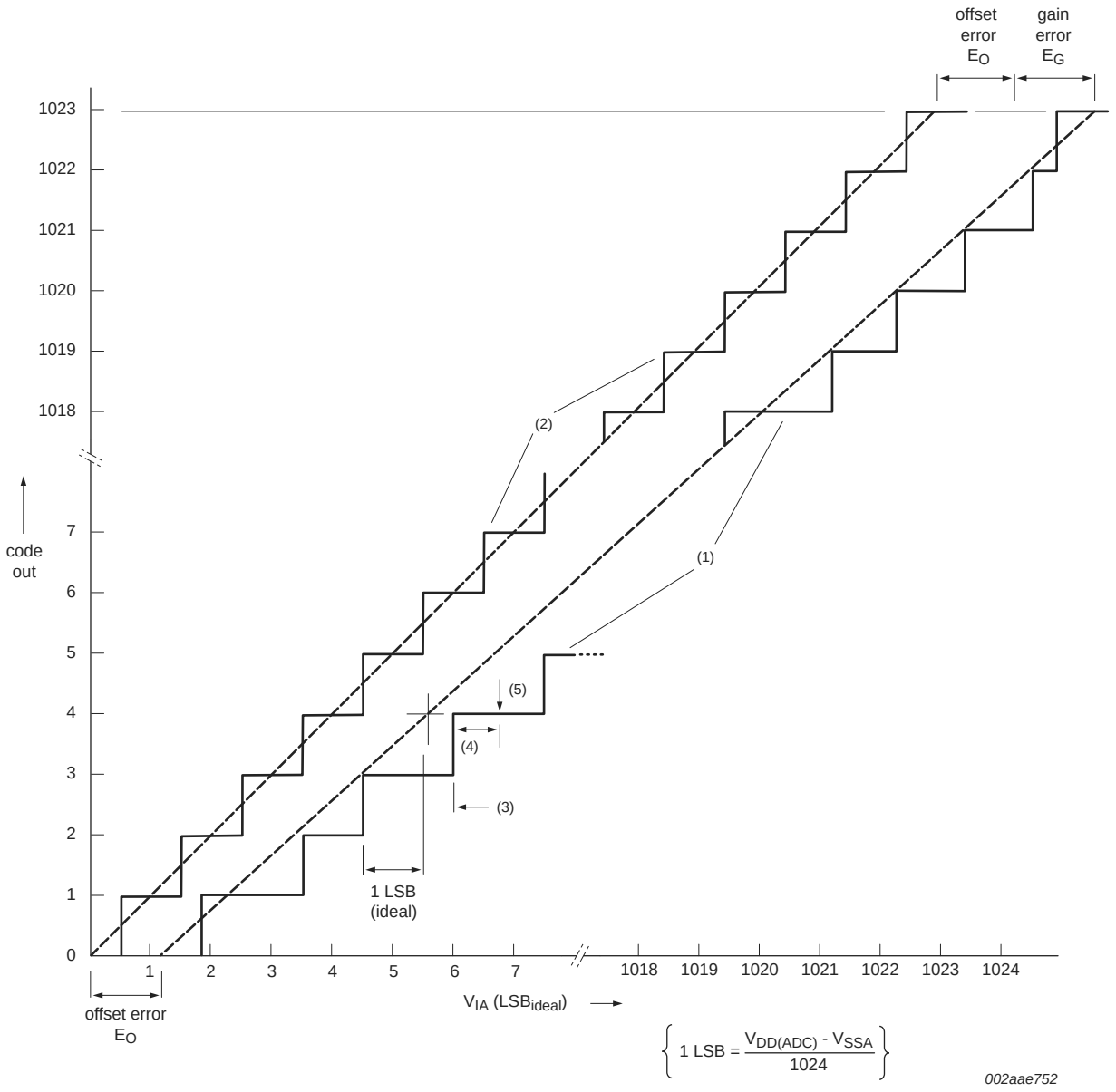
b) Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

[2] Dependent on package type.

[3] Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

Table 12: Static characteristics *…continued*
T_{amb} = −40 °C to +85 °C unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{latch}	I/O latch-up current	$-(1.5V_{DD(IO)}) < V_I < (1.5V_{DD(IO)})$	[1]	-	-	100	mA
I_{pu}	pull-up current	inputs with pull-up; V_I = 0;					
		SUP4; SUP8; 1.8 V mode	[1]	47	65	103	μA
		SUP4; SUP8; 3.3 V mode	[1]	45	50	101	μA
		SUP3		29	50	76	μA
I_{pd}	pull-down current	inputs with pull-down; $V_I = V_{DD(IO)}$;					
		SUP4; SUP8; 1.8 V mode	[1]	49	75	110	μA
		SUP4; SUP8; 3.3 V mode	[1]	56	50	110	μA
		SUP3	[1]	25	50	68	μA
Output pins and I/O pins configured as output							
V_O	output voltage			-	-	$V_{DD(IO)}$	V
V_{OH}	HIGH-level output voltage	SUP4; SUP8; I_{OH} = 6 mA:					
		1.8 V mode		$V_{DD(IO)} - 0.36$	-	-	V
		3.3 V mode		$V_{DD(IO)} - 0.32$	-	-	V
		SUP3; I_{OH} = 6 mA		$V_{DD(IO)} - 0.26$	-	-	V
		SUP3; I_{OH} = 30 mA		$V_{DD(IO)} - 0.38$	-	-	V
V_{OL}	LOW-level output voltage	SUP4; SUP8 outputs; I_{OL} = 4 mA					
		1.8 V mode		-	-	0.2	V
		3.3 V mode	[1]	-	-	0.4	V
		SUP3; I_{OL} = 4 mA		-	-	0.4	V
I_{OH}	HIGH-level output current	$V_{DD(IO)}$ = 1.8 V; $V_{OH} = V_{DD} - 0.4$ V		1	-	-	mA
		$V_{DD(IO)}$ = 3.3 V; $V_{OH} = V_{DD} - 0.4$ V		2.5	-	-	mA
I_{OL}	LOW-level output current	$V_{DD(IO)}$ = 1.8 V; V_{OL} = 0.4 V		4.3	-	-	mA
		$V_{DD(IO)}$ = 3.3 V; V_{OL} = 0.4 V		6.2	-	-	mA
I_{OZ}	OFF-state output current	V_O = 0 V; $V_O = V_{DD}$; no pull-up/down		-	-	0.064	μA
Z_o	output impedance	V_{DD} = VDDE_IOx (x = A, B, C)					
		1.8 V mode	[1]	-	45	-	Ω
		3.3 V mode	[1]	-	35	-	Ω
I^2C0-bus pins							



(1) Example of an actual transfer curve.

(2) The ideal transfer curve.

(3) Differential linearity error (E_D).

(4) Integral non-linearity ($E_{L(adj)}$).

(5) Center of a step of the actual transfer curve.

Fig 10. ADC characteristics

8.1 Power consumption

Table 14. Power consumption

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Standby power mode[1]						
I_{DD}	Supply current	core; VDDI = 1.2 V	-	1.1	-	mA
		all other SUP1 supplies: VDDA12 = 1.2 V; USB_VDDA12_PL = 1.2 V	-	0.175	-	mA
		VDDE_IOA = 1.8 V	-	0.001	-	mA
		VDDE_IOB = 1.8 V	-	0.0008	-	mA
		VDDE_IOC = 3.3 v	-	0.065	-	mA
		ADC10B_VDDA33 = 3.3 V	-	0	-	mA
		USB_VDDA33 = 3.3 V	-	0	-	mA
		USB_VDDA_DRV = 3.3 V	-	0	-	mA
P	Power dissipation	Total for supply domains SUP1, SUP3, SUP4, SUP8	-	1.75	-	mW
External SDRAM based system (operating frequency 270 MHz (core)/ 90 MHz (bus)); heavy SDRAM load power; without dynamic clock scaling[2]						
I_{DD}	Supply current	core; VDDI = 1.2 V	-	86	-	mA
		all other SUP1 supplies: VDDA12 = 1.2 V; USB_VDDA12_PL = 1.2 V	-	1.61	-	mA
		VDDE_IOA = 1.8 V	-	10.5	-	mA
		VDDE_IOB = 1.8 V	-	5.8	-	mA
		VDDE_IOC = 3.3 V	-	0.52	-	mA
		ADC10B_VDDA33 = 3.3 V	-	0.0002	-	mA
		USB_VDDA33 = 3.3 V	-	1.66	-	mA
		USB_VDDA_DRV = 3.3 V	-	0.895	-	mA
P	Power dissipation	Total for supply domains SUP1, SUP3, SUP4, SUP8	-	144.6	-	mW
External SDRAM based system (operating frequency 270 MHz (core)/ 90 MHz (bus)); heavy SDRAM load power; with dynamic clock scaling[2][3]						
I_{DD}	Supply current	core; VDDI = 1.2 V	-	67	-	mA
		all other SUP1 supplies: VDDA12 = 1.2 V; USB_VDDA12_PL = 1.2 V	-	1.61	-	mA
		VDDE_IOA = 1.8 V	-	10.5	-	mA
		VDDE_IOB = 1.8 V	-	5.8	-	mA
		VDDE_IOC = 3.3 V	-	0.52	-	mA
		ADC10B_VDDA33 = 3.3 V	-	0.0002	-	mA
		USB_VDDA33 = 3.3 V	-	1.66	-	mA
		USB_VDDA_DRV = 3.3 V	-	0.895	-	mA
P	Power dissipation	Total for supply domains SUP1, SUP3, SUP4, SUP8	-	121.8	-	mW

Table 14. Power consumption *…continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
External SDRAM based system (operating frequency 270 MHz (core)/ 90 MHz (bus)); normal mode power; without dynamic clock scaling[4]						
I_{DD}	Supply current	core; VDDI = 1.2 V	-	36.1	-	mA
		all other SUP1 supplies: VDDA12 = 1.2 V; USB_VDDA12_PL = 1.2 V	-	1.61	-	mA
		VDDE_IOA = 1.8 V	-	3.79	-	mA
		VDDE_IOB = 1.8 V	-	3.75	-	mA
		VDDE_IOC = 3.3 V	-	0.67	-	mA
		ADC10B_VDDA33 = 3.3 V	-	0.0002	-	mA
		USB_VDDA33 = 3.3 V	-	1.66	-	mA
		USB_VDDA_DRV = 3.3 V	-	0.895	-	mA
P	Power dissipation	Total for supply domains SUP1, SUP3, SUP4, SUP8	-	69.46	-	mW
External SDRAM based system (operating frequency 270 MHz (core)/ 90 MHz (bus)); normal mode power; with dynamic clock scaling[3][4]						
I_{DD}	Supply current	core; VDDI = 1.2 V	-	17.8	-	mA
		all other SUP1 supplies: VDDA12 = 1.2 V; USB_VDDA12_PL = 1.2 V	-	1.61	-	mA
		VDDE_IOA = 1.8 V	-	3.79	-	mA
		VDDE_IOB = 1.8 V	-	3.75	-	mA
		VDDE_IOC = 3.3 V	-	0.67	-	mA
		ADC10B_VDDA33 = 3.3 V	-	0.0002	-	mA
		USB_VDDA33 = 3.3 V	-	1.66	-	mA
		USB_VDDA_DRV = 3.3 V	-	0.895	-	mA
P	Power dissipation	Total for supply domains SUP1, SUP3, SUP4, SUP8	-	47.5	-	mW
Internal SRAM based system (operating frequency 270 MHz (core)/ 90 MHz (bus)); normal mode power; without dynamic clock scaling; MMU on[5]						
I_{DD}	Supply current	core; VDDI = 1.2 V	-	60.8	-	mA
		all other SUP1 supplies: VDDA12 = 1.2 V; USB_VDDA12_PL = 1.2 V	-	2.1	-	mA
		VDDE_IOA = 1.8 V	-	2.25	-	mA
		VDDE_IOB = 1.8 V	-	0	-	mA
		VDDE_IOC = 3.3 V	-	0.79	-	mA
		ADC10B_VDDA33 = 3.3 V	-	0.0002	-	mA
		USB_VDDA33 = 3.3 V	-	0.89	-	mA
		USB_VDDA_DRV = 3.3 V	-	1.75	-	mA
P	Power dissipation	Total for supply domains SUP1, SUP3, SUP4, SUP8	-	90.86	-	mW

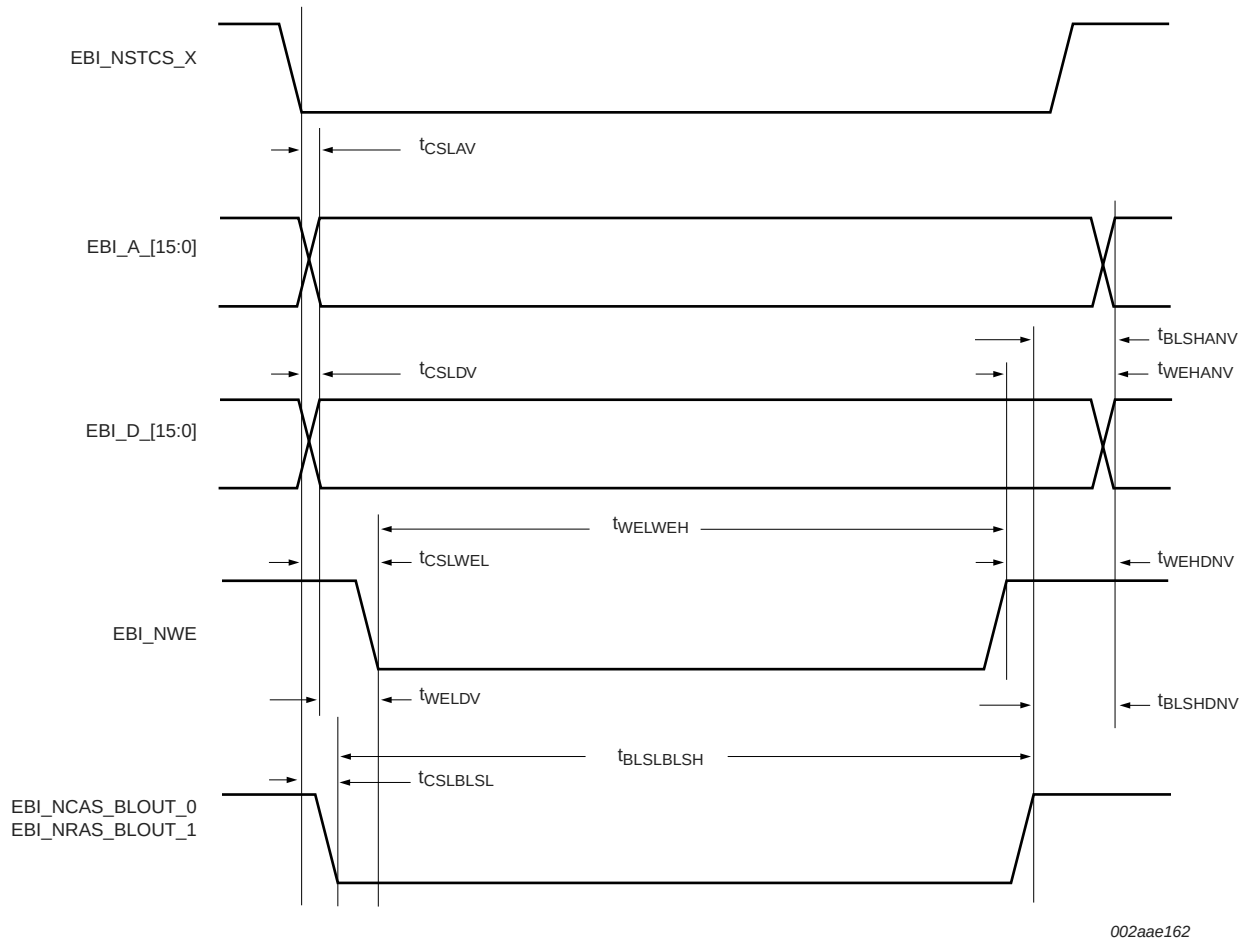
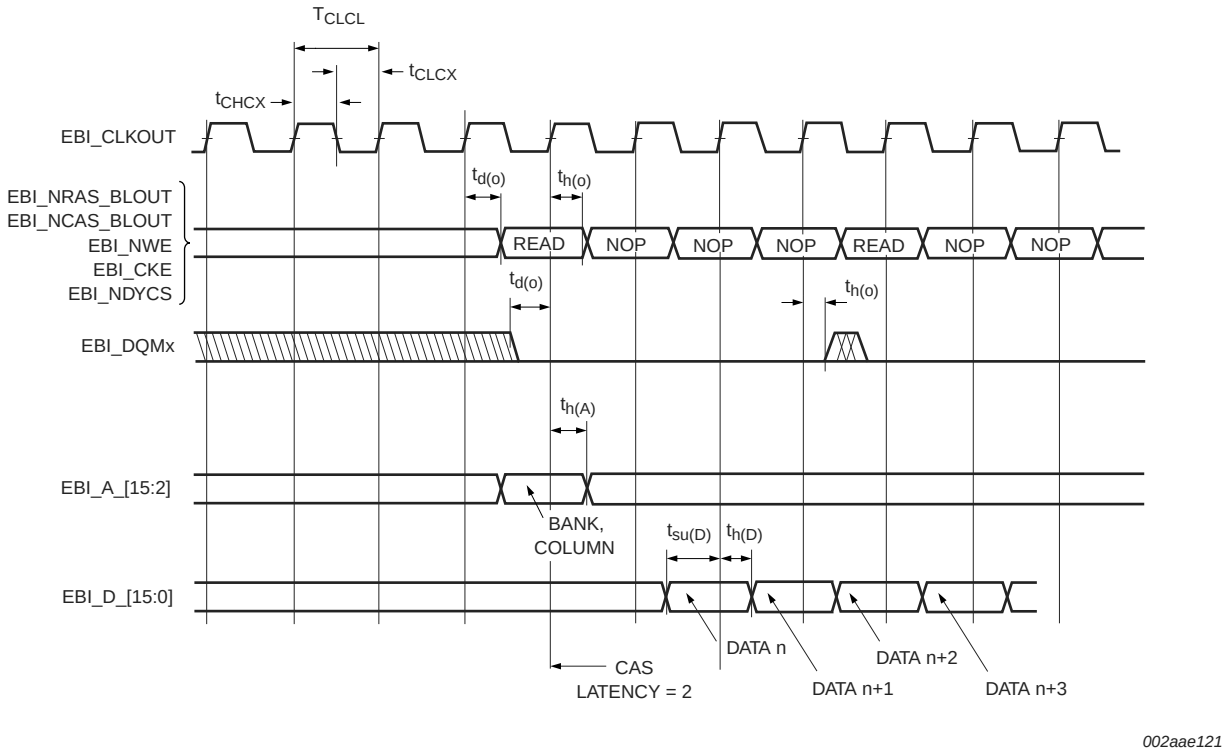


Fig 15. External memory write access to static memory



EBI_CKE is HIGH.

Fig 16. SDRAM burst read timing

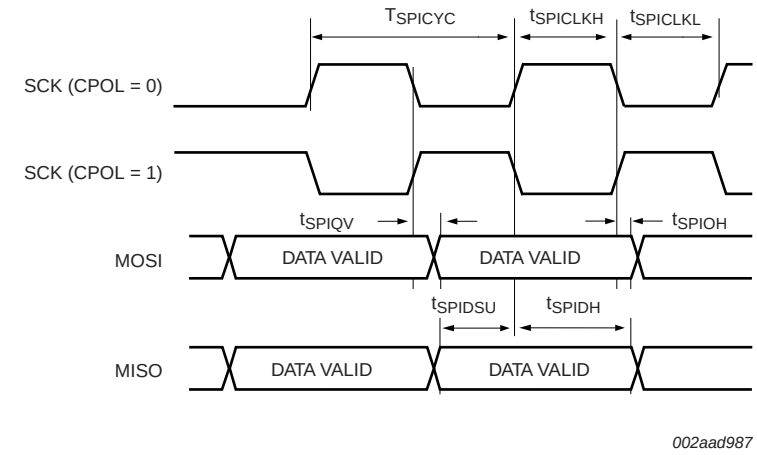


Fig 20. SPI master timing (CPHA = 0)

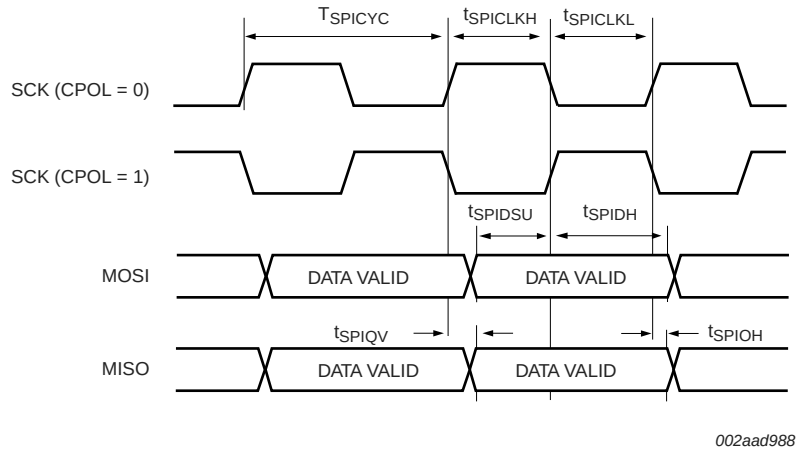


Fig 21. SPI slave timing (CPHA = 1)

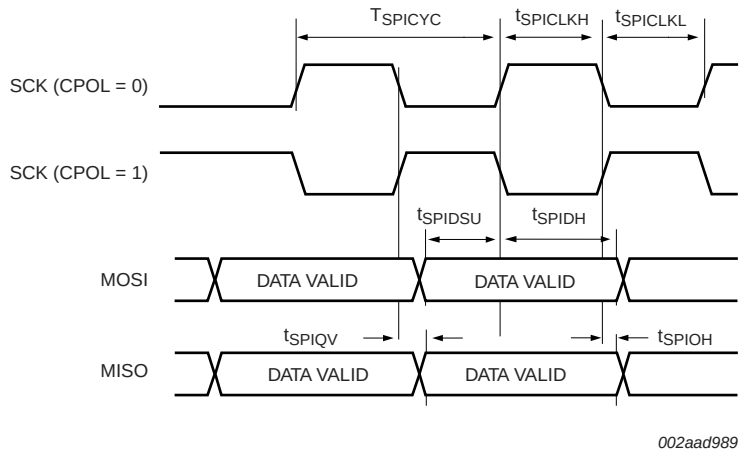


Fig 22. SPI slave timing (CPHA = 0)

9.6.1 Texas Instruments synchronous serial mode (SSI mode)

Table 23. Dynamic characteristic: SPI interface (SSI mode)
T_{amb} = −40 °C to +85 °C; $V_{DD(IO)}$ (SUP3) over specified ranges.[1]

Symbol	Parameter	Conditions	Min	Typ[2]	Max	Unit
$t_{su(SPI\_MISO)}$	SPI_MISO set-up time	T_{amb} = 25 °C; measured in SPI Master mode; see Figure 23	-	11	-	ns

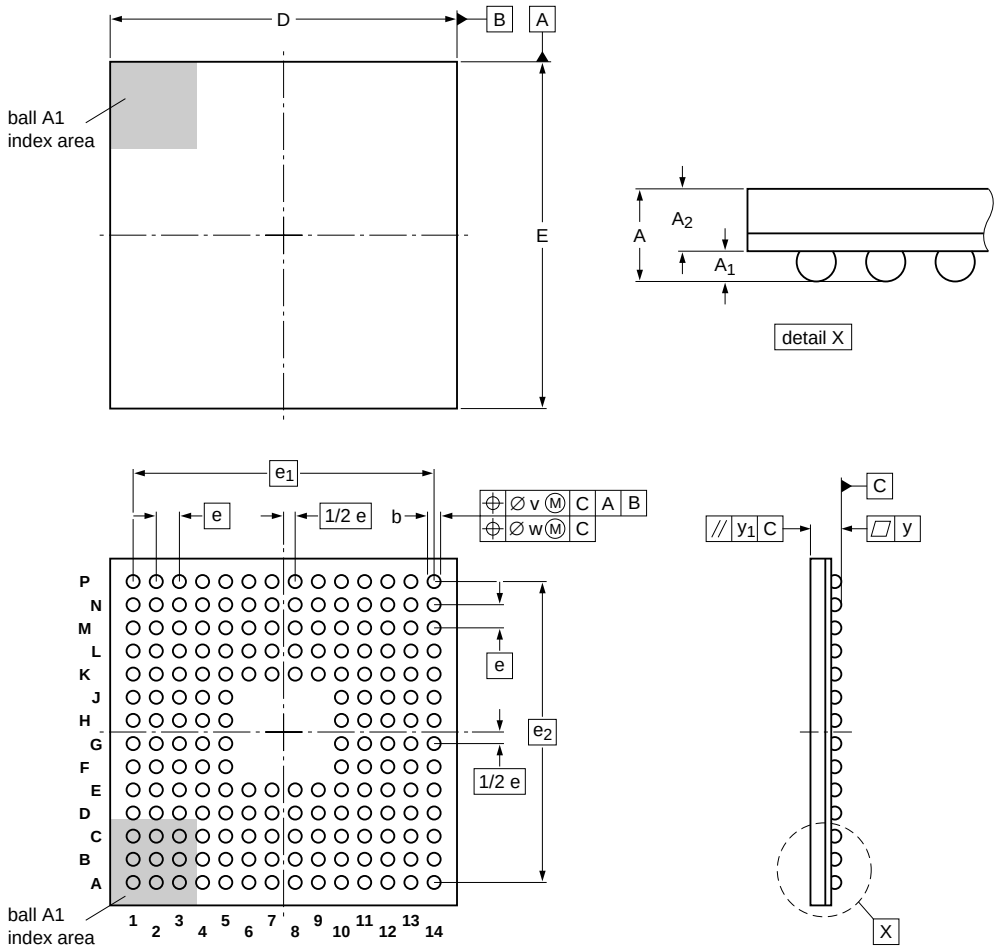
[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

Remark: Note that the signal names SCK, MISO, and MOSI correspond to signals on pins SPI_SCK, SPI_MOSI, and SPI_MISO in the following SPI timing diagram.

12. Package outline

TFBGA180: thin fine-pitch ball grid array package; 180 balls **SOT570-3**



DIMENSIONS (mm are the original dimensions)

UNIT		A	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	y_1
mm	max	1.20	0.40	0.80	0.50	12.1	12.1	0.8	10.4	10.4	0.15	0.05	0.12	0.1
	nom	1.06	0.35	0.71	0.45	12.0	12.0							
	min	0.95	0.30	0.65	0.40	11.9	11.9							

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT570-3						~~08-07-09~~ 10-04-15

Fig 24. LPC3141/3143 TFBGA180 package outline

Table 27. Abbreviations *…continued*

Acronym	Description
RNG	Random Number Generator
ROM	Read-Only Memory
SD	Secure Digital
SDHC	Secure Digital High Capacity
SDIO	Secure Digital Input Output
SDR SDRAM	Single Data Rate Synchronous Dynamic Random Access Memory
SE0	Single Ended 0
SIR	Serial IrDA
SPI	Serial Peripheral Interface
SSI	Serial Synchronous Interface
SysCReg	System Control Registers
TAP	Test Access Port
TDO	Test Data Out
UART	Universal Asynchronous Receiver Transmitter
USB	Universal Serial Bus
UTMI	USB 2.0 Transceiver Macrocell Interface
WDT	WatchDog Timer

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