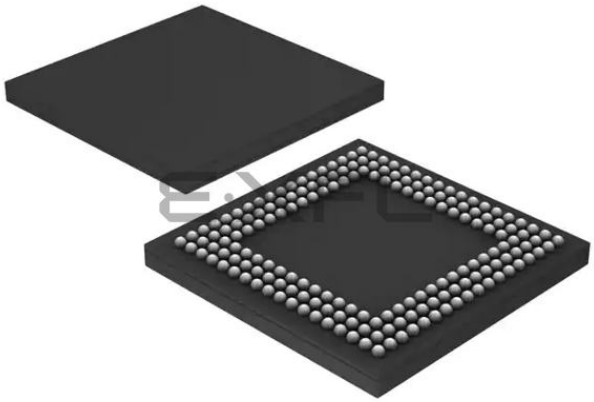


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	ARM926EJ-S
Core Size	16/32-Bit
Speed	270MHz
Connectivity	EBI/EMI, I²C, IrDA, Memory Card, PCM, SPI, UART/USART, USB OTG
Peripherals	DMA, I²S, LCD, PWM, WDT
Number of I/O	20
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	192K x 8
Voltage - Supply (Vcc/Vdd)	1.1V ~ 3.6V
Data Converters	A/D 4x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	180-TFBGA
Supplier Device Package	180-TFBGA (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc3143fet180-551

4. Block diagram

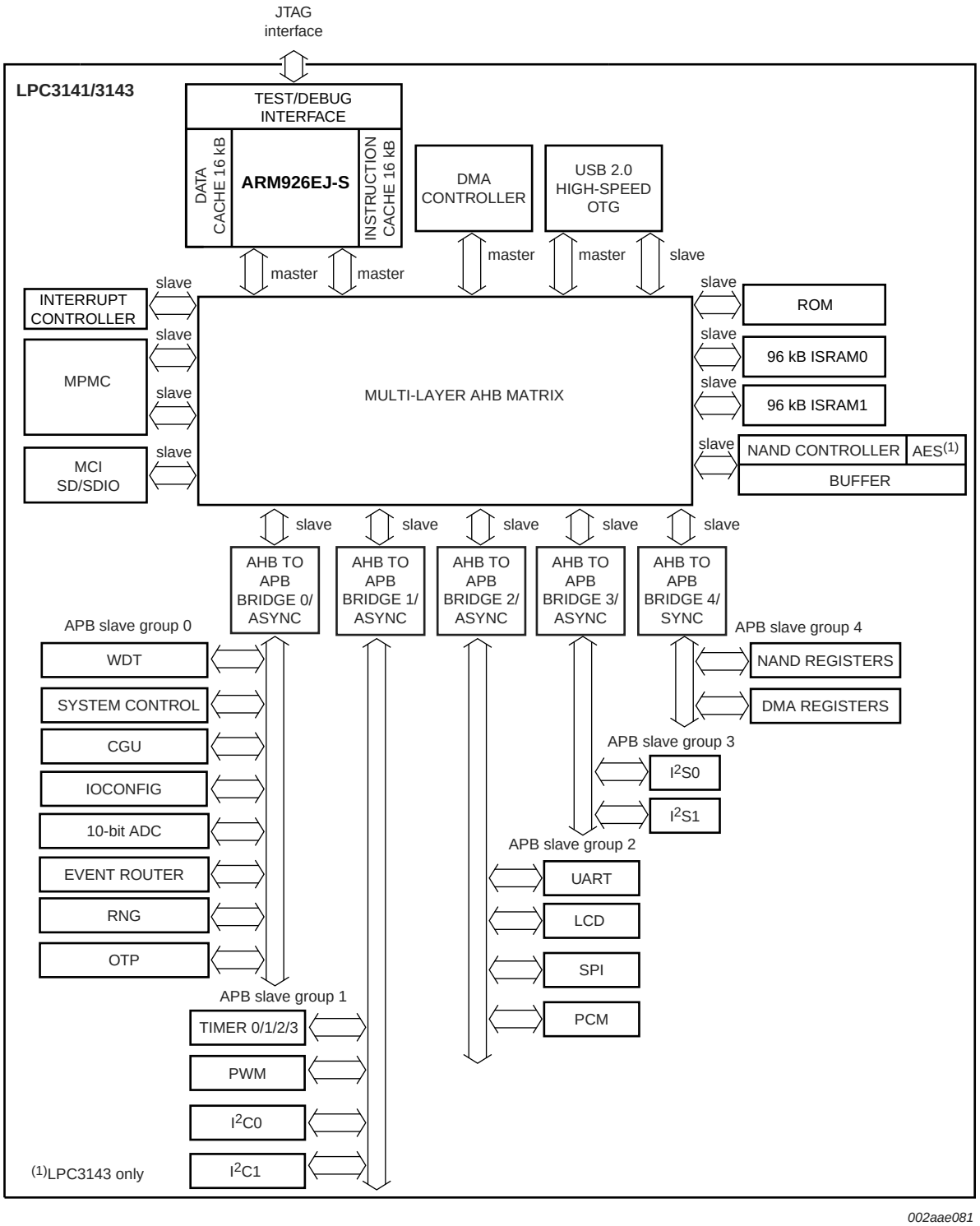


Fig 1. LPC3141/3143 block diagram

Table 3. Pin allocation table *…continued*

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
Row E							
1	EBI_D_3	2	EBI_D_4	3	EBI_D_14	4	VSSE_IOA
5	VDDE_IOA	6	mNAND_RYBN0	7	mNAND_RYBN1	8	VDDE_IOC
9	VSSA12	10	VDDA12	11	ARM_TDO	12	I2C_SDA1
13	I2C_SCL1	14	I2STX_BCK1	-	-	-	-
Row F							
1	EBI_D_2	2	EBI_D_1	3	EBI_D_15	4	VSSE_IOA
5	VDDE_IOA	10	SCAN_TDO	11	BUF_TRST_N	12	I2STX_DATA1
13	I2SRX_WS1	14	I2SRX_BCK1	-	-	-	-
Row G							
1	EBI_NCAS_BLOUT_0	2	EBI_D_0	3	EBI_D_12	4	VSSI
5	VDDE_IOA	10	I2STX_WS1	11	VSSE_IOC	12	VDDE_IOC
13	SYSCLK_O	14	I2SRX_DATA1	-	-	-	-
Row H							
1	EBI_DQM_0_NOE	2	EBI_NRAS_BLOUT_1	3	VDDI	4	VSSE_IOA
5	VDDE_IOA	10	GPIO12	11	GPIO19	12	CLK_256FS_O
13	GPIO11	14	RSTIN_N	-	-	-	-
Row J							
1	NAND_NCS_0	2	EBI_NWE	3	NAND_NCS_1	4	CLOCK_OUT
5	USB_RREF	10	GPIO1	11	GPIO16	12	GPIO13
13	GPIO15	14	GPIO14	-	-	-	-
Row K							
1	NAND_NCS_2	2	NAND_NCS_3	3	VSSE_IOA	4	USB_VSSA_REF
5	mLCD_DB_12	6	mLCD_DB_6	7	mLCD_DB_10	8	mLCD_CSB
9	TDI	10	GPIO0	11	VDDE_IOC	12	GPIO17
13	GPIO20	14	GPIO18	-	-	-	-
Row L							
1	USB_VDDA12_PLL	2	USB_VBUS	3	USB_VSSA_TERM	4	VDDE_IOB
5	mLCD_DB_9	6	VSSI	7	VDDI	8	mLCD_E_RD
9	VSSE_IOC	10	VDDE_IOC	11	VSSI	12	VDDI
13	VSSE_IOC	14	GPIO2	-	-	-	-
Row M							
1	USB_ID	2	USB_VDDA33_DRV	3	VSSE_IOB	4	VSSE_IOB
5	VDDE_IOB	6	VSSE_IOB	7	VDDE_IOB	8	VSSE_IOB
9	VDDE_IOB	10	I2SRX_DATA0	11	mI2STX_WS0	12	mI2STX_BCK0
13	mI2STX_DATA0	14	TCK	-	-	-	-
Row N							
1	USB_GNDA	2	USB_DM	3	mLCD_DB_15	4	mLCD_DB_11
5	mLCD_DB_8	6	mLCD_DB_2	7	mLCD_DB_4	8	mLCD_DB_0
9	mLCD_RW_WR	10	I2SRX_BCK0	11	JTAGSEL	12	UART_TXD
13	mUART_CTS_N	14	mI2STX_CLK0	-	-	-	-

Table 4. Pin description *…continued*

Pin names with prefix m are multiplexed pins. See Table 10 for pin function selection of multiplexed pins.

Pin name	BGA Ball	Digital I/O level [1]	Application function	Pin state after reset [2]	Cell type [3]	Description
Serial Peripheral Interface (SPI)						
SPI_CS_OUT0 [4]	A7	SUP3	DO	O	DIO4	SPI chip select output (master).
SPI_SCK [4]	A8	SUP3	DIO	I	DIO4	SPI clock input (slave)/clock output (master).
SPI_MISO [4]	C8	SUP3	DIO	I	DIO4	SPI data input (master)/data output (slave).
SPI_MOSI [4]	B7	SUP3	DIO	I	DIO4	SPI data output (master)/data input (slave).
SPI_CS_IN [4]	B8	SUP3	DI	I	DIO4	SPI chip select input (slave).
Digital power supply						
VDDI	H3; L7; L12; C12; C6	SUP1	Supply	-	CS2	Digital core supply.
VSSI	A11; C7; D12; G4; L6; L11		Ground	-	CG2	Digital core ground.
Peripheral power supply						
VDDE_IOA	B2; E5; F5; G5; H5	SUP4	Supply	-	PS1	Peripheral supply for NAND flash interface.
VDDE_IOB	L4; M5; M7; M9	SUP8	Supply	-	PS1	Peripheral supply for SDRAM/LCD.
VDDE_IOC	C13; D5; D7; E8; G12; L10; K11	SUP3	Supply	-	PS1	Peripheral supply.
VSSE_IOA	C3; C4; E4; F4; H4; K3	-	Ground	-	PG1	-
VSSE_IOB	M3; M4; M6; M8	-	Ground	-	PG1	-

- Support for 8-bit and 16-bit flash devices.
- Support for any page size from 0.5 kB upwards.
- Programmable NAND flash timing parameters.
- Support for up to 4 NAND devices.
- Hardware AES decryption (LPC3143 only).
- Error Correction Module (ECC) for MLC NAND flash support:
  - Reed-Solomon error correction encoding and decoding.
  - Uses Reed-Solomon code words with 9-bit symbols over GF(2^9), a total codeword length of 469 symbols, including 10 parity symbols, giving a minimum Hamming distance of 11.
  - Up to 8 symbol errors can be corrected per codeword.
  - Error correction can be turned on and off to match the demands of the application.
  - Parity generator for error correction encoding.
  - Wear leveling information can be integrated into protected data.
  - Interrupts generated after completion of error correction task with three interrupt registers.
  - Error correction statistics distributed to ARM using interrupt scheme.
  - Interface is compatible with the ARM External Bus Interface (EBI).

6.5 Multi-Port Memory Controller (MPMC)

The multi-port memory controller supports the interface to different memory types, for example:

- SDRAM
- Low-power SDRAM
- Static memory interface

This module has the following features:

- Dynamic memory interface support including SDRAM, JEDEC low-power SDRAM.
- Address line supporting up to 128 MB (two 64Mx8 devices connected to a single chip select) of dynamic memory.
- The MPMC has two AHB interfaces:
  a. an interface for accessing external memory.
  b. a separate control interface to program the MPMC. This enables the MPMC registers to be situated in memory with other system peripheral registers.
- Low transaction latency.
- Read and write buffers to reduce latency and to improve performance, particularly for un-cached processors.
- Static memory features include:
  - asynchronous page mode read
  - programmable wait states
  - bus turnaround delay

The LPC3141 ROM memory has the following features:

- Supports booting from SPI flash, NAND flash, SD/SDHC/MMC cards, UART, and USB (DFU class) interfaces.
- Supports option to perform CRC32 checking on the boot image.
- Contains pre-defined MMU table (16 kB) for simple systems.
- Supports booting from managed NAND devices such as movi-NAND, iNAND, eMMC-NAND and eSD-NAND using SD/MMC boot mode.

The boot ROM determines the boot mode based on reset state of GPIO0, GPIO1, and GPIO2 pins. To ensure that GPIO0, GPIO1 and GPIO2 pins come up as inputs, pins TRST_N and JTAGSEL must be LOW during power-on reset (see *UM10362 JTAG chapter* for details). Table 8 shows the various boot modes supported on the LPC3141/3143:

Table 8. LPC3141/3143 boot modes

Boot mode	GPIO0	GPIO1	GPIO2	Description
NAND	0	0	0	Boots from NAND flash. If proper image is not found, boot ROM will switch to DFU boot mode.
SPI	0	0	1	Boot from SPI NOR flash connected to SPI_CS_OUT0. If proper image is not found, boot ROM will switch to DFU boot mode.
DFU	0	1	0	Device boots via USB using DFU class specification.
SD/MMC	0	1	1	Boot ROM searches all the partitions on the SD/MMC/SDHC/MMC+/eMMC/eSD card for boot image. If partition table is missing, it will start searching from sector 0. A valid image is said to be found if a valid image header is found, followed by a valid image. If a proper image is not found, boot ROM will switch to DFU boot mode.
Reserved 0	1	0	0	Reserved for testing.
NOR flash	1	0	1	Boot from parallel NOR flash connected to EBI_NSTCS_1.[1]
UART	1	1	0	Boot ROM tries to download boot image from UART ((115200 - 8 - n -1) assuming 12 MHz FFAST clock).
Test	1	1	1	Boot ROM is testing ISRAM using memory pattern test. Switches to UART boot mode on receiving three ASCI dots ("...") on UART.

[1] For security reasons this mode is disabled when JTAG security feature is used.

6.8 Internal RAM memory

The ISRAM (Internal Static RAM Memory) controller module is used as controller between the AHB bus and the internal RAM memory. The internal RAM memory can be used as working memory for the ARM processor and as temporary storage to execute the code that is loaded by boot ROM from external devices such as SPI flash, NAND flash, and SD/MMC cards.

This module has the following features:

- Capacity of 192 kB

- Implemented as two independent 96 kB memory banks

6.9 Memory Card Interface (MCI)

The MCI controller interface can be used to access memory cards according to the Secure Digital (SD) and Multi-Media Card (MMC) standards. The host controller can be used to interface to small form factor expansion cards compliant to the SDIO card standard as well. Finally, the MCI supports CE-ATA 1.1 compliant hard disk drives.

This module has the following features:

- One 8-bit wide interface.
- Supports high-speed SD, versions 1.01, 1.10 and 2.0.
- Supports SDIO version 1.10.
- Supports MMCplus, MMCmobile and MMCmicro cards based on MMC 4.1.
- Supports SDHC memory cards.
- CRC generation and checking.
- Supports 1/4-bit SD cards.
- Card detection and write protection.
- FIFO buffers of 16 byte deep.
- Host pull-up control.
- SDIO suspend and resume.
- 1 to 65 535 byte blocks.
- Suspend and resume operations.
- SDIO read-wait.
- Individual clock and power ON/OFF features to each card.
- Maximum clock speed of 52 MHz (MMC 4.1).
- Supports CE-ATA 1.1.
- Supports 1-bit, 4-bit, and 8-bit MMC cards and CE-ATA devices.

6.10 High-speed Universal Serial Bus 2.0 On-The-Go (OTG)

The USB OTG module allows the LPC3141/3143 to connect directly to a USB host such as a PC (in device mode) or to a USB device in host mode. In addition, the LPC3141/3143 has a special, built-in mode in which it enumerates as a Device Firmware Upgrade (DFU) class, and which allows for a (factory) download of the device firmware through USB.

This module has the following features:

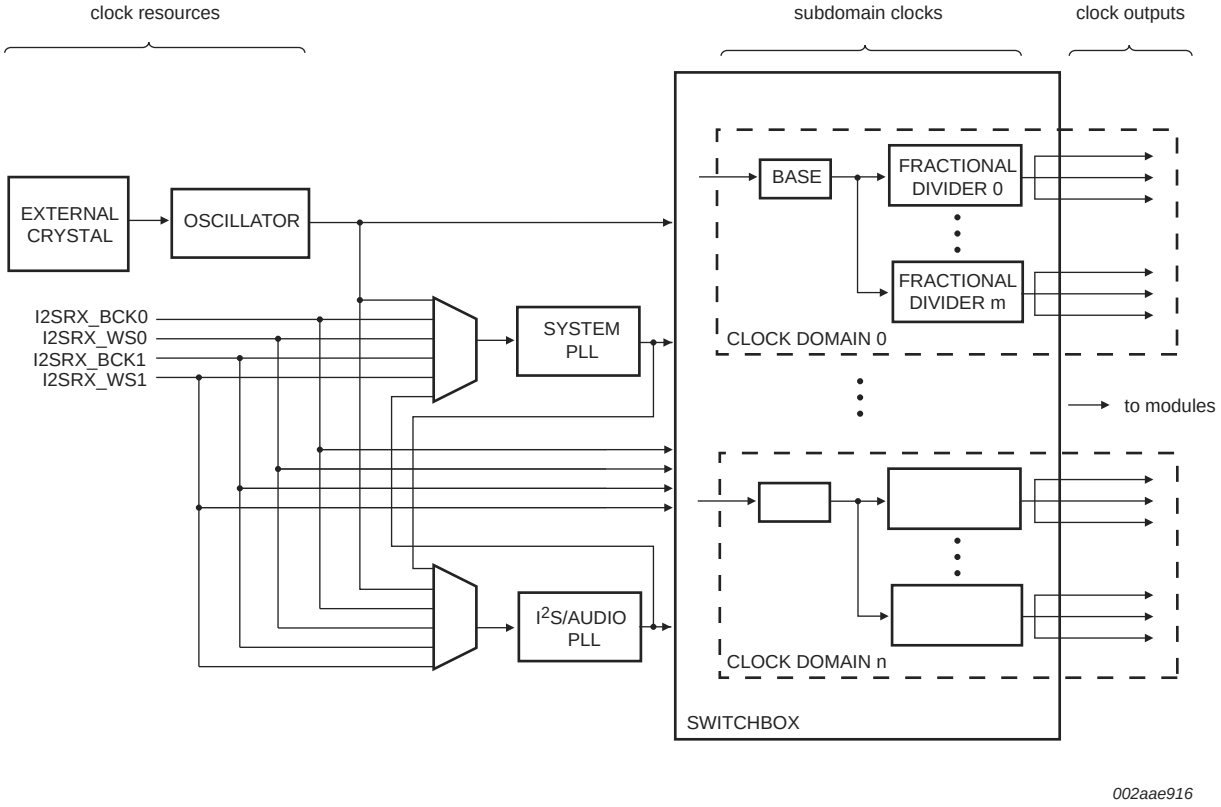
- Complies with *Universal Serial Bus specification 2.0*.
- Complies with *USB On-The-Go supplement*.
- Complies with *Enhanced Host Controller Interface Specification*.
- Supports auto USB 2.0 mode discovery.
- Supports all high-speed USB-compliant peripherals.
- Supports all full-speed USB-compliant peripherals.

Multiple masters can have access to different slaves at the same time.

Figure 5 gives an overview of the multi-layer AHB configuration in the LPC3141/3143. AHB masters and slaves are numbered according to their AHB port number.

- Each base clock can be programmed to have any one of the clock sources as an input clock.
- Fractional dividers can be used to divide a base clock by a fractional number to a lower clock frequency.
- Fractional dividers support clock stretching to obtain a (near) 50% duty cycle output clock.

- Register interface to reset all modules under software control.
- Based on the input of the Watchdog timer (see also Section 6.16), the CGU can generate a system-wide reset in the case of a system stall.



The LPC3141/3143 has 11 clock domains (n = 11). The number of fractional dividers m depends on the clock domain.

Fig 6. CGU block diagram

6.16 Watchdog Timer (WDT)

The watchdog timer can be used to generate a system reset if there is a CPU/software crash. In addition the watchdog timer can be used as an ordinary timer. Figure 7 shows how the watchdog timer module is connected in the system.

This module has the following features:

- In the event of a software or hardware failure, generates a chip-wide reset request when its programmed time-out period has expired (output m1).
- Watchdog counter can be reset by a periodical software trigger.

The SPI/SSI-bus is a 5-wire interface, and it is suitable for low, medium, and high data rate transfers.

This module has the following features:

- Supports Motorola SPI frame format with a word size of 8/16 bits.
- Texas Instruments SSI (Synchronous Serial Interface) frame format with a word size of 4 bit to 16 bit.
- Receive FIFO and transmit FIFO of 64 half-words each.
- Serial clock rate master mode maximum 45 MHz.
- Serial clock rate slave mode maximum 25 MHz.
- Support for single data access DMA.
- Full-duplex operation.
- Supports up to three slaves.
- Supports maskable interrupts.
- Supports DMA transfers.

6.24 Universal Asynchronous Receiver Transmitter (UART)

The UART module supports the industry standard serial interface.

This module has the following features:

- Programmable baud rate with a maximum of 1049 kBd.
- Programmable data length (5 bit to 8 bit).
- Implements only asynchronous UART.
- Transmit break character length indication.
- Programmable 1 to 2 stops bits in transmission.
- Odd/Even/Force parity check/generation.
- Frame error, overrun error and break detection.
- Automatic hardware flow control.
- Independent control of transmit, receive, line status, data set interrupts, and FIFOs.
- SIR-IrDA encoder/decoder (from 2400 to 115 kBd).
- Supports maskable interrupts.
- Supports DMA transfers.

6.25 Pulse Code Modulation (PCM) interface

The PCM interface supports the PCM and IOM interfaces.

This module has the following features:

- Four-wire serial interface.
- Can function in both Master and Slave modes.
- Supports:
  - PCM: Pulse code modulation. Single clocking physical format.

2. Dedicated LCD interface only: This is the LCD mode. The NAND flash supply voltage (SUP4) can be different from the LCD supply voltage (SUP8).

6.29 Timer module

The LPC3141/3143 contains four fully independent timer modules, which can be used to generate interrupts after a pre-set time interval has elapsed.

This module has the following features:

- Each timer is a 32 bit wide down-counter with selectable pre-scale. The pre-scaler allows using either the module clock directly or the clock divided by 16 or 256.
- Two modes of operation:
  - Free-running timer: The timer generates an interrupt when the counter reaches zero. The timer wraps around to 0xFFFF FFFF and continues counting down.
  - Periodic timer: The timer generates an interrupt when the counter reaches zero. It reloads the value from a load register and continues counting down from that value. An interrupt will be generated every time the counter reaches zero. This effectively gives a repeated interrupt at a regular interval.
- At any time the current timer value can be read.
- At any time the value in the load register may be re-written, causing the timer to restart.

6.30 Pulse Width Modulation (PWM) module

This PWM can be used to generate a pulse width modulated or a pulse density modulated signal. With an external low pass filter, the module can be used to generate a low frequent analog signal. A typical use of the output of the module is to control the backlight of an LCD display.

This module has the following features:

- Supports Pulse Width Modulation (PWM) with software controlled duty cycle.
- Supports Pulse Density Modulation (PDM) with software controlled pulse density.

6.31 System control registers

The System Control Registers (SysCReg) module provides a register interface for some of the high-level settings in the system such as multiplexers and mode settings. This is an auxiliary module included in this overview for the sake of completeness.

6.32 I^2S

The I^2S receive/I^2S transmit modules have the following features:

- Audio interface compatible with the I^2S standard.
- I^2S receive block supports master mode and slave mode.
- I^2S transmit block supports master mode.
- Supports LSB justified words of 16, 18, 20 and 24 bit.
- Supports a configurable number of bit clock periods per word select period (up to 128 bit clock periods).

Table 12: Static characteristics *…continued*
T_{amb} = −40 °C to +85 °C unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{OZ}	OFF-state output current	V_O = 0 V; V_O = V_{DD}; no pull-up/down		-	-	7.25	μA
V_{IH}	HIGH-level input voltage		[1]	0.7VDDE_IOC	-	-	V
V_{IL}	LOW-level input voltage		[1]	-	-	0.3VDDE_IOC	V
V_{hys}	hysteresis voltage			0.1VDDE_IOC	-	-	V
V_{OL}	LOW-level output voltage	I_{OLS} = 3 mA		-	-	0.298	V
I_{LI}	input leakage current	VDDE voltage domain; T_{amb} = 25 °C	[1]	-	1.7	-	μA
		VDD voltage domain; T_{amb} = 25 °C	[1]	-	0.01	-	μA
USB							
V_{IC}	common-mode input voltage	high-speed mode		−50	200	500	mV
		full-speed/low-speed mode		800	-	2500	mV
		chirp mode		−50	-	600	mV
$V_{i(dif)}$	differential input voltage			100	400	1100	mV

[1] The parameter values specified are simulated values.

Table 14. Power consumption *…continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Internal SRAM based system (operating frequency 270 MHz (core)/ 90 MHz (bus)); normal mode power; without dynamic clock scaling; MMU off[6]						
I_{DD}	Supply current	core; VDDI = 1.2 V	-	37.95	-	mA
		all other SUP1 supplies: VDDA12 = 1.2 V; USB_VDDA12_PL = 1.2 V	-	2.1	-	mA
		VDDE_IOA = 1.8 V	-	2.25	-	mA
		VDDE_IOB = 1.8 V	-	0	-	mA
		VDDE_IOC = 3.3 V	-	0.79	-	mA
		ADC10B_VDDA33 = 3.3 V	-	0.0002	-	mA
		USB_VDDA33 = 3.3 V	-	0.89	-	mA
		USB_VDDA_DRV = 3.3 V	-	1.75	-	mA
P	Power dissipation	Total for supply domains SUP1, SUP3, SUP4, SUP8	-	63.44	-	mW
Internal SRAM based system (operating frequency 270 MHz (core)/ 90 MHz (bus)); normal mode power; with dynamic clock scaling; MMU off[3][6]						
I_{DD}	Supply current	core; VDDI = 1.2 V	-	17.8	-	mA
		all other SUP1 supplies: VDDA12 = 1.2 V; USB_VDDA12_PL = 1.2 V	-	2.1	-	mA
		VDDE_IOA = 1.8 V	-	2.25	-	mA
		VDDE_IOB = 1.8 V	-	0	-	mA
		VDDE_IOC = 3.3 V	-	0.79	-	mA
		ADC10B_VDDA33 = 3.3 V	-	0.0002	-	mA
		USB_VDDA33 = 3.3 V	-	0.89	-	mA
		USB_VDDA_DRV = 3.3 V	-	1.75	-	mA
P	Power dissipation	Total for supply domains SUP1, SUP3, SUP4, SUP8	-	39.26	-	mW

[1] 12 Mhz oscillator running; PLLs off; SYS_BASE and AHB_APB0_BASE Base domain clocks are enabled, driven by 12 Mhz oscillator; all peripherals off; SUP4 buffers set to input w/PD; SUP8 and SUP3 buffers set to input w/repeater. Shutting off the 12 Mhz osc will reduce power to 1.4 mW (requires a RSTIN_N to run again).

[2] Running Linux with 100% load; all peripherals on; instruction and data caches on; MMU on.

[3] Dynamic clock scaling active; hardware will automatically switch the SYSBASE clocks to a slow clock (180 / 64 = 2.81 MHz) during times of bus inactivity. ARM926 and NAND flash clocks are not scaled for this test.

[4] Running Linux idle at prompt; all peripherals on; instruction and data caches on; MMU on.

[5] Running Dhrystone test (600 k/sec); UART and timers enabled; instruction and data caches on; MMU on.

[6] Running Dhrystone test (121.83 k/sec); UART and timers enabled; instruction and data caches off; MMU off.

9.3 SDRAM controller

Table 19. Dynamic characteristics of SDR SDRAM memory interface

T_{amb} = −40 °C to +85 °C, unless otherwise specified; $V_{DD(IO)}$ = 1.8 V and 3.3 V (SUP8).[1][2][3]

Symbol	Parameter	Conditions		Min	Typical	Max	Unit
f_{oper}	operating frequency		[4]	-	80	90	MHz
t_{CLCX}	clock LOW time			-	5.55	-	ns
t_{CHCX}	clock HIGH time			-	5.55	-	ns
$t_{d(o)}$	output delay time	on pin EBI_CKE	[5]	-	-	3.6	ns
		on pins EBI_NRAS_BLOUT, EBI_NCAS_BLOUT, EBI_NWE, EBI_NDYCS		-	-	3.6	ns
		on pins EBI_DQM_1, EBI_DQM_0_NOE		-	-	5	ns
$t_{h(o)}$	output hold time	on pin EBI_CKE	[5]	0.13	-	3.6	ns
		on pins EBI_NRAS_BLOUT, EBI_NCAS_BLOUT, EBI_NWE, EBI_NDYCS		−0.1	-	3.6	ns
		on pins EBI_DQM_1, EBI_DQM_0_NOE		1.7	-	5	ns
$t_{d(AV)}$	address valid delay time		[5]	-	-	5	ns
$t_{h(A)}$	address hold time		[5]	−0.1	-	5	ns
$t_{d(QV)}$	data output valid delay time		[5]	-	-	9	ns
$t_{h(Q)}$	data output hold time		[5]	4	-	10	ns
t_{QZ}	data output high-impedance time			-	-	$<T_{CLCL}$	ns

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] All values valid for pads set to high slew rate. VDDE_IOA = VDDE_IOB = 1.8 ± 0.15 V. VDDI = 1.2 ± 0.1 V.

[3] Refer to the LPC3141/3143 user manual for the programming of MPMCDynamicReadConfig and SYSCREG_MPMP_DELAYMODES registers

[4] $f_{oper} = 1 / T_{CLCL}$

[5] $t_{d(o)}$, $t_{h(o)}$, $t_{d(AV)}$, $t_{h(A)}$, $t_{d(QV)}$, $t_{h(Q)}$ times are dependent on MPMCDynamicReadConfig register value and SYSCREG_MPMP_DELAYMODES register bits 11:6

[6] $t_{su(D)}$, $t_{h(D)}$ times are dependent on SYSCREG_MPMP_DELAYMODES register bits 5:0

9.4 NAND flash memory controller

Table 20. Dynamic characteristics of the NAND Flash memory controller
T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter		Typical	Unit
t_{REH}	$\overline{RE}$ HIGH hold time	[1][2][3]	T_{HCLK} × (TREH)	ns
t_{RP}	$\overline{RE}$ pulse width	[1][2][3]	T_{HCLK} × (TRP)	ns
t_{WH}	$\overline{WE}$ HIGH hold time	[1][2][3]	T_{HCLK} × (TWH)	ns
t_{WP}	$\overline{WE}$ pulse width	[1][2][3]	T_{HCLK} × (TWP)	ns
t_{CLS}	CLE set-up time	[1][2][3]	T_{HCLK} × (TCLS)	ns
t_{CLH}	CLE hold time	[1][2][3]	T_{HCLK} × (TCLH)	ns
t_{ALS}	ALE set-up time	[1][2][3]	T_{HCLK} × (TALS)	ns
t_{ALH}	ALE hold time	[1][2][3]	T_{HCLK} × (TALH)	ns
t_{CS}	$\overline{CE}$ set-up time	[1][2][3]	T_{HCLK} × (TCS)	ns
t_{CH}	$\overline{CE}$ hold time	[1][2][3]	T_{HCLK} × (TCH)	ns

[1] T_{HCLK} = 1 / NANDFLASH_NAND_CLK, see *LPC314x user manual*.

[2] See registers NandTiming1 and NandTiming2 in the *LPC314x user manual*.

[3] Each timing parameter can be set from 7 nand_clk clock cycles to 1 nand_clk clock cycle. (A programmed zero value is treated as a one).

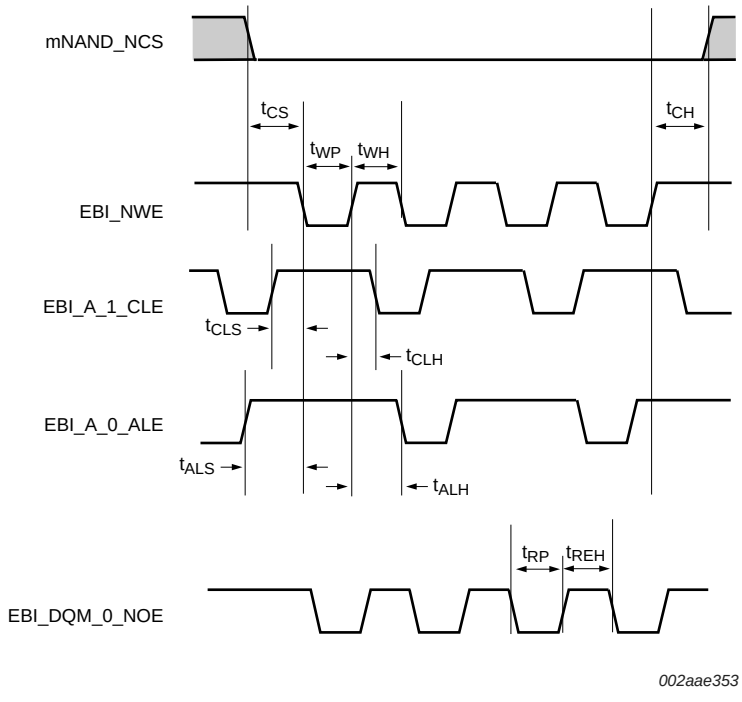


Fig 18. NAND flash controller write and read timing

9.5 Crystal oscillator

Table 21: Dynamic characteristics: crystal oscillator

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{osc}	oscillator frequency		10	12	25	MHz
δ_{clk}	clock duty cycle		45	50	55	%
C_{xtal}	crystal capacitance	input; on pin FFAST_IN	-	-	2	pF
		output; on pin FFAST_OUT	-	-	0.74	pF
$t_{startup}$	start-up time		-	500	-	µs
P_{drive}	drive power		100	-	500	µW

9.6 SPI

Table 22. Dynamic characteristics of SPI pins
T_{amb} = −40 °C to +85 °C for industrial applications

Symbol	Parameter	Min	Typ	Max	Unit
SPI master					
T_{SPICYC}	SPI cycle time	22.2	-	-	ns
$t_{SPICLKH}$	SPICLK HIGH time	11.09	-	11.14	ns
$t_{SPICLKL}$	SPICLK LOW time	11.09	-	11.14	ns
t_{SPIQV}	SPI data output valid time	-	-	14	ns
t_{SPIOH}	SPI output data hold time	9.9	-	-	ns
SPI slave					
t_{SPIOH}	SPI output data hold time	9.9	-	-	ns

Remark: Note that the signal names SCK, MISO, and MOSI correspond to signals on pins SPI_SCK, SPI_MOSI, and SPI_MISO in the following SPI timing diagrams.

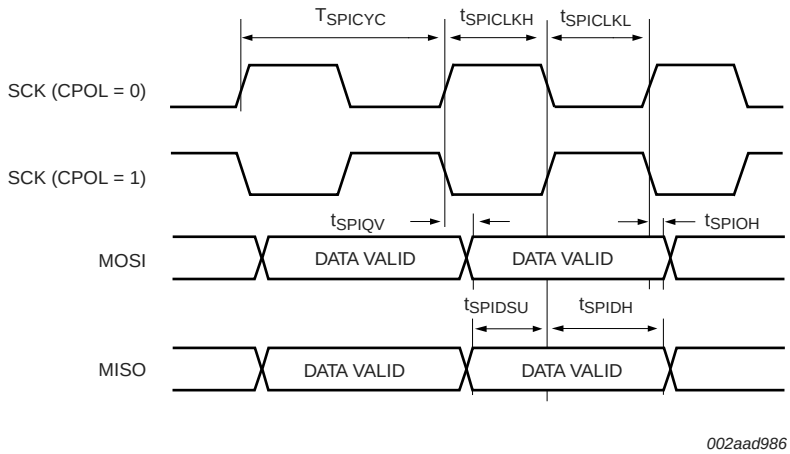


Fig 19. SPI master timing (CPHA = 1)

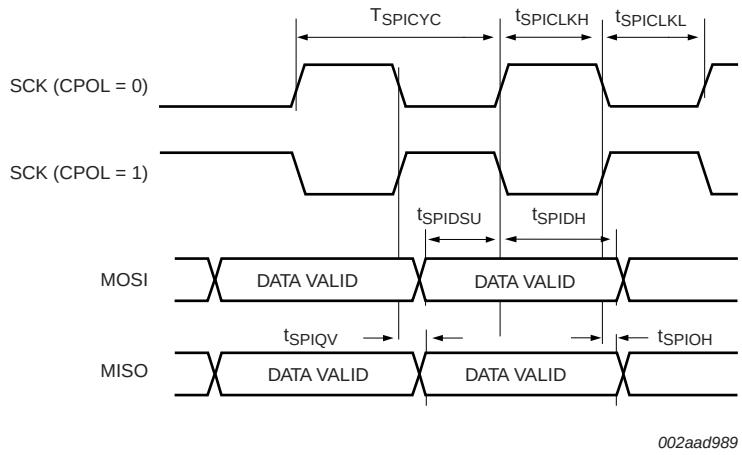


Fig 22. SPI slave timing (CPHA = 0)

9.6.1 Texas Instruments synchronous serial mode (SSI mode)

Table 23. Dynamic characteristic: SPI interface (SSI mode)
T_{amb} = −40 °C to +85 °C; $V_{DD(IO)}$ (SUP3) over specified ranges.[1]

Symbol	Parameter	Conditions	Min	Typ[2]	Max	Unit
$t_{su(SPI\_MISO)}$	SPI_MISO set-up time	T_{amb} = 25 °C; measured in SPI Master mode; see Figure 23	-	11	-	ns

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

Remark: Note that the signal names SCK, MISO, and MOSI correspond to signals on pins SPI_SCK, SPI_MOSI, and SPI_MISO in the following SPI timing diagram.

10. Application information

Table 25. LCD panel connections

TFBGA pin #	Pin name	Reset function (default)	LCD mode					
			Parallel					Serial
			LCD panel data mapping			Control function		
			16 bit	8 bit	4 bit	6800	8080	
K8	mLCD_CSB/EBI_NSTCS_0	LCD_CSB	-	-	-	LCD_CSB	LCD_CSB	LCD_CSB
L8	mLCD_E_RD/EBI_CKE	LCD_E_RD	-	-	-	LCD_E	LCD_RD	-
P8	mLCD_RS/EBI_NDYCS	LCD_RS	-	-	-	LCD_RS	LCD_RS	LCD_RS
N9	mLCD_RW_WR/EBI_DQM_1	LCD_RW_WR	-	-	-	LCD_RW	LCD_WR	-
N8	mLCD_DB_0/EBI_CLKOUT	LCD_DB_0	LCD_DB_0	-	-	-	-	-
P9	mLCD_DB_1/EBI_NSTCS_1	LCD_DB_1	LCD_DB_1	-	-	-	-	-
N6	mLCD_DB_2/EBI_A_2	LCD_DB_2	LCD_DB_2	-	-	-	-	-
P6	mLCD_DB_3/EBI_A_3	LCD_DB_3	LCD_DB_3	-	-	-	-	-
N7	mLCD_DB_4/EBI_A_4	LCD_DB_4	LCD_DB_4	-	-	-	-	-
P7	mLCD_DB_5/EBI_A_5	LCD_DB_5	LCD_DB_5	-	-	-	-	-
K6	mLCD_DB_6/EBI_A_6	LCD_DB_6	LCD_DB_6	-	-	-	-	-
P5	mLCD_DB_7/EBI_A_7	LCD_DB_7	LCD_DB_7	-	-	-	-	-
N5	mLCD_DB_8/EBI_A_8	LCD_DB_8	LCD_DB_8	LCD_DB_0	-	-	-	-
L5	mLCD_DB_9/EBI_A_9	LCD_DB_9	LCD_DB_9	LCD_DB_1	-	-	-	-
K7	mLCD_DB_10/EBI_A_10	LCD_DB_10	LCD_DB_10	LCD_DB_2	-	-	-	-
N4	mLCD_DB_11/EBI_A_11	LCD_DB_11	LCD_DB_11	LCD_DB_3	-	-	-	-
K5	mLCD_DB_12/EBI_A_12	LCD_DB_12	LCD_DB_12	LCD_DB_4	LCD_DB_0	-	-	-
P4	mLCD_DB_13/EBI_A_13	LCD_DB_13	LCD_DB_13	LCD_DB_5	LCD_DB_1	-	-	SER_CLK
P3	mLCD_DB_14/EBI_A_14	LCD_DB_14	LCD_DB_14	LCD_DB_6	LCD_DB_2	-	-	SER_DAT_IN
N3	mLCD_DB_15/EBI_A_15	LCD_DB_15	LCD_DB_15	LCD_DB_7	LCD_DB_3	-	-	SER_DAT_OUT

Table 27. Abbreviations *…continued*

Acronym	Description
RNG	Random Number Generator
ROM	Read-Only Memory
SD	Secure Digital
SDHC	Secure Digital High Capacity
SDIO	Secure Digital Input Output
SDR SDRAM	Single Data Rate Synchronous Dynamic Random Access Memory
SE0	Single Ended 0
SIR	Serial IrDA
SPI	Serial Peripheral Interface
SSI	Serial Synchronous Interface
SysCReg	System Control Registers
TAP	Test Access Port
TDO	Test Data Out
UART	Universal Asynchronous Receiver Transmitter
USB	Universal Serial Bus
UTMI	USB 2.0 Transceiver Macrocell Interface
WDT	WatchDog Timer

14. Revision history

Table 28: Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC3141_43 v.1	20120604	Product data sheet	-	-

17. Contents

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 4 June 2012
Document identifier: LPC3141_43