Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	S08
Core Size	8-Bit
Speed	40MHz
Connectivity	I²C, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	34
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LQFP
Supplier Device Package	44-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc9s08aw32mfge

Part Number	Package Description	Original (gold wire) package document number	Current (copper wire) package document number
MC68HC908JW32	48 QFN	98ARH99048A	98ASA00466D
MC9S08AC16			
MC9S908AC60			
MC9S08AC128			
MC9S08AW60			
MC9S08GB60A			
MC9S08GT16A			
MC9S08JM16			
MC9S08JM60			
MC9S08LL16			
MC9S08QE128			
MC9S08QE32			
MC9S08RG60			
MCF51CN128			
MC9RS08LA8	48 QFN	98ARL10606D	98ASA00466D
MC9S08GT16A	32 QFN	98ARH99035A	98ASA00473D
MC9S908QE32	32 QFN	98ARE10566D	98ASA00473D
MC9S908QE8	32 QFN	98ASA00071D	98ASA00736D
MC9S08JS16	24 QFN	98ARL10608D	98ASA00734D
MC9S08QB8			
MC9S08QG8	24 QFN	98ARL10605D	98ASA00474D
MC9S08SH8	24 QFN	98ARE10714D	98ASA00474D
MC9RS08KB12	24 QFN	98ASA00087D	98ASA00602D
MC9S08QG8	16 QFN	98ARE10614D	98ASA00671D
MC9RS08KB12	8 DFN	98ARL10557D	98ASA00672D
MC9S08QG8			
MC9RS08KA2	6 DFN	98ARL10602D	98ASA00735D

Chapter 14
Analog-to-Digital Converter (S08ADC10V1)

14.1 Overview 233
14.2 Channel Assignments 233
14.2.1 Alternate Clock 234
14.2.2 Hardware Trigger 234
14.2.3 Temperature Sensor 235
14.2.4 Features 237
14.2.5 Block Diagram 237
14.3 External Signal Description 238
14.3.1 Analog Power (V_{DDAD}) 239
14.3.2 Analog Ground (V_{SSAD}) 239
14.3.3 Voltage Reference High (V_{REFH}) 239
14.3.4 Voltage Reference Low (V_{REFL}) 239
14.3.5 Analog Channel Inputs (ADx) 239
14.4 Register Definition 239
14.4.1 Status and Control Register 1 (ADC1SC1) 239
14.4.2 Status and Control Register 2 (ADC1SC2) 241
14.4.3 Data Result High Register (ADC1RH) 242
14.4.4 Data Result Low Register (ADC1RL) 242
14.4.5 Compare Value High Register (ADC1CVH) 243
14.4.6 Compare Value Low Register (ADC1CVL) 243
14.4.7 Configuration Register (ADC1CFG) 243
14.4.8 Pin Control 1 Register (APCTL1) 245
14.4.9 Pin Control 2 Register (APCTL2) 246
14.4.10 Pin Control 3 Register (APCTL3) 247
14.5 Functional Description 248
14.5.1 Clock Select and Divide Control 248
14.5.2 Input Select and Pin Control 249
14.5.3 Hardware Trigger 249
14.5.4 Conversion Control 249
14.5.5 Automatic Compare Function 252
14.5.6 MCU Wait Mode Operation 252
14.5.7 MCU Stop3 Mode Operation 252
14.5.8 MCU Stop1 and Stop2 Mode Operation 253
14.6 Initialization Information 253
14.6.1 ADC Module Initialization Example 253
14.7 Application Information 255
14.7.1 External Pins and Routing 255
14.7.2 Sources of Error 257

Chapter 15
Development Support

15.1 Introduction 261
15.1.1 Features 262
15.2 Background Debug Controller (BDC) 262
15.2.1 BKGD Pin Description 263
15.2.2 Communication Details 264
15.2.3 BDC Commands 268
15.2.4 BDC Hardware Breakpoint 270
15.3 On-Chip Debug System (DBG) 271
15.3.1 Comparators A and B 271
15.3.2 Bus Capture Information and FIFO Operation 271
15.3.3 Change-of-Flow Information 272
15.3.4 Tag vs. Force Breakpoints and Triggers 272
15.3.5 Trigger Modes 273
15.3.6 Hardware Breakpoints 275
15.4 Register Definition 275
15.4.1 BDC Registers and Control Bits 275
15.4.2 System Background Debug Force Reset Register (SBDFR) 277
15.4.3 DBG Registers and Control Bits 278

Appendix A
Electrical Characteristics and Timing Specifications

A.1 Introduction 283
A.2 Parameter Classification 283
A.3 Absolute Maximum Ratings 283
A.4 Thermal Characteristics 285
A.5 ESD Protection and Latch-Up Immunity 286
A.6 DC Characteristics 287
A.7 Supply Current Characteristics 291
A.8 ADC Characteristics 293
A.9 Internal Clock Generation Module Characteristics 296
A.9.1 ICG Frequency Specifications 297
A.10 AC Characteristics 300
A.10.1 Control Timing 300
A.10.2 Timer/PWM (TPM) Module Timing 302
A.11 SPI Characteristics 303
A.12 FLASH Specifications 306
A.13 EMC Performance 307
A.13.1 Radiated Emissions 307
A.13.2 Conducted Transient Susceptibility 307

When IRQ is configured as the IRQ input and is set to detect rising edges, a pulldown device rather than a pullup device is enabled.

In EMC-sensitive applications, an external RC filter is recommended on the IRQ pin. See Figure 2-4 for an example.

2.3.7 General-Purpose I/O and Peripheral Ports

The remaining pins are shared among general-purpose I/O and on-chip peripheral functions such as timers and serial I/O systems. Immediately after reset, all of these pins are configured as high-impedance general-purpose inputs with internal pullup devices disabled.

NOTE

To avoid extra current drain from floating input pins, the reset initialization routine in the application program should either enable on-chip pullup devices or change the direction of unused pins to outputs so the pins do not float.

For information about controlling these pins as general-purpose I/O pins, see Chapter 6, "Parallel Input/Output." For information about how and when on-chip peripheral systems use these pins, refer to the appropriate chapter from Table 2-1.

Table 2-1. Pin Sharing Priority

Lowest <- Pin Function Priority -> Highest			Reference[1]
Port Pins	**Alternate Function**	**Alternate Function**	
PTB7–PTB0	AD1P7–AD1P0		Chapter 14, "Analog-to-Digital Converter (S08ADC10V1)"
PTC5, PTC3	RxD2–TxD2		Chapter 11, "Serial Communications Interface (S08SCIV2)"
PTC2	MCLK		Chapter 5, "Resets, Interrupts, and System Configuration"
PTC1–PTC0	SCL1–SDA1		Chapter 13, "Inter-Integrated Circuit (S08IICV1)"
PTD7	KBI1P7	AD1P15	Chapter 14, "Analog-to-Digital Converter (S08ADC10V1)" Chapter 9, "Keyboard Interrupt (S08KBIV1)"
PTD6	TPM1CLK	AD1P14	Chapter 14, "Analog-to-Digital Converter (S08ADC10V1)" Chapter 10, "Timer/PWM (S08TPMV2)"
PTD5	AD1P13	AD1P13	Chapter 14, "Analog-to-Digital Converter (S08ADC10V1)"
PTD4	TPM2CLK	AD1P12	Chapter 14, "Analog-to-Digital Converter (S08ADC10V1)" Chapter 10, "Timer/PWM (S08TPMV2)"
PTD3–PTD2	KBI1P6–KBI1P5	AD1P11–AD1P10	Chapter 14, "Analog-to-Digital Converter (S08ADC10V1)" Chapter 9, "Keyboard Interrupt (S08KBIV1)"
PTD1–PTD0	AD1P9–AD1P8		Chapter 14, "Analog-to-Digital Converter (S08ADC10V1)"
PTE7 PTE6 PTE5 PTE4	SPSCK1 MOSI1 MISO1 $\overline{SS1}$		Chapter 12, "Serial Peripheral Interface (S08SPIV3)"
PTE3–PTE2	TPM1CH1– TPM1CH0		Chapter 10, "Timer/PWM (S08TPMV2)"
PTE1–PTE0	RxD1–TxD1		Chapter 11, "Serial Communications Interface (S08SCIV2)"
PTF5–PTF4	TPM2CH1– TPM2CH0		Chapter 10, "Timer/PWM (S08TPMV2)"

Table 4-2. Direct-Page Register Summary (Sheet 3 of 3)

Address	Register Name	Bit 7	6	5	4	3	2	1	Bit 0
$0050	**SPI1C1**	SPIE	SPE	SPTIE	MSTR	CPOL	CPHA	SSOE	LSBFE
$0051	**SPI1C2**	0	0	0	MODFEN	BIDIROE	0	SPISWAI	SPC0
$0052	**SPI1BR**	0	SPPR2	SPPR1	SPPR0	0	SPR2	SPR1	SPR0
$0053	**SPI1S**	SPRF	0	SPTEF	MODF	0	0	0	0
$0054	Reserved	0	0	0	0	0	0	0	0
$0055	**SPI1D**	Bit 7	6	5	4	3	2	1	Bit 0
$0056–$0057	Reserved	— —	— —	— —	— —	— —	— —	— —	— —
$0058	**IIC1A**	ADDR							0
$0059	**IIC1F**	MULT		ICR					
$005A	**IIC1C**	IICEN	IICIE	MST	TX	TXAK	RSTA	0	0
$005B	**IIC1S**	TCF	IAAS	BUSY	ARBL	0	SRW	IICIF	RXAK
$005C	**IIC1D**	DATA							
$005D–$005F	Reserved	— —	— —	— —	— —	— —	— —	— —	— —
$0060	**TPM2SC**	TOF	TOIE	CPWMS	CLKSB	CLKSA	PS2	PS1	PS0
$0061	**TPM2CNTH**	Bit 15	14	13	12	11	10	9	Bit 8
$0062	**TPM2CNTL**	Bit 7	6	5	4	3	2	1	Bit 0
$0063	**TPM2MODH**	Bit 15	14	13	12	11	10	9	Bit 8
$0064	**TPM2MODL**	Bit 7	6	5	4	3	2	1	Bit 0
$0065	**TPM2C0SC**	CH0F	CH0IE	MS0B	MS0A	ELS0B	ELS0A	0	0
$0066	**TPM2C0VH**	Bit 15	14	13	12	11	10	9	Bit 8
$0067	**TPM2C0VL**	Bit 7	6	5	4	3	2	1	Bit 0
$0068	**TPM2C1SC**	CH1F	CH1IE	MS1B	MS1A	ELS1B	ELS1A	0	0
$0069	**TPM2C1VH**	Bit 15	14	13	12	11	10	9	Bit 8
$006A	**TPM2C1VL**	Bit 7	6	5	4	3	2	1	Bit 0
$006B–$006F	Reserved	— —	— —	— —	— —	— —	— —	— —	— —

Table 4-7. FLASH Clock Divider Settings

f_{Bus}	PRDIV8 (Binary)	DIV5:DIV0 (Decimal)	f_{FCLK}	Program/Erase Timing Pulse (5 µs Min, 6.7 µs Max)
20 MHz	1	12	192.3 kHz	5.2 µs
10 MHz	0	49	200 kHz	5 µs
8 MHz	0	39	200 kHz	5 µs
4 MHz	0	19	200 kHz	5 µs
2 MHz	0	9	200 kHz	5 µs
1 MHz	0	4	200 kHz	5 µs
200 kHz	0	0	200 kHz	5 µs
150 kHz	0	0	150 kHz	6.7 µs

4.6.2 FLASH Options Register (FOPT and NVOPT)

During reset, the contents of the nonvolatile location NVOPT are copied from FLASH into FOPT. Bits 5 through 2 are not used and always read 0. This register may be read at any time, but writes have no meaning or effect. To change the value in this register, erase and reprogram the NVOPT location in FLASH memory as usual and then issue a new MCU reset.

	7	6	5	4	3	2	1	0
R	KEYEN	FNORED	0	0	0	0	SEC01	SEC00
W								
Reset	This register is loaded from nonvolatile location NVOPT during reset.							

= Unimplemented or Reserved

Figure 4-7. FLASH Options Register (FOPT)

Table 4-8. FOPT Register Field Descriptions

Field	Description
7 KEYEN	**Backdoor Key Mechanism Enable** — When this bit is 0, the backdoor key mechanism cannot be used to disengage security. The backdoor key mechanism is accessible only from user (secured) firmware. BDM commands cannot be used to write key comparison values that would unlock the backdoor key. For more detailed information about the backdoor key mechanism, refer to Section 4.5, “Security.” 0 No backdoor key access allowed. 1 If user firmware writes an 8-byte value that matches the nonvolatile backdoor key (NVBACKKEY through NVBACKKEY+7 in that order), security is temporarily disengaged until the next MCU reset.
6 FNORED	**Vector Redirection Disable** — When this bit is 1, then vector redirection is disabled. 0 Vector redirection enabled. 1 Vector redirection disabled.
1:0 SEC0[1:0]	**Security State Code** — This 2-bit field determines the security state of the MCU as shown in Table 4-9. When the MCU is secure, the contents of RAM and FLASH memory cannot be accessed by instructions from any unsecured source including the background debug interface. For more detailed information about security, refer to Section 4.5, “Security.”

5.9.8 System Power Management Status and Control 1 Register (SPMSC1)

	7	6	5	4	3	2	1[1]	0
R	LVDF	0	LVDIE	LVDRE[(2)]	LVDSE[(2)]	LVDE[(2)]		BGBE
W		LVDACK						
Reset	0	0	0	1	1	1	0	0

= Unimplemented or Reserved

1 Bit 1 is a reserved bit that must always be written to 0.

2 This bit can be written only one time after reset. Additional writes are ignored.

Figure 5-10. System Power Management Status and Control 1 Register (SPMSC1)

Table 5-11. SPMSC1 Register Field Descriptions

Field	Description
7 LVDF	**Low-Voltage Detect Flag** — Provided LVDE = 1, this read-only status bit indicates a low-voltage detect event.
6 LVDACK	**Low-Voltage Detect Acknowledge** — This write-only bit is used to acknowledge low voltage detection errors (write 1 to clear LVDF). Reads always return 0.
5 LVDIE	**Low-Voltage Detect Interrupt Enable** — This read/write bit enables hardware interrupt requests for LVDF. 0 Hardware interrupt disabled (use polling). 1 Request a hardware interrupt when LVDF = 1.
4 LVDRE	**Low-Voltage Detect Reset Enable** — This read/write bit enables LVDF events to generate a hardware reset (provided LVDE = 1). 0 LVDF does not generate hardware resets. 1 Force an MCU reset when LVDF = 1.
3 LVDSE	**Low-Voltage Detect Stop Enable** — Provided LVDE = 1, this read/write bit determines whether the low-voltage detect function operates when the MCU is in stop mode. 0 Low-voltage detect disabled during stop mode. 1 Low-voltage detect enabled during stop mode.
2 LVDE	**Low-Voltage Detect Enable** — This read/write bit enables low-voltage detect logic and qualifies the operation of other bits in this register. 0 LVD logic disabled. 1 LVD logic enabled.
0 BGBE	**Bandgap Buffer Enable** — The BGBE bit is used to enable an internal buffer for the bandgap voltage reference for use by the ADC module on one of its internal channels. 0 Bandgap buffer disabled. 1 Bandgap buffer enabled.

Chapter 6
Parallel Input/Output

6.1 Introduction

This chapter explains software controls related to parallel input/output (I/O). The MC9S08AW60 has seven I/O ports which include a total of 54 general-purpose I/O pins. See Chapter 2, “Pins and Connections” for more information about the logic and hardware aspects of these pins.

Many of these pins are shared with on-chip peripherals such as timer systems, communication systems, or keyboard interrupts. When these other modules are not controlling the port pins, they revert to general-purpose I/O control.

Pins that are not used in the application must be terminated. This prevents excess current caused by floating inputs and enhances immunity during noise or transient events. Termination methods include:

- Configuring unused pins as outputs driving high or low
- Configuring unused pins as inputs and using internal or external pullups

Never connect unused pins to V_{DD} or V_{SS}.

Table 6-1. KBI and Parallel I/O Interaction

PTxPEn (Pull Enable)	PTxDDn (Data Direction)	KBIPEn (KBI Pin Enable)	KBEDGn (KBI Edge Select)	Pullup	Pulldown
0	0	0	x[1]	disabled	disabled
1	0	0	x	enabled	disabled
x	1	0	x	disabled	disabled
1	x	1	0	enabled	disabled
1	x	1	1	disabled	enabled
0	x	1	x	disabled	disabled

1 x = Don’t care

6.2 Features

Parallel I/O and Pin Control features, depending on package choice, include:

- A total of 54 general-purpose I/O pins in seven ports
- Hysteresis input buffers
- Software-controlled pullups on each input pin

- Software-controlled slew rate output buffers
- Eight port A pins
- Eight port B pins shared with ADC1
- Seven port C pins shared with SCI2, IIC1, and MCLK
- Eight port D pins shared with ADC1, KBI1, and TPM1 and TPM2 external clock inputs
- Eight port E pins shared with SCI1, TPM1, and SPI1
- Eight port F pins shared with TPM1 and TPM2
- Seven port G pins shared with XTAL, EXTAL, and KBI1

6.3 Pin Descriptions

The MC9S08AW60 Series has a total of 54 parallel I/O pins in seven ports (PTA–PTG). Not all pins are bonded out in all packages. Consult the pin assignment in Chapter 2, "Pins and Connections," for available parallel I/O pins. All of these pins are available for general-purpose I/O when they are not used by other on-chip peripheral systems.

After reset, the shared peripheral functions are disabled so that the pins are controlled by the parallel I/O. All of the parallel I/O are configured as inputs (PTxDDn = 0). The pin control functions for each pin are configured as follows: slew rate control enabled (PTxSEn = 1), low drive strength selected (PTxDSn = 0), and internal pullups disabled (PTxPEn = 0).

The following paragraphs discuss each port and the software controls that determine each pin's use.

6.3.1 Port A

Port A		Bit 7	6	5	4	3	2	1	Bit 0
	MCU Pin:	PTA7	PTA6	PTA5	PTA4	PTA3	PTA2	PTA1	PTA0

Figure 6-1. Port A Pin Names

Port A pins are general-purpose I/O pins. Parallel I/O function is controlled by the port A data (PTAD) and data direction (PTADD) registers which are located in page zero register space. The pin control registers, pullup enable (PTAPE), slew rate control (PTASE), and drive strength select (PTADS) are located in the high page registers. Refer to Section 6.4, "Parallel I/O Control" for more information about general-purpose I/O control and Section 6.5, "Pin Control" for more information about pin control.

6.3.2 Port B

Port B		Bit 7	6	5	4	3	2	1	Bit 0
	MCU Pin:	PTB7/ AD1P7	PTB6/ AD1P6	PTB5/ AD1P5	PTB4/ AD1P4	PTB3/ AD1P3	PTB2/ AD1P2	PTB1/ AD1P1	PTB0/ AD1P0

Figure 6-2. Port B Pin Names

6.7.9 Port E I/O Registers (PTED and PTEDD)

Port E parallel I/O function is controlled by the registers listed below.

	7	6	5	4	3	2	1	0
R W	PTED7	PTED6	PTED5	PTED4	PTED3	PTED2	PTED1	PTED0
Reset	0	0	0	0	0	0	0	0

Figure 6-29. Port E Data Register (PTED)

Table 6-22. PTED Register Field Descriptions

Field	Description
7:0 PTED[7:0]	**Port E Data Register Bits** — For port E pins that are inputs, reads return the logic level on the pin. For port E pins that are configured as outputs, reads return the last value written to this register. Writes are latched into all bits of this register. For port E pins that are configured as outputs, the logic level is driven out the corresponding MCU pin. Reset forces PTED to all 0s, but these 0s are not driven out the corresponding pins because reset also configures all port pins as high-impedance inputs with pullups disabled.

	7	6	5	4	3	2	1	0
R W	PTEDD7	PTEDD6	PTEDD5	PTEDD4	PTEDD3	PTEDD2	PTEDD1	PTEDD0
Reset	0	0	0	0	0	0	0	0

Figure 6-30. Data Direction for Port E (PTEDD)

Table 6-23. PTEDD Register Field Descriptions

Field	Description
7:0 PTEDD[7:0]	**Data Direction for Port E Bits** — These read/write bits control the direction of port E pins and what is read for PTED reads. 0 Input (output driver disabled) and reads return the pin value. 1 Output driver enabled for port E bit n and PTED reads return the contents of PTEDn.

0	=	Bit forced to 0
1	=	Bit forced to 1
	=	Bit set or cleared according to results of operation
U	=	Undefined after the operation

Machine coding notation

dd	=	Low-order 8 bits of a direct address 0x0000–0x00FF (high byte assumed to be 0x00)
ee	=	Upper 8 bits of 16-bit offset
ff	=	Lower 8 bits of 16-bit offset or 8-bit offset
ii	=	One byte of immediate data
jj	=	High-order byte of a 16-bit immediate data value
kk	=	Low-order byte of a 16-bit immediate data value
hh	=	High-order byte of 16-bit extended address
ll	=	Low-order byte of 16-bit extended address
rr	=	Relative offset

Source form

Everything in the source forms columns, *except expressions in italic characters,* is literal information that must appear in the assembly source file exactly as shown. The initial 3- to 5-letter mnemonic is always a literal expression. All commas, pound signs (#), parentheses, and plus signs (+) are literal characters.

n	—	Any label or expression that evaluates to a single integer in the range 0–7
opr8i	—	Any label or expression that evaluates to an 8-bit immediate value
opr16i	—	Any label or expression that evaluates to a 16-bit immediate value
opr8a	—	Any label or expression that evaluates to an 8-bit value. The instruction treats this 8-bit value as the low order 8 bits of an address in the direct page of the 64-Kbyte address space (0x00xx).
opr16a	—	Any label or expression that evaluates to a 16-bit value. The instruction treats this value as an address in the 64-Kbyte address space.
oprx8	—	Any label or expression that evaluates to an unsigned 8-bit value, used for indexed addressing
oprx16	—	Any label or expression that evaluates to a 16-bit value. Because the HCS08 has a 16-bit address bus, this can be either a signed or an unsigned value.
rel	—	Any label or expression that refers to an address that is within –128 to +127 locations from the next address after the last byte of object code for the current instruction. The assembler will calculate the 8-bit signed offset and include it in the object code for this instruction.

Address modes

INH	=	Inherent (no operands)
IMM	=	8-bit or 16-bit immediate
DIR	=	8-bit direct
EXT	=	16-bit extended

ICGTRM = $xx

Bit 7:0 TRIM — Only need to write when trimming internal oscillator; done in separate operation (see example #4)

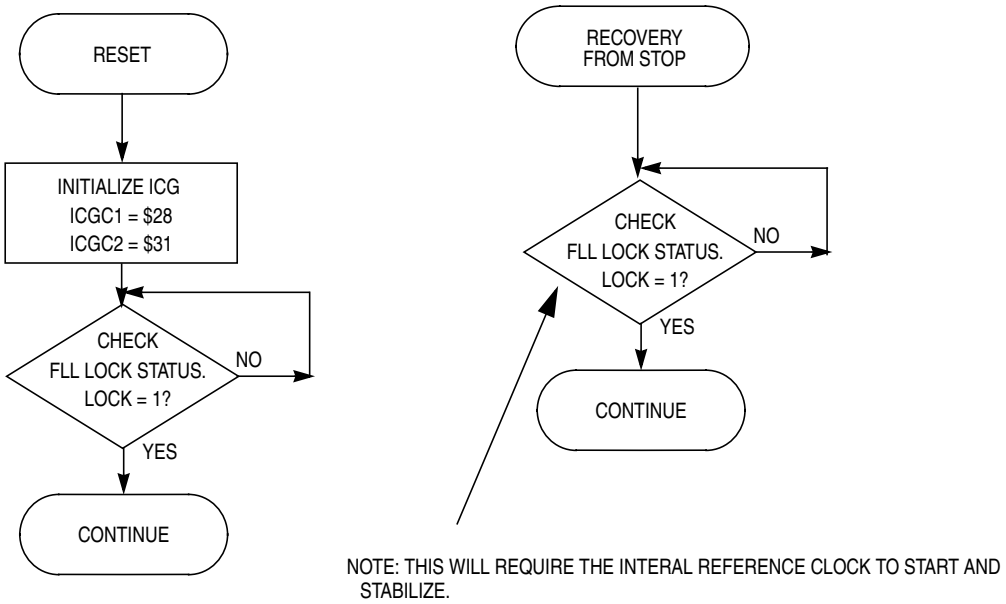


Figure 8-16. ICG Initialization and Stop Recovery for Example #3

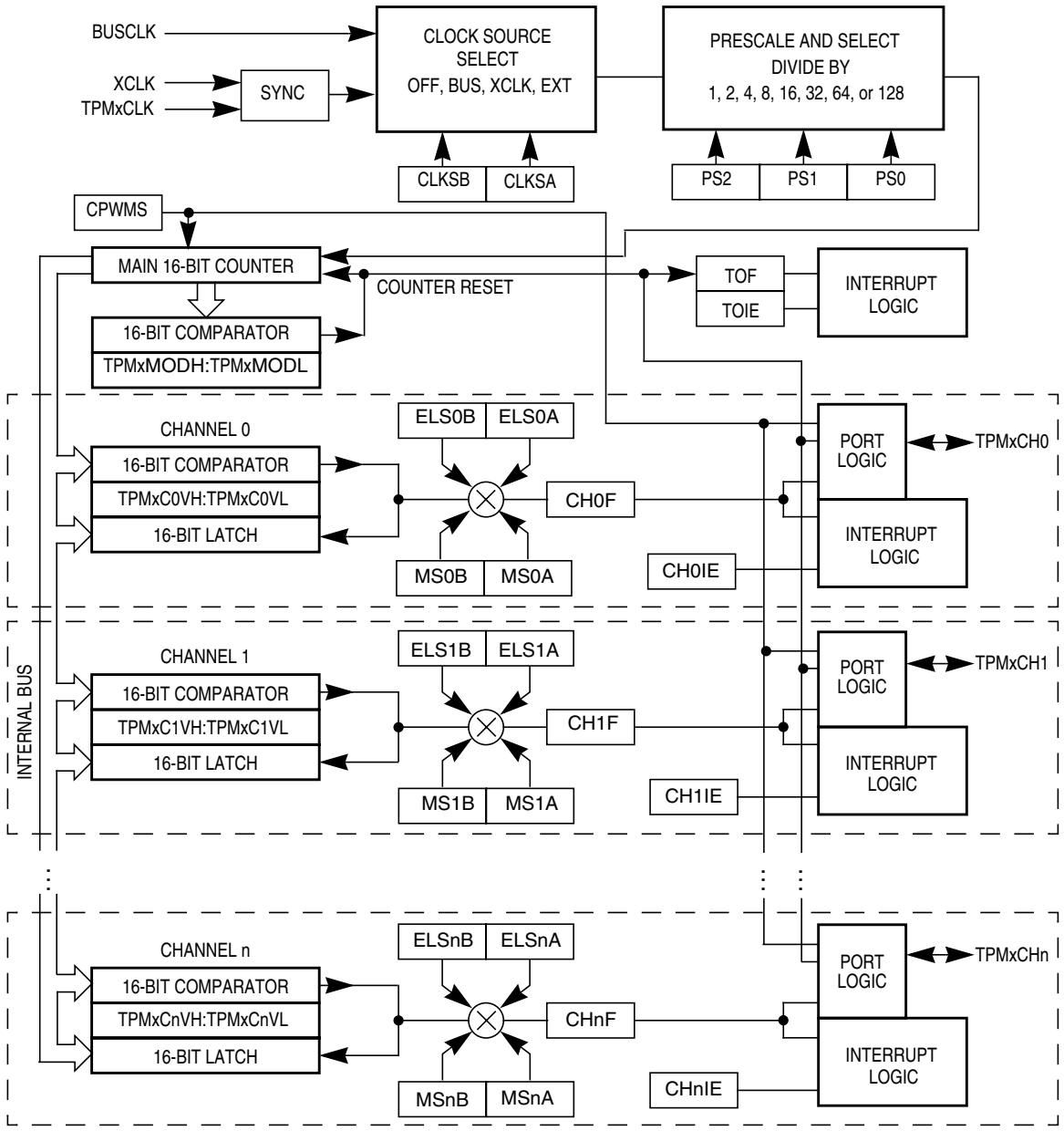
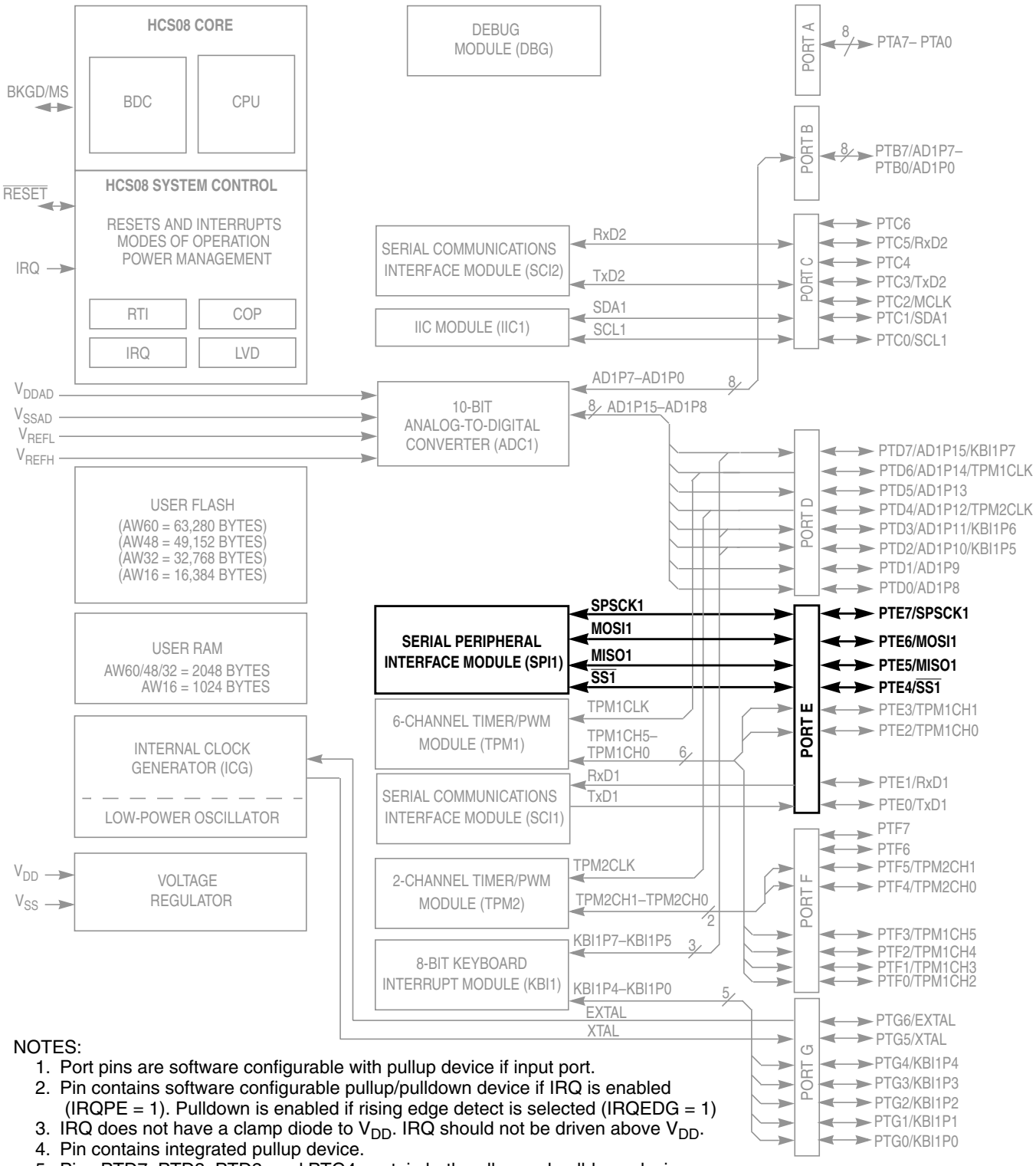


Figure 10-2. TPM Block Diagram

The central component of the TPM is the 16-bit counter that can operate as a free-running counter, a modulo counter, or an up-/down-counter when the TPM is configured for center-aligned PWM. The TPM counter (when operating in normal up-counting mode) provides the timing reference for the input capture, output compare, and edge-aligned PWM functions. The timer counter modulo registers, TPMxMODH:TPMxMODL, control the modulo value of the counter. (The values 0x0000 or 0xFFFF effectively make the counter free running.) Software can read the counter value at any time without affecting the counting sequence. Any write to either byte of the TPMxCNT counter resets the counter regardless of the data value written.



NOTES:
1. Port pins are software configurable with pullup device if input port.
2. Pin contains software configurable pullup/pulldown device if IRQ is enabled (IRQPE = 1). Pulldown is enabled if rising edge detect is selected (IRQEDG = 1)
3. IRQ does not have a clamp diode to V_{DD}. IRQ should not be driven above V_{DD}.
4. Pin contains integrated pullup device.
5. Pins PTD7, PTD3, PTD2, and PTG4 contain both pullup and pulldown devices. Pulldown enabled when KBI is enabled (KBIPEn = 1) and rising edge is selected (KBEDGn = 1).

Figure 12-1. Block Diagram Highlighting the SPI Module

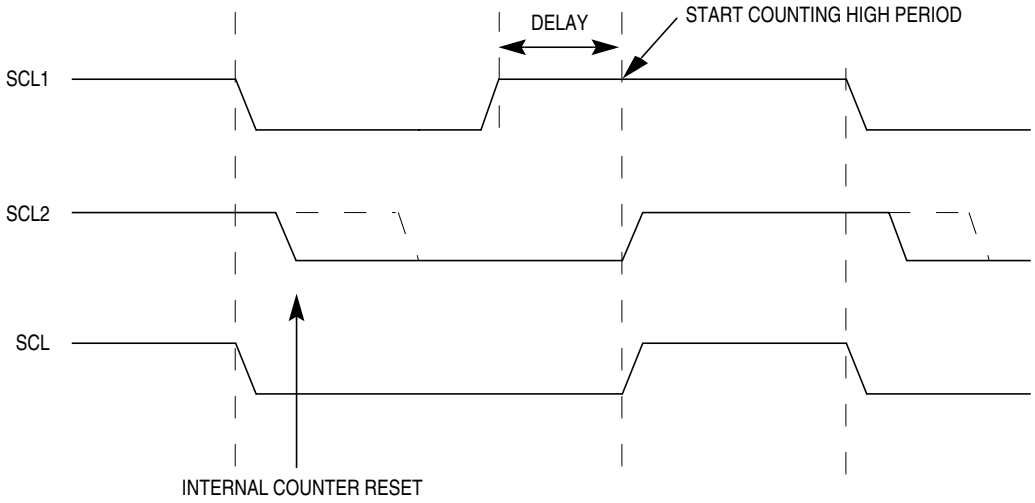


Figure 13-9. IIC Clock Synchronization

13.4.1.8 Handshaking

The clock synchronization mechanism can be used as a handshake in data transfer. Slave devices may hold the SCL low after completion of one byte transfer (9 bits). In such case, it halts the bus clock and forces the master clock into wait states until the slave releases the SCL line.

13.4.1.9 Clock Stretching

The clock synchronization mechanism can be used by slaves to slow down the bit rate of a transfer. After the master has driven SCL low the slave can drive SCL low for the required period and then release it. If the slave SCL low period is greater than the master SCL low period then the resulting SCL bus signal low period is stretched.

13.5 Resets

The IIC is disabled after reset. The IIC cannot cause an MCU reset.

13.6 Interrupts

The IIC generates a single interrupt.

An interrupt from the IIC is generated when any of the events in Table 13-7 occur provided the IICIE bit is set. The interrupt is driven by bit IICIF (of the IIC status register) and masked with bit IICIE (of the IIC control register). The IICIF bit must be cleared by software by writing a one to it in the interrupt routine. The user can determine the interrupt type by reading the status register.

Table 13-7. Interrupt Summary

Interrupt Source	Status	Flag	Local Enable
Complete 1-byte transfer	TCF	IICIF	IICIE
Match of received calling address	IAAS	IICIF	IICIE
Arbitration Lost	ARBL	IICIF	IICIE

Figure 14-4. Input Channel Select (continued)

ADCH	Input Select
01000	AD8
01001	AD9
01010	AD10
01011	AD11
01100	AD12
01101	AD13
01110	AD14
01111	AD15

ADCH	Input Select
11000	AD24
11001	AD25
11010	AD26
11011	AD27
11100	Reserved
11101	V_{REFH}
11110	V_{REFL}
11111	Module disabled

14.4.2 Status and Control Register 2 (ADC1SC2)

The ADC1SC2 register is used to control the compare function, conversion trigger and conversion active of the ADC module.

	7	6	5	4	3	2	1	0
R	ADACT	ADTRG	ACFE	ACFGT	0	0	R[1]	R[1]
W								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

[1] Bits 1 and 0 are reserved bits that must always be written to 0.

Figure 14-5. Status and Control Register 2 (ADC1SC2)

Table 14-4. ADC1SC2 Register Field Descriptions

Field	Description
7 ADACT	**Conversion Active** — ADACT indicates that a conversion is in progress. ADACT is set when a conversion is initiated and cleared when a conversion is completed or aborted. 0 Conversion not in progress 1 Conversion in progress
6 ADTRG	**Conversion Trigger Select** — ADTRG is used to select the type of trigger to be used for initiating a conversion. Two types of trigger are selectable: software trigger and hardware trigger. When software trigger is selected, a conversion is initiated following a write to ADC1SC1. When hardware trigger is selected, a conversion is initiated following the assertion of the ADHWT input. 0 Software trigger selected 1 Hardware trigger selected

	7	6	5	4	3	2	1	0
R	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0
W								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 14-7. Data Result Low Register (ADC1RL)

14.4.5 Compare Value High Register (ADC1CVH)

This register holds the upper two bits of the 10-bit compare value. These bits are compared to the upper two bits of the result following a conversion in 10-bit mode when the compare function is enabled.In 8-bit operation, ADC1CVH is not used during compare.

	7	6	5	4	3	2	1	0
R	0	0	0	0			ADCV9	ADCV8
W								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 14-8. Compare Value High Register (ADC1CVH)

14.4.6 Compare Value Low Register (ADC1CVL)

This register holds the lower 8 bits of the 10-bit compare value, or all 8 bits of the 8-bit compare value. Bits ADCV7:ADCV0 are compared to the lower 8 bits of the result following a conversion in either 10-bit or 8-bit mode.

	7	6	5	4	3	2	1	0
R	ADCV7	ADCV6	ADCV5	ADCV4	ADCV3	ADCV2	ADCV1	ADCV0
W								
Reset:	0	0	0	0	0	0	0	0

Figure 14-9. Compare Value Low Register(ADC1CVL)

14.4.7 Configuration Register (ADC1CFG)

ADC1CFG is used to select the mode of operation, clock source, clock divide, and configure for low power or long sample time.

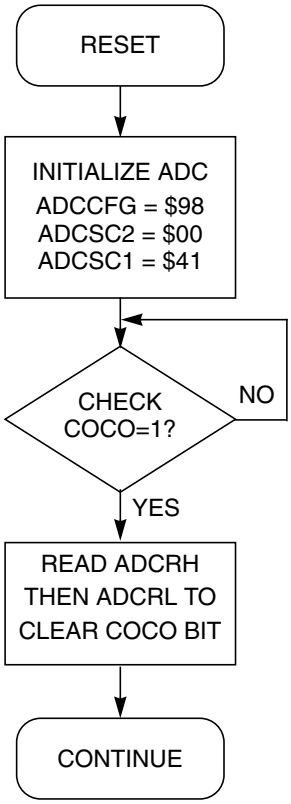


Figure 14-14. Initialization Flowchart for Example

14.7 Application Information

This section contains information for using the ADC module in applications. The ADC has been designed to be integrated into a microcontroller for use in embedded control applications requiring an A/D converter.

14.7.1 External Pins and Routing

The following sections discuss the external pins associated with the ADC module and how they should be used for best results.

14.7.1.1 Analog Supply Pins

The ADC module has analog power and ground supplies (V_{DDAD} and V_{SSAD}) which are available as separate pins on some devices. On other devices, V_{SSAD} is shared on the same pin as the MCU digital V_{SS}, and on others, both V_{SSAD} and V_{DDAD} are shared with the MCU digital supply pins. In these cases, there are separate pads for the analog supplies which are bonded to the same pin as the corresponding digital supply so that some degree of isolation between the supplies is maintained.

When available on a separate pin, both V_{DDAD} and V_{SSAD} must be connected to the same voltage potential as their corresponding MCU digital supply (V_{DD} and V_{SS}) and must be routed carefully for maximum noise immunity and bypass capacitors placed as near as possible to the package.

Appendix A
Electrical Characteristics and Timing Specifications

A.1 Introduction

This section contains electrical and timing specifications.

A.2 Parameter Classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give you a better understanding, the following classification is used and the parameters are tagged accordingly in the tables where appropriate:

Table A-1. Parameter Classifications

P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

NOTE

The classification is shown in the column labeled “C” in the parameter tables where appropriate.

A.3 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in Table A-2 may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this section.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either V_{SS} or V_{DD}).

Table A-12. ICG Frequency Specifications (continued)

(V_{DDA} = V_{DDA} (min) to V_{DDA} (max), Temperature Range = –40 to 125°C Ambient)

Num	C	Characteristic	Symbol	Min	Typ[1]	Max	Unit
19		**MC9S08AW*xx*:** Internal oscillator deviation from trimmed frequency[9]					
	C	V_{DD} = 2.7 – 5.5 V, (constant temperature)	ACC_{int}	—	±0.5	±2	%
	P	V_{DD} = 5.0 V ±10%, –40° C to 125°C		—	±0.5	±2	%
		S9S08AW*xx*: Internal oscillator deviation from trimmed frequency[9]					
	C	V_{DD} = 2.7 – 5.5 V, (constant temperature)	ACC_{int}	—	±0.5	±1.5	%
	P	V_{DD} = 5.0 V ±10%, –40° C to 85°C		—	±0.5	±1.5	%
	P	V_{DD} = 5.0 V ±10%, –40° C to 125°C		—	±0.5	±2	%

1 Typical values are based on characterization data at V_{DD} = 5.0V, 25°C unless otherwise stated.

2 Self-clocked mode frequency is the frequency that the DCO generates when the FLL is open-loop.

3 Loss of reference frequency is the reference frequency detected internally, which transitions the ICG into self-clocked mode if it is not in the desired range.

4 Loss of DCO frequency is the DCO frequency detected internally, which transitions the ICG into FLL bypassed external mode (if an external reference exists) if it is not in the desired range.

5 This parameter is characterized before qualification rather than 100% tested.

6 Proper PC board layout procedures must be followed to achieve specifications.

7 This specification applies to the period of time required for the FLL to lock after entering FLL engaged internal or external modes. If a crystal/resonator is being used as the reference, this specification assumes it is already running.

8 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{ICGOUT}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry via V_{DDA} and V_{SSA} and variation in crystal oscillator frequency increase the C_{Jitter} percentage for a given interval.

9 See Figure A-9.