NXP USA Inc. - <u>MC9S08AW60MFUER Datasheet</u>





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Details

Product Status	Active
Core Processor	S08
Core Size	8-Bit
Speed	40MHz
Connectivity	I ² C, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	54
Program Memory Size	60KB (60K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-QFP
Supplier Device Package	64-QFP (14x14)
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MC9S08AW60 MC9S08AW48 MC9S08AW32 MC9S08AW16

Data Sheet

HCS08 Microcontrollers

MC9S08AW60 Rev 2 12/2006



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Chapter 1 Introduction



5. Pins PTD7, PTD3, PTD2, and PTG4 contain both pullup and pulldown devices. Pulldown enabled when KBI is enabled (KBIPEn = 1) and rising edge is selected (KBEDGn = 1).





Chapter 3 Modes of Operation

3.1 Introduction

The operating modes of the MC9S08AW60 Series are described in this chapter. Entry into each mode, exit from each mode, and functionality while in each of the modes are described.

3.2 Features

- Active background mode for code development
- Wait mode:
 - CPU shuts down to conserve power
 - System clocks running
 - Full voltage regulation maintained
- Stop modes:
 - System clocks stopped; voltage regulator in standby
 - Stop2 Partial power down of internal circuits, RAM contents retained
 - Stop3 All internal circuits powered for fast recovery

3.3 Run Mode

This is the normal operating mode for the MC9S08AW60 Series. This mode is selected when the BKGD/MS pin is high at the rising edge of reset. In this mode, the CPU executes code from internal memory with execution beginning at the address fetched from memory at \$FFFE:\$FFFF after reset.

3.4 Active Background Mode

The active background mode functions are managed through the background debug controller (BDC) in the HCS08 core. The BDC, together with the on-chip debug module (DBG), provide the means for analyzing MCU operation during software development.

Active background mode is entered in any of five ways:

- When the BKGD/MS pin is low at the rising edge of reset
- When a BACKGROUND command is received through the BKGD pin
- When a BGND instruction is executed
- When encountering a BDC breakpoint
- When encountering a DBG breakpoint



Chapter 4 Memory

4.1 MC9S08AW60 Series Memory Map

Figure 4-1 shows the memory map for the MC9S08AW60 and MC9S08AW48 MCUs. Figure 4-2 shows the memory map for the MC9S08AW32 and MC9S08AW16 MCUs. On-chip memory in the MC9S08AW60 Series of MCUs consists of RAM, FLASH program memory for nonvolatile data storage, plus I/O and control/status registers. The registers are divided into three groups:

- Direct-page registers (\$0000 through \$006F)
- High-page registers (\$1800 through \$185F)
- Nonvolatile registers (\$FFB0 through \$FFBF)



Chapter 4 Memory

4.1.1 Reset and Interrupt Vector Assignments

Figure 4-1 shows address assignments for reset and interrupt vectors. The vector names shown in this table are the labels used in the Freescale-provided equate file for the MC9S08AW60 Series. For more details about resets, interrupts, interrupt priority, and local interrupt mask controls, refer to Chapter 5, "Resets, Interrupts, and System Configuration."

Address (High/Low)	Vector	Vector Name
\$FFC0:FFC1	Unused Vector Space	
\$	(available for user program)	
\$FFCA:FFCB		
\$FFCC:FFCD	RTI	Vrti
\$FFCE:FFCF	IIC1	Viic1
\$FFD0:FFD1	ADC1 Conversion	Vadc1
\$FFD2:FFD3	KBI1	Vkeyboard1
\$FFD4:FFD5	SCI2 Transmit	Vsci2tx
\$FFD6:FFD7	SCI2 Receive	Vsci2rx
\$FFD8:FFD9	SCI2 Error	Vsci2err
\$FFDA:FFDB	SCI1 Transmit	Vsci1tx
\$FFDC:FFDD	SCI1 Receive	Vsci1rx
\$FFDE:FFDF	SCI1 Error	Vsci1err
\$FFE0:FFE1	SPI1	Vspi1
\$FFE2:FFE3	TPM2 Overflow	Vtpm2ovf
\$FFE4:FFE5	TPM2 Channel 1	Vtpm2ch1
\$FFE6:FFE7	TPM2 Channel 0	Vtpm2ch0
\$FFE8:FFE9	TPM1 Overflow	Vtpm1ovf
\$FFEA:FFEB	TPM1 Channel 5	Vtpm1ch5
\$FFEC:FFED	TPM1 Channel 4	Vtpm1ch4
\$FFEE:FFEF	TPM1 Channel 3	Vtpm1ch3
\$FFF0:FFF1	TPM1 Channel 2	Vtpm1ch2
\$FFF2:FFF3	TPM1 Channel 1	Vtpm1ch1
\$FFF4:FFF5	TPM1 Channel 0	Vtpm1ch0
\$FFF6:FFF7	ICG	Vicg
\$FFF8:FFF9	Low Voltage Detect	Vlvd
\$FFFA:FFFB	IRQ	Virq
\$FFFC:FFFD	SWI	Vswi
\$FFFE:FFFF	Reset	Vreset

Table	4-1.	Reset	and	Interrupt	Vectors
abio			ana	monap	



High-page registers, shown in Table 4-3, are accessed much less often than other I/O and control registers so they have been located outside the direct addressable memory space, starting at \$1800.

Address	Register Name	Bit 7	6	5	4	3	2	1	Bit 0
\$1800	SRS	POR	PIN	COP	ILOP	0	ICG	LVD	0
\$1801	SBDFR	0	0	0	0	0	0	0	BDFR
\$1802	SOPT	COPE	COPT	STOPE	—	0	0	—	—
\$1803	SMCLK	0	0	0	MPE	0		MCSEL	
\$1804 — \$1805	Reserved	_	_	_	_	_	_	_	_
\$1806	SDIDH	REV3	REV2	REV1	REV0	ID11	ID10	ID9	ID8
\$1807	SDIDL	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
\$1808	SRTISC	RTIF	RTIACK	RTICLKS	RTIE	0	RTIS2	RTIS1	RTIS0
\$1809	SPMSC1	LVDF	LVDACK	LVDIE	LVDRE	LVDSE	LVDE	0 ¹	BGBE
\$180A	SPMSC2	LVWF	LVWACK	LVDV	LVWV	PPDF	PPDACK	_	PPDC
\$180B– \$180F	Reserved	_	_		_	_	_	_	_
\$1810	DBGCAH	Bit 15	14	13	12	11	10	9	Bit 8
\$1811	DBGCAL	Bit 7	6	5	4	3	2	1	Bit 0
\$1812	DBGCBH	Bit 15	14	13	12	11	10	9	Bit 8
\$1813	DBGCBL	Bit 7	6	5	4	3	2	1	Bit 0
\$1814	DBGFH	Bit 15	14	13	12	11	10	9	Bit 8
\$1815	DBGFL	Bit 7	6	5	4	3	2	1	Bit 0
\$1816	DBGC	DBGEN	ARM	TAG	BRKEN	RWA	RWAEN	RWB	RWBEN
\$1817	DBGT	TRGSEL	BEGIN	0	0	TRG3	TRG2	TRG1	TRG0
\$1818	DBGS	AF	BF	ARMF	0	CNT3	CNT2	CNT1	CNT0
\$1819– \$181F	Reserved	_	_		_	_	_	_	_
\$1820	FCDIV	DIVLD	PRDIV8	DIV5	DIV4	DIV3	DIV2	DIV1	DIV0
\$1821	FOPT	KEYEN	FNORED	0	0	0	0	SEC01	SEC00
\$1822	Reserved		—	_	—	—		—	—
\$1823	FCNFG	0	0	KEYACC	0	0	0	0	0
\$1824	FPROT	FPS7	FPS6	FPS5	FPS4	FPS3	FPS2	FPS1	FPDIS
\$1825	FSTAT	FCBEF	FCCF	FPVIOL	FACCERR	0	FBLANK	0	0
\$1826	FCMD	FCMD7	FCMD6	FCMD5	FCMD4	FCMD3	FCMD2	FCMD1	FCMD0
\$1827– \$183F	Reserved	_	_		_	_	_	_	_
\$1840	PTAPE	PTAPE7	PTAPE6	PTAPE5	PTAPE4	PTAPE3	PTAPE2	PTAPE1	PTAPE0
\$1841	PTASE	PTASE7	PTASE6	PTASE5	PTASE4	PTASE3	PTASE2	PTASE1	PTASE0
\$1842	PTADS	PTADS7	PTADS6	PTADS5	PTADS4	PTADS3	PTADS2	PTADS1	PTADS0
\$1843	Reserved	—	—	—	—	—	—	—	—
\$1844	PTBPE	PTBPE7	PTBPE6	PTBPE5	PTBPE4	PTBPE3	PTBPE2	PTBPE1	PTBPE0
\$1845	PTBSE	PTBSE7	PTBSE6	PTBSE5	PTBSE4	PTBSE3	PTBSE2	PTBSE1	PTBSE0

Table 4-3. High-Page Register Summary (Sheet 1 of 2)

SEC01:SEC00	Description
0:0	secure
0:1	secure
1:0	unsecured
1:1	secure

Table 4-9. Security States

SEC01:SEC00 changes to 1:0 after successful backdoor key entry or a successful blank check of FLASH.

4.6.3 FLASH Configuration Register (FCNFG)

Bits 7 through 5 may be read or written at any time. Bits 4 through 0 always read 0 and cannot be written.



Figure 4-8. FLASH Configuration Register (FCNFG)

Table 4-10	. FCNFG	Register	Field	Descriptions
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Field	Description
5 KEYACC	 Enable Writing of Access Key — This bit enables writing of the backdoor comparison key. For more detailed information about the backdoor key mechanism, refer to Section 4.5, "Security." 0 Writes to \$FFB0-\$FFB7 are interpreted as the start of a FLASH programming or erase command. 1 Writes to NVBACKKEY (\$FFB0-\$FFB7) are interpreted as comparison key writes.



Chapter 5 Resets, Interrupts, and System Configuration

5.9.7 System Real-Time Interrupt Status and Control Register (SRTISC)

This register contains one read-only status flag, one write-only acknowledge bit, three read/write delay selects, and three unimplemented bits, which always read 0.



Figure 5-9. System RTI Status and Control Register (SRTISC)

Field	Description
7 RTIF	 Real-Time Interrupt Flag — This read-only status bit indicates the periodic wakeup timer has timed out. 0 Periodic wakeup timer not timed out. 1 Periodic wakeup timer timed out.
6 RTIACK	Real-Time Interrupt Acknowledge — This write-only bit is used to acknowledge real-time interrupt request (write 1 to clear RTIF). Writing 0 has no meaning or effect. Reads always return logic 0.
5 RTICLKS	 Real-Time Interrupt Clock Select — This read/write bit selects the clock source for the real-time interrupt. Real-time interrupt request clock source is internal 1-kHz oscillator. Real-time interrupt request clock source is external clock.
4 RTIE	 Real-Time Interrupt Enable — This read-write bit enables real-time interrupts. 0 Real-time interrupts disabled. 1 Real-time interrupts enabled.
2:0 RTIS[2:0]	Real-Time Interrupt Delay Selects — These read/write bits select the wakeup delay for the RTI. The clock source for the real-time interrupt is a self-clocked source which oscillates at about 1 kHz, is independent of other MCU clock sources. Using external clock source the delays will be crystal frequency divided by value in RTIS2:RTIS1:RTIS0. See Table 5-10.

Table 5-9. SRTISC Register Field Descriptions

Table 5-10. Real-Time Interrupt Frequency

RTIS2:RTIS1:RTIS0	1-kHz Clock Source Delay ¹	Using External Clock Source Delay (Crystal Frequency)
0:0:0	Disable periodic wakeup timer	Disable periodic wakeup timer
0:0:1	8 ms	divide by 256
0:1:0	32 ms	divide by 1024
0:1:1	64 ms	divide by 2048
1:0:0	128 ms	divide by 4096
1:0:1	256 ms	divide by 8192
1:1:0	512 ms	divide by 16384
1:1:1	1.024 s	divide by 32768

¹ Normal values are shown in this column based on f_{RTI} = 1 kHz. See Appendix A, "Electrical Characteristics and Timing Specifications," f_{RTI} for the tolerance on these values.



7.3 Addressing Modes

Addressing modes define the way the CPU accesses operands and data. In the HCS08, all memory, status and control registers, and input/output (I/O) ports share a single 64-Kbyte linear address space so a 16-bit binary address can uniquely identify any memory location. This arrangement means that the same instructions that access variables in RAM can also be used to access I/O and control registers or nonvolatile program space.

Some instructions use more than one addressing mode. For instance, move instructions use one addressing mode to specify the source operand and a second addressing mode to specify the destination address. Instructions such as BRCLR, BRSET, CBEQ, and DBNZ use one addressing mode to specify the location of an operand for a test and then use relative addressing mode to specify the branch destination address when the tested condition is true. For BRCLR, BRSET, CBEQ, and DBNZ, the addressing mode listed in the instruction set tables is the addressing mode needed to access the operand to be tested, and relative addressing mode is implied for the branch destination.

7.3.1 Inherent Addressing Mode (INH)

In this addressing mode, operands needed to complete the instruction (if any) are located within CPU registers so the CPU does not need to access memory to get any operands.

7.3.2 Relative Addressing Mode (REL)

Relative addressing mode is used to specify the destination location for branch instructions. A signed 8-bit offset value is located in the memory location immediately following the opcode. During execution, if the branch condition is true, the signed offset is sign-extended to a 16-bit value and is added to the current contents of the program counter, which causes program execution to continue at the branch destination address.

7.3.3 Immediate Addressing Mode (IMM)

In immediate addressing mode, the operand needed to complete the instruction is included in the object code immediately following the instruction opcode in memory. In the case of a 16-bit immediate operand, the high-order byte is located in the next memory location after the opcode, and the low-order byte is located in the next memory location after that.

7.3.4 Direct Addressing Mode (DIR)

In direct addressing mode, the instruction includes the low-order eight bits of an address in the direct page (0x0000-0x00FF). During execution a 16-bit address is formed by concatenating an implied 0x00 for the high-order half of the address and the direct address from the instruction to get the 16-bit address where the desired operand is located. This is faster and more memory efficient than specifying a complete 16-bit address for the operand.



7.4.5 BGND Instruction

The BGND instruction is new to the HCS08 compared to the M68HC08. BGND would not be used in normal user programs because it forces the CPU to stop processing user instructions and enter the active background mode. The only way to resume execution of the user program is through reset or by a host debug system issuing a GO, TRACE1, or TAGGO serial command through the background debug interface.

Software-based breakpoints can be set by replacing an opcode at the desired breakpoint address with the BGND opcode. When the program reaches this breakpoint address, the CPU is forced to active background mode rather than continuing the user program.



8.4.1 Off Mode (Off)

Normally when the CPU enters stop mode, the ICG will cease all clock activity and is in the off state. However there are two cases to consider when clock activity continues while the CPU is in stop mode,

8.4.1.1 BDM Active

When the BDM is enabled, the ICG continues activity as originally programmed. This allows access to memory and control registers via the BDC controller.

8.4.1.2 OSCSTEN Bit Set

When the oscillator is enabled in stop mode (OSCSTEN = 1), the individual clock generators are enabled but the clock feed to the rest of the MCU is turned off. This option is provided to avoid long oscillator startup times if necessary, or to run the RTI from the oscillator during stop3.

8.4.1.3 Stop/Off Mode Recovery

Upon the CPU exiting stop mode due to an interrupt, the previously set control bits are valid and the system clock feed resumes. If FEE is selected, the ICG will source the internal reference until the external clock is stable. If FBE is selected, the ICG will wait for the external clock to stabilize before enabling ICGOUT.

Upon the CPU exiting stop mode due to a reset, the previously set ICG control bits are ignored and the default reset values applied. Therefore the ICG will exit stop in SCM mode configured for an approximately 8 MHz DCO output (4 MHz bus clock) with trim value maintained. If using a crystal, 4096 clocks are detected prior to engaging ICGERCLK. This is incorporated in crystal start-up time.

8.4.2 Self-Clocked Mode (SCM)

Self-clocked mode (SCM) is the default mode of operation and is entered when any of the following conditions occur:

- After any reset.
- Exiting from off mode when CLKS does not equal 10. If CLKS = X1, the ICG enters this state temporarily until the DCO is stable (DCOS = 1).
- CLKS bits are written from X1 to 00.
- CLKS = 1X and ICGERCLK is not detected (both ERCS = 0 and LOCS = 1).

In this state, the FLL loop is open. The DCO is on, and the output clock signal ICGOUT frequency is given by $f_{ICGDCLK}$ / R. The ICGDCLK frequency can be varied from 8 MHz to 40 MHz by writing a new value into the filter registers (ICGFLTH and ICGFLTL). This is the only mode in which the filter registers can be written.

If this mode is entered due to a reset, $f_{ICGDCLK}$ will default to f_{Self_reset} which is nominally 8 MHz. If this mode is entered from FLL engaged internal, $f_{ICGDCLK}$ will maintain the previous frequency. If this mode is entered from FLL engaged external (either by programming CLKS or due to a loss of external reference clock), $f_{ICGDCLK}$ will maintain the previous frequency, but ICGOUT will double if the FLL was unlocked. If this mode is entered from off mode, $f_{ICGDCLK}$ will be equal to the frequency of ICGDCLK before



CPWMS	MSnB:MSnA	ELSnB:ELSnA	Mode	Configuration	
Х	ХХ	00	Pin not used for TPM channel; use as an external clock for the TPM or revert to general-purpose I/O		
0	00	01	Input capture	Capture on rising edge only	
		10		Capture on falling edge only	
		11		Capture on rising or falling edge	
	01	00	Output	Software compare only	
		01	compare	Toggle output on compare	
10 Clear output on compare		Clear output on compare			
		11		Set output on compare	
	1X	10	Edge-aligned	High-true pulses (clear output on compare)	
		X1	PWM	Low-true pulses (set output on compare)	
1	XX 10	10	Center-aligned	High-true pulses (clear output on compare-up)	
		X1	PWM	Low-true pulses (set output on compare-up)	

Tahle	10-5	Mode	Edge	and I	l evel	Selection
lane	10-5.	woue,	Luye,	anu	LEVEI	Selection

If the associated port pin is not stable for at least two bus clock cycles before changing to input capture mode, it is possible to get an unexpected indication of an edge trigger. Typically, a program would clear status flags after changing channel configuration bits and before enabling channel interrupts or using the status flags to avoid any unexpected behavior.

10.4.5 Timer x Channel Value Registers (TPMxCnVH:TPMxCnVL)

These read/write registers contain the captured TPM counter value of the input capture function or the output compare value for the output compare or PWM functions. The channel value registers are cleared by reset.

_	7	6	5	4	3	2	1	0
R W	Bit 15	14	13	12	11	10	9	Bit 8
Reset	0	0	0	0	0	0	0	0



	7	6	5	4	3	2	1	0
R W	Bit 7	6	5	4	3	2	1	Bit 0
Reset	0	0	0	0	0	0	0	0

Figure 10-10. Timer Channel Value Register Low (TPMxCnVL)

In input capture mode, reading either byte (TPMxCnVH or TPMxCnVL) latches the contents of both bytes into a buffer where they remain latched until the other byte is read. This latching mechanism also resets (becomes unlatched) when the TPMxCnSC register is written.



Field	Description
1 RWU	 Receiver Wakeup Control — This bit can be written to 1 to place the SCI receiver in a standby state where it waits for automatic hardware detection of a selected wakeup condition. The wakeup condition is either an idle line between messages (WAKE = 0, idle-line wakeup), or a logic 1 in the most significant data bit in a character (WAKE = 1, address-mark wakeup). Application software sets RWU and (normally) a selected hardware condition automatically clears RWU. Refer to Section 11.3.3.2, "Receiver Wakeup Operation" for more details. 0 Normal SCI receiver operation. 1 SCI receiver in standby waiting for wakeup condition.
0 SBK	 Send Break — Writing a 1 and then a 0 to SBK queues a break character in the transmit data stream. Additional break characters of 10 or 11 bit times of logic 0 are queued as long as SBK = 1. Depending on the timing of the set and clear of SBK relative to the information currently being transmitted, a second break character may be queued before software clears SBK. Refer to Section 11.3.2.1, "Send Break and Queued Idle" for more details. 0 Normal transmitter operation. 1 Queue break character(s) to be sent.

11.2.4 SCI Status Register 1 (SCIxS1)

This register has eight read-only status flags. Writes have no effect. Special software sequences (which do not involve writing to this register) are used to clear these status flags.



Figure 11-8. SCI Status Register 1 (SCIxS1)

Table 11-5. SCI	xS1 Register	Field Descript	ions
-----------------	--------------	----------------	------

Field	Description
7 TDRE	Transmit Data Register Empty Flag — TDRE is set out of reset and when a transmit data value transfers from the transmit data buffer to the transmit shifter, leaving room for a new character in the buffer. To clear TDRE, read SCIxS1 with TDRE = 1 and then write to the SCI data register (SCIxD). 0 Transmit data register (buffer) full. 1 Transmit data register (buffer) empty.
6 TC	 Transmission Complete Flag — TC is set out of reset and when TDRE = 1 and no data, preamble, or break character is being transmitted. 0 Transmitter active (sending data, a preamble, or a break). 1 Transmitter idle (transmission activity complete). TC is cleared automatically by reading SCIxS1 with TC = 1 and then doing one of the following three things: Write to the SCI data register (SCIxD) to transmit new data Queue a preamble by changing TE from 0 to 1 Queue a break character by writing 1 to SBK in SCIxC2



Field	Description
5 RDRF	Receive Data Register Full Flag — RDRF becomes set when a character transfers from the receive shifter into the receive data register (SCIxD). In 8-bit mode, to clear RDRF, read SCIxS1 with RDRF = 1 and then read the SCI data register (SCIxD). In 9-bit mode, to clear RDRF, read SCIxS1 with RDRF = 1 and then read SCIxD and the SCI control 3 register (SCIxC3). SCIxD and SCIxC3 can be read in any order, but the flag is cleared only after both data registers are read. 0 Receive data register full.
4 IDLE	Idle Line Flag — IDLE is set when the SCI receive line becomes idle for a full character time after a period of activity. When ILT = 0, the receiver starts counting idle bit times after the start bit. So if the receive character is all 1s, these bit times and the stop bit time count toward the full character time of logic high (10 or 11 bit times depending on the M control bit) needed for the receiver to detect an idle line. When ILT = 1, the receiver doesn't start counting idle bit times until after the stop bit. So the stop bit and any logic high bit times at the end of the previous character do not count toward the full character time of logic high needed for the receiver to detect an idle line. To clear IDLE, read SCIxS1 with IDLE = 1 and then read the SCI data register (SCIxD). After IDLE has been cleared, it cannot become set again until after a new character has been received and RDRF has been set. IDLE will get set only once even if the receive line remains idle for an extended period. 0 No idle line was detected.
3 OR	 Receiver Overrun Flag — OR is set when a new serial character is ready to be transferred to the receive data register (buffer), but the previously received character has not been read from SCIxD yet. In this case, the new character (and all associated error information) is lost because there is no room to move it into SCIxD. To clear OR, read SCIxS1 with OR = 1 and then read the SCI data register (SCIxD). 0 No overrun. 1 Receive overrun (new SCI data lost).
2 NF	 Noise Flag — The advanced sampling technique used in the receiver takes seven samples during the start bit and three samples in each data bit and the stop bit. If any of these samples disagrees with the rest of the samples within any bit time in the frame, the flag NF will be set at the same time as the flag RDRF gets set for the character. To clear NF, read SCIxS1 and then read the SCI data register (SCIxD). 0 No noise detected. 1 Noise detected in the received character in SCIxD.
1 FE	 Framing Error Flag — FE is set at the same time as RDRF when the receiver detects a logic 0 where the stop bit was expected. This suggests the receiver was not properly aligned to a character frame. To clear FE, read SCIxS1 with FE = 1 and then read the SCI data register (SCIxD). 0 No framing error detected. This does not guarantee the framing is correct. 1 Framing error.
0 PF	 Parity Error Flag — PF is set at the same time as RDRF when parity is enabled (PE = 1) and the parity bit in the received character does not agree with the expected parity value. To clear PF, read SCIxS1 and then read the SCI data register (SCIxD). 0 No parity error. 1 Parity error.



Field	Description
7 SPRF	 SPI Read Buffer Full Flag — SPRF is set at the completion of an SPI transfer to indicate that received data may be read from the SPI data register (SPI1D). SPRF is cleared by reading SPRF while it is set, then reading the SPI data register. No data available in the receive data buffer Data available in the receive data buffer
5 SPTEF	SPI Transmit Buffer Empty Flag — This bit is set when there is room in the transmit data buffer. It is cleared by reading SPI1S with SPTEF set, followed by writing a data value to the transmit buffer at SPI1D. SPI1S must be read with SPTEF = 1 before writing data to SPI1D or the SPI1D write will be ignored. SPTEF generates an SPTEF CPU interrupt request if the SPTIE bit in the SPI1C1 is also set. SPTEF is automatically set when a data byte transfers from the transmit buffer into the transmit shift register. For an idle SPI (no data in the transmit buffer or the shift register and no transfer in progress), data written to SPI1D is transferred to the shifter almost immediately so SPTEF is set within two bus cycles allowing a second 8-bit data value to be queued into the transmit buffer. After completion of the transfer of the value in the shift register, the queued value from the transmit buffer. If no new data is waiting in the transmit buffer, SPTEF simply remains set and no data moves from the buffer to the shifter.
4 MODF	Master Mode Fault Flag — MODF is set if the SPI is configured as a master and the slave select input goes low, indicating some other SPI device is also configured as a master. The \overline{SS} pin acts as a mode fault error input only when MSTR = 1, MODFEN = 1, and SSOE = 0; otherwise, MODF will never be set. MODF is cleared by reading MODF while it is 1, then writing to SPI control register 1 (SPI1C1). 0 No mode fault error 1 Mode fault error detected

12.3.5 SPI Data Register (SPI1D)

	7	6	5	4	3	2	1	0
R W	Bit 7	6	5	4	3	2	1	Bit 0
Reset	0	0	0	0	0	0	0	0

Figure 12-9. SPI Data Register (SPI1D)

Reads of this register return the data read from the receive data buffer. Writes to this register write data to the transmit data buffer. When the SPI is configured as a master, writing data to the transmit data buffer initiates an SPI transfer.

Data should not be written to the transmit data buffer unless the SPI transmit buffer empty flag (SPTEF) is set, indicating there is room in the transmit buffer to queue a new transmit byte.

Data may be read from SPI1D any time after SPRF is set and before another transfer is finished. Failure to read the data out of the receive data buffer before a new transfer ends causes a receive overrun condition and the data from the new transfer is lost.



Chapter 13 Inter-Integrated Circuit (S08IICV1)

13.1 Introduction

The MC9S08AW60 Series of microcontrollers has an inter-integrated circuit (IIC) module for communication with other integrated circuits. The two pins associated with this module, SCL and SDA, are open-drain outputs and are shared with port C pins 0 and 1, respectively.



Appendix A Electrical Characteristics and Timing Specifications

Solving equations 1 and 2 for K gives:

$$K = P_D \times (T_A + 273^{\circ}C) + \theta_{JA} \times (P_D)^2 \qquad \qquad Eqn. A-3$$

where K is a constant pertaining to the particular part. K can be determined from equation 3 by measuring P_D (at equilibrium) for a known T_A . Using this value of K, the values of P_D and T_J can be obtained by solving equations 1 and 2 iteratively for any value of T_A .

A.5 ESD Protection and Latch-Up Immunity

Although damage from electrostatic discharge (ESD) is much less common on these devices than on early CMOS circuits, normal handling precautions should be used to avoid exposure to static discharge. Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage.

All ESD testing is in conformity with AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits. During the device qualification ESD stresses were performed for the Human Body Model (HBM), the Machine Model (MM) and the Charge Device Model (CDM).

A device is defined as a failure if after exposure to ESD pulses the device no longer meets the device specification. Complete DC parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

Model	Description	Symbol	Value	Unit
Liver en De du	Series Resistance	R1	1500	Ω
Model	Storage Capacitance	С	100	pF
	Number of Pulse per pin	_	3	
	Series Resistance	R1	0	Ω
Machine Model	Storage Capacitance	С	200	pF
	Number of Pulse per pin	_	3	
Latch-Un	Minimum input voltage limit		-2.5	V
	Maximum input voltage limit		7.5	V

Table A-4. ESD and Latch-up Test Conditions

Table A-5	. ESD a	ind Latch	-Up	Protection	Characteristics
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Num	С	Rating	Symbol	Min	Max	Unit
1	С	Human Body Model (HBM)	V _{HBM}	± 2000	—	V
2	С	Machine Model (MM)	V _{MM}	± 200	—	V
3	С	Charge Device Model (CDM)	V _{CDM}	± 500	—	V
4	С	Latch-up Current at $T_A = 125^{\circ}C$	I _{LAT}	± 100	_	mA



Appendix A Electrical Characteristics and Timing Specifications





