

Welcome to E-XFL.COM

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	S08
Core Size	8-Bit
Speed	40MHz
Connectivity	I ² C, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	38
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	48-VQFN Exposed Pad
Supplier Device Package	48-QFN-EP (7x7)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=s9s08aw16ae0mft

Table 1-3 lists the functional versions of the on-chip modules.

Table 1-3. Versions of On-Chip Modules

Module	Version
Analog-to-Digital Converter (S08ADC10)	1
Internal Clock Generator (S08ICG)	4
Inter-Integrated Circuit (S08IIC)	1
Keyboard Interrupt (S08KBI)	1
Serial Communications Interface (S08SCI)	2
Serial Peripheral Interface (S08SPI)	3
Timer Pulse-Width Modulator (S08TPM)	2
Central Processing Unit (S08CPU)	2
Debug Module (DBG)	2

1.3 System Clock Distribution

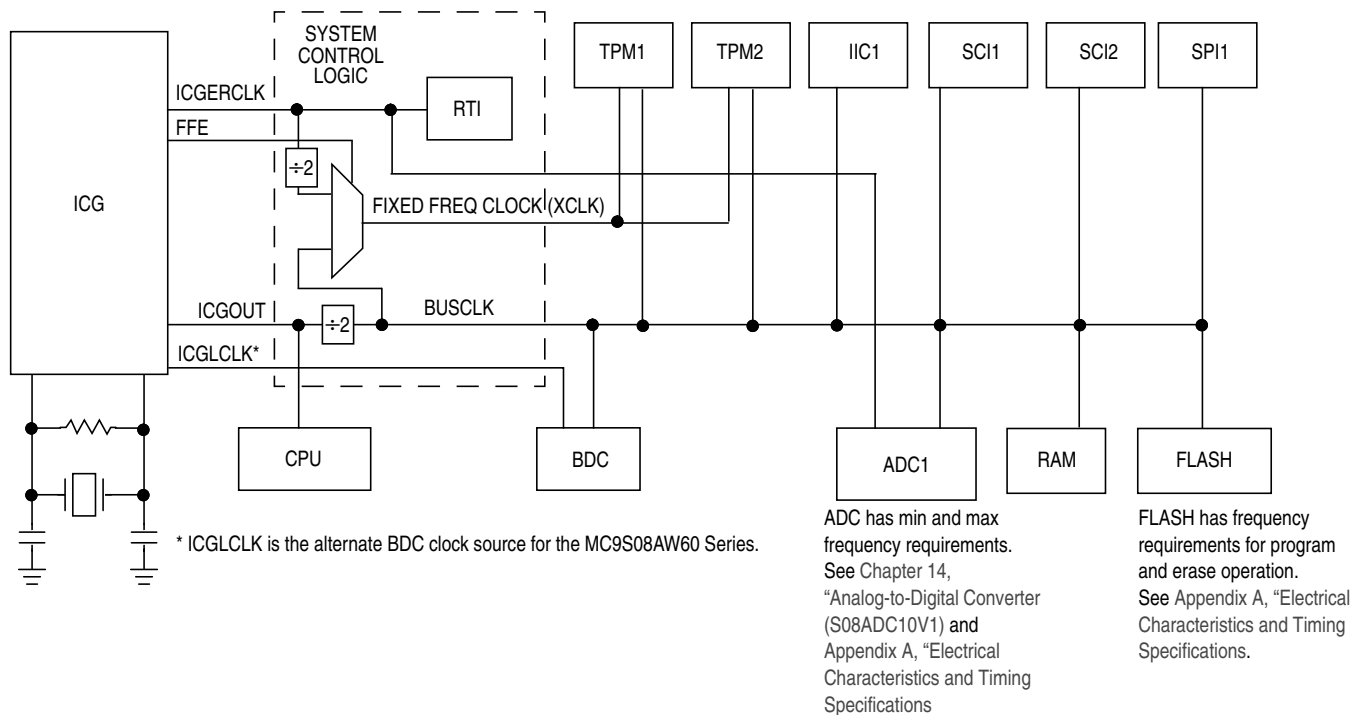


Figure 1-2. System Clock Distribution Diagram

Some of the modules inside the MCU have clock source choices. Figure 1-2 shows a simplified clock connection diagram. The ICG supplies the clock sources:

- ICGOUT is an output of the ICG module. It is one of the following:
 - The external crystal oscillator
 - An external clock source

- The output of the digitally-controlled oscillator (DCO) in the frequency-locked loop sub-module
- Control bits inside the ICG determine which source is connected.
- FFE is a control signal generated inside the ICG. If the frequency of ICGOUT $> 4 \times$ the frequency of ICGERCLK, this signal is a logic 1 and the fixed-frequency clock will be ICGERCLK/2. Otherwise the fixed-frequency clock will be BUSCLK.
- ICGLCLK — Development tools can select this internal self-clocked source (~ 8 MHz) to speed up BDC communications in systems where the bus clock is slow.
- ICGERCLK — External reference clock can be selected as the real-time interrupt clock source. Can also be used as the ALTCLK input to the ADC module.

High-page registers, shown in Table 4-3, are accessed much less often than other I/O and control registers so they have been located outside the direct addressable memory space, starting at \$1800.

Table 4-3. High-Page Register Summary (Sheet 1 of 2)

Address	Register Name	Bit 7	6	5	4	3	2	1	Bit 0
\$1800	SRS	POR	PIN	COP	ILOP	0	ICG	LVD	0
\$1801	SBD FR	0	0	0	0	0	0	0	BDFR
\$1802	SOPT	COPE	COPT	STOPE	—	0	0	—	—
\$1803	SMCLK	0	0	0	MPE	0	MCSEL		
\$1804 – \$1805	Reserved	—	—	—	—	—	—	—	—
\$1806	SDIDH	REV3	REV2	REV1	REV0	ID11	ID10	ID9	ID8
\$1807	SDIDL	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
\$1808	SRTISC	RTIF	RTIACK	RTICLKS	RTIE	0	RTIS2	RTIS1	RTIS0
\$1809	SPMSC1	LVDF	LVDACK	LVDIE	LVDRE	LVDSE	LVDE	0 ¹	BGBE
\$180A	SPMSC2	LVWF	LVWACK	LVDV	LVWV	PPDF	PPDACK	—	PPDC
\$180B – \$180F	Reserved	—	—	—	—	—	—	—	—
\$1810	DBGCAH	Bit 15	14	13	12	11	10	9	Bit 8
\$1811	DBGCAL	Bit 7	6	5	4	3	2	1	Bit 0
\$1812	DBGCBH	Bit 15	14	13	12	11	10	9	Bit 8
\$1813	DBGCBL	Bit 7	6	5	4	3	2	1	Bit 0
\$1814	DBGFH	Bit 15	14	13	12	11	10	9	Bit 8
\$1815	DBGFL	Bit 7	6	5	4	3	2	1	Bit 0
\$1816	DBG C	DBGEN	ARM	TAG	BRKEN	RWA	RWAEN	RWB	RWBEN
\$1817	DBG T	TRGSEL	BEGIN	0	0	TRG3	TRG2	TRG1	TRG0
\$1818	DBG S	AF	BF	ARMF	0	CNT3	CNT2	CNT1	CNT0
\$1819 – \$181F	Reserved	—	—	—	—	—	—	—	—
\$1820	FCDIV	DIVLD	PRDIV8	DIV5	DIV4	DIV3	DIV2	DIV1	DIV0
\$1821	FOPT	KEYEN	FNORED	0	0	0	0	SEC01	SEC00
\$1822	Reserved	—	—	—	—	—	—	—	—
\$1823	FCNFG	0	0	KEYACC	0	0	0	0	0
\$1824	FPROT	FPS7	FPS6	FPS5	FPS4	FPS3	FPS2	FPS1	FPDIS
\$1825	FSTAT	FCBEF	FCCF	FPVIOL	FACCERR	0	FBLANK	0	0
\$1826	FCMD	FCMD7	FCMD6	FCMD5	FCMD4	FCMD3	FCMD2	FCMD1	FCMD0
\$1827 – \$183F	Reserved	—	—	—	—	—	—	—	—
\$1840	PTAPE	PTAPE7	PTAPE6	PTAPE5	PTAPE4	PTAPE3	PTAPE2	PTAPE1	PTAPE0
\$1841	PTASE	PTASE7	PTASE6	PTASE5	PTASE4	PTASE3	PTASE2	PTASE1	PTASE0
\$1842	PTADS	PTADS7	PTADS6	PTADS5	PTADS4	PTADS3	PTADS2	PTADS1	PTADS0
\$1843	Reserved	—	—	—	—	—	—	—	—
\$1844	PTBPE	PTBPE7	PTBPE6	PTBPE5	PTBPE4	PTBPE3	PTBPE2	PTBPE1	PTBPE0
\$1845	PTBSE	PTBSE7	PTBSE6	PTBSE5	PTBSE4	PTBSE3	PTBSE2	PTBSE1	PTBSE0

4.4.1 Features

Features of the FLASH memory include:

- FLASH Size
 - MC9S08AW60 — 63280 bytes (124 pages of 512 bytes each)
 - MC9S08AW48 — 49152 bytes (96 pages of 512 bytes each)
 - MC9S08AW32 — 32768 bytes (64 pages of 512 bytes each)
 - MC9S08AW16 — 16384 bytes (32 pages of 512 bytes each)
- Single power supply program and erase
- Command interface for fast program and erase operation
- Up to 100,000 program/erase cycles at typical voltage and temperature
- Flexible block protection
- Security feature for FLASH and RAM
- Auto power-down for low-frequency read accesses

4.4.2 Program and Erase Times

Before any program or erase command can be accepted, the FLASH clock divider register (FCDIV) must be written to set the internal clock for the FLASH module to a frequency (f_{FCLK}) between 150 kHz and 200 kHz (see Section 4.6.1, “FLASH Clock Divider Register (FCDIV)”). This register can be written only once, so normally this write is done during reset initialization. FCDIV cannot be written if the access error flag, FACCERR in FSTAT, is set. The user must ensure that FACCERR is not set before writing to the FCDIV register. One period of the resulting clock ($1/f_{FCLK}$) is used by the command processor to time program and erase pulses. An integer number of these timing pulses are used by the command processor to complete a program or erase command.

Table 4-5 shows program and erase times. The bus clock frequency and FCDIV determine the frequency of FCLK (f_{FCLK}). The time for one cycle of FCLK is $t_{FCLK} = 1/f_{FCLK}$. The times are shown as a number of cycles of FCLK and as an absolute time for the case where $t_{FCLK} = 5 \mu\text{s}$. Program and erase times shown include overhead for the command state machine and enabling and disabling of program and erase voltages.

Table 4-5. Program and Erase Times

Parameter	Cycles of FCLK	Time if FCLK = 200 kHz
Byte program	9	45 μs
Byte program (burst)	4	20 μs ¹
Page erase	4000	20 ms ²
Mass erase	20,000	100 ms ²

¹ Excluding start/end overhead

² Because the page and mass erase times can be longer than the COP watchdog timeout, the COP should be serviced during any software erase routine.

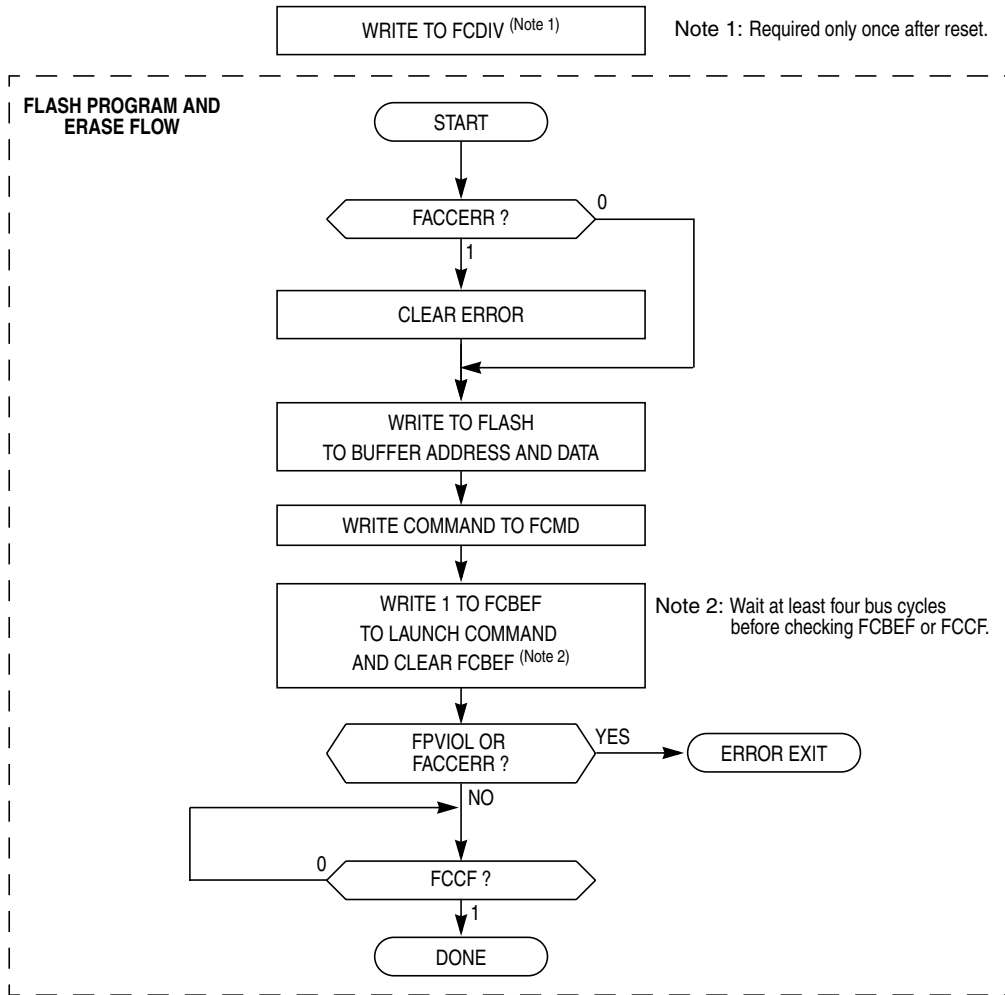


Figure 4-3. FLASH Program and Erase Flowchart

4.4.4 Burst Program Execution

The burst program command is used to program sequential bytes of data in less time than would be required using the standard program command. This is possible because the high voltage to the FLASH array does not need to be disabled between program operations. Ordinarily, when a program or erase command is issued, an internal charge pump associated with the FLASH memory must be enabled to supply high voltage to the array. Upon completion of the command, the charge pump is turned off. When a burst program command is issued, the charge pump is enabled and then remains enabled after completion of the burst program operation if these two conditions are met:

- The next burst program command has been queued before the current program operation has completed.
- The next sequential address selects a byte on the same physical row as the current byte being programmed. A row of FLASH memory consists of 64 bytes. A byte within a row is selected by addresses A5 through A0. A new row begins when addresses A5 through A0 are all zero.

4.6 FLASH Registers and Control Bits

The FLASH module has nine 8-bit registers in the high-page register space, three locations in the nonvolatile register space in FLASH memory which are copied into three corresponding high-page control registers at reset. There is also an 8-byte comparison key in FLASH memory. Refer to Table 4-3 and Table 4-4 for the absolute address assignments for all FLASH registers. This section refers to registers and control bits only by their names. A Freescale-provided equate or header file normally is used to translate these names into the appropriate absolute addresses.

4.6.1 FLASH Clock Divider Register (FCDIV)

Bit 7 of this register is a read-only status flag. Bits 6 through 0 may be read at any time but can be written only one time. Before any erase or programming operations are possible, write to this register to set the frequency of the clock for the nonvolatile memory system within acceptable limits.

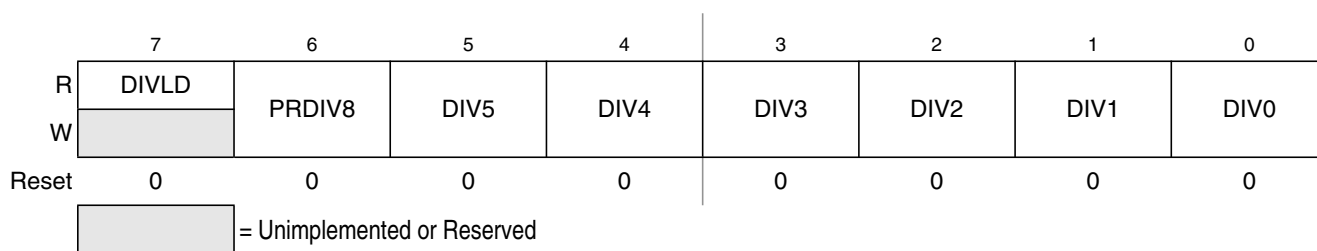


Figure 4-6. FLASH Clock Divider Register (FCDIV)

Table 4-6. FCDIV Register Field Descriptions

Field	Description
7 DIVLD	<p>Divisor Loaded Status Flag — When set, this read-only status flag indicates that the FCDIV register has been written since reset. Reset clears this bit and the first write to this register causes this bit to become set regardless of the data written.</p> <p>0 FCDIV has not been written since reset; erase and program operations disabled for FLASH. 1 FCDIV has been written since reset; erase and program operations enabled for FLASH.</p>
6 PRDIV8	<p>Prescale (Divide) FLASH Clock by 8</p> <p>0 Clock input to the FLASH clock divider is the bus rate clock. 1 Clock input to the FLASH clock divider is the bus rate clock divided by 8.</p>
5:0 DIV[5:0]	<p>Divisor for FLASH Clock Divider — The FLASH clock divider divides the bus rate clock (or the bus rate clock divided by 8 if PRDIV8 = 1) by the value in the 6-bit DIV5:DIV0 field plus one. The resulting frequency of the internal FLASH clock must fall within the range of 200 kHz to 150 kHz for proper FLASH operations. Program/Erase timing pulses are one cycle of this internal FLASH clock which corresponds to a range of 5 μs to 6.7 μs. The automated programming logic uses an integer number of these pulses to complete an erase or program operation. See Equation 4-1, Equation 4-2, and Table 4-6.</p>

$$\text{if PRDIV8} = 0 \text{ — } f_{\text{CLK}} = f_{\text{Bus}} \div ([\text{DIV5:DIV0}] + 1) \tag{Eqn. 4-1}$$

$$\text{if PRDIV8} = 1 \text{ — } f_{\text{CLK}} = f_{\text{Bus}} \div (8 \times ([\text{DIV5:DIV0}] + 1)) \tag{Eqn. 4-2}$$

Table 4-7 shows the appropriate values for PRDIV8 and DIV5:DIV0 for selected bus frequencies.

- Illegal opcode detect
- Background debug forced reset
- The reset pin ($\overline{\text{RESET}}$)
- Clock generator loss of lock and loss of clock reset

Each of these sources, with the exception of the background debug forced reset, has an associated bit in the system reset status register. Whenever the MCU enters reset, the internal clock generator (ICG) module switches to self-clocked mode with the frequency of $f_{\text{Self_reset}}$ selected. The reset pin is driven low for 34 bus cycles where the internal bus frequency is half the ICG frequency. After the 34 bus cycles are completed, the pin is released and will be pulled up by the internal pullup resistor, unless it is held low externally. After the pin is released, it is sampled after another 38 bus cycles to determine whether the reset pin is the cause of the MCU reset.

5.4 Computer Operating Properly (COP) Watchdog

The COP watchdog is intended to force a system reset when the application software fails to execute as expected. To prevent a system reset from the COP timer (when it is enabled), application software must reset the COP timer periodically. If the application program gets lost and fails to reset the COP before it times out, a system reset is generated to force the system back to a known starting point. The COP watchdog is enabled by the COPE bit in SOPT (see Section 5.9.4, “System Options Register (SOPT)” for additional information). The COP timer is reset by writing any value to the address of SRS. This write does not affect the data in the read-only SRS. Instead, the act of writing to this address is decoded and sends a reset signal to the COP timer.

After any reset, the COP timer is enabled. This provides a reliable way to detect code that is not executing as intended. If the COP watchdog is not used in an application, it can be disabled by clearing the COPE bit in the write-once SOPT register. Also, the COPT bit can be used to choose one of two timeout periods (2^{18} or 2^{13} cycles of the bus rate clock). Even if the application will use the reset default settings in COPE and COPT, the user should write to write-once SOPT during reset initialization to lock in the settings. That way, they cannot be changed accidentally if the application program gets lost.

The write to SRS that services (clears) the COP timer should not be placed in an interrupt service routine (ISR) because the ISR could continue to be executed periodically even if the main application program fails.

When the MCU is in active background mode, the COP timer is temporarily disabled.

5.5 Interrupts

Interrupts provide a way to save the current CPU status and registers, execute an interrupt service routine (ISR), and then restore the CPU status so processing resumes where it left off before the interrupt. Other than the software interrupt (SWI), which is a program instruction, interrupts are caused by hardware events such as an edge on the IRQ pin or a timer-overflow event. The debug module can also generate an SWI under certain circumstances.

If an event occurs in an enabled interrupt source, an associated read-only status flag will become set. The CPU will not respond until and unless the local interrupt enable is a logic 1 to enable the interrupt. The

6.7.6 Port C Pin Control Registers (PTCPE, PTCSE, PTCDS)

In addition to the I/O control, port C pins are controlled by the registers listed below.

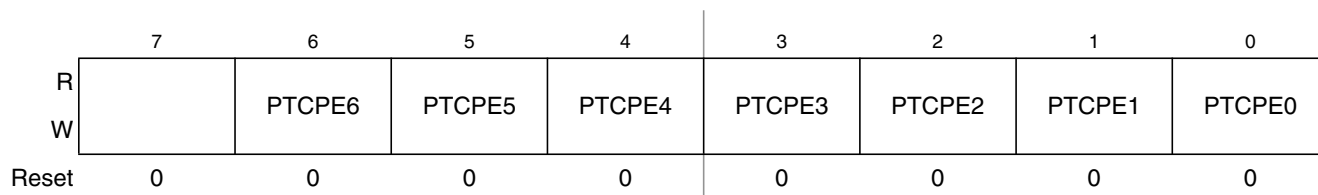


Figure 6-21. Internal Pullup Enable for Port C (PTCPE)

Table 6-14. PTCPE Register Field Descriptions

Field	Description
6:0 PTCPE[6:0]	Internal Pullup Enable for Port C Bits — Each of these control bits determines if the internal pullup device is enabled for the associated PTC pin. For port C pins that are configured as outputs, these bits have no effect and the internal pullup devices are disabled. 0 Internal pullup device disabled for port C bit n. 1 Internal pullup device enabled for port C bit n.

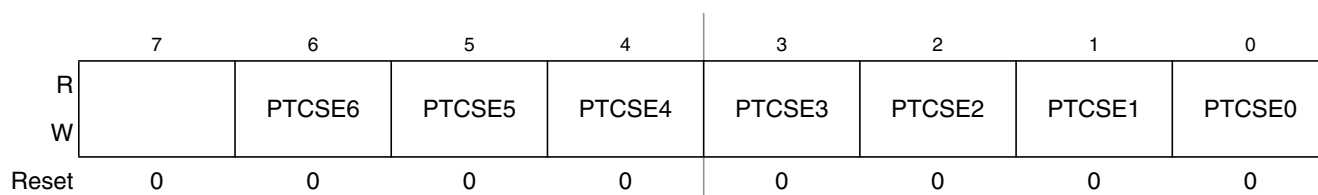


Figure 6-22. Output Slew Rate Control Enable for Port C (PTCSE)

Table 6-15. PTCSE Register Field Descriptions

Field	Description
6:0 PTCSE[6:0]	Output Slew Rate Control Enable for Port C Bits — Each of these control bits determine whether output slew rate control is enabled for the associated PTC pin. For port C pins that are configured as inputs, these bits have no effect. 0 Output slew rate control disabled for port C bit n. 1 Output slew rate control enabled for port C bit n.

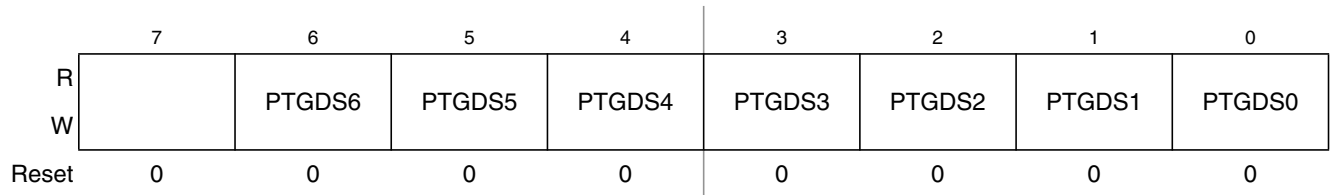


Figure 6-43. Output Drive Strength Selection for Port G (PTGDS)

Table 6-36. PTGDS Register Field Descriptions

Field	Description
6:0 PTGDS[6:0]	<p>Output Drive Strength Selection for Port G Bits — Each of these control bits selects between low and high output drive for the associated PTG pin.</p> <p>0 Low output drive enabled for port G bit n.</p> <p>1 High output drive enabled for port G bit n.</p>

7.2 Programmer's Model and CPU Registers

Figure 7-1 shows the five CPU registers. CPU registers are not part of the memory map.

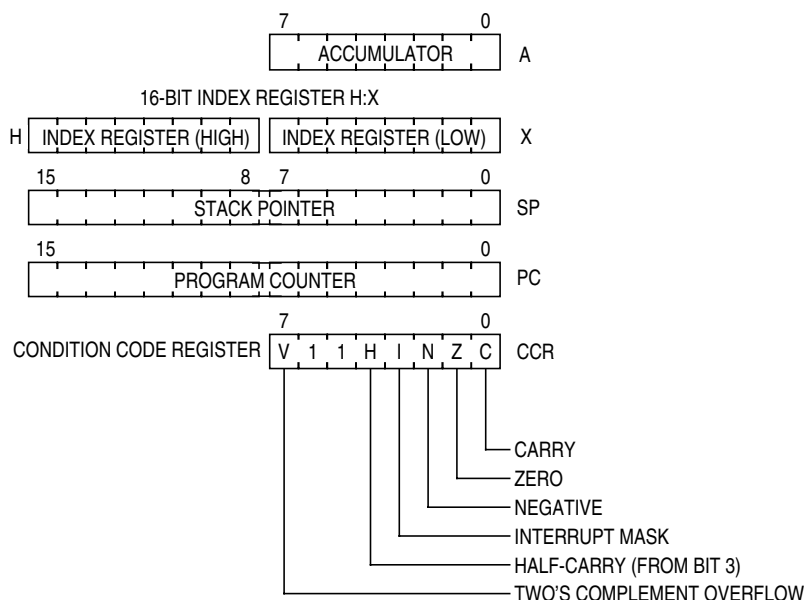


Figure 7-1. CPU Registers

7.2.1 Accumulator (A)

The A accumulator is a general-purpose 8-bit register. One operand input to the arithmetic logic unit (ALU) is connected to the accumulator and the ALU results are often stored into the A accumulator after arithmetic and logical operations. The accumulator can be loaded from memory using various addressing modes to specify the address where the loaded data comes from, or the contents of A can be stored to memory using various addressing modes to specify the address where data from A will be stored.

Reset has no effect on the contents of the A accumulator.

7.2.2 Index Register (H:X)

This 16-bit register is actually two separate 8-bit registers (H and X), which often work together as a 16-bit address pointer where H holds the upper byte of an address and X holds the lower byte of the address. All indexed addressing mode instructions use the full 16-bit value in H:X as an index reference pointer; however, for compatibility with the earlier M68HC05 family, some instructions operate only on the low-order 8-bit half (X).

Many instructions treat X as a second general-purpose 8-bit register that can be used to hold 8-bit data values. X can be cleared, incremented, decremented, complemented, negated, shifted, or rotated. Transfer instructions allow data to be transferred from A or transferred to A where arithmetic and logical operations can then be performed.

For compatibility with the earlier M68HC05 family, H is forced to 0x00 during reset. Reset has no effect on the contents of X.

Table 8-12. MFD and RFD Decode Table

101	14	101	÷32
110	16	110	÷64
111	18	111	÷128

8.5.2 Example #1: External Crystal = 32 kHz, Bus Frequency = 4.19 MHz

In this example, the FLL will be used (in FEE mode) to multiply the external 32 kHz oscillator up to 8.38 MHz to achieve 4.19 MHz bus frequency.

After the MCU is released from reset, the ICG is in self-clocked mode (SCM) and supplies approximately 8 MHz on ICGOUT, which corresponds to a 4 MHz bus frequency (f_{Bus}).

The clock scheme will be FLL engaged, external (FEE). So

$$f_{\text{ICGOUT}} = f_{\text{ext}} * P * N / R ; P = 64, f_{\text{ext}} = 32 \text{ kHz} \quad \text{Eqn. 8-1}$$

Solving for N / R gives:

$$N / R = 8.38 \text{ MHz} / (32 \text{ kHz} * 64) = 4 ; \text{ we can choose } N = 4 \text{ and } R = 1 \quad \text{Eqn. 8-2}$$

The values needed in each register to set up the desired operation are:

ICGC1 = \$38 (%00111000)

Bit 7	HGO	0	Configures oscillator for low power
Bit 6	RANGE	0	Configures oscillator for low-frequency range; FLL prescale factor is 64
Bit 5	REFS	1	Oscillator using crystal or resonator is requested
Bits 4:3	CLKS	11	FLL engaged, external reference clock mode
Bit 2	OSCSTEN	0	Oscillator disabled
Bit 1	LOCD	0	Loss-of-clock detection enabled
Bit 0		0	Unimplemented or reserved, always reads zero

ICGC2 = \$00 (%00000000)

Bit 7	LOLRE	0	Generates an interrupt request on loss of lock
Bits 6:4	MFD	000	Sets the MFD multiplication factor to 4
Bit 3	LOCRES	0	Generates an interrupt request on loss of clock
Bits 2:0	RFD	000	Sets the RFD division factor to ÷1

ICGS1 = \$xx

This is read only except for clearing interrupt flag

ICGS2 = \$xx

This is read only; should read DCOS = 1 before performing any time critical tasks

ICGFLTLU/L = \$xx

Only needed in self-clocked mode; FLT will be adjusted by loop to give 8.38 MHz DCO clock
 Bits 15:12 unused 0000

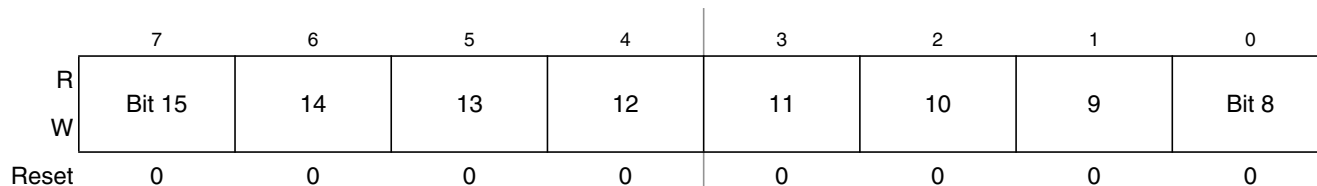
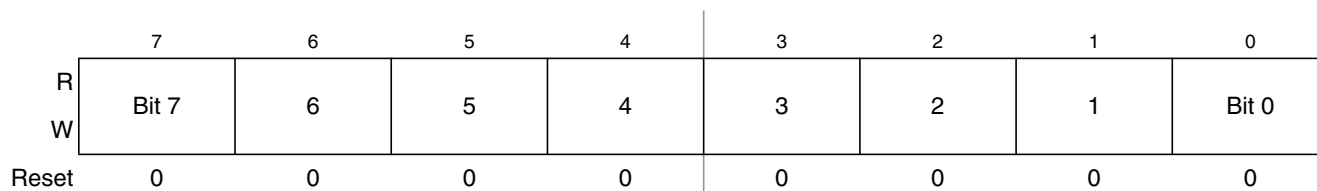
Table 10-5. Mode, Edge, and Level Selection

CPWMS	MSnB:MSnA	ELSnB:ELSnA	Mode	Configuration
X	XX	00		Pin not used for TPM channel; use as an external clock for the TPM or revert to general-purpose I/O
0	00	01	Input capture	Capture on rising edge only
		10		Capture on falling edge only
		11		Capture on rising or falling edge
	01	00	Output compare	Software compare only
		01		Toggle output on compare
		10		Clear output on compare
1X	10	Edge-aligned PWM	High-true pulses (clear output on compare)	
	X1		Low-true pulses (set output on compare)	
1	XX	10	Center-aligned PWM	High-true pulses (clear output on compare-up)
		X1		Low-true pulses (set output on compare-up)

If the associated port pin is not stable for at least two bus clock cycles before changing to input capture mode, it is possible to get an unexpected indication of an edge trigger. Typically, a program would clear status flags after changing channel configuration bits and before enabling channel interrupts or using the status flags to avoid any unexpected behavior.

10.4.5 Timer x Channel Value Registers (TPMxCnVH:TPMxCnVL)

These read/write registers contain the captured TPM counter value of the input capture function or the output compare value for the output compare or PWM functions. The channel value registers are cleared by reset.


Figure 10-9. Timer x Channel Value Register High (TPMxCnVH)

Figure 10-10. Timer Channel Value Register Low (TPMxCnVL)

In input capture mode, reading either byte (TPMxCnVH or TPMxCnVL) latches the contents of both bytes into a buffer where they remain latched until the other byte is read. This latching mechanism also resets (becomes unlatched) when the TPMxCnSC register is written.

pin from a master and the MISO waveform applies to the MISO output from a slave. The \overline{SS} OUT waveform applies to the slave select output from a master (provided MODFEN and SSOE = 1). The master \overline{SS} output goes to active low one-half SPSCK cycle before the start of the transfer and goes back high at the end of the eighth bit time of the transfer. The \overline{SS} IN waveform applies to the slave select input of a slave.

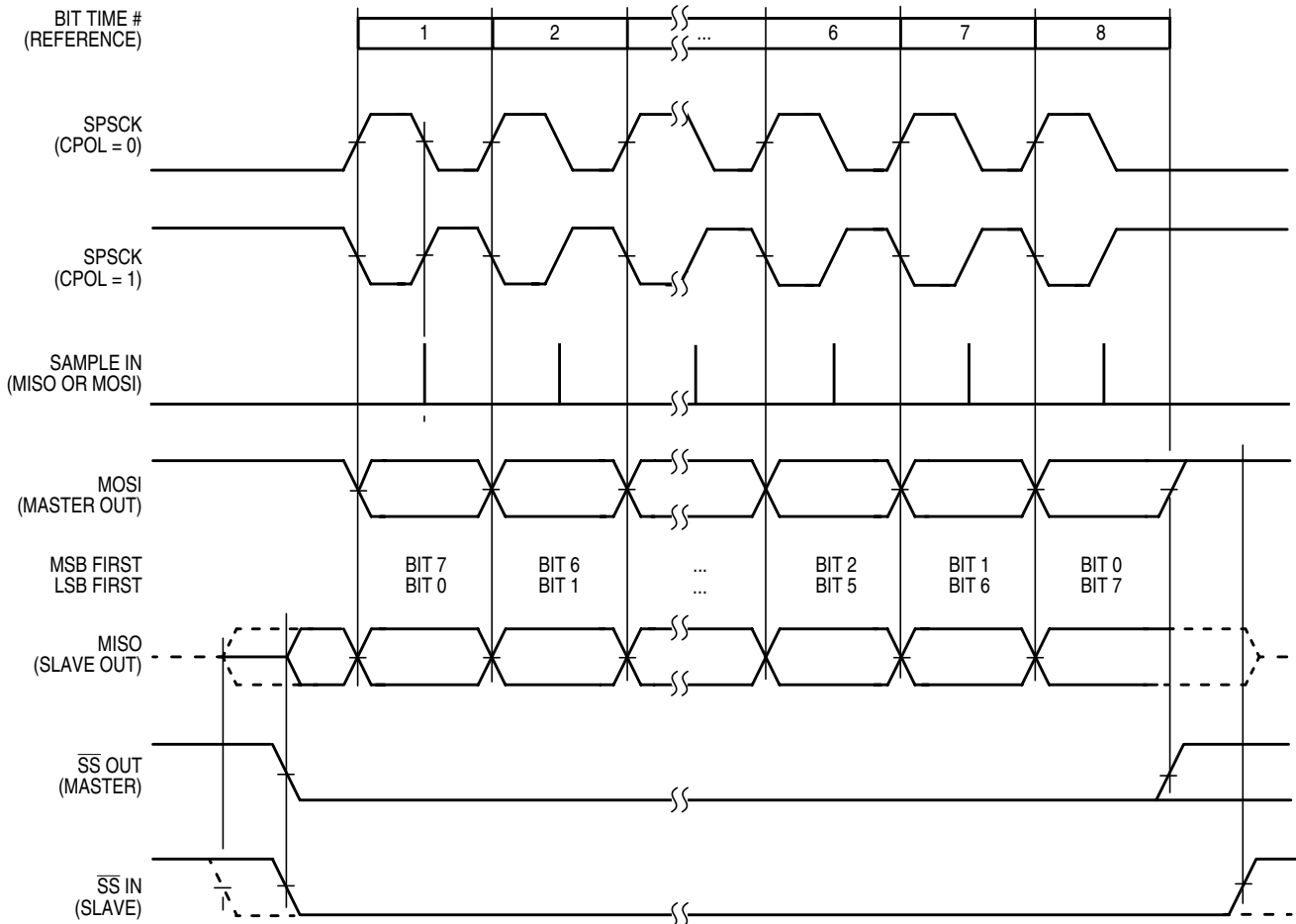


Figure 12-10. SPI Clock Formats (CPHA = 1)

When CPHA = 1, the slave begins to drive its MISO output when \overline{SS} goes to active low, but the data is not defined until the first SPSCK edge. The first SPSCK edge shifts the first bit of data from the shifter onto the MOSI output of the master and the MISO output of the slave. The next SPSCK edge causes both the master and the slave to sample the data bit values on their MISO and MOSI inputs, respectively. At the third SPSCK edge, the SPI shifter shifts one bit position which shifts in the bit value that was just sampled, and shifts the second data bit value out the other end of the shifter to the MOSI and MISO outputs of the master and slave, respectively. When CPHA = 1, the slave's \overline{SS} input is not required to go to its inactive high level between transfers.

Figure 12-11 shows the clock formats when CPHA = 0. At the top of the figure, the eight bit times are shown for reference with bit 1 starting as the slave is selected (\overline{SS} IN goes low), and bit 8 ends at the last SPSCK edge. The MSB first and LSB first lines show the order of SPI data bits depending on the setting

13.1.3 Block Diagram

Figure 13-2 is a block diagram of the IIC.

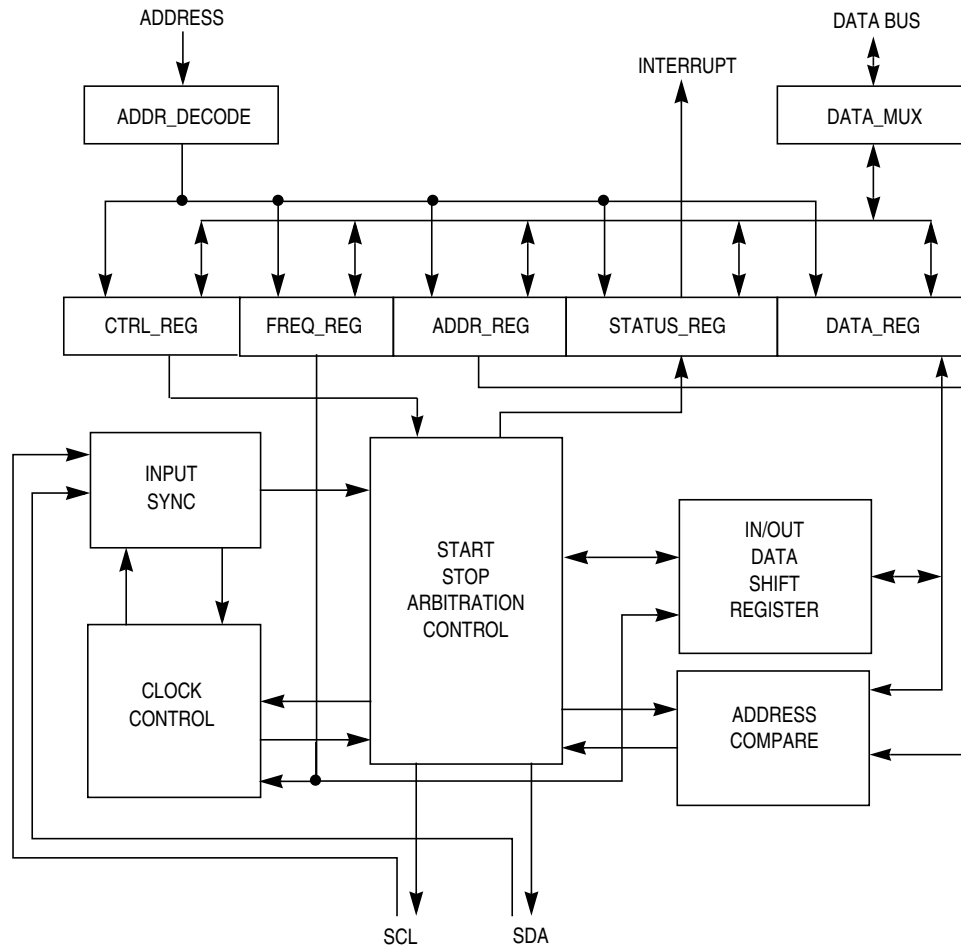


Figure 13-2. IIC Functional Block Diagram

13.2 External Signal Description

This section describes each user-accessible pin signal.

13.2.1 SCL — Serial Clock Line

The bidirectional SCL is the serial clock line of the IIC system.

13.2.2 SDA — Serial Data Line

The bidirectional SDA is the serial data line of the IIC system.

13.3 Register Definition

This section consists of the IIC register descriptions in address order.

Table 14-9. APCTL1 Register Field Descriptions (continued)

Field	Description
1 ADPC1	ADC Pin Control 1 — ADPC1 is used to control the pin associated with channel AD1. 0 AD1 pin I/O control enabled 1 AD1 pin I/O control disabled
0 ADPC0	ADC Pin Control 0 — ADPC0 is used to control the pin associated with channel AD0. 0 AD0 pin I/O control enabled 1 AD0 pin I/O control disabled

14.4.9 Pin Control 2 Register (APCTL2)

APCTL2 is used to control channels 8–15 of the ADC module.

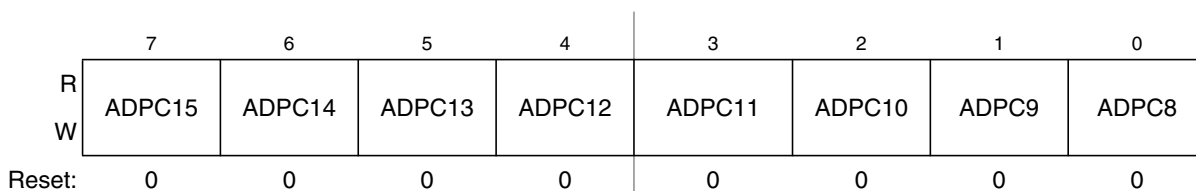


Figure 14-12. Pin Control 2 Register (APCTL2)

Table 14-10. APCTL2 Register Field Descriptions

Field	Description
7 ADPC15	ADC Pin Control 15 — ADPC15 is used to control the pin associated with channel AD15. 0 AD15 pin I/O control enabled 1 AD15 pin I/O control disabled
6 ADPC14	ADC Pin Control 14 — ADPC14 is used to control the pin associated with channel AD14. 0 AD14 pin I/O control enabled 1 AD14 pin I/O control disabled
5 ADPC13	ADC Pin Control 13 — ADPC13 is used to control the pin associated with channel AD13. 0 AD13 pin I/O control enabled 1 AD13 pin I/O control disabled
4 ADPC12	ADC Pin Control 12 — ADPC12 is used to control the pin associated with channel AD12. 0 AD12 pin I/O control enabled 1 AD12 pin I/O control disabled
3 ADPC11	ADC Pin Control 11 — ADPC11 is used to control the pin associated with channel AD11. 0 AD11 pin I/O control enabled 1 AD11 pin I/O control disabled
2 ADPC10	ADC Pin Control 10 — ADPC10 is used to control the pin associated with channel AD10. 0 AD10 pin I/O control enabled 1 AD10 pin I/O control disabled

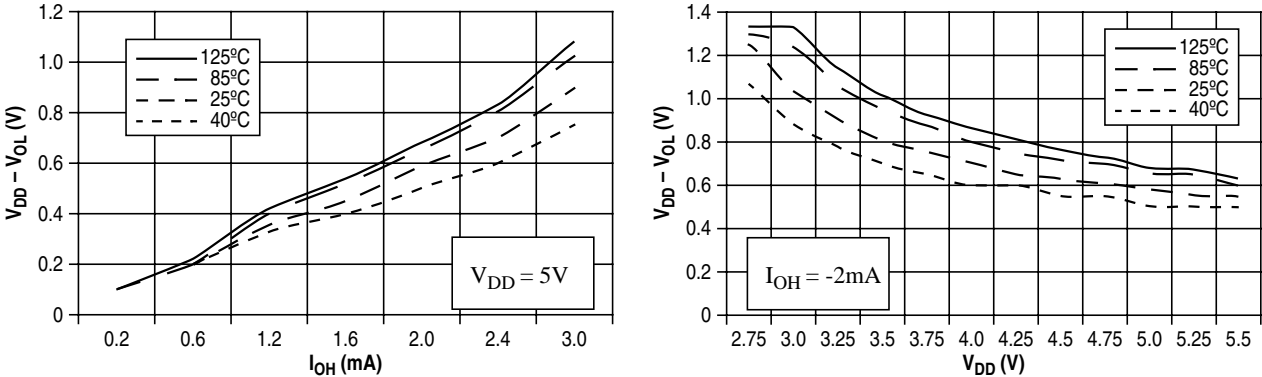


Figure A-3. Typical High-Side (Source) Characteristics — Low Drive ($PTxDS_n = 0$)

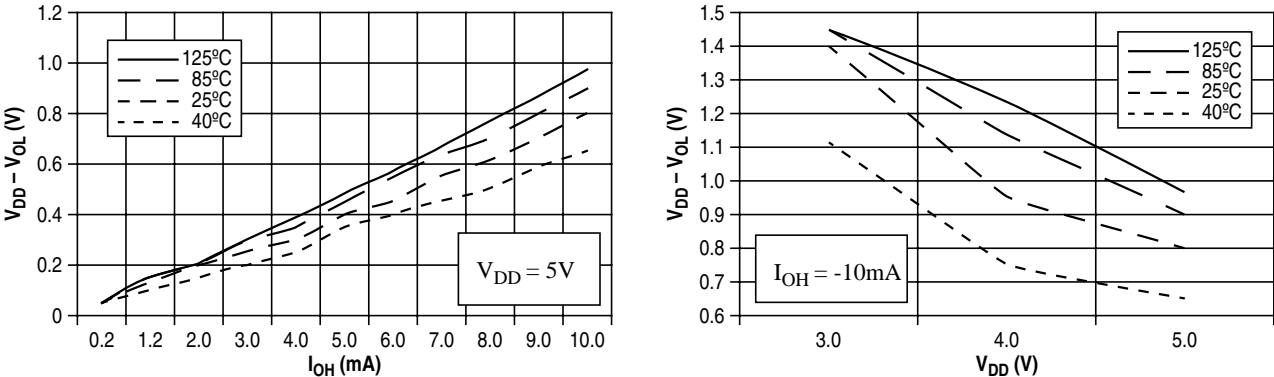


Figure A-4. Typical High-Side (Source) Characteristics — High Drive ($PTxDS_n = 1$)

Table A-12. ICG Frequency Specifications (continued)
 ($V_{DDA} = V_{DDA} \text{ (min)}$ to $V_{DDA} \text{ (max)}$, Temperature Range = -40 to 125°C Ambient)

Num	C	Characteristic	Symbol	Min	Typ ¹	Max	Unit
19	MC9S08AWxx: Internal oscillator deviation from trimmed frequency ⁹						
	C	$V_{DD} = 2.7 - 5.5 \text{ V}$, (constant temperature)	ACC_{int}	—	± 0.5	± 2	%
	P	$V_{DD} = 5.0 \text{ V} \pm 10\%$, -40°C to 125°C		—	± 0.5	± 2	%
	S9S08AWxx: Internal oscillator deviation from trimmed frequency ⁹						
	C	$V_{DD} = 2.7 - 5.5 \text{ V}$, (constant temperature)	ACC_{int}	—	± 0.5	± 1.5	%
	P	$V_{DD} = 5.0 \text{ V} \pm 10\%$, -40°C to 85°C		—	± 0.5	± 1.5	%
	P	$V_{DD} = 5.0 \text{ V} \pm 10\%$, -40°C to 125°C		—	± 0.5	± 2	%

- ¹ Typical values are based on characterization data at $V_{DD} = 5.0\text{V}$, 25°C unless otherwise stated.
- ² Self-clocked mode frequency is the frequency that the DCO generates when the FLL is open-loop.
- ³ Loss of reference frequency is the reference frequency detected internally, which transitions the ICG into self-clocked mode if it is not in the desired range.
- ⁴ Loss of DCO frequency is the DCO frequency detected internally, which transitions the ICG into FLL bypassed external mode (if an external reference exists) if it is not in the desired range.
- ⁵ This parameter is characterized before qualification rather than 100% tested.
- ⁶ Proper PC board layout procedures must be followed to achieve specifications.
- ⁷ This specification applies to the period of time required for the FLL to lock after entering FLL engaged internal or external modes. If a crystal/resonator is being used as the reference, this specification assumes it is already running.
- ⁸ Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{ICGOUT} . Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry via V_{DDA} and V_{SSA} and variation in crystal oscillator frequency increase the C_{Jitter} percentage for a given interval.
- ⁹ See Figure A-9.

Appendix B

Ordering Information and Mechanical Drawings

B.1 Ordering Information

This section contains ordering numbers for MC9S08AW60 Series devices. See below for an example of the device numbering system.

Table B-1. Consumer and Industrial Device Numbering System

Device Number ¹	Memory		Available Packages ²
	FLASH	RAM	Type
MC9S08AW60	63,280	2048	64-pin LQFP
MC9S08AW48	49,152		64-pin QFP
MC9S08AW32	32,768		48-pin QFN
MC9S08AW16	16,384	1024	44-pin LQFP

¹ See Table 1-1 for a complete description of modules included on each device.

² See Table B-3 for package information.

Table B-2. Automotive Device Numbering System

Device Number ¹	Memory		Available Packages ²
	FLASH	RAM	Type
S9S08AW60	63,280	2048	64-pin LQFP
S9S08AW48	49,152		48-pin QFN
S9S08AW32	32,768		44-pin LQFP
S9S08AW16	16,384	1024	48-pin QFN 44-pin LQFP

¹ See Table 1-1 for a complete description of modules included on each device.

² See Table B-3 for package information.