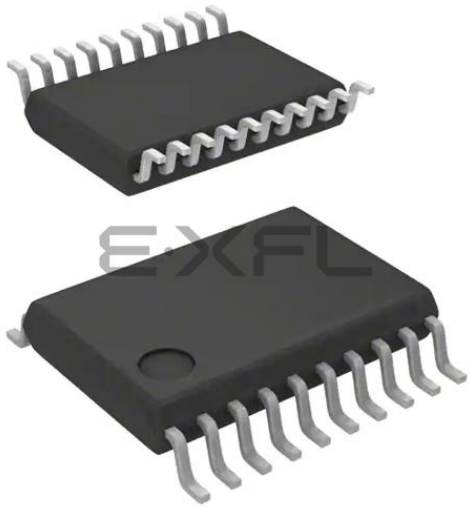

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	I²C, LINbus, SIO, SSU, UART/USART
Peripherals	POR, PWM, Voltage Detect, WDT
Number of I/O	15
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-LSSOP (0.173", 4.40mm Width)
Supplier Device Package	20-LSSOP
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f21321cdsp-w4

1.1.2 Specifications

Tables 1.1 and 1.2 outline the Specifications for R8C/32C Group.

Table 1.1 Specifications for R8C/32C Group (1)

Item	Function	Specification
CPU	Central processing unit	R8C CPU core • Number of fundamental instructions: 89 • Minimum instruction execution time: 50 ns (f(XIN) = 20 MHz, VCC = 2.7 to 5.5 V) 200 ns (f(XIN) = 5 MHz, VCC = 1.8 to 5.5 V) • Multiplier: 16 bits × 16 bits → 32 bits • Multiply-accumulate instruction: 16 bits × 16 bits + 32 bits → 32 bits • Operation mode: Single-chip mode (address space: 1 Mbyte)
Memory	ROM, RAM, Data flash	Refer to **Table 1.3 Product List for** R8C/32C Group.
Power Supply Voltage Detection	Voltage detection circuit	• Power-on reset • Voltage detection 3 (detection level of voltage detection 0 and voltage detection 1 selectable)
I/O Ports	Programmable I/O ports	• Input-only: 1 pin • CMOS I/O ports: 15, selectable pull-up resistor • High current drive ports: 15
Clock	Clock generation circuits	4 circuits: XIN clock oscillation circuit, XCIN clock oscillation circuit (32 kHz) High-speed on-chip oscillator (with frequency adjustment function), Low-speed on-chip oscillator, • Oscillation stop detection: XIN clock oscillation stop detection function • Frequency divider circuit: Dividing selectable 1, 2, 4, 8, and 16 • Low power consumption modes: Standard operating mode (high-speed clock, low-speed clock, high-speed on-chip oscillator, low-speed on-chip oscillator), wait mode, stop mode
		Real-time clock (timer RE)
Interrupts		• Number of interrupt vectors: 69 • External Interrupt: 7 ($\overline{\text{INT}}$ × 3, Key input × 4) • Priority levels: 7 levels
Watchdog Timer		• 14 bits × 1 (with prescaler) • Reset start selectable • Low-speed on-chip oscillator for watchdog timer selectable
DTC (Data Transfer Controller)		• 1 channel • Activation sources: 21 • Transfer modes: 2 (normal mode, repeat mode)
Timer	Timer RA	8 bits × 1 (with 8-bit prescaler) Timer mode (period timer), pulse output mode (output level inverted every period), event counter mode, pulse width measurement mode, pulse period measurement mode
	Timer RB	8 bits × 1 (with 8-bit prescaler) Timer mode (period timer), programmable waveform generation mode (PWM output), programmable one-shot generation mode, programmable wait one-shot generation mode
	Timer RC	16 bits × 1 (with 4 capture/compare registers) Timer mode (input capture function, output compare function), PWM mode (output 3 pins), PWM2 mode (PWM output pin)
	Timer RE	8 bits × 1 Real-time clock mode (count seconds, minutes, hours, days of week), output compare mode

1.3 Block Diagram

Figure 1.2 shows a Block Diagram.

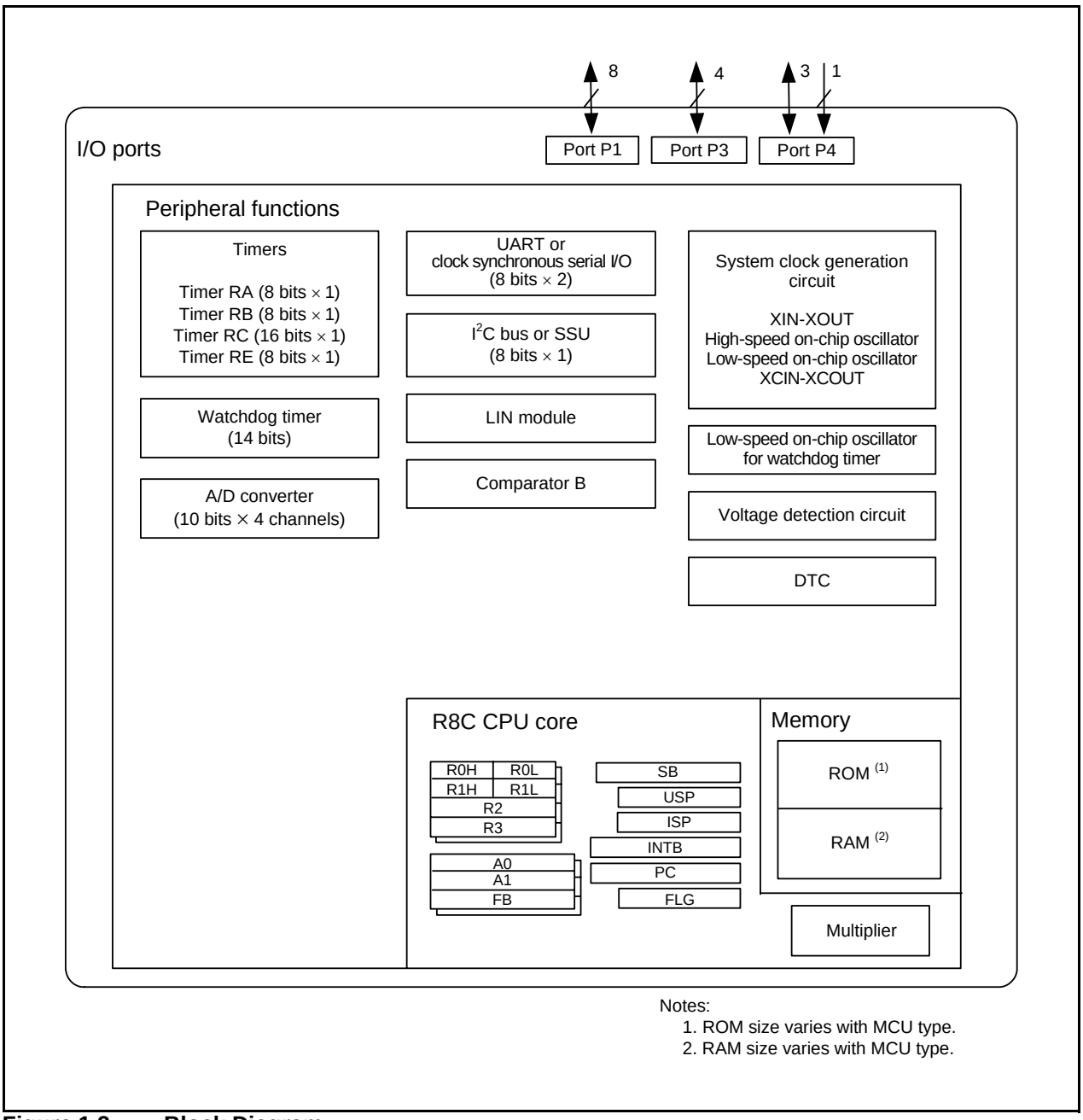


Figure 1.2 Block Diagram

1.4 Pin Assignment

Figure 1.3 shows Pin Assignment (Top View). Table 1.4 outlines the Pin Name Information by Pin Number.

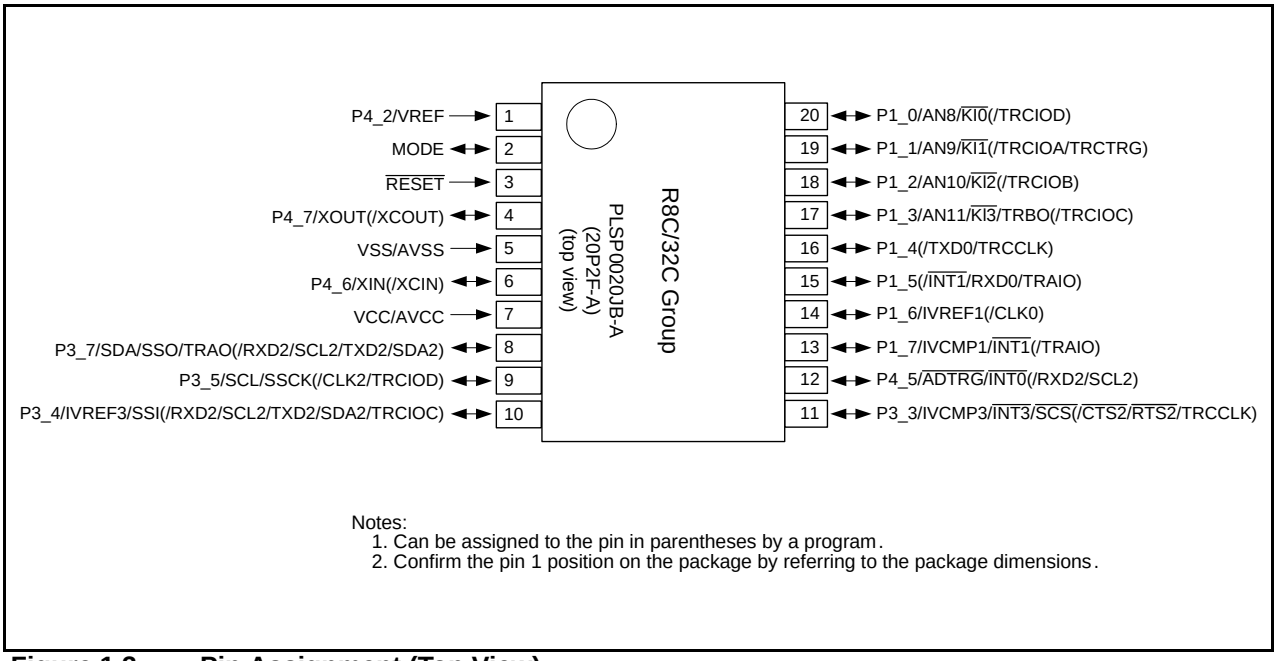
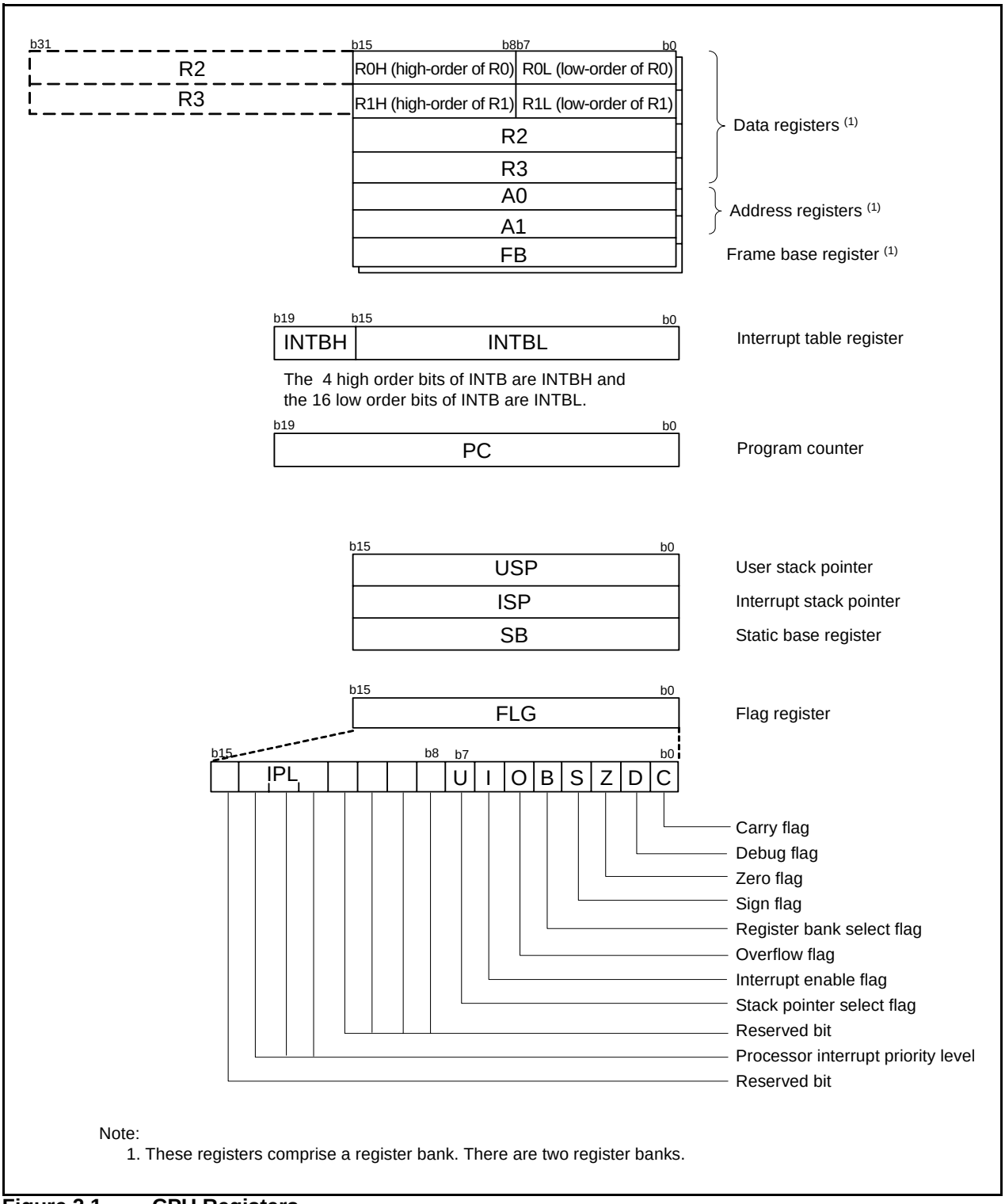


Figure 1.3 Pin Assignment (Top View)

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU Registers. The CPU contains 13 registers. R0, R1, R2, R3, A0, A1, and FB configure a register bank. There are two sets of register bank.



Note:
1. These registers comprise a register bank. There are two register banks.

Figure 2.1 CPU Registers

Table 4.3 SFR Information (3) (1)

Address	Register	Symbol	After Reset
0080h	DTC Activation Control Register	DTCTL	00h
0081h			
0082h			
0083h			
0084h			
0085h			
0086h			
0087h			
0088h	DTC Activation Enable Register 0	DTCEN0	00h
0089h	DTC Activation Enable Register 1	DTCEN1	00h
008Ah	DTC Activation Enable Register 2	DTCEN2	00h
008Bh	DTC Activation Enable Register 3	DTCEN3	00h
008Ch			
008Dh	DTC Activation Enable Register 5	DTCEN5	00h
008Eh	DTC Activation Enable Register 6	DTCEN6	00h
008Fh			
0090h			
0091h			
0092h			
0093h			
0094h			
0095h			
0096h			
0097h			
0098h			
0099h			
009Ah			
009Bh			
009Ch			
009Dh			
009Eh			
009Fh			
00A0h	UART0 Transmit / Receive Mode Register	U0MR	00h
00A1h	UART0 Bit Rate Register	U0BRG	XXh
00A2h	UART0 Transmit Buffer Register	U0TB	XXh
00A3h			XXh
00A4h	UART0 Transmit / Receive Control Register 0	U0C0	00001000b
00A5h	UART0 Transmit / Receive Control Register 1	U0C1	00000010b
00A6h	UART0 Receive Buffer Register	U0RB	XXh
00A7h			XXh
00A8h	UART2 Transmit / Receive Mode Register	U2MR	00h
00A9h	UART2 Bit Rate Register	U2BRG	XXh
00AAh	UART2 Transmit Buffer Register	U2TB	XXh
00ABh			XXh
00ACh	UART2 Transmit / Receive Control Register 0	U2C0	00001000b
00ADh	UART2 Transmit / Receive Control Register 1	U2C1	00000010b
00AEh	UART2 Receive Buffer Register	U2RB	XXh
00AFh			XXh
00B0h	UART2 Digital Filter Function Select Register	URXDF	00h
00B1h			
00B2h			
00B3h			
00B4h			
00B5h			
00B6h			
00B7h			
00B8h			
00B9h			
00BAh			
00BBh	UART2 Special Mode Register 5	U2SMR5	00h
00BCh	UART2 Special Mode Register 4	U2SMR4	00h
00BDh	UART2 Special Mode Register 3	U2SMR3	000X0X0Xb
00BEh	UART2 Special Mode Register 2	U2SMR2	X0000000b
00BFh	UART2 Special Mode Register	U2SMR	X0000000b

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.5 SFR Information (5) (1)

Address	Register	Symbol	After Reset
0100h	Timer RA Control Register	TRACR	00h
0101h	Timer RA I/O Control Register	TRAIOC	00h
0102h	Timer RA Mode Register	TRAMR	00h
0103h	Timer RA Prescaler Register	TRAPRE	FFh
0104h	Timer RA Register	TRA	FFh
0105h	LIN Control Register 2	LINCR2	00h
0106h	LIN Control Register	LINCR	00h
0107h	LIN Status Register	LINST	00h
0108h	Timer RB Control Register	TRBCR	00h
0109h	Timer RB One-Shot Control Register	TRBOCR	00h
010Ah	Timer RB I/O Control Register	TRBIOC	00h
010Bh	Timer RB Mode Register	TRBMR	00h
010Ch	Timer RB Prescaler Register	TRBPRE	FFh
010Dh	Timer RB Secondary Register	TRBSC	FFh
010Eh	Timer RB Primary Register	TRBPR	FFh
010Fh			
0110h			
0111h			
0112h			
0113h			
0114h			
0115h			
0116h			
0117h			
0118h	Timer RE Second Data Register / Counter Data Register	TRESEC	00h
0119h	Timer RE Minute Data Register / Compare Data Register	TREMIN	00h
011Ah	Timer RE Hour Data Register	TREHR	00h
011Bh	Timer RE Day of Week Data Register	TREWK	00h
011Ch	Timer RE Control Register 1	TRECR1	00h
011Dh	Timer RE Control Register 2	TRECR2	00h
011Eh	Timer RE Count Source Select Register	TRECSR	00001000b
011Fh			
0120h	Timer RC Mode Register	TRCMR	01001000b
0121h	Timer RC Control Register 1	TRCCR1	00h
0122h	Timer RC Interrupt Enable Register	TRCIER	01110000b
0123h	Timer RC Status Register	TRCSR	01110000b
0124h	Timer RC I/O Control Register 0	TRCIOR0	10001000b
0125h	Timer RC I/O Control Register 1	TRCIOR1	10001000b
0126h	Timer RC Counter	TRC	00h
0127h			00h
0128h	Timer RC General Register A	TRCGRA	FFh
0129h			FFh
012Ah	Timer RC General Register B	TRCGRB	FFh
012Bh			FFh
012Ch	Timer RC General Register C	TRCGRC	FFh
012Dh			FFh
012Eh	Timer RC General Register D	TRCGRD	FFh
012Fh			FFh
0130h	Timer RC Control Register 2	TRCCR2	00011000b
0131h	Timer RC Digital Filter Function Select Register	TRCDF	00h
0132h	Timer RC Output Master Enable Register	TRCOER	01111111b
0133h	Timer RC Trigger Control Register	TRCADCR	00h
0134h			
0135h			
0136h			
0137h			
0138h			
0139h			
013Ah			
013Bh			
013Ch			
013Dh			
013Eh			
013Fh			

Note:
1. The blank areas are reserved and cannot be accessed by users.

Table 4.7 SFR Information (7) (1)

Address	Register	Symbol	After Reset
0180h	Timer RA Pin Select Register	TRASR	00h
0181h	Timer RC Pin Select Register	TRBRCSR	00h
0182h	Timer RC Pin Select Register 0	TRCPSR0	00h
0183h	Timer RC Pin Select Register 1	TRCPSR1	00h
0184h			
0185h			
0186h			
0187h			
0188h	UART0 Pin Select Register	U0SR	00h
0189h			
018Ah	UART2 Pin Select Register 0	U2SR0	00h
018Bh	UART2 Pin Select Register 1	U2SR1	00h
018Ch	SSU / IIC Pin Select Register	SSUIICSR	00h
018Dh			
018Eh	INT Interrupt Input Pin Select Register	INTSR	00h
018Fh	I/O Function Pin Select Register	PINSR	00h
0190h			
0191h			
0192h			
0193h	SS Bit Counter Register	SSBR	11111000b
0194h	SS Transmit Data Register L / IIC bus Transmit Data Register (2)	SSTDR / ICDRT	FFh
0195h	SS Transmit Data Register H (2)	SSTDRH	FFh
0196h	SS Receive Data Register L / IIC bus Receive Data Register (2)	SSRDR / ICDRR	FFh
0197h	SS Receive Data Register H (2)	SSRDRH	FFh
0198h	SS Control Register H / IIC bus Control Register 1 (2)	SSCRH / ICCR1	00h
0199h	SS Control Register L / IIC bus Control Register 2 (2)	SSCRL / ICCR2	01111101b
019Ah	SS Mode Register / IIC bus Mode Register (2)	SSMR / ICMR	00010000b / 00011000b
019Bh	SS Enable Register / IIC bus Interrupt Enable Register (2)	SSER / ICIER	00h
019Ch	SS Status Register / IIC bus Status Register (2)	SSSR / ICSR	00h / 0000X000b
019Dh	SS Mode Register 2 / Slave Address Register (2)	SSMR2 / SAR	00h
019Eh			
019Fh			
01A0h			
01A1h			
01A2h			
01A3h			
01A4h			
01A5h			
01A6h			
01A7h			
01A8h			
01A9h			
01AAh			
01ABh			
01ACh			
01ADh			
01AEh			
01AFh			
01B0h			
01B1h			
01B2h	Flash Memory Status Register	FST	10000X00b
01B3h			
01B4h	Flash Memory Control Register 0	FMR0	00h
01B5h	Flash Memory Control Register 1	FMR1	00h
01B6h	Flash Memory Control Register 2	FMR2	00h
01B7h			
01B8h			
01B9h			
01BAh			
01BBh			
01BCh			
01BDh			
01BEh			
01BFh			

X: Undefined

Notes:
1. The blank areas are reserved and cannot be accessed by users.
2. Selectable by the IICSEL bit in the SSUIICSR register.

Table 4.12 SFR Information (12) (1)

Address	Register	Symbol	After Reset
2CF0h	DTC Control Data 22	DTCD22	XXh
2CF1h			XXh
2CF2h			XXh
2CF3h			XXh
2CF4h			XXh
2CF5h			XXh
2CF6h			XXh
2CF7h			XXh
2CF8h	DTC Control Data 23	DTCD23	XXh
2CF9h			XXh
2CFAh			XXh
2CFBh			XXh
2CFCh			XXh
2CFDh			XXh
2CFEh			XXh
2CFFh			XXh
2D00h			
:			
2FFFh			

X: Undefined
Note:
1. The blank areas are reserved and cannot be accessed by users.

Table 4.13 ID Code Areas and Option Function Select Area

Address	Area Name	Symbol	After Reset
:			
FFDBh	Option Function Select Register 2	OFS2	(Note 1)
:			
FFDFh	ID1		(Note 2)
:			
FFE3h	ID2		(Note 2)
:			
FFEBh	ID3		(Note 2)
:			
FFEFh	ID4		(Note 2)
:			
FFF3h	ID5		(Note 2)
:			
FFF7h	ID6		(Note 2)
:			
FFFBh	ID7		(Note 2)
:			
FFFFh	Option Function Select Register	OFS	(Note 1)

Notes:
1. The option function select area is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
Do not write additions to the option function select area. If the block including the option function select area is erased, the option function select area is set to FFh.
When blank products are shipped, the option function select area is set to FFh. It is set to the written value after written by the user.
When factory-programming products are shipped, the value of the option function select area is the value programmed by the user.
2. The ID code areas are allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
Do not write additions to the ID code areas. If the block including the ID code areas is erased, the ID code areas are set to FFh.
When blank products are shipped, the ID code areas are set to FFh. They are set to the written value after written by the user.
When factory-programming products are shipped, the value of the ID code areas is the value programmed by the user.

Table 5.2 Recommended Operating Conditions

Symbol	Parameter				Conditions	Standard			Unit
						Min.	Typ.	Max.	
V_{CC}/AV_{CC}	Supply voltage					1.8	–	5.5	V
V_{SS}/AV_{SS}	Supply voltage					–	0	–	V
V_{IH}	Input “H” voltage	Other than CMOS input				0.8 V_{CC}	–	V_{CC}	V
		CMOS input	Input level switching function (I/O port)	Input level selection : 0.35 V_{CC}	4.0 V ≤ V_{CC} ≤ 5.5 V	0.5 V_{CC}	–	V_{CC}	V
					2.7 V ≤ V_{CC} < 4.0 V	0.55 V_{CC}	–	V_{CC}	V
					1.8 V ≤ V_{CC} < 2.7 V	0.65 V_{CC}	–	V_{CC}	V
				Input level selection : 0.5 V_{CC}	4.0 V ≤ V_{CC} ≤ 5.5 V	0.65 V_{CC}	–	V_{CC}	V
					2.7 V ≤ V_{CC} < 4.0 V	0.7 V_{CC}	–	V_{CC}	V
					1.8 V ≤ V_{CC} < 2.7 V	0.8 V_{CC}	–	V_{CC}	V
				Input level selection : 0.7 V_{CC}	4.0 V ≤ V_{CC} ≤ 5.5 V	0.85 V_{CC}	–	V_{CC}	V
					2.7 V ≤ V_{CC} < 4.0 V	0.85 V_{CC}	–	V_{CC}	V
					1.8 V ≤ V_{CC} < 2.7 V	0.85 V_{CC}	–	V_{CC}	V
		External clock input (XOUT)				1.2	–	V_{CC}	V
VIL	Input “L” voltage	Other than CMOS input				0	–	0.2 V_{CC}	V
		CMOS input	Input level switching function (I/O port)	Input level selection : 0.35 V_{CC}	4.0 V ≤ V_{CC} ≤ 5.5 V	0	–	0.2 V_{CC}	V
					2.7 V ≤ V_{CC} < 4.0 V	0	–	0.2 V_{CC}	V
					1.8 V ≤ V_{CC} < 2.7 V	0	–	0.2 V_{CC}	V
				Input level selection : 0.5 V_{CC}	4.0 V ≤ V_{CC} ≤ 5.5 V	0	–	0.4 V_{CC}	V
					2.7 V ≤ V_{CC} < 4.0 V	0	–	0.3 V_{CC}	V
					1.8 V ≤ V_{CC} < 2.7 V	0	–	0.2 V_{CC}	V
				Input level selection : 0.7 V_{CC}	4.0 V ≤ V_{CC} ≤ 5.5 V	0	–	0.55 V_{CC}	V
					2.7 V ≤ V_{CC} < 4.0 V	0	–	0.45 V_{CC}	V
					1.8 V ≤ V_{CC} < 2.7 V	0	–	0.35 V_{CC}	V
		External clock input (XOUT)				0	–	0.4	V
$I_{OH(sum)}$	Peak sum output “H” current	Sum of all pins $I_{OH(peak)}$				–	–	–160	mA
$I_{OH(sum)}$	Average sum output “H” current	Sum of all pins $I_{OH(avg)}$				–	–	–80	mA
$I_{OH(peak)}$	Peak output “H” current	Drive capacity Low				–	–	–10	mA
		Drive capacity High				–	–	–40	mA
$I_{OH(avg)}$	Average output “H” current	Drive capacity Low				–	–	–5	mA
		Drive capacity High				–	–	–20	mA
$I_{OL(sum)}$	Peak sum output “L” current	Sum of all pins $I_{OL(peak)}$				–	–	160	mA
$I_{OL(sum)}$	Average sum output “L” current	Sum of all pins $I_{OL(avg)}$				–	–	80	mA
$I_{OL(peak)}$	Peak output “L” current	Drive capacity Low				–	–	10	mA
		Drive capacity High				–	–	40	mA
$I_{OL(avg)}$	Average output “L” current	Drive capacity Low				–	–	5	mA
		Drive capacity High				–	–	20	mA
$f_{(XIN)}$	XIN clock input oscillation frequency				2.7 V ≤ V_{CC} ≤ 5.5 V	–	–	20	MHz
					1.8 V ≤ V_{CC} < 2.7 V	–	–	5	MHz
$f_{(XCIN)}$	XCIN clock input oscillation frequency				1.8 V ≤ V_{CC} ≤ 5.5 V	–	32.768	50	kHz
fOCO40M	When used as the count source for timer RC (3)				2.7 V ≤ V_{CC} ≤ 5.5 V	32	–	40	MHz
fOCO-F	fOCO-F frequency				2.7 V ≤ V_{CC} ≤ 5.5 V	–	–	20	MHz
					1.8 V ≤ V_{CC} < 2.7 V	–	–	5	MHz
–	System clock frequency				2.7 V ≤ V_{CC} ≤ 5.5 V	–	–	20	MHz
					1.8 V ≤ V_{CC} < 2.7 V	–	–	5	MHz
$f_{(BCLK)}$	CPU clock frequency				2.7 V ≤ V_{CC} ≤ 5.5 V	–	–	20	MHz
					1.8 V ≤ V_{CC} < 2.7 V	–	–	5	MHz

Notes:
1. V_{CC} = 1.8 to 5.5 V and T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.
2. The average output current indicates the average value of current measured during 100 ms.
3. fOCO40M can be used as the count source for timer RC in the range of V_{CC} = 2.7 V to 5.5V.

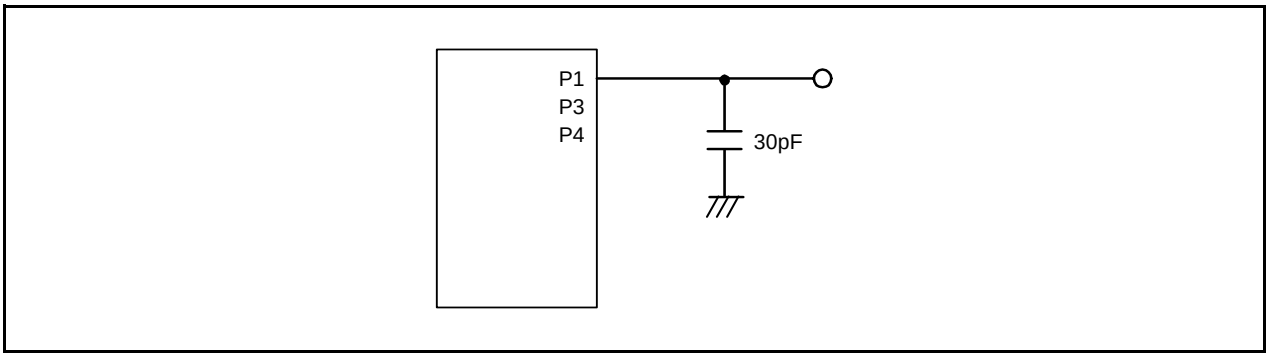


Figure 5.1 Ports P1, P3, P4 Timing Measurement Circuit

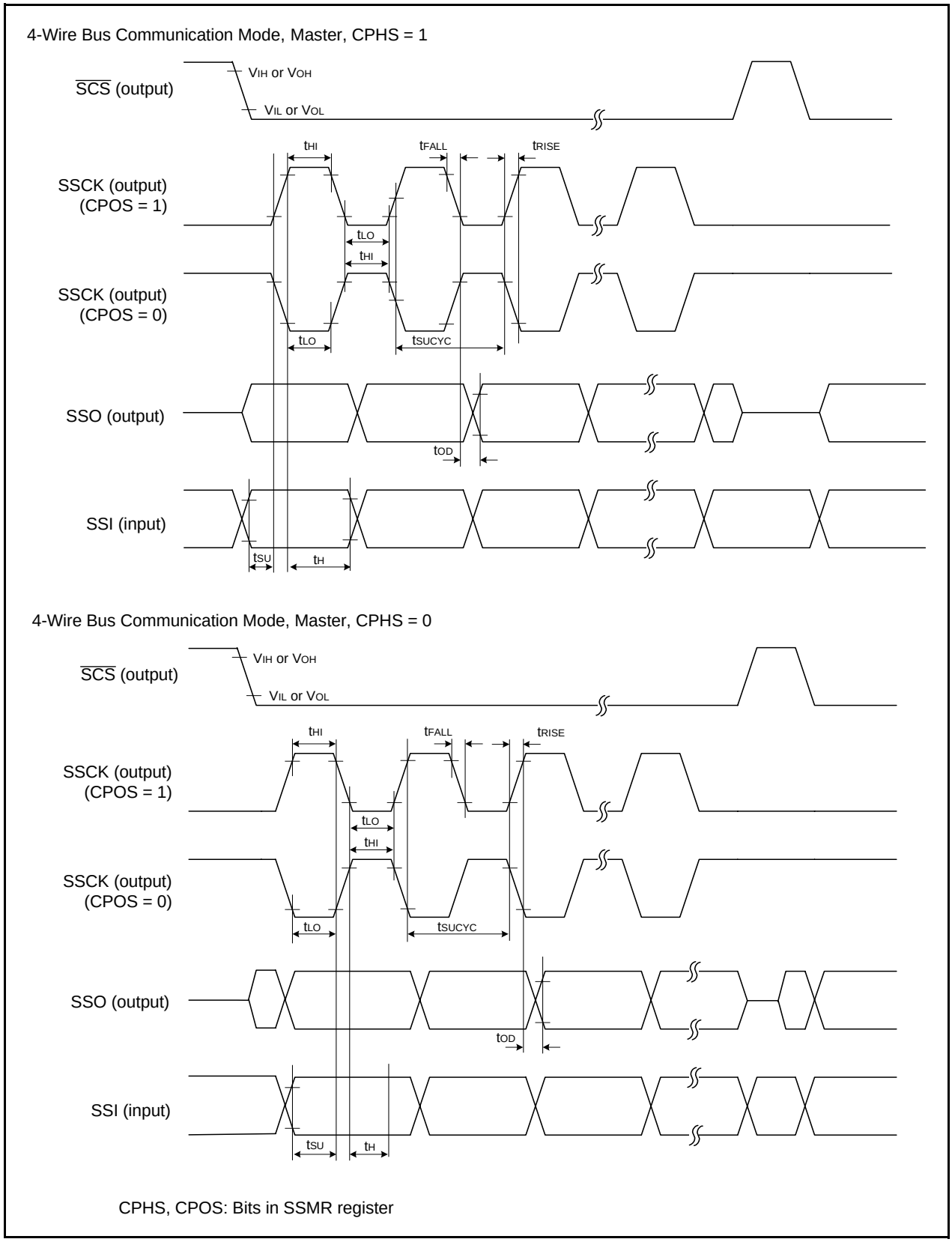


Figure 5.4 I/O Timing of Synchronous Serial Communication Unit (SSU) (Master)

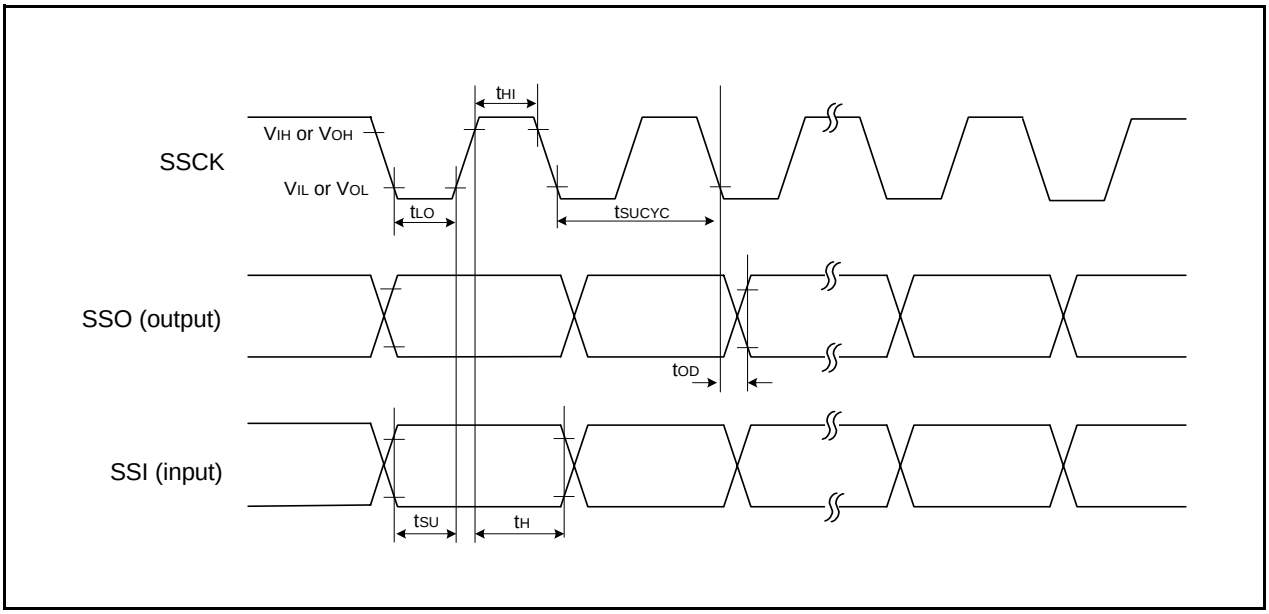


Figure 5.6 I/O Timing of Synchronous Serial Communication Unit (SSU) (Clock Synchronous Communication Mode)

Table 5.16 Electrical Characteristics (1) [4.2 V ≤ Vcc ≤ 5.5 V]

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V_{OH}	Output “H” voltage	Other than XOUT	Drive capacity High V_{CC} = 5 V	I_{OH} = –20 mA	V_{CC} – 2.0	–	V_{CC}	V
			Drive capacity Low V_{CC} = 5 V	I_{OH} = –5 mA	V_{CC} – 2.0	–	V_{CC}	V
		XOUT	V_{CC} = 5 V	I_{OH} = –200 μA	1.0	–	V_{CC}	V
V_{OL}	Output “L” voltage	Other than XOUT	Drive capacity High V_{CC} = 5 V	I_{OL} = 20 mA	–	–	2.0	V
			Drive capacity Low V_{CC} = 5 V	I_{OL} = 5 mA	–	–	2.0	V
		XOUT	V_{CC} = 5 V	I_{OL} = 200 μA	–	–	0.5	V
V_{T+}-V_{T-}	Hysteresis	$\overline{INT0}$, $\overline{INT1}$, $\overline{INT3}$, $\overline{KI0}$, $\overline{KI1}$, $\overline{KI2}$, $\overline{KI3}$, TRAIO, TRBO, TRCIOA, TRCIOB, TRCIOC, TRCIOD, TRCTRG, $\overline{TRCCLK}$, $\overline{ADTRG}$, RXD0, RXD2, CLK0, CLK2, SSI, SCL, SDA, SSO			0.1	1.2	–	V
		$\overline{RESET}$			0.1	1.2	–	V
I_{IH}	Input “H” current		VI = 5 V, V_{CC} = 5.0 V		–	–	5.0	μA
I_{IL}	Input “L” current		VI = 0 V, V_{CC} = 5.0 V		–	–	–5.0	μA
R_{PULLUP}	Pull-up resistance		VI = 0 V, V_{CC} = 5.0 V		25	50	100	kΩ
R_{fXIN}	Feedback resistance	XIN			–	0.3	–	MΩ
R_{fXCIN}	Feedback resistance	XCIN			–	8	–	MΩ
V_{RAM}	RAM hold voltage		During stop mode		1.8	–	–	V

Note:
1. 4.2 V ≤ V_{CC} ≤ 5.5 V and T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version), f(XIN) = 20 MHz, unless otherwise specified.

Table 5.17 Electrical Characteristics (2) [3.3 V ≤ Vcc ≤ 5.5 V]
(Topr = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition		Standard			Unit
				Min.	Typ.	Max.	
Icc	Power supply current (Vcc = 3.3 to 5.5 V) Single-chip mode, output pins are open, other pins are Vss	High-speed clock mode	XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	6.5	15	mA
			XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	5.3	12.5	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	3.6	–	mA
			XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	3.0	–	mA
			XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	2.2	–	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	1.5	–	mA
		High-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator on fOCO-F = 20 MHz Low-speed on-chip oscillator on = 125 kHz No division	–	7.0	15	mA
			XIN clock off High-speed on-chip oscillator on fOCO-F = 20 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	3.0	–	mA
			XIN clock off High-speed on-chip oscillator on fOCO-F = 4 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-16 MSTIIC = MSTTRD = MSTTRC = 1	–	1	–	mA
		Low-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR27 = 1, VCA20 = 0	–	90	400	µA
		Low-speed clock mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz No division FMR27 = 1, VCA20 = 0	–	85	400	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz No division Program operation on RAM Flash memory off, FMSTP = 1, VCA20 = 0	–	47	–	µA
		Wait mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	15	100	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	4	90	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (peripheral clock off) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	3.5	–	µA
		Stop mode	XIN clock off, Topr = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	–	2.0	5.0	µA
			XIN clock off, Topr = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	–	5.0	–	µA

Table 5.23 Electrical Characteristics (4) [2.7 V ≤ Vcc < 3.3 V]
(Topr = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition		Standard			Unit
				Min.	Typ.	Max.	
Icc	Power supply current (Vcc = 2.7 to 3.3 V) Single-chip mode, output pins are open, other pins are Vss	High-speed clock mode	XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	3.5	10	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	1.5	7.5	mA
		High-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator on fOCO-F = 20 MHz Low-speed on-chip oscillator on = 125 kHz No division	–	7.0	15	mA
			XIN clock off High-speed on-chip oscillator on fOCO-F = 20 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	3.0	–	mA
			XIN clock off High-speed on-chip oscillator on fOCO-F = 10 MHz Low-speed on-chip oscillator on = 125 kHz No division	–	4.0	–	mA
			XIN clock off High-speed on-chip oscillator on fOCO-F = 10 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	1.5	–	mA
			XIN clock off High-speed on-chip oscillator on fOCO-F = 4 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-16 MSTIIC = MSTTRD = MSTTRC = 1	–	1	–	mA
		Low-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR27 = 1, VCA20 = 0	–	90	390	µA
		Low-speed clock mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz No division FMR27 = 1, VCA20 = 0	–	80	400	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz No division Program operation on RAM Flash memory off, FMSTP = 1, VCA20 = 0	–	40	–	µA
		Wait mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0, VCA20 = 1	–	15	90	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0, VCA20 = 1	–	4	80	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (peripheral clock off) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0, VCA20 = 1	–	3.5	–	µA
		Stop mode	XIN clock off, Topr = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	–	2.0	5.0	µA
			XIN clock off, Topr = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	–	5.0	–	µA

Timing requirements
(Unless Otherwise Specified: V_{CC} = 3 V, V_{SS} = 0 V at Topr = 25°C)

Table 5.24 External Clock Input (XOUT, XCIN)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XOUT)}$	XOUT input cycle time	50	–	ns
$t_{WH(XOUT)}$	XOUT input “H” width	24	–	ns
$t_{WL(XOUT)}$	XOUT input “L” width	24	–	ns
$t_{c(XCIN)}$	XCIN input cycle time	14	–	µs
$t_{WH(XCIN)}$	XCIN input “H” width	7	–	µs
$t_{WL(XCIN)}$	XCIN input “L” width	7	–	µs

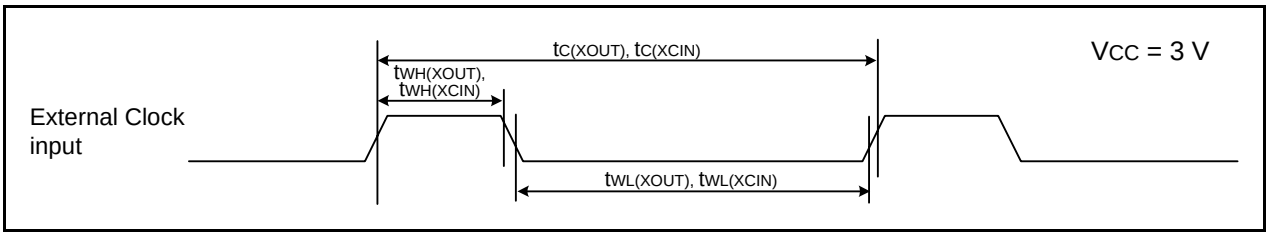


Figure 5.12 External Clock Input Timing Diagram when V_{CC} = 3 V

Table 5.25 TRAIO Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRAIO)}$	TRAIO input cycle time	300	–	ns
$t_{WH(TRAIO)}$	TRAIO input “H” width	120	–	ns
$t_{WL(TRAIO)}$	TRAIO input “L” width	120	–	ns

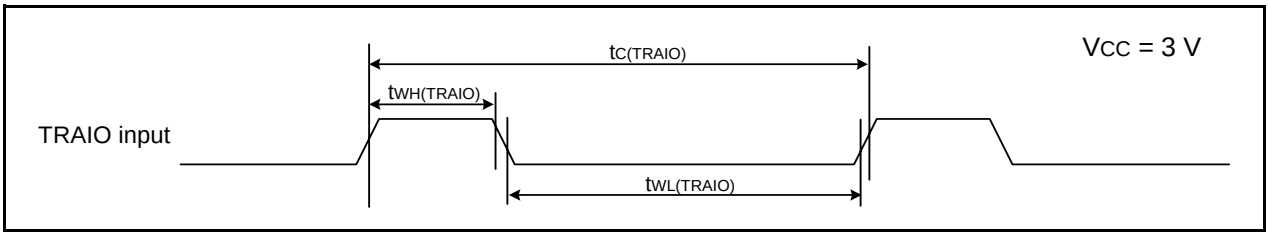


Figure 5.13 TRAIO Input Timing Diagram when V_{CC} = 3 V

Table 5.26 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	300	–	ns
$t_{W(CKH)}$	CLKi input “H” width	150	–	ns
$t_{W(CKL)}$	CLKi Input “L” width	150	–	ns
$t_{d(C-Q)}$	TXDi output delay time	–	80	ns
$t_{h(C-Q)}$	TXDi hold time	0	–	ns
$t_{su(D-C)}$	RXDi input setup time	70	–	ns
$t_{h(C-D)}$	RXDi input hold time	90	–	ns

i = 0, 2

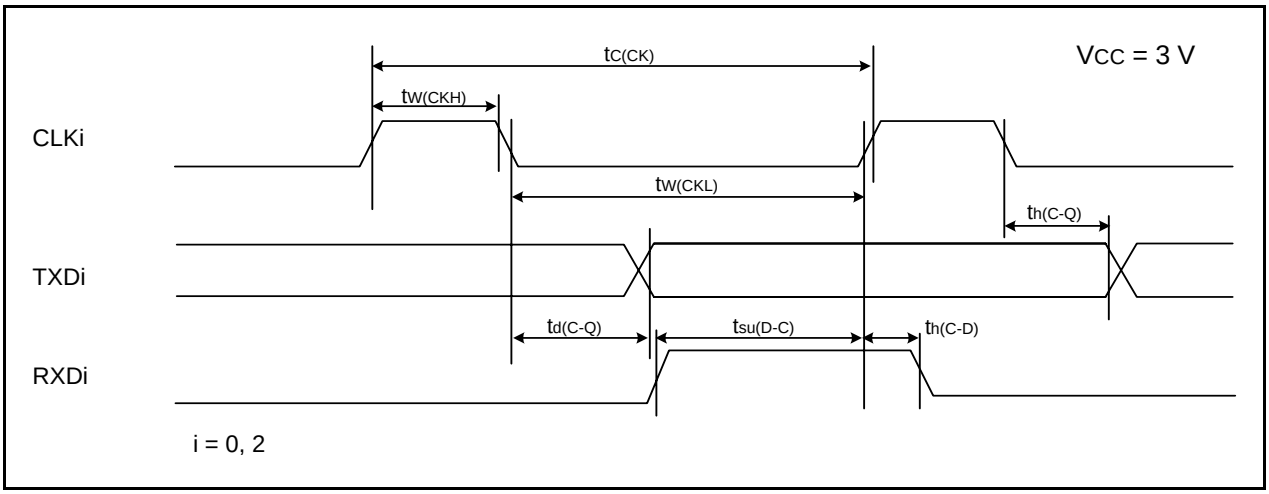


Figure 5.14 Serial Interface Timing Diagram when VCC = 3 V

Table 5.27 External Interrupt $\overline{INTi}$ (i = 0, 1, 3) Input, Key Input Interrupt $\overline{KIi}$ (i = 0 to 3)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{W(INH)}$	$\overline{INTi}$ input “H” width, $\overline{KIi}$ input “H” width	380 (1)	–	ns
$t_{W(INL)}$	$\overline{INTi}$ input “L” width, $\overline{KIi}$ input “L” width	380 (2)	–	ns

Notes:
1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

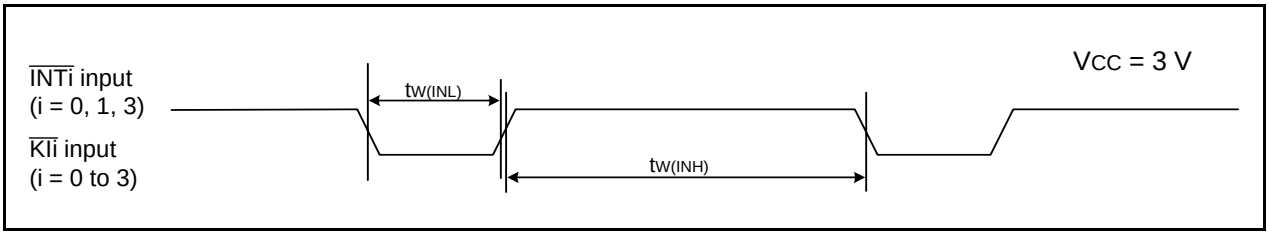


Figure 5.15 Input Timing Diagram for External Interrupt INTi and Key Input Interrupt KIi when Vcc = 3 V

Table 5.32 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	800	–	ns
$t_{W(CKH)}$	CLKi input “H” width	400	–	ns
$t_{W(CKL)}$	CLKi input “L” width	400	–	ns
$t_{d(C-Q)}$	TXDi output delay time	–	200	ns
$t_{h(C-Q)}$	TXDi hold time	0	–	ns
$t_{su(D-C)}$	RXDi input setup time	150	–	ns
$t_{h(C-D)}$	RXDi input hold time	90	–	ns

i = 0, 2

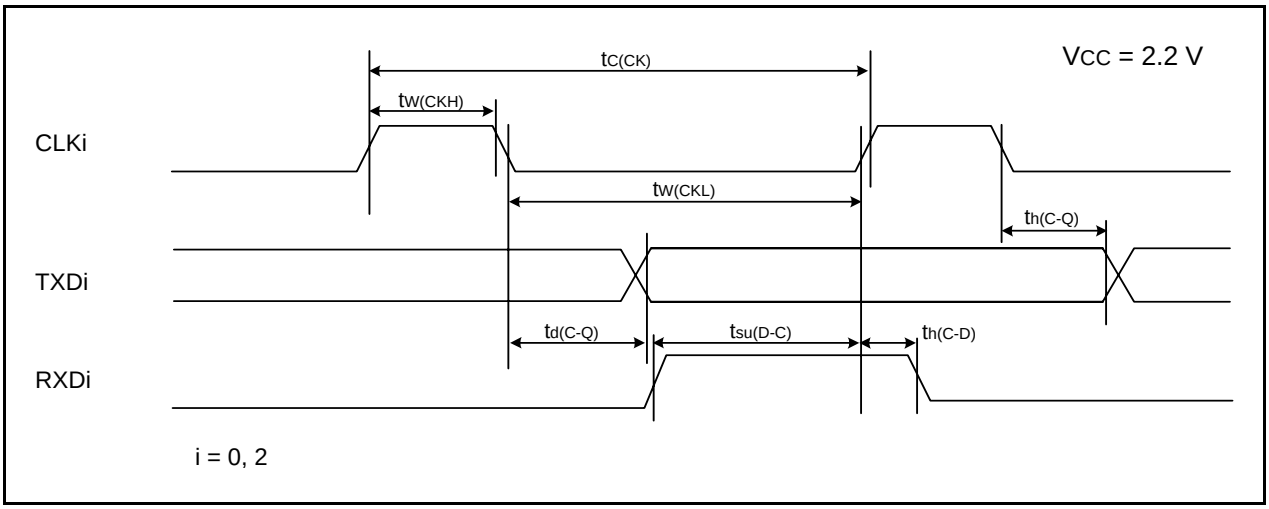


Figure 5.18 Serial Interface Timing Diagram when VCC = 2.2 V

Table 5.33 External Interrupt $\overline{INTi}$ (i = 0, 1, 3) Input, Key Input Interrupt $\overline{KIi}$ (i = 0 to 3)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{W(INH)}$	$\overline{INTi}$ input “H” width, $\overline{KIi}$ input “H” width	1000 (1)	–	ns
$t_{W(INL)}$	$\overline{INTi}$ input “L” width, $\overline{KIi}$ input “L” width	1000 (2)	–	ns

Notes:
1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

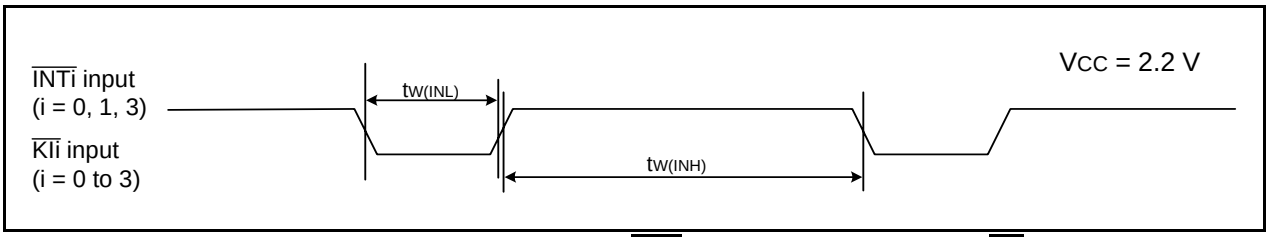


Figure 5.19 Input Timing for External Interrupt $\overline{INTi}$ and Key Input Interrupt $\overline{KIi}$ when Vcc = 2.2 V

REVISION HISTORY	R8C/32C Group Datasheet

Rev.	Date	Description	
		Page	Summary
0.10	Sep. 01, 2009	–	First Edition issued
1.00	Aug. 24, 2010	All	“Preliminary” and “Under development” deleted
		4	Table1.3 revised
		26 to 51	“5. Electrical Characteristics” added

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