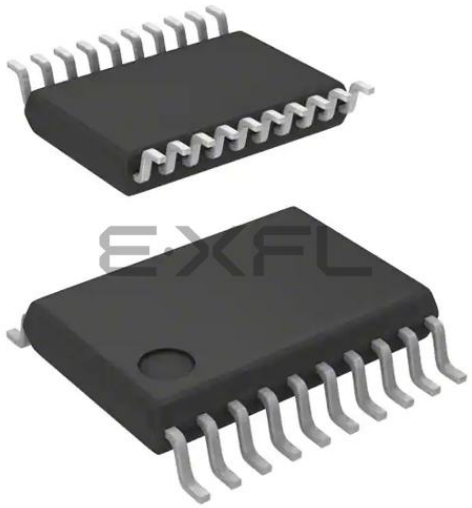
# Renesas Electronics America Inc - R5F21321CNSP#U0 Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Not For New Designs |
| Core Processor | R8C |
| Core Size | 16-Bit |
| Speed | 20MHz |
| Connectivity | I²C, LINbus, SIO, SSU, UART/USART |
| Peripherals | POR, PWM, Voltage Detect, WDT |
| Number of I/O | 15 |
| Program Memory Size | 4KB (4K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 4K x 8 |
| RAM Size | 512 x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.8V ~ 5.5V |
| Data Converters | A/D 4x10b |
| Oscillator Type | Internal |
| Operating Temperature | -20°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 20-LSSOP (0.173", 4.40mm Width) |
| Supplier Device Package | 20-LSSOP |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f21321cnsp-u0 |

### 1.1.2 Specifications

Tables 1.1 and 1.2 outline the Specifications for R8C/32C Group.

**Table 1.1 Specifications for R8C/32C Group (1)**

| Item | Function | Specification |
|---|---|---|
| CPU | Central processing unit | R8C CPU core<br>• Number of fundamental instructions: 89<br>• Minimum instruction execution time:<br>50 ns (f(XIN) = 20 MHz, VCC = 2.7 to 5.5 V)<br>200 ns (f(XIN) = 5 MHz, VCC = 1.8 to 5.5 V)<br>• Multiplier: 16 bits × 16 bits → 32 bits<br>• Multiply-accumulate instruction: 16 bits × 16 bits + 32 bits → 32 bits<br>• Operation mode: Single-chip mode (address space: 1 Mbyte) |
| Memory | ROM, RAM, Data flash | Refer to **Table 1.3 Product List for** R8C/32C Group. |
| Power Supply Voltage Detection | Voltage detection circuit | • Power-on reset<br>• Voltage detection 3 (detection level of voltage detection 0 and voltage detection 1 selectable) |
| I/O Ports | Programmable I/O ports | • Input-only: 1 pin<br>• CMOS I/O ports: 15, selectable pull-up resistor<br>• High current drive ports: 15 |
| Clock | Clock generation circuits | 4 circuits: XIN clock oscillation circuit,<br>XCIN clock oscillation circuit (32 kHz)<br>High-speed on-chip oscillator (with frequency adjustment function),<br>Low-speed on-chip oscillator,<br>• Oscillation stop detection: XIN clock oscillation stop detection function<br>• Frequency divider circuit: Dividing selectable 1, 2, 4, 8, and 16<br>• Low power consumption modes:<br>Standard operating mode (high-speed clock, low-speed clock, high-speed on-chip oscillator, low-speed on-chip oscillator), wait mode, stop mode |
| | | Real-time clock (timer RE) |
| Interrupts | | • Number of interrupt vectors: 69<br>• External Interrupt: 7 ($\overline{\text{INT}}$ × 3, Key input × 4)<br>• Priority levels: 7 levels |
| Watchdog Timer | | • 14 bits × 1 (with prescaler)<br>• Reset start selectable<br>• Low-speed on-chip oscillator for watchdog timer selectable |
| DTC (Data Transfer Controller) | | • 1 channel<br>• Activation sources: 21<br>• Transfer modes: 2 (normal mode, repeat mode) |
| Timer | Timer RA | 8 bits × 1 (with 8-bit prescaler)<br>Timer mode (period timer), pulse output mode (output level inverted every period), event counter mode, pulse width measurement mode, pulse period measurement mode |
| | Timer RB | 8 bits × 1 (with 8-bit prescaler)<br>Timer mode (period timer), programmable waveform generation mode (PWM output), programmable one-shot generation mode, programmable wait one-shot generation mode |
| | Timer RC | 16 bits × 1 (with 4 capture/compare registers)<br>Timer mode (input capture function, output compare function), PWM mode (output 3 pins), PWM2 mode (PWM output pin) |
| | Timer RE | 8 bits × 1<br>Real-time clock mode (count seconds, minutes, hours, days of week), output compare mode |

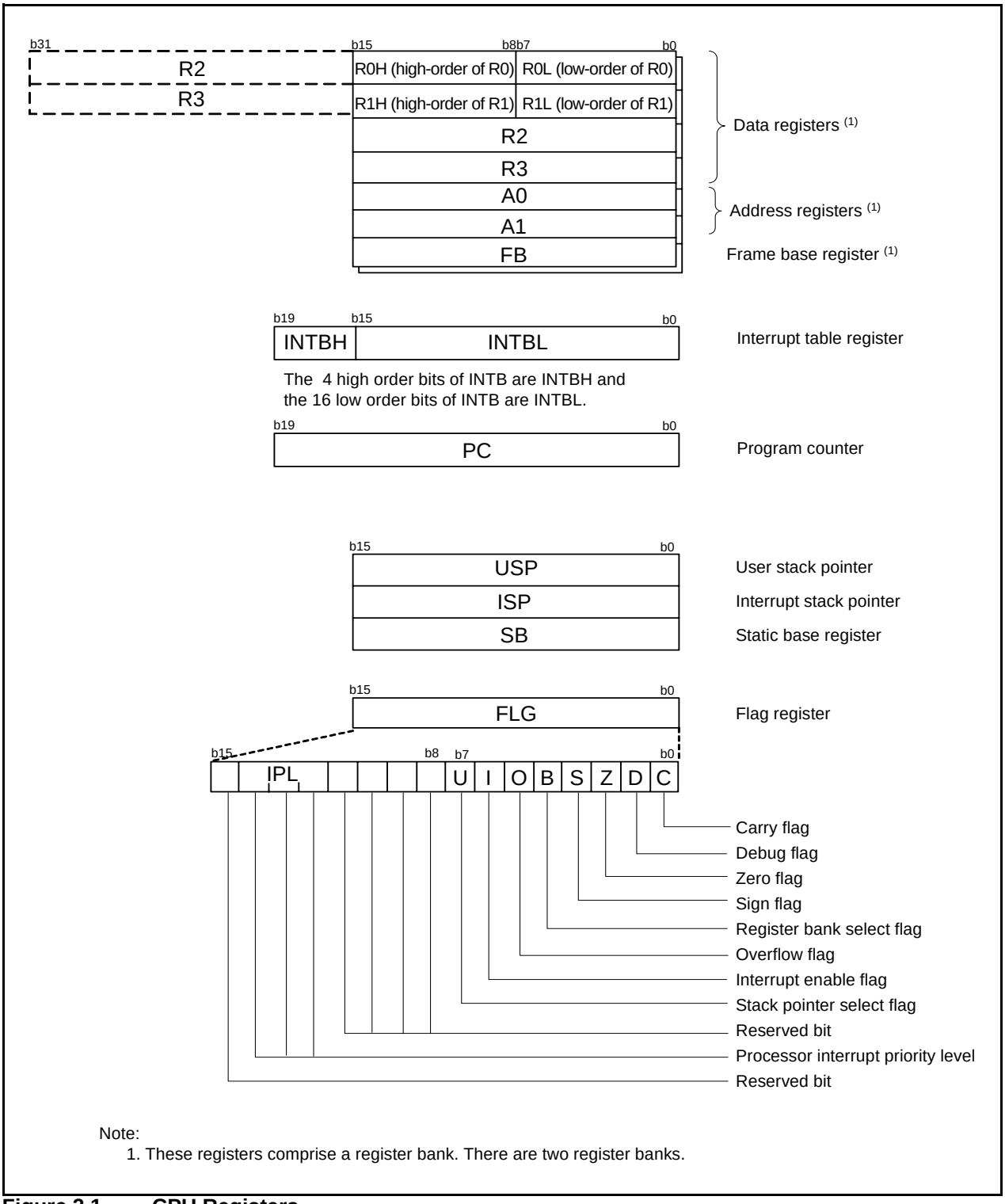
**Table 1.4 Pin Name Information by Pin Number**

| Pin Number | Control Pin | Port | I/O Pin Functions for Peripheral Modules | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | Interrupt | Timer | Serial Interface | SSU | $I^2C$ bus | A/D Converter, Comparator B |
| 1 | | P4_2 | | | | | | VREF |
| 2 | MODE | | | | | | | |
| 3 | $\overline{\text{RESET}}$ | | | | | | | |
| 4 | XOUT(/XCOUT) | P4_7 | | | | | | |
| 5 | VSS/AVSS | | | | | | | |
| 6 | XIN(/XCIN) | P4_6 | | | | | | |
| 7 | VCC/AVCC | | | | | | | |
| 8 | | P3_7 | | TRAO | (RXD2/SCL2/ TXD2/SDA2) | SSO | SDA | |
| 9 | | P3_5 | | (TRCIOD) | (CLK2) | SSCK | SCL | |
| 10 | | P3_4 | | (TRCIOC) | (RXD2/SCL2/ TXD2/SDA2) | SSI | | IVREF3 |
| 11 | | P3_3 | $\overline{\text{INT3}}$ | (TRCCLK) | ($\overline{\text{CTS2}}$/$\overline{\text{RTS2}}$) | $\overline{\text{SCS}}$ | | IVCMP3 |
| 12 | | P4_5 | $\overline{\text{INT0}}$ | | (RXD2/SCL2) | | | $\overline{\text{ADTRG}}$ |
| 13 | | P1_7 | $\overline{\text{INT1}}$ | (TRAIO) | | | | IVCMP1 |
| 14 | | P1_6 | | | (CLK0) | | | IVREF1 |
| 15 | | P1_5 | ($\overline{\text{INT1}}$) | (TRAIO) | (RXD0) | | | |
| 16 | | P1_4 | | (TRCCLK) | (TXD0) | | | |
| 17 | | P1_3 | $\overline{\text{KI3}}$ | TRBO (/TRCIOC) | | | | AN11 |
| 18 | | P1_2 | $\overline{\text{KI2}}$ | (TRCIOB) | | | | AN10 |
| 19 | | P1_1 | $\overline{\text{KI1}}$ | (TRCIOA/ TRCTRG) | | | | AN9 |
| 20 | | P1_0 | $\overline{\text{KI0}}$ | (TRCIOD) | | | | AN8 |

Note:
1. Can be assigned to the pin in parentheses by a program.

# 2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU Registers. The CPU contains 13 registers. R0, R1, R2, R3, A0, A1, and FB configure a register bank. There are two sets of register bank.




Note:
1. These registers comprise a register bank. There are two register banks.

**Figure 2.1 CPU Registers**

### 2.8.7 Interrupt Enable Flag (I)

The I flag enables maskable interrupts.
Interrupts are disabled when the I flag is set to 0, and are enabled when the I flag is set to 1. The I flag is set to 0 when an interrupt request is acknowledged.

### 2.8.8 Stack Pointer Select Flag (U)

ISP is selected when the U flag is set to 0; USP is selected when the U flag is set to 1.
The U flag is set to 0 when a hardware interrupt request is acknowledged or the INT instruction of software interrupt numbers 0 to 31 is executed.

### 2.8.9 Processor Interrupt Priority Level (IPL)

IPL is 3 bits wide and assigns processor interrupt priority levels from level 0 to level 7.
If a requested interrupt has higher priority than IPL, the interrupt is enabled.

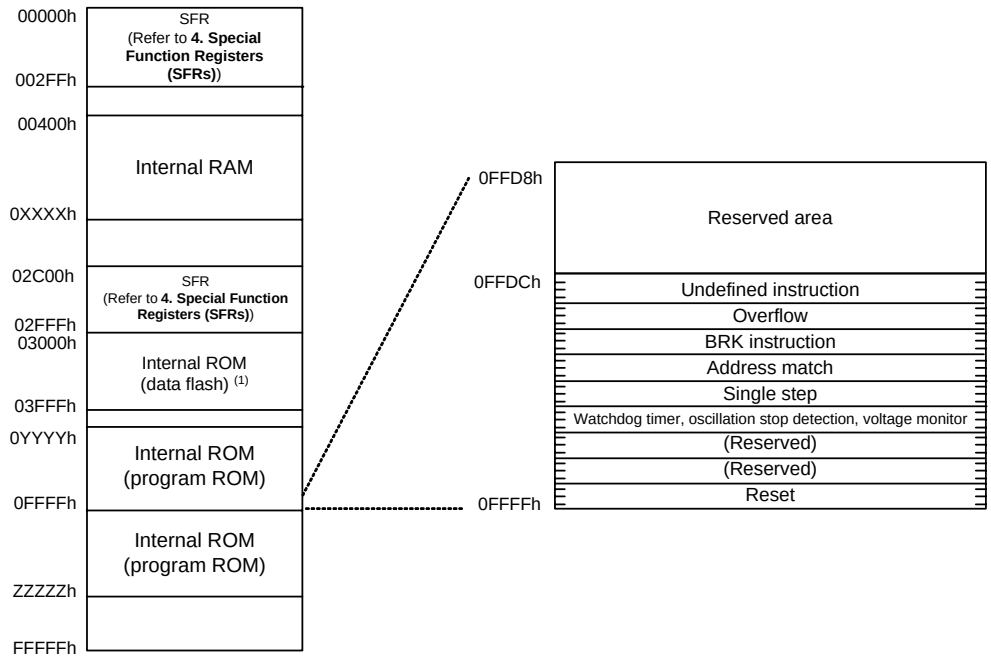
### 2.8.10 Reserved Bit

If necessary, set to 0. When read, the content is undefined.

# 3. Memory

## 3.1 R8C/32C Group

Figure 3.1 is a Memory Map of R8C/32C Group. The R8C/32C Group has a 1-Mbyte address space from addresses 00000h to FFFFFh. The internal ROM (program ROM) is allocated lower addresses, beginning with address 0FFFFh. For example, a 16-Kbyte internal ROM area is allocated addresses 0C000h to 0FFFFh.
The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. The starting address of each interrupt routine is stored here.
The internal ROM (data flash) is allocated addresses 03000h to 03FFFh.
The internal RAM is allocated higher addresses, beginning with address 00400h. For example, a 1.5-Kbyte internal RAM area is allocated addresses 00400h to 009FFh. The internal RAM is used not only for data storage but also as a stack area when a subroutine is called or when an interrupt request is acknowledged.
Special function registers (SFRs) are allocated addresses 00000h to 002FFh and 02C00h to 02FFFh. Peripheral function control registers are allocated here. All unallocated spaces within the SFRs are reserved and cannot be accessed by users.




Notes:
1. Data flash indicates block A (1 Kbyte), block B (1 Kbyte), block C (1 Kbyte), and block D (1 Kbyte).
2. The blank areas are reserved and cannot be accessed by users.

| Part Number | Internal ROM | | | Internal RAM | |
|---|---|---|---|---|---|
| | Size | Address 0YYYYh | Address ZZZZZh | Size | Address 0XXXXh |
| R5F21321CNFP, R5F21321CDFP | 4 Kbytes | 0F000h | – | 512 bytes | 005FFh |
| R5F21322CNFP, R5F21322CDFP | 8 Kbytes | 0E000h | – | 1 Kbyte | 007FFh |
| R5F21324CNFP, R5F21324CDFP | 16 Kbytes | 0C000h | – | 1.5 Kbytes | 009FFh |

**Figure 3.1 Memory Map of R8C/32C Group**

# 4. Special Function Registers (SFRs)

An SFR (special function register) is a control register for a peripheral function. Tables 4.1 to 4.12 list the special function registers and Table 4.13 lists the ID Code Areas and Option Function Select Area.

**Table 4.1 SFR Information (1) (1)**

| Address | Register | Symbol | After Reset |
|---|---|---|---|
| 0000h | | | |
| 0001h | | | |
| 0002h | | | |
| 0003h | | | |
| 0004h | Processor Mode Register 0 | PM0 | 00h |
| 0005h | Processor Mode Register 1 | PM1 | 00h |
| 0006h | System Clock Control Register 0 | CM0 | 00101000b |
| 0007h | System Clock Control Register 1 | CM1 | 00100000b |
| 0008h | Module Standby Control Register | MSTCR | 00h |
| 0009h | System Clock Control Register 3 | CM3 | 00h |
| 000Ah | Protect Register | PRCR | 00h |
| 000Bh | Reset Source Determination Register | RSTFR | 0XXXXXXXb (2) |
| 000Ch | Oscillation Stop Detection Register | OCD | 00000100b |
| 000Dh | Watchdog Timer Reset Register | WDTR | XXh |
| 000Eh | Watchdog Timer Start Register | WDTS | XXh |
| 000Fh | Watchdog Timer Control Register | WDTC | 00111111b |
| 0010h | | | |
| 0011h | | | |
| 0012h | | | |
| 0013h | | | |
| 0014h | | | |
| 0015h | High-Speed On-Chip Oscillator Control Register 7 | FRA7 | When shipping |
| 0016h | | | |
| 0017h | | | |
| 0018h | | | |
| 0019h | | | |
| 001Ah | | | |
| 001Bh | | | |
| 001Ch | Count Source Protection Mode Register | CSPR | 00h<br>10000000b (3) |
| 001Dh | | | |
| 001Eh | | | |
| 001Fh | | | |
| 0020h | | | |
| 0021h | | | |
| 0022h | | | |
| 0023h | High-Speed On-Chip Oscillator Control Register 0 | FRA0 | 00h |
| 0024h | High-Speed On-Chip Oscillator Control Register 1 | FRA1 | When shipping |
| 0025h | High-Speed On-Chip Oscillator Control Register 2 | FRA2 | 00h |
| 0026h | On-Chip Reference Voltage Control Register | OCVREFCR | 00h |
| 0027h | | | |
| 0028h | Clock Prescaler Reset Flag | CPSRF | 00h |
| 0029h | High-Speed On-Chip Oscillator Control Register 4 | FRA4 | When Shipping |
| 002Ah | High-Speed On-Chip Oscillator Control Register 5 | FRA5 | When Shipping |
| 002Bh | High-Speed On-Chip Oscillator Control Register 6 | FRA6 | When Shipping |
| 002Ch | | | |
| 002Dh | | | |
| 002Eh | | | |
| 002Fh | High-Speed On-Chip Oscillator Control Register 3 | FRA3 | When shipping |
| 0030h | Voltage Monitor Circuit Control Register | CMPA | 00h |
| 0031h | Voltage Monitor Circuit Edge Select Register | VCAC | 00h |
| 0032h | | | |
| 0033h | Voltage Detect Register 1 | VCA1 | 00001000b |
| 0034h | Voltage Detect Register 2 | VCA2 | 00h (4)<br>00100000b (5) |
| 0035h | | | |
| 0036h | Voltage Detection 1 Level Select Register | VD1LS | 00000111b |
| 0037h | | | |
| 0038h | Voltage Monitor 0 Circuit Control Register | VW0C | 1100X010b (4)<br>1100X011b (5) |
| 0039h | Voltage Monitor 1 Circuit Control Register | VW1C | 10001010b |

X: Undefined

Notes:
1. The blank areas are reserved and cannot be accessed by users.
2. The CWR bit in the RSTFR register is set to 0 after power-on and voltage monitor 0 reset. Hardware reset, software reset, or watchdog timer reset does not affect this bit.
3. The CSPROINI bit in the OFS register is set to 0.
4. The LVDAS bit in the OFS register is set to 1.
5. The LVDAS bit in the OFS register is set to 0.

**Table 4.2 SFR Information (2) (1)**

| Address | Register | Symbol | After Reset |
|---|---|---|---|
| 003Ah | Voltage Monitor 2 Circuit Control Register | VW2C | 10000010b |
| 003Bh | | | |
| 003Ch | | | |
| 003Dh | | | |
| 003Eh | | | |
| 003Fh | | | |
| 0040h | | | |
| 0041h | Flash Memory Ready Interrupt Control Register | FMRDYIC | XXXXX000b |
| 0042h | | | |
| 0043h | | | |
| 0044h | | | |
| 0045h | | | |
| 0046h | | | |
| 0047h | Timer RC Interrupt Control Register | TRCIC | XXXXX000b |
| 0048h | | | |
| 0049h | | | |
| 004Ah | Timer RE Interrupt Control Register | TREIC | XXXXX000b |
| 004Bh | UART2 Transmit Interrupt Control Register | S2TIC | XXXXX000b |
| 004Ch | UART2 Receive Interrupt Control Register | S2RIC | XXXXX000b |
| 004Dh | Key Input Interrupt Control Register | KUPIC | XXXXX000b |
| 004Eh | A/D Conversion Interrupt Control Register | ADIC | XXXXX000b |
| 004Fh | SSU Interrupt Control Register / IIC bus Interrupt Control Register (2) | SSUIC / IICIC | XXXXX000b |
| 0050h | | | |
| 0051h | UART0 Transmit Interrupt Control Register | S0TIC | XXXXX000b |
| 0052h | UART0 Receive Interrupt Control Register | S0RIC | XXXXX000b |
| 0053h | | | |
| 0054h | | | |
| 0055h | | | |
| 0056h | Timer RA Interrupt Control Register | TRAIC | XXXXX000b |
| 0057h | | | |
| 0058h | Timer RB Interrupt Control Register | TRBIC | XXXXX000b |
| 0059h | INT1 Interrupt Control Register | INT1IC | XX00X000b |
| 005Ah | INT3 Interrupt Control Register | INT3IC | XX00X000b |
| 005Bh | | | |
| 005Ch | | | |
| 005Dh | INT0 Interrupt Control Register | INT0IC | XX00X000b |
| 005Eh | UART2 Bus Collision Detection Interrupt Control Register | U2BCNIC | XXXXX000b |
| 005Fh | | | |
| 0060h | | | |
| 0061h | | | |
| 0062h | | | |
| 0063h | | | |
| 0064h | | | |
| 0065h | | | |
| 0066h | | | |
| 0067h | | | |
| 0068h | | | |
| 0069h | | | |
| 006Ah | | | |
| 006Bh | | | |
| 006Ch | | | |
| 006Dh | | | |
| 006Eh | | | |
| 006Fh | | | |
| 0070h | | | |
| 0071h | | | |
| 0072h | Voltage Monitor 1 Interrupt Control Register | VCMP1IC | XXXXX000b |
| 0073h | Voltage Monitor 2 Interrupt Control Register | VCMP2IC | XXXXX000b |
| 0074h | | | |
| 0075h | | | |
| 0076h | | | |
| 0077h | | | |
| 0078h | | | |
| 0079h | | | |
| 007Ah | | | |
| 007Bh | | | |
| 007Ch | | | |
| 007Dh | | | |
| 007Eh | | | |
| 007Fh | | | |

X: Undefined

Notes:
1. The blank areas are reserved and cannot be accessed by users.
2. Selectable by the IICSEL bit in the SSUIICSR register.

**Table 4.5 SFR Information (5) (1)**

| Address | Register | Symbol | After Reset |
|---|---|---|---|
| 0100h | Timer RA Control Register | TRACR | 00h |
| 0101h | Timer RA I/O Control Register | TRAIOC | 00h |
| 0102h | Timer RA Mode Register | TRAMR | 00h |
| 0103h | Timer RA Prescaler Register | TRAPRE | FFh |
| 0104h | Timer RA Register | TRA | FFh |
| 0105h | LIN Control Register 2 | LINCR2 | 00h |
| 0106h | LIN Control Register | LINCR | 00h |
| 0107h | LIN Status Register | LINST | 00h |
| 0108h | Timer RB Control Register | TRBCR | 00h |
| 0109h | Timer RB One-Shot Control Register | TRBOCR | 00h |
| 010Ah | Timer RB I/O Control Register | TRBIOC | 00h |
| 010Bh | Timer RB Mode Register | TRBMR | 00h |
| 010Ch | Timer RB Prescaler Register | TRBPRE | FFh |
| 010Dh | Timer RB Secondary Register | TRBSC | FFh |
| 010Eh | Timer RB Primary Register | TRBPR | FFh |
| 010Fh | | | |
| 0110h | | | |
| 0111h | | | |
| 0112h | | | |
| 0113h | | | |
| 0114h | | | |
| 0115h | | | |
| 0116h | | | |
| 0117h | | | |
| 0118h | Timer RE Second Data Register / Counter Data Register | TRESEC | 00h |
| 0119h | Timer RE Minute Data Register / Compare Data Register | TREMIN | 00h |
| 011Ah | Timer RE Hour Data Register | TREHR | 00h |
| 011Bh | Timer RE Day of Week Data Register | TREWK | 00h |
| 011Ch | Timer RE Control Register 1 | TRECR1 | 00h |
| 011Dh | Timer RE Control Register 2 | TRECR2 | 00h |
| 011Eh | Timer RE Count Source Select Register | TRECSR | 00001000b |
| 011Fh | | | |
| 0120h | Timer RC Mode Register | TRCMR | 01001000b |
| 0121h | Timer RC Control Register 1 | TRCCR1 | 00h |
| 0122h | Timer RC Interrupt Enable Register | TRCIER | 01110000b |
| 0123h | Timer RC Status Register | TRCSR | 01110000b |
| 0124h | Timer RC I/O Control Register 0 | TRCIOR0 | 10001000b |
| 0125h | Timer RC I/O Control Register 1 | TRCIOR1 | 10001000b |
| 0126h | Timer RC Counter | TRC | 00h |
| 0127h | | | 00h |
| 0128h | Timer RC General Register A | TRCGRA | FFh |
| 0129h | | | FFh |
| 012Ah | Timer RC General Register B | TRCGRB | FFh |
| 012Bh | | | FFh |
| 012Ch | Timer RC General Register C | TRCGRC | FFh |
| 012Dh | | | FFh |
| 012Eh | Timer RC General Register D | TRCGRD | FFh |
| 012Fh | | | FFh |
| 0130h | Timer RC Control Register 2 | TRCCR2 | 00011000b |
| 0131h | Timer RC Digital Filter Function Select Register | TRCDF | 00h |
| 0132h | Timer RC Output Master Enable Register | TRCOER | 01111111b |
| 0133h | Timer RC Trigger Control Register | TRCADCR | 00h |
| 0134h | | | |
| 0135h | | | |
| 0136h | | | |
| 0137h | | | |
| 0138h | | | |
| 0139h | | | |
| 013Ah | | | |
| 013Bh | | | |
| 013Ch | | | |
| 013Dh | | | |
| 013Eh | | | |
| 013Fh | | | |

Note:
1. The blank areas are reserved and cannot be accessed by users.

**Table 4.7 SFR Information (7) (1)**

| Address | Register | Symbol | After Reset |
|---|---|---|---|
| 0180h | Timer RA Pin Select Register | TRASR | 00h |
| 0181h | Timer RC Pin Select Register | TRBRCSR | 00h |
| 0182h | Timer RC Pin Select Register 0 | TRCPSR0 | 00h |
| 0183h | Timer RC Pin Select Register 1 | TRCPSR1 | 00h |
| 0184h | | | |
| 0185h | | | |
| 0186h | | | |
| 0187h | | | |
| 0188h | UART0 Pin Select Register | U0SR | 00h |
| 0189h | | | |
| 018Ah | UART2 Pin Select Register 0 | U2SR0 | 00h |
| 018Bh | UART2 Pin Select Register 1 | U2SR1 | 00h |
| 018Ch | SSU / IIC Pin Select Register | SSUIICSR | 00h |
| 018Dh | | | |
| 018Eh | INT Interrupt Input Pin Select Register | INTSR | 00h |
| 018Fh | I/O Function Pin Select Register | PINSR | 00h |
| 0190h | | | |
| 0191h | | | |
| 0192h | | | |
| 0193h | SS Bit Counter Register | SSBR | 11111000b |
| 0194h | SS Transmit Data Register L / IIC bus Transmit Data Register (2) | SSTDR / ICDRT | FFh |
| 0195h | SS Transmit Data Register H (2) | SSTDRH | FFh |
| 0196h | SS Receive Data Register L / IIC bus Receive Data Register (2) | SSRDR / ICDRR | FFh |
| 0197h | SS Receive Data Register H (2) | SSRDRH | FFh |
| 0198h | SS Control Register H / IIC bus Control Register 1 (2) | SSCRH / ICCR1 | 00h |
| 0199h | SS Control Register L / IIC bus Control Register 2 (2) | SSCRL / ICCR2 | 01111101b |
| 019Ah | SS Mode Register / IIC bus Mode Register (2) | SSMR / ICMR | 00010000b / 00011000b |
| 019Bh | SS Enable Register / IIC bus Interrupt Enable Register (2) | SSER / ICIER | 00h |
| 019Ch | SS Status Register / IIC bus Status Register (2) | SSSR / ICSR | 00h / 0000X000b |
| 019Dh | SS Mode Register 2 / Slave Address Register (2) | SSMR2 / SAR | 00h |
| 019Eh | | | |
| 019Fh | | | |
| 01A0h | | | |
| 01A1h | | | |
| 01A2h | | | |
| 01A3h | | | |
| 01A4h | | | |
| 01A5h | | | |
| 01A6h | | | |
| 01A7h | | | |
| 01A8h | | | |
| 01A9h | | | |
| 01AAh | | | |
| 01ABh | | | |
| 01ACh | | | |
| 01ADh | | | |
| 01AEh | | | |
| 01AFh | | | |
| 01B0h | | | |
| 01B1h | | | |
| 01B2h | Flash Memory Status Register | FST | 10000X00b |
| 01B3h | | | |
| 01B4h | Flash Memory Control Register 0 | FMR0 | 00h |
| 01B5h | Flash Memory Control Register 1 | FMR1 | 00h |
| 01B6h | Flash Memory Control Register 2 | FMR2 | 00h |
| 01B7h | | | |
| 01B8h | | | |
| 01B9h | | | |
| 01BAh | | | |
| 01BBh | | | |
| 01BCh | | | |
| 01BDh | | | |
| 01BEh | | | |
| 01BFh | | | |

X: Undefined

Notes:
1. The blank areas are reserved and cannot be accessed by users.
2. Selectable by the IICSEL bit in the SSUIICSR register.

**Table 4.8 SFR Information (8) (1)**

| Address | Register | Symbol | After Reset |
|---|---|---|---|
| 01C0h | Address Match Interrupt Register 0 | RMAD0 | XXh |
| 01C1h | | | XXh |
| 01C2h | | | 0000XXXXb |
| 01C3h | Address Match Interrupt Enable Register 0 | AIER0 | 00h |
| 01C4h | Address Match Interrupt Register 1 | RMAD1 | XXh |
| 01C5h | | | XXh |
| 01C6h | | | 0000XXXXb |
| 01C7h | Address Match Interrupt Enable Register 1 | AIER1 | 00h |
| 01C8h | | | |
| 01C9h | | | |
| 01CAh | | | |
| 01CBh | | | |
| 01CCh | | | |
| 01CDh | | | |
| 01CEh | | | |
| 01CFh | | | |
| 01D0h | | | |
| 01D1h | | | |
| 01D2h | | | |
| 01D3h | | | |
| 01D4h | | | |
| 01D5h | | | |
| 01D6h | | | |
| 01D7h | | | |
| 01D8h | | | |
| 01D9h | | | |
| 01DAh | | | |
| 01DBh | | | |
| 01DCh | | | |
| 01DDh | | | |
| 01DEh | | | |
| 01DFh | | | |
| 01E0h | Pull-Up Control Register 0 | PUR0 | 00h |
| 01E1h | Pull-Up Control Register 1 | PUR1 | 00h |
| 01E2h | | | |
| 01E3h | | | |
| 01E4h | | | |
| 01E5h | | | |
| 01E6h | | | |
| 01E7h | | | |
| 01E8h | | | |
| 01E9h | | | |
| 01EAh | | | |
| 01EBh | | | |
| 01ECh | | | |
| 01EDh | | | |
| 01EEh | | | |
| 01EFh | | | |
| 01F0h | Port P1 Drive Capacity Control Register | P1DRR | 00h |
| 01F1h | | | |
| 01F2h | Drive Capacity Control Register 0 | DRR0 | 00h |
| 01F3h | Drive Capacity Control Register 1 | DRR1 | 00h |
| 01F4h | | | |
| 01F5h | Input Threshold Control Register 0 | VLT0 | 00h |
| 01F6h | Input Threshold Control Register 1 | VLT1 | 00h |
| 01F7h | | | |
| 01F8h | Comparator B Control Register 0 | INTCMP | 00h |
| 01F9h | | | |
| 01FAh | External Input Enable Register 0 | INTEN | 00h |
| 01FBh | | | |
| 01FCh | INT Input Filter Select Register 0 | INTF | 00h |
| 01FDh | | | |
| 01FEh | Key Input Enable Register 0 | KIEN | 00h |
| 01FFh | | | |

X: Undefined
Note:
1. The blank areas are reserved and cannot be accessed by users.

**Table 4.9 SFR Information (9) (1)**

| Address | Register | Symbol | After Reset |
|---|---|---|---|
| 2C00h | DTC Transfer Vector Area | | XXh |
| 2C01h | DTC Transfer Vector Area | | XXh |
| 2C02h | DTC Transfer Vector Area | | XXh |
| 2C03h | DTC Transfer Vector Area | | XXh |
| 2C04h | DTC Transfer Vector Area | | XXh |
| 2C05h | DTC Transfer Vector Area | | XXh |
| 2C06h | DTC Transfer Vector Area | | XXh |
| 2C07h | DTC Transfer Vector Area | | XXh |
| 2C08h | DTC Transfer Vector Area | | XXh |
| 2C09h | DTC Transfer Vector Area | | XXh |
| 2C0Ah | DTC Transfer Vector Area | | XXh |
| : | DTC Transfer Vector Area | | XXh |
| : | DTC Transfer Vector Area | | XXh |
| 2C3Ah | DTC Transfer Vector Area | | XXh |
| 2C3Bh | DTC Transfer Vector Area | | XXh |
| 2C3Ch | DTC Transfer Vector Area | | XXh |
| 2C3Dh | DTC Transfer Vector Area | | XXh |
| 2C3Eh | DTC Transfer Vector Area | | XXh |
| 2C3Fh | DTC Transfer Vector Area | | XXh |
| 2C40h | DTC Control Data 0 | DTCD0 | XXh |
| 2C41h | | | XXh |
| 2C42h | | | XXh |
| 2C43h | | | XXh |
| 2C44h | | | XXh |
| 2C45h | | | XXh |
| 2C46h | | | XXh |
| 2C47h | | | XXh |
| 2C48h | DTC Control Data 1 | DTCD1 | XXh |
| 2C49h | | | XXh |
| 2C4Ah | | | XXh |
| 2C4Bh | | | XXh |
| 2C4Ch | | | XXh |
| 2C4Dh | | | XXh |
| 2C4Eh | | | XXh |
| 2C4Fh | | | XXh |
| 2C50h | DTC Control Data 2 | DTCD2 | XXh |
| 2C51h | | | XXh |
| 2C52h | | | XXh |
| 2C53h | | | XXh |
| 2C54h | | | XXh |
| 2C55h | | | XXh |
| 2C56h | | | XXh |
| 2C57h | | | XXh |
| 2C58h | DTC Control Data 3 | DTCD3 | XXh |
| 2C59h | | | XXh |
| 2C5Ah | | | XXh |
| 2C5Bh | | | XXh |
| 2C5Ch | | | XXh |
| 2C5Dh | | | XXh |
| 2C5Eh | | | XXh |
| 2C5Fh | | | XXh |
| 2C60h | DTC Control Data 4 | DTCD4 | XXh |
| 2C61h | | | XXh |
| 2C62h | | | XXh |
| 2C63h | | | XXh |
| 2C64h | | | XXh |
| 2C65h | | | XXh |
| 2C66h | | | XXh |
| 2C67h | | | XXh |
| 2C68h | DTC Control Data 5 | DTCD5 | XXh |
| 2C69h | | | XXh |
| 2C6Ah | | | XXh |
| 2C6Bh | | | XXh |
| 2C6Ch | | | XXh |
| 2C6Dh | | | XXh |
| 2C6Eh | | | XXh |
| 2C6Fh | | | XXh |

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

**Table 5.2 Recommended Operating Conditions**

| Symbol | Parameter | | | | Conditions | Standard | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Min. | Typ. | Max. | |
| $V_{CC}$/$AV_{CC}$ | Supply voltage | | | | | 1.8 | – | 5.5 | V |
| $V_{SS}$/$AV_{SS}$ | Supply voltage | | | | | – | 0 | – | V |
| $V_{IH}$ | Input “H” voltage | Other than CMOS input | | | | 0.8 $V_{CC}$ | – | $V_{CC}$ | V |
| | | CMOS input | Input level switching function (I/O port) | Input level selection : 0.35 $V_{CC}$ | 4.0 V ≤ $V_{CC}$ ≤ 5.5 V | 0.5 $V_{CC}$ | – | $V_{CC}$ | V |
| | | | | | 2.7 V ≤ $V_{CC}$ < 4.0 V | 0.55 $V_{CC}$ | – | $V_{CC}$ | V |
| | | | | | 1.8 V ≤ $V_{CC}$ < 2.7 V | 0.65 $V_{CC}$ | – | $V_{CC}$ | V |
| | | | | Input level selection : 0.5 $V_{CC}$ | 4.0 V ≤ $V_{CC}$ ≤ 5.5 V | 0.65 $V_{CC}$ | – | $V_{CC}$ | V |
| | | | | | 2.7 V ≤ $V_{CC}$ < 4.0 V | 0.7 $V_{CC}$ | – | $V_{CC}$ | V |
| | | | | | 1.8 V ≤ $V_{CC}$ < 2.7 V | 0.8 $V_{CC}$ | – | $V_{CC}$ | V |
| | | | | Input level selection : 0.7 $V_{CC}$ | 4.0 V ≤ $V_{CC}$ ≤ 5.5 V | 0.85 $V_{CC}$ | – | $V_{CC}$ | V |
| | | | | | 2.7 V ≤ $V_{CC}$ < 4.0 V | 0.85 $V_{CC}$ | – | $V_{CC}$ | V |
| | | | | | 1.8 V ≤ $V_{CC}$ < 2.7 V | 0.85 $V_{CC}$ | – | $V_{CC}$ | V |
| | | External clock input (XOUT) | | | | 1.2 | – | $V_{CC}$ | V |
| VIL | Input “L” voltage | Other than CMOS input | | | | 0 | – | 0.2 $V_{CC}$ | V |
| | | CMOS input | Input level switching function (I/O port) | Input level selection : 0.35 $V_{CC}$ | 4.0 V ≤ $V_{CC}$ ≤ 5.5 V | 0 | – | 0.2 $V_{CC}$ | V |
| | | | | | 2.7 V ≤ $V_{CC}$ < 4.0 V | 0 | – | 0.2 $V_{CC}$ | V |
| | | | | | 1.8 V ≤ $V_{CC}$ < 2.7 V | 0 | – | 0.2 $V_{CC}$ | V |
| | | | | Input level selection : 0.5 $V_{CC}$ | 4.0 V ≤ $V_{CC}$ ≤ 5.5 V | 0 | – | 0.4 $V_{CC}$ | V |
| | | | | | 2.7 V ≤ $V_{CC}$ < 4.0 V | 0 | – | 0.3 $V_{CC}$ | V |
| | | | | | 1.8 V ≤ $V_{CC}$ < 2.7 V | 0 | – | 0.2 $V_{CC}$ | V |
| | | | | Input level selection : 0.7 $V_{CC}$ | 4.0 V ≤ $V_{CC}$ ≤ 5.5 V | 0 | – | 0.55 $V_{CC}$ | V |
| | | | | | 2.7 V ≤ $V_{CC}$ < 4.0 V | 0 | – | 0.45 $V_{CC}$ | V |
| | | | | | 1.8 V ≤ $V_{CC}$ < 2.7 V | 0 | – | 0.35 $V_{CC}$ | V |
| | | External clock input (XOUT) | | | | 0 | – | 0.4 | V |
| $I_{OH(sum)}$ | Peak sum output “H” current | Sum of all pins $I_{OH(peak)}$ | | | | – | – | –160 | mA |
| $I_{OH(sum)}$ | Average sum output “H” current | Sum of all pins $I_{OH(avg)}$ | | | | – | – | –80 | mA |
| $I_{OH(peak)}$ | Peak output “H” current | Drive capacity Low | | | | – | – | –10 | mA |
| | | Drive capacity High | | | | – | – | –40 | mA |
| $I_{OH(avg)}$ | Average output “H” current | Drive capacity Low | | | | – | – | –5 | mA |
| | | Drive capacity High | | | | – | – | –20 | mA |
| $I_{OL(sum)}$ | Peak sum output “L” current | Sum of all pins $I_{OL(peak)}$ | | | | – | – | 160 | mA |
| $I_{OL(sum)}$ | Average sum output “L” current | Sum of all pins $I_{OL(avg)}$ | | | | – | – | 80 | mA |
| $I_{OL(peak)}$ | Peak output “L” current | Drive capacity Low | | | | – | – | 10 | mA |
| | | Drive capacity High | | | | – | – | 40 | mA |
| $I_{OL(avg)}$ | Average output “L” current | Drive capacity Low | | | | – | – | 5 | mA |
| | | Drive capacity High | | | | – | – | 20 | mA |
| $f_{(XIN)}$ | XIN clock input oscillation frequency | | | | 2.7 V ≤ $V_{CC}$ ≤ 5.5 V | – | – | 20 | MHz |
| | | | | | 1.8 V ≤ $V_{CC}$ < 2.7 V | – | – | 5 | MHz |
| $f_{(XCIN)}$ | XCIN clock input oscillation frequency | | | | 1.8 V ≤ $V_{CC}$ ≤ 5.5 V | – | 32.768 | 50 | kHz |
| fOCO40M | When used as the count source for timer RC (3) | | | | 2.7 V ≤ $V_{CC}$ ≤ 5.5 V | 32 | – | 40 | MHz |
| fOCO-F | fOCO-F frequency | | | | 2.7 V ≤ $V_{CC}$ ≤ 5.5 V | – | – | 20 | MHz |
| | | | | | 1.8 V ≤ $V_{CC}$ < 2.7 V | – | – | 5 | MHz |
| – | System clock frequency | | | | 2.7 V ≤ $V_{CC}$ ≤ 5.5 V | – | – | 20 | MHz |
| | | | | | 1.8 V ≤ $V_{CC}$ < 2.7 V | – | – | 5 | MHz |
| $f_{(BCLK)}$ | CPU clock frequency | | | | 2.7 V ≤ $V_{CC}$ ≤ 5.5 V | – | – | 20 | MHz |
| | | | | | 1.8 V ≤ $V_{CC}$ < 2.7 V | – | – | 5 | MHz |

Notes:
1. $V_{CC}$ = 1.8 to 5.5 V and $T_{opr}$ = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.
2. The average output current indicates the average value of current measured during 100 ms.
3. fOCO40M can be used as the count source for timer RC in the range of $V_{CC}$ = 2.7 V to 5.5V.

**Table 5.6 Flash Memory (Data flash Block A to Block D) Electrical Characteristics**

| Symbol | Parameter | Conditions | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| – | Program/erase endurance (2) | | 10,000 (3) | – | – | times |
| – | Byte program time (program/erase endurance ≤ 1,000 times) | | – | 160 | 1,500 | µs |
| – | Byte program time (program/erase endurance > 1,000 times) | | – | 300 | 1,500 | µs |
| – | Block erase time (program/erase endurance ≤ 1,000 times) | | – | 0.2 | 1 | s |
| – | Block erase time (program/erase endurance > 1,000 times) | | – | 0.3 | 1 | s |
| $t_{d(SR-SUS)}$ | Time delay from suspend request until suspend | | – | – | 5 + CPU clock × 3 cycles | ms |
| – | Interval from erase start/restart until following suspend request | | 0 | – | – | µs |
| – | Time from suspend until erase restart | | – | – | 30+CPU clock × 1 cycle | µs |
| $t_{d(CMDRST-READY)}$ | Time from when command is forcibly terminated until reading is enabled | | – | – | 30+CPU clock × 1 cycle | µs |
| – | Program, erase voltage | | 2.7 | – | 5.5 | V |
| – | Read voltage | | 1.8 | – | 5.5 | V |
| – | Program, erase temperature | | –20 (7) | – | 85 | °C |
| – | Data hold time (8) | Ambient temperature = 55 °C | 20 | – | – | year |

Notes:
1. $V_{CC}$ = 2.7 to 5.5 V and $T_{opr}$ = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.
2. Definition of programming/erasure endurance
   The programming and erasure endurance is defined on a per-block basis.
   If the programming and erasure endurance is n (n = 10,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.
   However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
3. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
4. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. In addition, averaging the erasure endurance between blocks A to D can further reduce the actual erasure endurance. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
5. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
6. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
7. –40°C for D version.
8. The data hold time includes time that the power supply is off or the clock is not supplied.

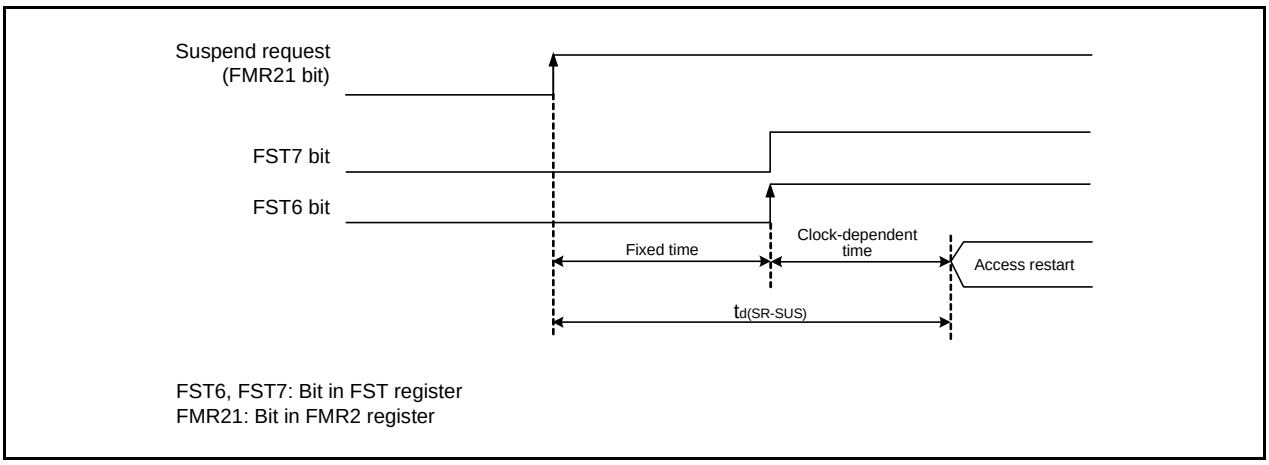
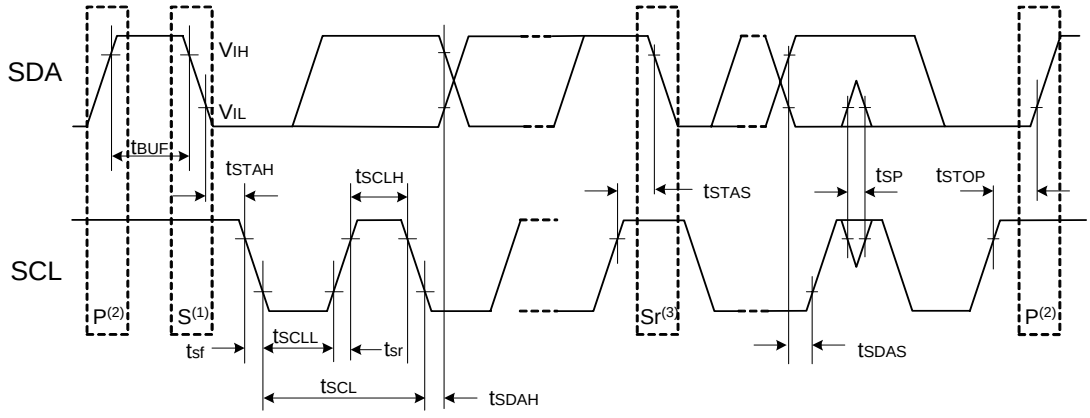



**Figure 5.2 Time delay until Suspend**

**Table 5.15 Timing Requirements of I²C bus Interface (1)**

| Symbol | Parameter | Condition | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $t_{SCL}$ | SCL input cycle time | | $12t_{CYC} + 600$ (2) | – | – | ns |
| $t_{SCLH}$ | SCL input “H” width | | $3t_{CYC} + 300$ (2) | – | – | ns |
| $t_{SCLL}$ | SCL input “L” width | | $5t_{CYC} + 500$ (2) | – | – | ns |
| $t_{sf}$ | SCL, SDA input fall time | | – | – | 300 | ns |
| $t_{SP}$ | SCL, SDA input spike pulse rejection time | | – | – | $1t_{CYC}$ (2) | ns |
| $t_{BUF}$ | SDA input bus-free time | | $5t_{CYC}$ (2) | – | – | ns |
| $t_{STAH}$ | Start condition input hold time | | $3t_{CYC}$ (2) | – | – | ns |
| $t_{STAS}$ | Retransmit start condition input setup time | | $3t_{CYC}$ (2) | – | – | ns |
| $t_{STOP}$ | Stop condition input setup time | | $3t_{CYC}$ (2) | – | – | ns |
| $t_{SDAS}$ | Data input setup time | | $1t_{CYC} + 40$ (2) | – | – | ns |
| $t_{SDAH}$ | Data input hold time | | 10 | – | – | ns |

Notes:
1. $V_{CC}$ = 1.8 to 5.5 V, $V_{SS}$ = 0 V and $T_{opr}$ = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.
2. $1t_{CYC} = 1/f1(s)$




Notes:
1. Start condition
2. Stop condition
3. Retransmit start condition

**Figure 5.7 I/O Timing of I²C bus Interface**

**Table 5.16 Electrical Characteristics (1) [4.2 V ≤ Vcc ≤ 5.5 V]**

| Symbol | Parameter | | Condition | | Standard | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min. | Typ. | Max. | |
| $V_{OH}$ | Output “H” voltage | Other than XOUT | Drive capacity High $V_{CC}$ = 5 V | $I_{OH}$ = –20 mA | $V_{CC}$ – 2.0 | – | $V_{CC}$ | V |
| | | | Drive capacity Low $V_{CC}$ = 5 V | $I_{OH}$ = –5 mA | $V_{CC}$ – 2.0 | – | $V_{CC}$ | V |
| | | XOUT | $V_{CC}$ = 5 V | $I_{OH}$ = –200 μA | 1.0 | – | $V_{CC}$ | V |
| $V_{OL}$ | Output “L” voltage | Other than XOUT | Drive capacity High $V_{CC}$ = 5 V | $I_{OL}$ = 20 mA | – | – | 2.0 | V |
| | | | Drive capacity Low $V_{CC}$ = 5 V | $I_{OL}$ = 5 mA | – | – | 2.0 | V |
| | | XOUT | $V_{CC}$ = 5 V | $I_{OL}$ = 200 μA | – | – | 0.5 | V |
| $V_{T+}$-$V_{T-}$ | Hysteresis | $\overline{INT0}$, $\overline{INT1}$, $\overline{INT3}$, $\overline{KI0}$, $\overline{KI1}$, $\overline{KI2}$, $\overline{KI3}$, TRAIO, TRBO, TRCIOA, TRCIOB, TRCIOC, TRCIOD, TRCTRG, $\overline{TRCCLK}$, $\overline{ADTRG}$, RXD0, RXD2, CLK0, CLK2, SSI, SCL, SDA, SSO | | | 0.1 | 1.2 | – | V |
| | | $\overline{RESET}$ | | | 0.1 | 1.2 | – | V |
| $I_{IH}$ | Input “H” current | | VI = 5 V, $V_{CC}$ = 5.0 V | | – | – | 5.0 | μA |
| $I_{IL}$ | Input “L” current | | VI = 0 V, $V_{CC}$ = 5.0 V | | – | – | –5.0 | μA |
| $R_{PULLUP}$ | Pull-up resistance | | VI = 0 V, $V_{CC}$ = 5.0 V | | 25 | 50 | 100 | kΩ |
| $R_{fXIN}$ | Feedback resistance | XIN | | | – | 0.3 | – | MΩ |
| $R_{fXCIN}$ | Feedback resistance | XCIN | | | – | 8 | – | MΩ |
| $V_{RAM}$ | RAM hold voltage | | During stop mode | | 1.8 | – | – | V |

Note:
1. 4.2 V ≤ $V_{CC}$ ≤ 5.5 V and $T_{opr}$ = –20 to 85°C (N version) / –40 to 85°C (D version), f(XIN) = 20 MHz, unless otherwise specified.

**Table 5.17 Electrical Characteristics (2) [3.3 V ≤ Vcc ≤ 5.5 V]**
**(Topr = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.)**

| Symbol | Parameter | Condition | | Standard | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | |
| Icc | Power supply current (Vcc = 3.3 to 5.5 V) Single-chip mode, output pins are open, other pins are Vss | High-speed clock mode | XIN = 20 MHz (square wave)<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>No division | – | 6.5 | 15 | mA |
| | | | XIN = 16 MHz (square wave)<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>No division | – | 5.3 | 12.5 | mA |
| | | | XIN = 10 MHz (square wave)<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>No division | – | 3.6 | – | mA |
| | | | XIN = 20 MHz (square wave)<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>Divide-by-8 | – | 3.0 | – | mA |
| | | | XIN = 16 MHz (square wave)<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>Divide-by-8 | – | 2.2 | – | mA |
| | | | XIN = 10 MHz (square wave)<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>Divide-by-8 | – | 1.5 | – | mA |
| | | High-speed on-chip oscillator mode | XIN clock off<br>High-speed on-chip oscillator on fOCO-F = 20 MHz<br>Low-speed on-chip oscillator on = 125 kHz<br>No division | – | 7.0 | 15 | mA |
| | | | XIN clock off<br>High-speed on-chip oscillator on fOCO-F = 20 MHz<br>Low-speed on-chip oscillator on = 125 kHz<br>Divide-by-8 | – | 3.0 | – | mA |
| | | | XIN clock off<br>High-speed on-chip oscillator on fOCO-F = 4 MHz<br>Low-speed on-chip oscillator on = 125 kHz<br>Divide-by-16<br>MSTIIC = MSTTRD = MSTTRC = 1 | – | 1 | – | mA |
| | | Low-speed on-chip oscillator mode | XIN clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>Divide-by-8, FMR27 = 1, VCA20 = 0 | – | 90 | 400 | µA |
| | | Low-speed clock mode | XIN clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator off<br>XCIN clock oscillator on = 32 kHz<br>No division<br>FMR27 = 1, VCA20 = 0 | – | 85 | 400 | µA |
| | | | XIN clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator off<br>XCIN clock oscillator on = 32 kHz<br>No division<br>Program operation on RAM<br>Flash memory off, FMSTP = 1, VCA20 = 0 | – | 47 | – | µA |
| | | Wait mode | XIN clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>While a WAIT instruction is executed<br>Peripheral clock operation<br>VCA27 = VCA26 = VCA25 = 0<br>VCA20 = 1 | – | 15 | 100 | µA |
| | | | XIN clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>While a WAIT instruction is executed<br>Peripheral clock off<br>VCA27 = VCA26 = VCA25 = 0<br>VCA20 = 1 | – | 4 | 90 | µA |
| | | | XIN clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator off<br>XCIN clock oscillator on = 32 kHz (peripheral clock off)<br>While a WAIT instruction is executed<br>VCA27 = VCA26 = VCA25 = 0<br>VCA20 = 1 | – | 3.5 | – | µA |
| | | Stop mode | XIN clock off, Topr = 25°C<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator off<br>CM10 = 1<br>Peripheral clock off<br>VCA27 = VCA26 = VCA25 = 0 | – | 2.0 | 5.0 | µA |
| | | | XIN clock off, Topr = 85°C<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator off<br>CM10 = 1<br>Peripheral clock off<br>VCA27 = VCA26 = VCA25 = 0 | – | 5.0 | – | µA |

**Table 5.20 Serial Interface**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(CK)}$ | CLKi input cycle time | 200 | – | ns |
| $t_{W(CKH)}$ | CLKi input “H” width | 100 | – | ns |
| $t_{W(CKL)}$ | CLKi input “L” width | 100 | – | ns |
| $t_{d(C-Q)}$ | TXDi output delay time | – | 50 | ns |
| $t_{h(C-Q)}$ | TXDi hold time | 0 | – | ns |
| $t_{su(D-C)}$ | RXDi input setup time | 50 | – | ns |
| $t_{h(C-D)}$ | RXDi input hold time | 90 | – | ns |

i = 0, 2

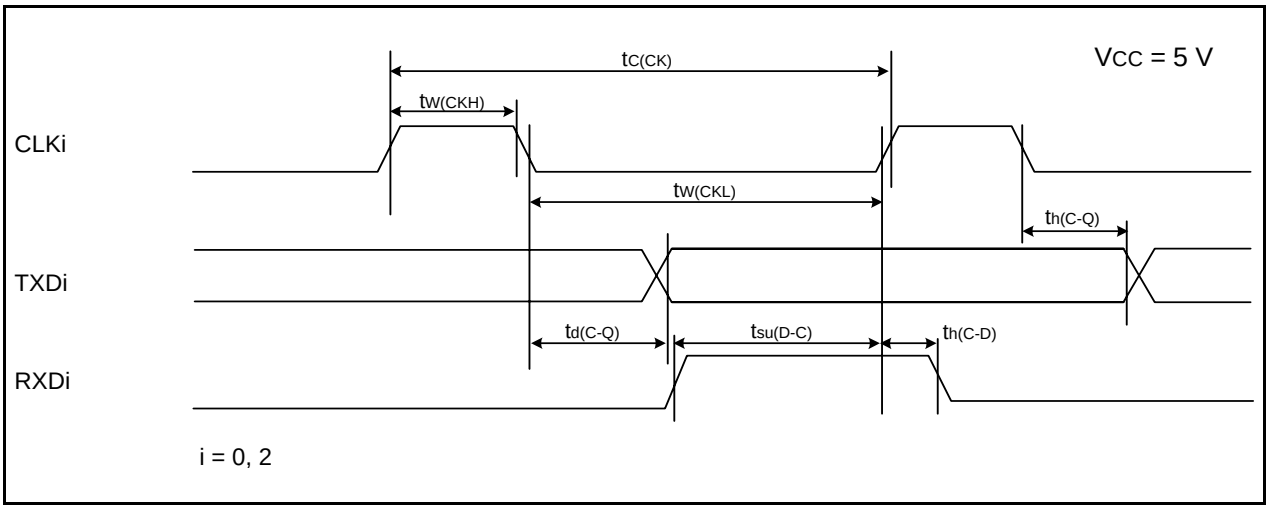



**Figure 5.10 Serial Interface Timing Diagram when VCC = 5 V**

**Table 5.21 External Interrupt $\overline{INTi}$ (i = 0, 1, 3) Input, Key Input Interrupt $\overline{KIi}$ (i = 0 to 3)**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{W(INH)}$ | $\overline{INTi}$ input “H” width, $\overline{KIi}$ input “H” width | 250 (1) | – | ns |
| $t_{W(INL)}$ | $\overline{INTi}$ input “L” width, $\overline{KIi}$ input “L” width | 250 (2) | – | ns |

Notes:
1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

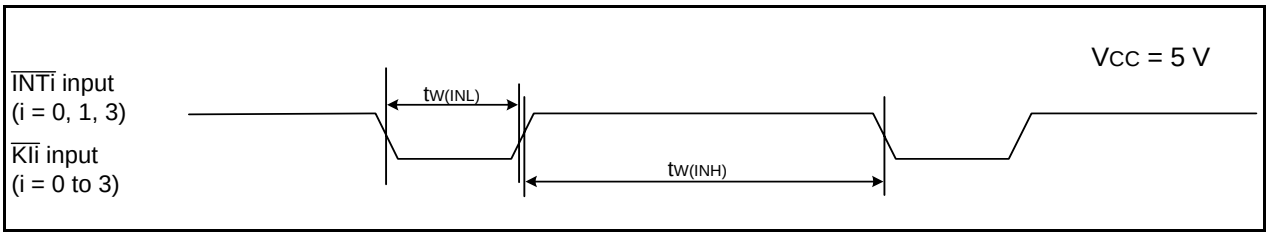



**Figure 5.11 Input Timing Diagram for External Interrupt INTi and Key Input Interrupt KIi when Vcc = 5 V**

**Table 5.26 Serial Interface**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(CK)}$ | CLKi input cycle time | 300 | – | ns |
| $t_{W(CKH)}$ | CLKi input “H” width | 150 | – | ns |
| $t_{W(CKL)}$ | CLKi Input “L” width | 150 | – | ns |
| $t_{d(C-Q)}$ | TXDi output delay time | – | 80 | ns |
| $t_{h(C-Q)}$ | TXDi hold time | 0 | – | ns |
| $t_{su(D-C)}$ | RXDi input setup time | 70 | – | ns |
| $t_{h(C-D)}$ | RXDi input hold time | 90 | – | ns |

i = 0, 2

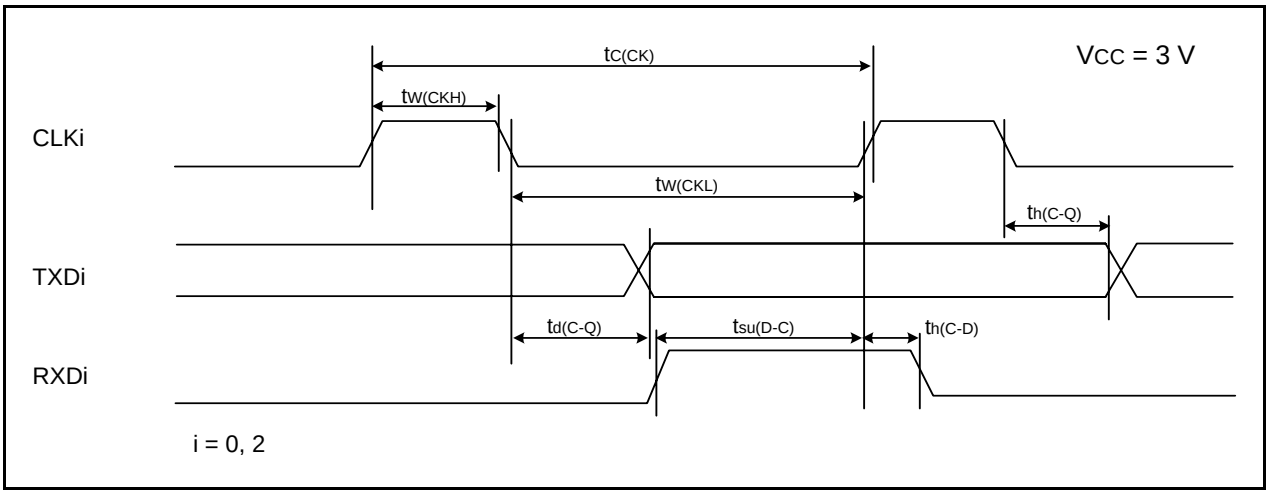



**Figure 5.14 Serial Interface Timing Diagram when VCC = 3 V**

**Table 5.27 External Interrupt $\overline{INTi}$ (i = 0, 1, 3) Input, Key Input Interrupt $\overline{KIi}$ (i = 0 to 3)**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{W(INH)}$ | $\overline{INTi}$ input “H” width, $\overline{KIi}$ input “H” width | 380 (1) | – | ns |
| $t_{W(INL)}$ | $\overline{INTi}$ input “L” width, $\overline{KIi}$ input “L” width | 380 (2) | – | ns |

Notes:
1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

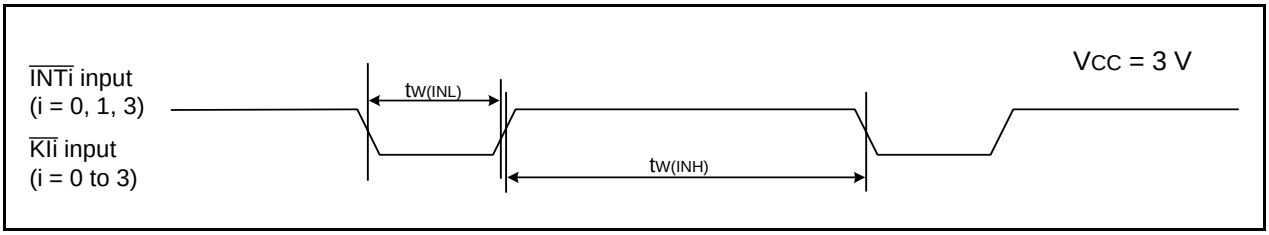



**Figure 5.15 Input Timing Diagram for External Interrupt INTi and Key Input Interrupt KIi when Vcc = 3 V**

**Table 5.29 Electrical Characteristics (6) [1.8 V ≤ Vcc < 2.7 V]**
**(Topr = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.)**

| Symbol | Parameter | Condition | | Standard | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | |
| ICC | Power supply current (VCC = 1.8 to 2.7 V) Single-chip mode, output pins are open, other pins are VSS | High-speed clock mode | XIN = 5 MHz (square wave)<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>No division | – | 2.2 | – | mA |
| | | | XIN = 5 MHz (square wave)<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>Divide-by-8 | – | 0.8 | – | mA |
| | | High-speed on-chip oscillator mode | XIN clock off<br>High-speed on-chip oscillator on fOCO-F = 5 MHz<br>Low-speed on-chip oscillator on = 125 kHz<br>No division | – | 2.5 | 10 | mA |
| | | | XIN clock off<br>High-speed on-chip oscillator on fOCO-F = 5 MHz<br>Low-speed on-chip oscillator on = 125 kHz<br>Divide-by-8 | – | 1.7 | – | mA |
| | | | XIN clock off<br>High-speed on-chip oscillator on fOCO-F = 4 MHz<br>Low-speed on-chip oscillator on = 125 kHz<br>Divide-by-16<br>MSTIIC = MSTTRD = MSTTRC = 1 | – | 1 | – | mA |
| | | Low-speed on-chip oscillator mode | XIN clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>Divide-by-8, FMR27 = 1, VCA20 = 0 | – | 90 | 300 | µA |
| | | Low-speed clock mode | XIN clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator off<br>XCIN clock oscillator on = 32 kHz<br>No division<br>FMR27 = 1, VCA20 = 0 | – | 80 | 350 | µA |
| | | | XIN clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator off<br>XCIN clock oscillator on = 32 kHz<br>No division<br>Program operation on RAM<br>Flash memory off, FMSTP = 1, VCA20 = 0 | – | 40 | – | µA |
| | | Wait mode | XIN clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>While a WAIT instruction is executed<br>Peripheral clock operation<br>VCA27 = VCA26 = VCA25 = 0<br>VCA20 = 1 | – | 15 | 90 | µA |
| | | | XIN clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>While a WAIT instruction is executed<br>Peripheral clock off<br>VCA27 = VCA26 = VCA25 = 0<br>VCA20 = 1 | – | 4 | 80 | µA |
| | | | XIN clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator off<br>XCIN clock oscillator on = 32 kHz (peripheral clock off)<br>While a WAIT instruction is executed<br>VCA27 = VCA26 = VCA25 = 0<br>VCA20 = 1 | – | 3.5 | – | µA |
| | | Stop mode | XIN clock off, Topr = 25°C<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator off<br>CM10 = 1<br>Peripheral clock off<br>VCA27 = VCA26 = VCA25 = 0 | – | 2.0 | 5 | µA |
| | | | XIN clock off, Topr = 85°C<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator off<br>CM10 = 1<br>Peripheral clock off<br>VCA27 = VCA26 = VCA25 = 0 | – | 5.0 | – | µA |

**Timing requirements**
**(Unless Otherwise Specified: $V_{CC}$ = 2.2 V, $V_{SS}$ = 0 V at Topr = 25°C)**

**Table 5.30 External Clock Input (XOUT, XCIN)**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(XOUT)}$ | XOUT input cycle time | 200 | – | ns |
| $t_{WH(XOUT)}$ | XOUT input “H” width | 90 | – | ns |
| $t_{WL(XOUT)}$ | XOUT input “L” width | 90 | – | ns |
| $t_{c(XCIN)}$ | XCIN input cycle time | 14 | – | µs |
| $t_{WH(XCIN)}$ | XCIN input “H” width | 7 | – | µs |
| $t_{WL(XCIN)}$ | XCIN input “L” width | 7 | – | µs |

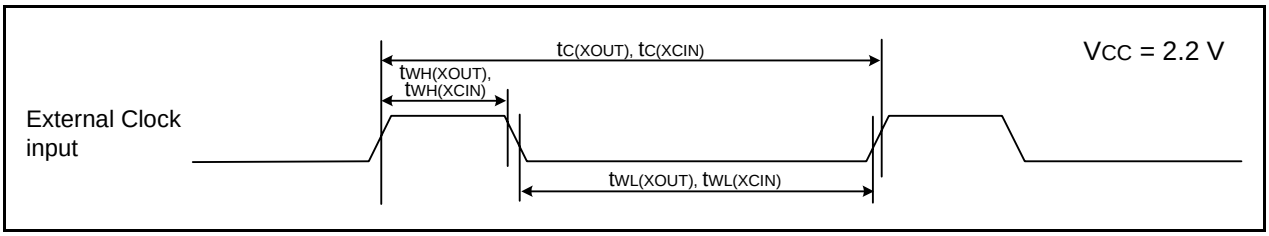



**Figure 5.16 External Clock Input Timing Diagram when $V_{CC}$ = 2.2 V**

**Table 5.31 TRAIO Input**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(TRAIO)}$ | TRAIO input cycle time | 500 | – | ns |
| $t_{WH(TRAIO)}$ | TRAIO input “H” width | 200 | – | ns |
| $t_{WL(TRAIO)}$ | TRAIO input “L” width | 200 | – | ns |

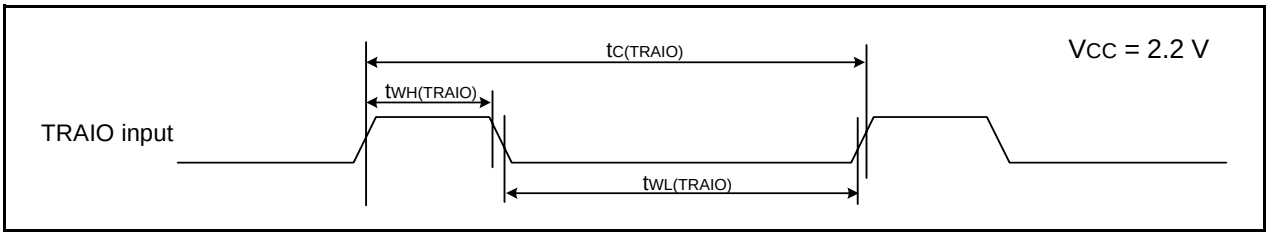



**Figure 5.17 TRAIO Input Timing Diagram when $V_{CC}$ = 2.2 V**