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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Details	
Product Status	Active
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	I ² C, LINbus, SIO, SSU, UART/USART
Peripherals	POR, PWM, Voltage Detect, WDT
Number of I/O	15
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-LSSOP (0.173", 4.40mm Width)
Supplier Device Package	20-LSSOP
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f21322cdsp-w4

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

ltem	Function	Specification
Serial	UART0	Clock synchronous serial I/O/UART
Interface	UART2	Clock synchronous serial I/O/UART, I ² C mode (I ² C-bus), multiprocessor communication function
Synchronous	Serial	1 (shared with I ² C-bus)
Communicat	ion Unit (SSU)	
I ² C bus		1 (shared with SSU)
LIN Module		Hardware LIN: 1 (timer RA, UART0)
A/D Converte	er	10-bit resolution × 4 channels, includes sample and hold function, with sweep mode
Comparator	В	2 circuits
Flash Memor	гy	 Programming and erasure voltage: VCC = 2.7 to 5.5 V
		 Programming and erasure endurance: 10,000 times (data flash)
		1,000 times (program ROM)
		 Program security: ROM code protect, ID code check
		 Debug functions: On-chip debug, on-board flash rewrite function
		 Background operation (BGO) function
Operating Fr	equency/Supply	f(XIN) = 20 MHz (VCC = 2.7 to 5.5 V)
Voltage		f(XIN) = 5 MHz (VCC = 1.8 to 5.5 V)
Current cons	umption	Typ. 6.5 mA (VCC = 5.0 V, f(XIN) = 20 MHz) Typ. 3.5 mA (VCC = 3.0 V, f(XIN) = 10 MHz) Typ. 3.5 μ A (VCC = 3.0 V, wait mode (f(XCIN) = 32 kHz)) Typ. 2.0 μ A (VCC = 3.0 V, stop mode)
Operating Ar	nbient Temperature	-20 to 85°C (N version) -40 to 85°C (D version) ⁽¹⁾
Package		20-pin LSSOP
0		Package code: PLSP0020JB-A (previous code: 20P2F-A)

Specifications for R8C/32C Group (2) Table 1.2

Note: 1. Specify the D version if D version functions are to be used.



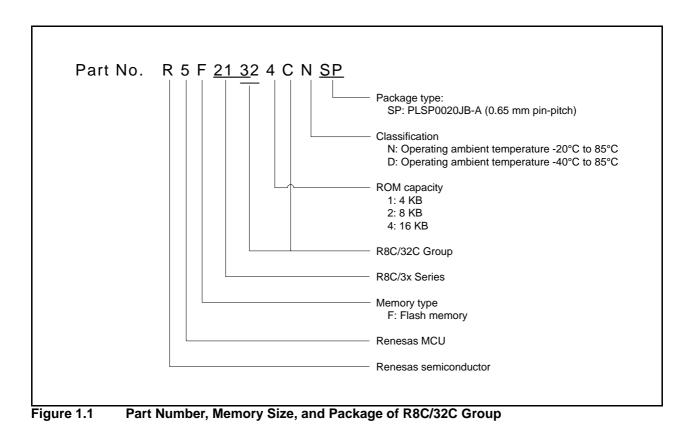
Current of Aug 2010

1.2 Product List

Table 1.3 lists Product List for R8C/32C Group, and Figure 1.1 shows a Part Number, Memory Size, and Package of R8C/32C Group.

Part No.	ROM C	Capacity	RAM	Package Type	Remarks
Fait NO.	Program ROM	Data flash	Capacity	Fackage Type	Remains
R5F21321CNSP	4 Kbytes	1 Kbyte × 4	512 bytes	PLSP0020JB-A	N version
R5F21322CNSP	8 Kbytes	1 Kbyte × 4	1 Kbyte	PLSP0020JB-A	
R5F21324CNSP	16 Kbytes	1 Kbyte × 4	1.5 Kbytes	PLSP0020JB-A	
R5F21321CDSP	4 Kbytes	1 Kbyte × 4	512 bytes	PLSP0020JB-A	D version
R5F21322CDSP	8 Kbytes	1 Kbyte × 4	1 Kbyte	PLSP0020JB-A	
R5F21324CDSP	16 Kbytes	1 Kbyte × 4	1.5 Kbytes	PLSP0020JB-A	

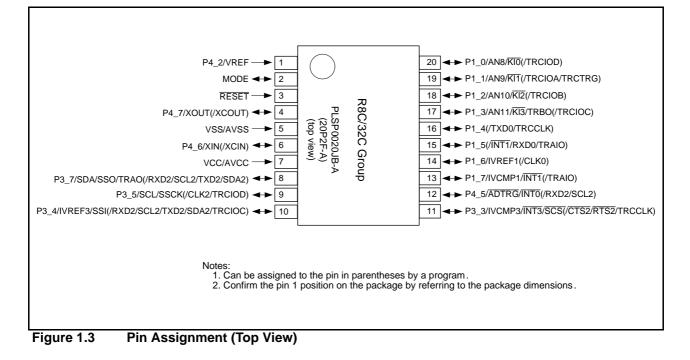
Table 1.3 Product List for R8C/32C Group





1.4 Pin Assignment

Figure 1.3 shows Pin Assignment (Top View). Table 1.4 outlines the Pin Name Information by Pin Number.





Pin		I/O Pin Functions for Peripheral Modules					ules	
Number	Control Pin	Port	Interrupt	Timer	Serial Interface	SSU	I ² C bus	A/D Converter, Comparator B
1		P4_2						VREF
2	MODE							
3	RESET							
4	XOUT(/XCOUT)	P4_7						
5	VSS/AVSS							
6	XIN(/XCIN)	P4_6						
7	VCC/AVCC							
8		P3_7		TRAO	(RXD2/SCL2/ TXD2/SDA2)	SSO	SDA	
9		P3_5		(TRCIOD)	(CLK2)	SSCK	SCL	
10		P3_4		(TRCIOC)	(RXD2/SCL2/ TXD2/SDA2)	SSI		IVREF3
11		P3_3	INT3	(TRCCLK)	(CTS2/RTS2)	SCS		IVCMP3
12		P4_5	INTO		(RXD2/SCL2)			ADTRG
13		P1_7	INT1	(TRAIO)				IVCMP1
14		P1_6			(CLK0)			IVREF1
15		P1_5	(INT1)	(TRAIO)	(RXD0)			
16		P1_4		(TRCCLK)	(TXD0)			
17		P1_3	KI3	TRBO (/TRCIOC)				AN11
18		P1_2	KI2	(TRCIOB)				AN10
19		P1_1	KI1	(TRCIOA/ TRCTRG)				AN9
20		P1_0	KI0	(TRCIOD)				AN8

Table 1.4 Pin Name Information by Pin Number

Note:

1. Can be assigned to the pin in parentheses by a program.



2.8.7 Interrupt Enable Flag (I)

The I flag enables maskable interrupts.

Interrupts are disabled when the I flag is set to 0, and are enabled when the I flag is set to 1. The I flag is set to 0 when an interrupt request is acknowledged.

2.8.8 Stack Pointer Select Flag (U)

ISP is selected when the U flag is set to 0; USP is selected when the U flag is set to 1. The U flag is set to 0 when a hardware interrupt request is acknowledged or the INT instruction of software interrupt numbers 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

IPL is 3 bits wide and assigns processor interrupt priority levels from level 0 to level 7. If a requested interrupt has higher priority than IPL, the interrupt is enabled.

2.8.10 Reserved Bit

If necessary, set to 0. When read, the content is undefined.



3. Memory

3.1 R8C/32C Group

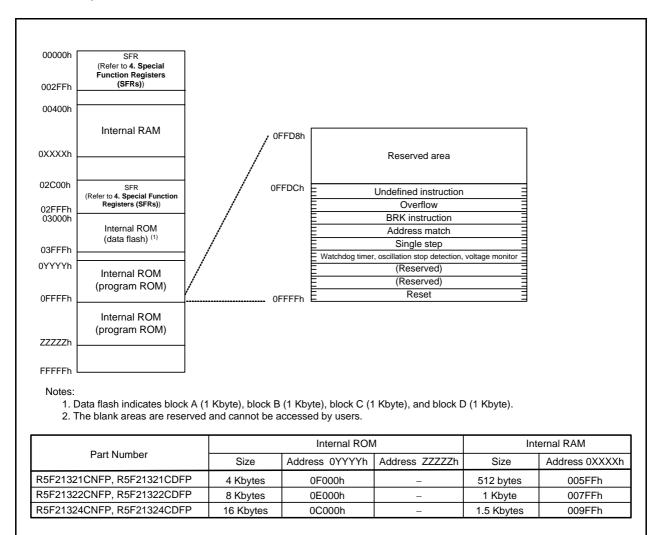
Figure 3.1 is a Memory Map of R8C/32C Group. The R8C/32C Group has a 1-Mbyte address space from addresses 00000h to FFFFh. The internal ROM (program ROM) is allocated lower addresses, beginning with address 0FFFFh. For example, a 16-Kbyte internal ROM area is allocated addresses 0C000h to 0FFFFh.

The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. The starting address of each interrupt routine is stored here.

The internal ROM (data flash) is allocated addresses 03000h to 03FFFh.

The internal RAM is allocated higher addresses, beginning with address 00400h. For example, a 1.5-Kbyte internal RAM area is allocated addresses 00400h to 009FFh. The internal RAM is used not only for data storage but also as a stack area when a subroutine is called or when an interrupt request is acknowledged.

Special function registers (SFRs) are allocated addresses 00000h to 002FFh and 02C00h to 02FFFh. Peripheral function control registers are allocated here. All unallocated spaces within the SFRs are reserved and cannot be accessed by users.







Special Function Registers (SFRs) 4.

An SFR (special function register) is a control register for a peripheral function. Tables 4.1 to 4.12 list the special function registers and Table 4.13 lists the ID Code Areas and Option Function Select Area.

Address	Register	Symbol	After Reset
0000h			
0001h			
0002h			
0003h			
0004h	Processor Mode Register 0	PM0	00h
0005h	Processor Mode Register 1	PM1	00h
0006h	System Clock Control Register 0	CM0	00101000b
0007h	System Clock Control Register 1	CM1	0010000b
0008h	Module Standby Control Register	MSTCR	00h
0009h	System Clock Control Register 3	CM3	00h
000Ah	Protect Register	PRCR	00h
000Bh	Reset Source Determination Register	RSTFR	0XXXXXXXb ⁽²⁾
000Ch	Oscillation Stop Detection Register	OCD	00000100b
000Dh	Watchdog Timer Reset Register	WDTR	XXh
000Eh	Watchdog Timer Start Register	WDTS	XXh
000Fh	Watchdog Timer Control Register	WDTC	00111111b
0010h			
0011h			
0012h			
0013h			
0014h			
0015h	High-Speed On-Chip Oscillator Control Register 7	FRA7	When shipping
0016h			
0017h			
0018h			
0019h			
001Ah			
001Bh			
001Ch	Count Source Protection Mode Register	CSPR	00h 10000000b ⁽³⁾
001Dh			
001Eh			
001Fh			
0020h			
0021h			
0022h			
0023h	High-Speed On-Chip Oscillator Control Register 0	FRA0	00h
0024h	High-Speed On-Chip Oscillator Control Register 1	FRA1	When shipping
0025h	High-Speed On-Chip Oscillator Control Register 2	FRA2	00h
0026h	On-Chip Reference Voltage Control Register	OCVREFCR	00h
0027h			
0028h	Clock Prescaler Reset Flag	CPSRF	00h
0029h	High-Speed On-Chip Oscillator Control Register 4	FRA4	When Shipping
002Ah	High-Speed On-Chip Oscillator Control Register 5	FRA5	When Shipping
002Bh	High-Speed On-Chip Oscillator Control Register 6	FRA6	When Shipping
002Ch			
002Dh			
002Eh			
002Fh	High-Speed On-Chip Oscillator Control Register 3	FRA3	When shipping
0030h	Voltage Monitor Circuit Control Register	CMPA	00h
0031h	Voltage Monitor Circuit Edge Select Register	VCAC	00h
0032h			
0033h	Voltage Detect Register 1	VCA1	00001000b
0034h	Voltage Detect Register 2	VCA2	00h ⁽⁴⁾ 00100000b ⁽⁵⁾
0035h			
0036h	Voltage Detection 1 Level Select Register	VD1LS	00000111b
0037h		ľ	1
0038h	Voltage Monitor 0 Circuit Control Register	VW0C	1100X010b ⁽⁴⁾
00005	Vallage Maniter 4 Circuit Control Devictor	1100/40	1100X011b ⁽⁵⁾
0039h	Voltage Monitor 1 Circuit Control Register	VW1C	10001010b

Table 4.1 SFR Information (1)⁽¹⁾

X: Undefined Notes:

1.

The blank areas are reserved and cannot be accessed by users. The CWR bit in the RSTFR register is set to 0 after power-on and voltage monitor 0 reset. Hardware reset, software reset, or watchdog timer 2. reset does not affect this bit.

The CSPROINI bit in the OFS register is set to 0. 3.

The LVDAS bit in the OFS register is set to 1. 4.

5. The LVDAS bit in the OFS register is set to 0.



0038h Volage Monitor 2 Circuit Control Register VV2C 195000105 0035h	Address	Register	Symbol	After Reset
0038h		5	,	
99320h			11120	100000105
003Dh				
0002h				
003Ph				
0040h Flash Memory Ready Interrupt Control Register FMRDYIC XXXXX00b 0041h Flash Memory Ready Interrupt Control Register XXXXX00b XXXXX00b 0043h Fred Interrupt Control Register RCIC XXXXX00b 0044h Fred Interrupt Control Register RCIC XXXXX00b 0044h Fred Interrupt Control Register SZIC XXXXX00b 0044h Fred Interrupt Control Register SZIC XXXXX00b 0044h Imer RE Interrupt Control Register SZIC XXXXX00b 0044h UART2 Transmit Interrupt Control Register SZIC XXXXX00b 0044h UART2 Receive Interrupt Control Register SZIC XXXXX00b XXXXX00b 0044h UART2 Transmit Interrupt Control Register SZIC XXXXX00b XXXXX00b 0044h UART0 Transmit Interrupt Control Register SZIC XXXXX00b XXXXX00b 0045h UART0 Transmit Interrupt Control Register SZIC XXXXX00b XXXXX00b 005h Timer RA Interrupt Control Register TRAIC XXXXX00b XXXXX00b XXXXX00b				
0041h Field Memory Ready Interrupt Control Register FMRDYIC XXXXX000b 0043h				
0043h		Flash Memory Ready Interrupt Control Register	FMRDYIC	XXXXX000b
0044h			-	
0044h				
0044h Timer RC Interrupt Control Register TREIC XXXXX000b 0044h Timer RC Interrupt Control Register TREIC XXXXX00b 0044h Timer RE Interrupt Control Register SZIC XXXXX00b 0044h Timer RE Interrupt Control Register SZIC XXXXX00b 0046h UART2 Transmit Interrupt Control Register KDIC XXXXX00b 0044h KPC XXXXX00b XXXXX00b 0044h KPC XXXXX00b XXXXX00b 0044h KPL LXXXXX00b XXXXX00b 0044h KPL XXXXX00b XXXXX00b 0044h KPL XXXXX00b XXXXX00b 0044h UART0 Transmit Interrupt Control Register SOTIC XXXXX00b 0055h UART0 Receive Interrupt Control Register SOTIC XXXXX00b 0056h Timer RA Interrupt Control Register TRAIC XXXXX00b 0056h Timer RA Interrupt Control Register INTGIC XXXXX00b 0056h Timer RB Interrupt Control Register INTGIC XXXXX00b	0044h			
0047h Timer RC Interrupt Control Register TRCIC XXXXX000b 0048h Timer RE Interrupt Control Register TREIC XXXXX00b 0044h UART2 Transmit Interrupt Control Register SZTIC XXXXX00b 0044h UART2 Tansmit Interrupt Control Register SZTIC XXXXX00b 0046h UART2 Tansmit Interrupt Control Register KUPIC XXXXX00b 0046h KAPT2 Receive Interrupt Control Register ADIC XXXXX00b 0046h MATO Receive Interrupt Control Register SUIC XXXXX00b 0055h Conversion Interrupt Control Register SOTIC XXXXX00b 0055h UART0 Receive Interrupt Control Register SORIC XXXXX00b 0055h Timer RB Interrupt Control Register TRAIC XXXXX00b <td>0045h</td> <td></td> <td></td> <td></td>	0045h			
0048h	0046h			
0049h Timer RE Interrupt Control Register TREIC XXXXX000b 0044h UART2 Transmit Interrupt Control Register SZTIC XXXXX000b 0044h UART2 Transmit Interrupt Control Register SZTIC XXXXX000b 0044h UART2 Transmit Interrupt Control Register KUPIC XXXXX00b 0044h KAIT2 Resceive Interrupt Control Register ADIC XXXXX00b 0044h KAIT2 Resceive Interrupt Control Register SUIC XXXXX00b 0055h Conversion Interrupt Control Register SORIC XXXXX00b 0055h File XXXXX00b XXXXX00b 0055h Timer RB Interrupt Control Register TRAIC XXXXX00b 0055h Interrupt Control Register INTOIC XXXXX00b 0055h<	0047h	Timer RC Interrupt Control Register	TRCIC	XXXXX000b
004Ah Timer RE Interrupt Control Register TREIC XXXXX000b 004Ah UMRT2 Transmit Interrupt Control Register SZRIC XXXXX00b 004Dh UART2 Receive Interrupt Control Register KUPIC XXXXX00b 004Dh Key Input Interrupt Control Register KUPIC XXXXX00b 004Dh Key Input Interrupt Control Register ADIC XXXXX00b 004Fh XD Conversion Interrupt Control Register SUIC/ IUCIC XXXXX00b 005h UART2 Reacenit Interrupt Control Register SORIC XXXX000b 005h UART0 Receive Interrupt Control Register SORIC XXXXX00b 0055h Imer RA Interrupt Control Register TRAIC XXXXX00b 0055h Immer RA Interrupt Control Register TRAIC XX00X00b				
004bh UART2 Transmit Interrupt Control Register S2TIC XXXXX000b 004Ch UART2 Receive Interrupt Control Register KUPIC XXXXX000b 004Dh Key Input Interrupt Control Register ADIC XXXXX000b 004Eh ADIC XXXXX00b XXXXX00b 004Eh ADIC XXXXX00b XXXXX00b 004Eh ADIC XXXXX00b XXXXX00b 004Eh ADIC XXXXX00b XXXXX00b 005h UART0 Receive Interrupt Control Register SOTIC XXXXX00b 0055h Interrupt Control Register TRAIC XXXXX00b 0055h Tmer RA Interrupt Control Register TRAIC XXXXX00b 0055h Tmer RB Interrupt Control Register TRAIC XXXXX00b 0055h Tmer RB Interrupt Control Register INTIC XX00X00b 0055h Tmer RB Interrupt Control Register INTIC XX00X00b 0055h INTI Interrupt Control Register INTIC XX00X00b 0055h UART2 Bus Collision Detection Interrupt Control Register INTIC <t< td=""><td></td><td></td><td></td><td></td></t<>				
0040h UAPT2 Receive Interrupt Control Register KUPIC XXXXX000b 0040h Key Input Interrupt Control Register ADIC XXXXX000b 0044h AD Conversion Interrupt Control Register / IIC bus Interrupt Control Register ADIC XXXXX000b 0047h SSUIC/ IICIC XXXXX000b XXXXX00b 0056h UART0 Receive Interrupt Control Register SOTC XXXXX00b 0055h UART0 Receive Interrupt Control Register SOTC XXXXX00b 0056n Interrupt Control Register SOTC XXXXX00b 0056n Inter RA Interrupt Control Register TRAIC XXXXX00b 0056n Inter RB Interrupt Control Register INT1C XX0XX00b 0056n Inter RB Interrupt Control Register INT1C XX0XX00b 0056n Introl Ration Detection Interrupt Control Register INT1CC XX0XX00b 0056n Introl Interrupt Control Register INT0IC XX0XX00b 0056n Introl Interrupt Control Register INT0IC XX00X00b 0056n Introl Interrupt Control Register INT0IC XX00X00b <td></td> <td>Timer RE Interrupt Control Register</td> <td>TREIC</td> <td></td>		Timer RE Interrupt Control Register	TREIC	
004bh Key Input Interrupt Control Register ADIC XXXXX000b 004bh ADIC XXXXX00b XXXXX00b 004bh SSUI Interrupt Control Register /IIC bus Interrupt Control Register (P) SSUIC /IICIC XXXXX00b 005bh UARTO Receive Interrupt Control Register SOTIC XXXXX00b 005bh UARTO Receive Interrupt Control Register SORIC XXXXX00b 005bh UARTO Receive Interrupt Control Register TRAIC XXXXX00b 005bh Timer RA Interrupt Control Register TRAIC XXXXX00b 005bh Timer RB Interrupt Control Register TRAIC XXXXX00b 005bh INT1 Interrupt Control Register INT3IC XX0XX00b 005bh INT3 Interrupt Control Register INT3IC XX0XX00b 005bh INT0 Interrupt Control Register INT0IC XX0XX00b		UART2 Transmit Interrupt Control Register		
004Fh AD Conversion Interrupt Control Register (/IC bus Interrupt Control Register //IC) XXXXX000b 005fh SUIT //ICC XXXXX000b 005fh SUIT //ICC XXXXX000b 005fh SUIT Receive Interrupt Control Register SOTIC XXXXX000b 0055h LIARTO Transmit Interrupt Control Register SORIC XXXX000b 0055h IARTO Transmit Interrupt Control Register TRAIC XXXX000b 0055h Immer RA Interrupt Control Register TRAIC XXXX000b 0056h Immer RB Interrupt Control Register INT1C XX0XX000b 0056h Immer RB Interrupt Control Register INT3C XX000b 0056h INT3 Interrupt Control Register INT3C XX000b 0056h INT0 Interrupt Control Register INT6C				
004Ph SSU Interrupt Control Register // IIC bus Interrupt Control Register SSU IC XXXXX000b 0050h UARTO Transmit Interrupt Control Register S0TIC XXXXX000b 0052h UARTO Transmit Interrupt Control Register S0RIC XXXXX000b 0054h S0RIC XXXXX000b 0056h Timer RA Interrupt Control Register TRAIC XXXXX000b 0056h Timer RA Interrupt Control Register TRBIC XXXXX000b 0057h Timer RB Interrupt Control Register INTIC XXXXX000b 0058h Timer RB Interrupt Control Register INTIC XX000b0b 0055h INT3 Interrupt Control Register INTIC XX000b0b 0055h UART2 Eus Collision Detection Interrupt Control Register U28CNIC XXXXX000b 0055h UART2 Eus Collision Detection Interrupt Control Register U28CNIC XXXXX000b 0056h INTO Interrupt Control Register INTIC XX000b 0056h INTO Interrupt Control Register U28CNIC XXXXX000b 0056h INTO Interrupt Control Register U28CNIC XXXXX000b		Key Input Interrupt Control Register		
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0052h UART0 Receive Interrupt Control Register SORC XXXX000b 0053h		UART0 Transmit Interrupt Control Register		
0054h		UART0 Receive Interrupt Control Register	SORIC	XXXXX000b
0055h mer KA Interupt Control Register TRAIC XXXXX000b 0057h Timer RB Interupt Control Register TRBIC XXXXX000b 0058h Timer RB Interupt Control Register INT1IC XX0XX000b 0058h INT1 Interupt Control Register INT1IC XX0XX000b 0058h INT3 Interupt Control Register INT3IC XX0XX000b 0055h UART2 Bus Collision Detection Interupt Control Register INT0IC XX00X00b 0055h UART2 Bus Collision Detection Interupt Control Register U2BCNIC XXXXX000b 0065h INT0 Interrupt Control Register INT0IC XX00X00b 0065h INT0 Interrupt Control Register INT0IC XX00X00b 0065h INT0 Interrupt Control Register INT0IC XX0XX00b 0066h INT0 Interrupt Control Register Interrupt Control Register Interrupt Control Register 0066h Interrupt Control Register Interrupt Control Register </td <td>0053h</td> <td></td> <td></td> <td></td>	0053h			
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005Ah INT3 Interrupt Control Register INT3IC XX00X00b 005Bh INT0 Interrupt Control Register INT0IC XX00X00b 005Dh INT0 Interrupt Control Register IUZBCNIC XXXXX00b 005Fh IUXRT2 Bus Collision Detection Interrupt Control Register IUZBCNIC XXXXX00b 005Fh INT0IC XXXXX00b INT0IC XXXXX00b 005Fh IUXRT2 Bus Collision Detection Interrupt Control Register IUZBCNIC XXXXX00b 0061h INT0IC XXXXX00b INT0IC XXXXX00b 0062h INT0IC XXXXX00b INT0IC				
Observed INTO Interrupt Control Register INTOIC XXX0000b 005Eh UART2 Bus Collision Detection Interrupt Control Register U2ECNIC XXXXX000b 005Eh UART2 Bus Collision Detection Interrupt Control Register U2ECNIC XXXXX000b 005Eh UART2 Bus Collision Detection Interrupt Control Register U2ECNIC XXXXX000b 005Eh UART2 Bus Collision Detection Interrupt Control Register U2ECNIC XXXXX000b 0061h				
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005Dh INT0 Interrupt Control Register INT0IC XX0000b 005Fh U28CNIC XXXX000b 0050h 0060h Image: Collision Detection Interrupt Control Register U28CNIC XXXX000b 0060h Image: Collision Detection Interrupt Control Register Image: Collision Detection Interrupt Control Register Image: Collision Detection Interrupt Control Register 0061h Image: Collision Detection Interrupt Control Register Image: Collision Detection Interrupt Control Register Image: Collision Detection Interrupt Control Register 0062h Image: Collision Detection Interrupt Control Register Image: Collision Detection Interrupt Control Register Image: Collision Detection Interrupt Control Register 0062h Image: Collision Detection Interrupt Control Register Image: Collision Detection Interrupt Control Register Image: Collision Detection Interrupt Control Register 0072h Voltage Monitor 1 Interrupt Control Register VCMP1IC XXXXX000b 0073h Voltage Monitor 2 Interrupt Control Register VCMP1IC XXXXX000b 0075h Image: Collision Detection Register VCMP2IC XXXXX000b 0075h Image: Collision Detection Register VCMP2IC XXXXX000b <td></td> <td></td> <td></td> <td></td>				
005Eh UART2 Bus Collision Detection Interrupt Control Register U2BCNIC XXXX000b 005Fh				
005Fh 0060h 0062h 0062h 0063h 0064h 0065h 0066h 0067h 0068h 0068h 0068h				
0060h		UART2 Bus Collision Detection Interrupt Control Register	U2BCNIC	XXXXX000b
0061h				
0062h				
0063h				
0064h				
0065h				
0066h				
0067h				
0068h				
0069h				
006Ah				
006Bh				
006Ch				
006Dh				
006Eh				
006Fh				
0070hImage: constraint of the second sec				
0071hImage: constraint of the second sec				
0072hVoltage Monitor 1 Interrupt Control RegisterVCMP1ICXXXX000b0073hVoltage Monitor 2 Interrupt Control RegisterVCMP2ICXXXX000b0074h0075h0076h0077h0078h0079h0077h0078h0078h0077h0078h0077h <t< td=""><td></td><td></td><td></td><td></td></t<>				
0073h Voltage Monitor 2 Interrupt Control Register VCMP2IC XXXX000b 0074h		Voltage Monitor 1 Interrupt Control Registor	VCMP1IC	XXXXX000b
0074h				
0075h 0076h 0077h 0078h 0079h 0079h 007Ah 007Ah 007Ah 007Ch 007Dh 007Eh 007Fh		volage monitor z interrupt control register	VOIVIFZIC	~~~~~
0076h				
0077h				
0078h				
0079h				
007Ah				
007Bh				
007Ch				
007Dh				
007Eh 007Fh 007Fh				
007Fh				
	X: Undefined		1	I

SFR Information (2)⁽¹⁾ Table 4.2

Notes: 1. 2.

The blank areas are reserved and cannot be accessed by users. Selectable by the IICSEL bit in the SSUIICSR register.



Address	Register	Symbol	After Reset
0080h	DTC Activation Control Register	DTCTL	00h
0081h			
0082h	-		
0083h			
0084h	+		
0085h			
0086h			
0087h			
0088h	DTC Activation Enable Register 0	DTCEN0	00h
0089h	DTC Activation Enable Register 1	DTCEN1	00h
008Ah	DTC Activation Enable Register 2	DTCEN2	00h
008Bh	DTC Activation Enable Register 3	DTCEN3	00h
008Ch			
008Dh	DTC Activation Enable Register 5	DTCEN5	00h
008Eh	DTC Activation Enable Register 6	DTCEN6	00h
008Fh			
0090h			
0091h			
0092h			
0093h			
0094h			
0095h			
0096h			
0097h			
0098h	1		
0099h			
009Ah	+		
009Bh			
009Ch			
009Dh			
009Eh			
009Fh			
00A0h	UART0 Transmit / Receive Mode Register	U0MR	00h
00A1h	UART0 Bit Rate Register	U0BRG	XXh
00A2h	UART0 Transmit Buffer Register	U0TB	XXh
00A3h	-		XXh
00A4h	UART0 Transmit / Receive Control Register 0	U0C0	00001000b
00A5h	UART0 Transmit / Receive Control Register 1	U0C1	00000010b
00A6h	UART0 Receive Buffer Register	UORB	XXh
00A7h			XXh
00A8h	UART2 Transmit / Receive Mode Register	U2MR	00h
00A9h	UART2 Bit Rate Register	U2BRG	XXh
00AAh	UART2 Transmit Buffer Register	U2TB	XXh
00ABh]		XXh
00ACh	UART2 Transmit / Receive Control Register 0	U2C0	00001000b
00ADh	UART2 Transmit / Receive Control Register 1	U2C1	00000010b
00AEh	UART2 Receive Buffer Register	U2RB	XXh
00AEh 00AFh		02100	XXh
00AFN 00B0h	UART2 Digital Filter Function Select Register		
	UARTZ DIgital Filter Function Select Register	URXDF	00h
00B1h			
00B2h			
00B3h			
00B4h			
00B5h			
00B6h			
00B7h	1	ł	
00B8h			
00B9h	+		
00BAh	LIADTO Or esist Made Desister 5	LIGONDE	0.01
00001	UART2 Special Mode Register 5	U2SMR5	00h
00BBh	UART2 Special Mode Register 4	U2SMR4	00h
00BCh			
	UART2 Special Mode Register 3	U2SMR3	000X0X0Xb
00BCh		U2SMR3 U2SMR2	000X0X0Xb X000000b

SFR Information (3)⁽¹⁾ Table 4.3

X: Undefined Note: 1. The blank areas are reserved and cannot be accessed by users.

Address	Register	Symbol	After Reset
01C0h	Address Match Interrupt Register 0	RMAD0	XXh
01C1h			XXh
01C2h			0000XXXXb
01C3h	Address Match Interrupt Enable Register 0	AIER0	00h
01C3h	Address Match Interrupt Register 1	RMAD1	XXh
01C4n	Address Match Interrupt Register 1	RMADT	XXh
01C6h			
	Address Match Internet Frickle Denister 4		0000XXXXb
01C7h	Address Match Interrupt Enable Register 1	AIER1	00h
01C8h			
01C9h			
01CAh			
01CBh			
01CCh			
01CDh			
01CEh			
01CFh			
01D0h			
01D1h			
01D2h			
01D3h			
01D4h			
01D5h			
01D6h			
01D7h			
01D8h			
01D9h			
01DAh			
01DBh			
01DCh			
01DDh			
01DEh			
01DFh			
01E0h	Pull-Up Control Register 0	PUR0	00h
01E1h	Pull-Up Control Register 1	PUR1	00h
01E11		FORT	0011
01E3h			
01E3h			
01E5h			
01E6h			
01E7h			
01E8h			
01E9h			
01EAh			
01EBh			
01ECh			
01EDh			
01EEh			
01EFh			
01F0h	Port P1 Drive Capacity Control Register	P1DRR	00h
01F1h			
01F2h	Drive Capacity Control Register 0	DRR0	00h
01F3h	Drive Capacity Control Register 1	DRR1	00h
01F4h			
01F5h	Input Threshold Control Register 0	VLT0	00h
01F6h	Input Threshold Control Register 1	VLT1	00h
01F7h			
01F8h	Comparator B Control Register 0	INTCMP	00h
01F9h			
01FAh	External Input Enable Register 0	INTEN	00h
01FBh	, , , , , , , , , , , , , , , , , , ,	l l	
01FCh	INT Input Filter Select Register 0	INTF	00h
01FDh			
01FEh	Key Input Enable Register 0	KIEN	00h
01FFh	· · · · · · · · · · · · · · · · · · ·		
Y: Undofined	1		

SFR Information (8)⁽¹⁾ Table 4.8

X: Undefined Note: 1. The blank areas are reserved and cannot be accessed by users.



Address Fregister Symbol Atter kees 20260 DTC Control Data 14 DTC DT4 XX 20261 XX XX XX 20268 XX XX XX 20268 DTC Control Data 15 DTCD15 XX 20268 XX XX XX 20268 DTC Control Data 15 XX XX 20268 ZCCAN XX XX 20268 ZCCAN XX XX 20268 DTC Control Data 15 XX XX 20268 DTC Control Data 16 XX XX 20200 TC Control Data 16 XX XX 20201 XX XX XX 20203 DTC Control Data 17 DTCD16 XX 20204 XX XX XX 20205 XX XX XX 20205 XX XX XX 20206 XX XX XX 20206 XX <th></th> <th></th> <th>0 1 1</th> <th></th>			0 1 1	
2CB1h Xh Xh 2CB2h Xh Xh 2CB4h Xh Xh 2CC4h Xh Xh 2CC5h Xh Xh 2CC6h Xh Xh	Address	Register	Symbol	After Reset
2C82h 2C83h 2C83h 2C85h 2		DTC Control Data 14	DTCD14	
2C83n Xh Xh 2C84n Xh Xh 2C62n Xh Xh	2CB1h			XXh
2C83n Xh Xh 2C84n Xh Xh 2C62n Xh Xh	2CB2h			XXh
2CB4h XXh 2CB5h XXh 2CB7h DTC Control Data 15 2CB8h XXh 2CB8h TC Control Data 16 2CC1h TC Control Data 16 2CC2h XXh 2CC3h XXh <td></td> <td></td> <td></td> <td></td>				
2C88h 2C89h 2C89h 2C89h 2C89h 2C89h 2C89h 2C89h 2C89h 2C89h 2C89h 2C89h 2C89h 2C89h 2C89h 2C89h 2C89h 2C8h 2C8h 2C8h 2C6h 2C6h 2C6h 2C6h 2C6h 2C6h 2C6h 2C6		-		
2C68h 2C68h 2C68h 2C68h 2C68h 2C68h 2C68h 2C68h 2C68h 2C68h 2C68h 2C68h 2C68h 2C68h 2C68h 2C68h 2C68h 2C68h 2C68h 2C66h 2C7 2C6h 2C7 2C6h 2C7 2C6h 2C7 2C6h 2C7 2C6h 2C7 2C6h 2C7 1 2		4		
2C87h TC Control Data 15 Xh 2C88h DTC Control Data 15 Xh 2C88h Xh Xh 2C88h Xh Xh 2C88h Xh Xh 2C88h Xh Xh 2C86h DTC Control Data 16 Xh 2CC3h ZCC3h Xh 2CC3h Xh Xh 2C				
2268h 266Ah 266Bh 2	2CB6h			XXh
2268h DTC Control Data 15 Xh 2268h Xh Xh 2268h TC Control Data 16 Xh 2262h Xh Xh 260h	2CB7h			XXh
2C89h 2C89h 2C8Ph 2C8Ph 2C8Ph 2C6Ph 2	2CB8h	DTC Control Data 15	DTCD15	
2CBAh Xxh 2CBBh Xxh 2CBBh Xxh 2CBDh Xxh 2CBPh Xxh 2CBPh Xxh 2CCPh DTC Control Data 16 2CC2h Xxh 2CC2h Xxh 2CC2h Xxh 2CC2h Xxh 2CC2h Xxh 2CC2h Xxh 2CC3h Xxh 2CC4h Xxh 2CC5h Xxh 2CC6h Xxh 2C0h Xxh 2C0h Xxh 2C0h Xxh 2C0h Xxh				
2C8Bh Xh Xh 2C8Bh Xh Xh 2C8Bh Xh Xh 2C8Bh Xh Xh 2C8Bh DTC Control Data 16 Xh 2C00h DTC Control Data 16 Xh 2C00h ZCCah Xh 2C00h ZCCAh Xh 2CC3h Xh Xh 2CC3h ZCCAh Xh		-		
22626.h Xxh 2268b.h Xxh 2268b.h Xxh 2268b.h DTC Control Data 16 2262b.h Xxh 2262b.h DTC Control Data 17 2262b.h DTC Control Data 17 2262b.h DTC Control Data 17 2262b.h ZCCBh 22CCBh ZCCCh 22CBh ZCCCh 22CBh ZCCh 22CCBh ZCCh 22CCh Xxh 22CBh ZCCh 22CBh ZCCh 22CBh ZCCh 22CDh ZCCh 22CBh ZCCh 22CBh ZCCh 22CBh ZCCh 22CBh		-		
2CBBh Xxh 2CBFh Xxh 2CC0h DTC Control Data 16 Xxh 2CC0h ZCCah Xxh 2CC2h Xxh Xxh 2CC2h Xxh Xxh 2CC3h Xxh Xxh 2CC6h DTC Control Data 17 Xxh 2CC8h ZCCAh Xxh 2CC8h ZCCCh Xxh 2CC8h ZCCCh Xxh 2CC8h ZCCh Xxh 2CC8h ZCCh Xxh 2C0bh ZCCh Xxh 2C0bh ZCCh Xxh 2C0bh ZCCh Xxh 2C0bh ZCDA Xxh 2C0bh ZCCh Xxh 2C0bh ZCDA Xxh 2C0bh ZCCh Xxh				
2208Eh 2208Fh 2203h 2003h 2003h 2003h 2003h 2003h 2003h 2003h 2003h 2005h	2CBCh			XXh
226Brh DTC Control Data 16 Xxh 22C0h DTC Control Data 16 Xxh 22C2h Xxh Xxh 22C3h Xxh Xxh 2C2Ch Xxh Xxh 2C2Ch Xxh Xxh 2C2Ch Xxh Xxh 2C2Ch Xxh Xxh 2CCBh DTC Control Data 17 Xxh 2CCCh Xxh Xxh 2CCCh Xxh Xxh 2CCCh Xxh Xxh 2CCDh DTC Control Data 18 Xxh 2CDh Xxh	2CBDh			XXh
226Brh DTC Control Data 16 Xxh 22C0h DTC Control Data 16 Xxh 22C2h Xxh Xxh 22C3h Xxh Xxh 2C2Ch Xxh Xxh 2C2Ch Xxh Xxh 2C2Ch Xxh Xxh 2C2Ch Xxh Xxh 2CCBh DTC Control Data 17 Xxh 2CCCh Xxh Xxh 2CCCh Xxh Xxh 2CCCh Xxh Xxh 2CCDh DTC Control Data 18 Xxh 2CDh Xxh	2CBEh			XXh
20C0h DTC Control Data 16 Xxh 20C1h Xxh Xxh 20C3h Xxh Xxh 20C3h Xxh Xxh 20C3h Xxh Xxh 20C6h Xxh Xxh 20C6h Xxh Xxh 20C6h DTC Control Data 17 DTCD17 Xxh 20C6h Xxh Xxh Xxh 20C9h DTC Control Data 18 DTCD18 Xxh 20D2h Xxh Xxh Xxh 20D3h		-		
20C2h Xh 20C2h Xh 20C3h DTC Control Data 17 20C3h Xh 20C3h Xh 20C6h Xh 200bh DTC Control Data 17 200bh DTC Control Data 18 200bh DTC Control Data 18 200bh Xh 200bh Xh 200bh Xh 200bh DTC Control Data 18 200bh Xh 200bh DTC Control Data 18 200bh DTC Control Data 19 200bh Xh 200bh Xh		DTC Control Data 16	DTCD16	
2CC2h XXh 2CC3h XXh 2CC5h XXh 2CC6h XXh 2CC6h XXh 2CC8h DTC Control Data 17 2CC8h DTC Control Data 17 2CC8h ZCC8h 2CC8h DTC Control Data 17 2CC8h ZCC8h 2CC8h ZCC8h 2CC8h ZCC8h 2CC8h ZCC8h 2CC8h ZCC8h 2CC8h ZC8h 2CC8h ZC8h 2CC8h ZC8h 2C28h ZC8h 2C28h ZC8h 2C28h ZC8h 2C28h ZC8h 2C29h ZC9h 2C18h Xh 2C29h ZC8h 2C28h ZC8h 2C29h ZC9h 2C09h ZC8h 2C9h ZC8h 2C9h Xh 2C9h ZC8h 2C9h Xh 2C9		DIC Control Data 16	DICD16	
20C3h Xh 20C4h Xh 20C6h Xh 20C7h DTC Control Data 17 20C7h DTCD17 Xh Xh 20C6h Xh 20C7h DTCD17 Xh Xh 20C7h Xh 20C6h Xh 200h DTC Control Data 18 200h DTC Control Data 18 200h DTC Control Data 18 200h Xh 200h ZCORh 200h Xh 200h ZCORh 200h ZC Control Data 18 200h ZCORh 200h ZCORh 200h ZC 200h ZC 200h ZC 200h				
2CC4h Xh 2CC5h Xh 2CC6h Xh 2CC8h DTC Control Data 17 2CC8h DTC Control Data 17 2CC8h Xh 2CC8h Xh 2CC8h DTC Control Data 17 2CC8h Xh 2C0h ZC6h 2C0h ZC7h 2C0h ZC7h 2C0h ZC8h 2C0h ZC7h 2C0h ZC7h 2C0h ZC7h 2C0h ZC7h 2C0h ZC7h 2C0h ZC8h 2C0h Xh 2C0h Xh 2C0h Xh 2C0h Xh 2C0h Xh	2CC2h			XXh
2CC4h Xh 2CC5h Xh 2CC6h Xh 2CC8h DTC Control Data 17 2CC8h DTC Control Data 17 2CC8h Xh 2CC8h Xh 2CC8h DTC Control Data 17 2CC8h Xh 2C0h ZC6h 2C0h ZC7h 2C0h ZC7h 2C0h ZC8h 2C0h ZC7h 2C0h ZC7h 2C0h ZC7h 2C0h ZC7h 2C0h ZC7h 2C0h ZC8h 2C0h Xh 2C0h Xh 2C0h Xh 2C0h Xh 2C0h Xh	2CC3h]		XXh
2CC5h Xh 2CC5h Xh 2CC7h DTC Control Data 17 2CC8h DTC Control Data 17 2CC8h ZCC9h 2CC6h Xh 2C01h Xh 2C02h Xh 2C02h Xh 2C03h Xh 2C05h Xh 2C		1		
2CC6h Xxh 2CC7h Xxh 2CC8h DTC Control Data 17 Xxh 2CC8h ZCCAh Xxh 2CC8h ZCCAh Xxh 2CC8h ZCCAh Xxh 2CCCh Xxh Xxh 2CCDh DTC Control Data 18 DTCD18 Xxh 2CD3h Xxh Xxh Xxh 2CD3h Xxh Xxh Xxh 2CD5h DTC Control Data 19 Xxh Xxh 2CD5h DTC Control Data 19 Xxh Xxh 2CD5h DTC Control Data 20 Xxh Xxh 2CD5h ZCDFh Xxh Xxh 2CD5h ZCE3h Xxh Xxh ZCE3h Xxh		4		
2CC7h Xh 2CC8h DTC Control Data 17 Xh 2CC9h DTC Control Data 17 Xh 2CC8h XXh XXh 2CC6h XXh XXh 2C01h XXh XXh 2C03h ZCD1h XXh 2C03h ZCD3h XXh 2C03h ZCD6h XXh 2C03h ZC0h XXh 2C05h ZC0h XXh 2C05h ZC0h XXh ZC0Ah ZC0h XXh ZC0Ah ZC0h XXh ZC0Bh ZCCh XXh ZC0Dh ZCCh XXh		4		
2CC8h DTC Control Data 17 Xxh 2CC8h Xxh Xxh 2CC8h DTC Control Data 18 Xxh 2C0bh DTC Control Data 18 Xxh 2CD2h Xxh Xxh 2CD3h Xxh Xxh 2CD5h Xxh Xxh 2CE1h DTC Control Data 20<		4		
2CC9h Xh 2CCBh Xh 2CCCh Xh 2CCEh Xh 2CCEh Xh 2CCEh Xh 2CCEh Xh 2CCEh Xh 2CCEh Xh 2CDh Xh 2CEh Xh 2CEh Xh 2				
2CCAh XXh 2CCBh XXh 2CCDh XXh 2CCFh XXh 2CD0h DTC Control Data 18 2CD1h XXh 2CD2h XXh 2CD2h XXh 2CD2h XXh 2CD2h XXh 2CD2h XXh 2CD5h XXh 2CD6h XXh 2CD6h XXh 2CD7h XXh 2CD6h XXh 2CD6h XXh 2CD7h XXh 2CD6h XXh 2CD7h XXh 2CD6h XXh 2CD6h XXh 2CD7h XXh 2CD7h XXh 2CE1h XXh 2CE2h XXh	2CC8h	DTC Control Data 17	DTCD17	XXh
2CCAh XXh 2CCBh XXh 2CCDh XXh 2CCFh XXh 2CD0h DTC Control Data 18 2CD1h XXh 2CD2h XXh 2CD2h XXh 2CD2h XXh 2CD2h XXh 2CD2h XXh 2CD5h XXh 2CD6h XXh 2CD6h XXh 2CD7h XXh 2CD6h XXh 2CD6h XXh 2CD7h XXh 2CD6h XXh 2CD7h XXh 2CD6h XXh 2CD6h XXh 2CD7h XXh 2CD7h XXh 2CE1h XXh 2CE2h XXh	2CC9h			XXh
2CCBh Xxh 2CCDh Xxh 2CCFh Xxh 2CCPh Xxh 2CDh Xxh 2CDbh Xxh 2CDbh Xxh 2CDBh DTC Control Data 19 2CDBh DTC Control Data 19 2CDBh Xxh 2CDBh Xxh 2CDBh Xxh 2CDFh Xxh 2CDFh Xxh 2CEth Xxh				
2CCCh Xh 2CCEh Xh 2CCFh Xh 2CCFh Xh 2CDh DTC Control Data 18 2CDh DTC Control Data 18 2CDh DTC Control Data 18 2CD2h XXh 2CD3h XXh 2CD5h XXh 2CD6h XXh 2CD7h XXh 2CD8h XXh 2CE9h DTC Control Data 20 XXh XXh XXh		-		
2CCDh Xh 2CCFh Xh 2CCDh DTC Control Data 18 2CDh DTC Control Data 18 2CD3h XXh 2CD3h XXh 2CD6h XXh 2CD3h XXh 2CD6h XXh 2CD8h DTC Control Data 19 2CD8h DTC Control Data 19 2CD6h XXh 2CE1h XXh 2CE3h ZCE4h 2CE3h ZCE6h 2CE6h		4		
2CCEh XXh 2CCPh XXh 2CDh DTC Control Data 18 DTCD18 XXh 2CD2h XXh XXh XXh 2CD3h XXh XXh XXh 2CD3h XXh XXh XXh 2CD3h XXh XXh XXh 2CD5h XXh XXh XXh 2CD7h DTC Control Data 19 XXh XXh 2CD3h DTC Control Data 19 XXh XXh 2CDAh ZCDAh XXh XXh 2CEOH DTC Control Data 20 ZCDAH XXh 2CE3h ZCE3h				
2CCFh XXh 2CD0h DTC Control Data 18 XXh 2CD2h XXh XXh 2CD3h DTC Control Data 19 XXh 2CD3h DTC Control Data 19 XXh 2CD3h XXh XXh 2C50h DTC Control Data 20 XXh<				
2CD0h 2CD1hDTC Control Data 18DTC D18XXh XXh2CD3h 2CD3h2CD3h 2CD5hXXhXXh XXh2CD3h 2CD5hDTC Control Data 19XXh XXhXXh XXh2CD8h 2CD9hDTC Control Data 19DTCD19XXh XXh2CD8h 2CD8hDTC Control Data 19DTCD19XXh XXh2CD8h 2CD6hDTC Control Data 20DTCD19XXh XXh2CD6h 2CDFhDTC Control Data 20DTCD20XXh XXh2CE3h 2CE3hDTC Control Data 20DTCD20XXh XXh2CE6h 2CE7hDTC Control Data 21DTCD21XXh XXh2CE8h 2CE8hDTC Control Data 21DTCD21XXh XXh	2CCEh			XXh
2CD0h 2CD1hDTC Control Data 18DTC D18XXh XXh2CD3h 2CD3h2CD3h 2CD5hXXhXXh XXh2CD3h 2CD5hDTC Control Data 19XXh XXhXXh XXh2CD8h 2CD9hDTC Control Data 19DTCD19XXh XXh2CD8h 2CD8hDTC Control Data 19DTCD19XXh XXh2CD8h 2CD6hDTC Control Data 20DTCD19XXh XXh2CD6h 2CDFhDTC Control Data 20DTCD20XXh XXh2CE3h 2CE3hDTC Control Data 20DTCD20XXh XXh2CE6h 2CE7hDTC Control Data 21DTCD21XXh XXh2CE8h 2CE8hDTC Control Data 21DTCD21XXh XXh				
2CD1h XXh 2CD2h XXh 2CD3h XXh 2CD5h XXh 2CD6h XXh 2CD7n XXh 2CD8h DTC Control Data 19 2CD8h DTC Control Data 19 2CD8h DTC Control Data 19 2CD8h XXh 2CD8h XXh 2CD8h XXh 2CD0h XXh 2CDCh XXh 2CDCh XXh 2CDCh XXh 2CDCh XXh 2CDCh XXh 2CDCh XXh 2CE0h DTC Control Data 20 2CE2h DTC Control Data 20 2CE2h XXh 2CE3h XXh		DTC Control Data 18	DTCD18	
2CD2h XXh 2CD3h XXh 2CD5h XXh 2CD6h XXh 2CD7h XXh 2CD8h DTC Control Data 19 2CD8h DTC Control Data 19 2CD8h XXh 2CD8h XXh 2CD8h DTC Control Data 19 2CD8h XXh 2CD8h XXh 2CDBh XXh 2CDCh XXh 2CDEh ZCDFh 2CDFh XXh 2CE2hh ZCE1h 2CE2h DTC Control Data 20 2CE2h DTC Control Data 20 2CE2h XXh 2CE2h XXh 2CE2h XXh 2CE2h XXh 2CE3h XXh 2CE3h XXh 2CE3h XXh 2CE3h XXh 2CE3h XXh 2CE3h DTC Control Data 21 2CE3h XXh 2CE3h XXh			BIGBIG	
2CD3h XXh 2CD5h XXh 2CD6h XXh 2CD7h XXh 2CD8h XXh 2CD9h XXh 2CD9h XXh 2CD9h XXh 2CD9h XXh 2CD9h XXh 2CD9h XXh 2CD0h XXh 2CDDh XXh 2CDDh XXh 2CDFh XXh 2CDFh XXh 2CE0h DTC Control Data 20 2CE2h XXh 2CE2h XXh 2CE2h XXh 2CE3h XXh 2CE5h XXh 2CE6h XXh 2CE8h XXh 2CE8h XXh 2CE8h XXh		-		
2CD4h 2CD5h 2CD6h XXh 2CD7h XXh 2CD8h DTC Control Data 19 2CD8h DTC Control Data 19 2CD8h DTC Control Data 19 2CD8h ZCDAh 2CD8h DTC Control Data 19 2CD8h XXh 2CD8h XXh 2CDCh XXh 2CDFh XXh 2CDFh XXh 2CDFh XXh 2CE0h DTC Control Data 20 2CE1h XXh 2CE2h DTC Control Data 20 2CE3h ZCE4h 2CE3h XXh				
2CD5h XXh 2CD7h XXh 2CD8h DTC Control Data 19 DTCD19 2CD8h DTCD19 XXh 2CD8h ZCD6h XXh 2CD8h DTC Control Data 19 DTCD19 XXh 2CD8h ZCD6h XXh XXh 2CD8h ZCD6h XXh XXh 2CD8h ZCD6h XXh XXh 2CD6h ZCD6h XXh XXh 2CD7h DTC Control Data 20 ZCE0h XXh 2CE2h DTC Control Data 20 DTCD20 XXh 2CE2h ZCE6h XXh XXh 2CE3h ZCE6h XXh XXh 2CE6h ZCE6h XXh XXh 2CE6h DTC Control Data 21 DTCD21 XXh 2CE8h DTC Control Data 21 XXh XXh 2CE8h DTC Control Data 21 XXh XXh				
2CD5h XXh 2CD7h XXh 2CD8h DTC Control Data 19 DTCD19 2CD8h DTCD19 XXh 2CD8h ZCD6h XXh 2CD8h DTC Control Data 19 DTCD19 XXh 2CD8h ZCD6h XXh XXh 2CD8h ZCD6h XXh XXh 2CD8h ZCD6h XXh XXh 2CD6h ZCD6h XXh XXh 2CD7h DTC Control Data 20 ZCE0h XXh 2CE2h DTC Control Data 20 DTCD20 XXh 2CE2h ZCE6h XXh XXh 2CE3h ZCE6h XXh XXh 2CE6h ZCE6h XXh XXh 2CE6h DTC Control Data 21 DTCD21 XXh 2CE8h DTC Control Data 21 XXh XXh 2CE8h DTC Control Data 21 XXh XXh	2CD4h			XXh
2CD6h XXh 2CD7h XXh 2CD8h DTC Control Data 19 XXh 2CD9h DTCD19 XXh 2CD8h XXh XXh 2CD8h DTC Control Data 20 DTCD20 XXh 2CE9h DTC Control Data 20 DTCD20 XXh 2CE3h 2CE3h XXh XXh 2CE8h DTC Control Data 21 XXh XXh 2CE8h DTC Control Data 21 DTCD21 XXh 2CE8h XXh XXh XXh 2CE8h XXh XXh XXh				XXh
2CD7h XXh 2CD8h DTC Control Data 19 XXh 2CD9h DTCD19 XXh 2CD8h XXh XXh 2CD0h ZCD6h XXh 2CD8h DTC Control Data 20 XXh 2CE6h DTC Control Data 20 DTCD20 XXh 2CE2h ZCE3h XXh XXh 2CE5h ZCE6h XXh XXh 2CE5h ZCE6h XXh XXh 2CE6h DTC Control Data 21 ZCE6h XXh 2CE6h ZCE6h XXh XXh 2CE6h DTC Control Data 21 ZCE6h XXh 2CE8h DTC Control Data 21 XXh XXh 2CE8h ZCE8h XXh XXh				
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2CEAh XXh 2CEBh XXh		Di C Control Data 21	DTCD21	
2CEBh XXh				
		1		
		1		
2CEDh XXh		4		
		4		
2CEEh XXh		4		
2CEFh XXh	2CEFh			XXh

SFR Information (11)⁽¹⁾ Table 4.11

X: Undefined Note: 1. The blank areas are reserved and cannot be accessed by users.



Symbol		Por	ameter		Conditions		Standard	_	Unit
Symbol		Fai	ameter		Conditions	Min.	Тур.	Max.	Onit
Vcc/AVcc	Supply voltage					1.8	-	5.5	V
Vss/AVss	Supply voltage					-	0	-	V
Viн	Input "H" voltage	Other than	n CMOS inp			0.8 Vcc	-	Vcc	V
		CMOS		Input level selection	$4.0~V \leq Vcc \leq 5.5~V$	0.5 Vcc	-	Vcc	V
		input	switching	: 0.35 Vcc	$2.7~\text{V} \leq \text{Vcc} < 4.0~\text{V}$	0.55 Vcc	-	Vcc	V
			function (I/O port)		$1.8~\text{V} \leq \text{Vcc} < 2.7~\text{V}$	0.65 Vcc	-	Vcc	V
			(i/O port)	Input level selection	$4.0~V \leq Vcc \leq 5.5~V$	0.65 Vcc	-	Vcc	V
				: 0.5 Vcc	$2.7~V \leq Vcc < 4.0~V$	0.7 Vcc	-	Vcc	V
					$1.8~\text{V} \leq \text{Vcc} < 2.7~\text{V}$	0.8 Vcc	-	Vcc	V
				Input level selection	$4.0~V \leq Vcc \leq 5.5~V$	0.85 Vcc	-	Vcc	V
				: 0.7 Vcc	$2.7~V \leq Vcc < 4.0~V$	0.85 Vcc	-	Vcc	V
					$1.8~V \leq Vcc < 2.7~V$	0.85 Vcc	-	Vcc	V
		External c	lock input (X	(OUT)		1.2	-	Vcc	V
VIL	Input "L" voltage	Other than	n CMOS inp	ut		0	-	0.2 Vcc	V
		CMOS		Input level selection	$4.0~V \leq Vcc \leq 5.5~V$	0	-	0.2 Vcc	V
		input	switching	: 0.35 Vcc	$2.7~V \leq Vcc < 4.0~V$	0	-	0.2 Vcc	V
			function		$1.8~\text{V} \leq \text{Vcc} < 2.7~\text{V}$	0	-	0.2 Vcc	V
			(I/O port)	Input level selection	$4.0~V \leq Vcc \leq 5.5~V$	0	-	0.4 Vcc	V
				: 0.5 Vcc	$2.7~\text{V} \leq \text{Vcc} < 4.0~\text{V}$	0	-	0.3 Vcc	V
					$1.8~\text{V} \leq \text{Vcc} < 2.7~\text{V}$	0	-	0.2 Vcc	V
				Input level selection	$4.0~V \leq Vcc \leq 5.5~V$	0	-	0.55 Vcc	V
				: 0.7 Vcc	$2.7~\text{V} \leq \text{Vcc} < 4.0~\text{V}$	0	-	0.45 Vcc	V
					$1.8~\text{V} \leq \text{Vcc} < 2.7~\text{V}$	0	-	0.35 Vcc	V
		External c	lock input (X	OUT)		0	-	0.4	V
IOH(sum)	Peak sum output "	H" current	Sum of all	pins IOH(peak)		-	-	-160	mA
IOH(sum)	Average sum output	"H" current	Sum of all	pins IOH(avg)		-	-	-80	mA
IOH(peak)	Peak output "H" c	urrent	Drive capa	city Low		-	-	-10	mA
			Drive capa	city High		-	-	-40	mA
IOH(avg)	Average output "H	l" current	Drive capa	city Low		-	-	-5	mA
			Drive capa	city High		-	-	-20	mA
IOL(sum)	Peak sum output '	'L" current	Sum of all	pins IOL(peak)		-	-	160	mA
IOL(sum)	Average sum output	"L" current	Sum of all	pins IOL(avg)		-	-	80	mA
IOL(peak)	Peak output "L" cu	urrent	Drive capa	city Low		-	-	10	mA
			Drive capa	city High		-	-	40	mA
IOL(avg)	Average output "L	" current	Drive capa	city Low		-	-	5	mA
			Drive capa	city High		-	-	20	mA
f(XIN)	XIN clock input os	cillation free	quency		$2.7 \text{ V} \leq \text{Vcc} \leq 5.5 \text{ V}$	-	-	20	MHz
	-				$1.8 \text{ V} \le \text{Vcc} < 2.7 \text{ V}$	-	-	5	MHz
f(XCIN)	XCIN clock input of	oscillation fr	equency		$1.8 \text{ V} \le \text{Vcc} \le 5.5 \text{ V}$	-	32.768	50	kHz
fOCO40M	When used as the o	count source	for timer RC	(3)	$2.7 \text{ V} \leq \text{Vcc} \leq 5.5 \text{ V}$	32	-	40	MHz
fOCO-F	fOCO-F frequency		-		2.7 V ≤ Vcc ≤ 5.5 V	_	- 1	20	MHz
-	- 1,				$1.8 \text{ V} \leq \text{Vcc} < 2.7 \text{ V}$	-	-	5	MHz
_	System clock freq	uency			$2.7 \text{ V} \leq \text{Vcc} \leq 5.5 \text{ V}$	_	_	20	MHz
	,				$1.8 \text{ V} \le \text{Vcc} < 2.7 \text{ V}$	_	_	5	MHz
f(BCLK)	CPU clock freque	ncy			$2.7 \text{ V} \le \text{Vcc} \le 5.5 \text{ V}$	_	_	20	MHz
、 /					$1.8 \text{ V} \le \text{Vcc} < 2.7 \text{ V}$	_	_	5	MHz
					~ . . . _ . _ . _ .			Ĩ	1

Table 5.2 Recommended Operating Conditions

Notes:

1. Vcc = 1.8 to 5.5 V and Topr = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.

2. The average output current indicates the average value of current measured during 100 ms.

3. fOCO40M can be used as the count source for timer RC in the range of Vcc = 2.7 V to 5.5V.



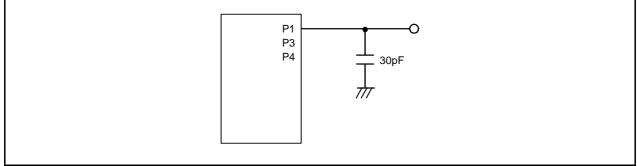


Figure 5.1 Ports P1, P3, P4 Timing Measurement Circuit



Symbol	Parameter	Condition		Unit			
Symbol	Farameter	Condition	Min.	Тур.	Max.	Unit	
Vdet2	Voltage detection level Vdet2_0	At the falling of Vcc	3.70	4.00	4.30	V	
-	Hysteresis width at the rising of Vcc in voltage detection 2 circuit		_	0.10	-	V	
-	Voltage detection 2 circuit response time ⁽²⁾	At the falling of Vcc from 5 V to (Vdet2_0 – 0.1) V	_	20	150	μS	
-	Voltage detection circuit self power consumption	VCA27 = 1, Vcc = 5.0 V	-	1.7	-	μA	
td(E-A)	Waiting time until voltage detection circuit operation starts ⁽³⁾		-	-	100	μS	

Table 5.9 Voltage Detection 2 Circuit Electrical Characteristics

Notes:

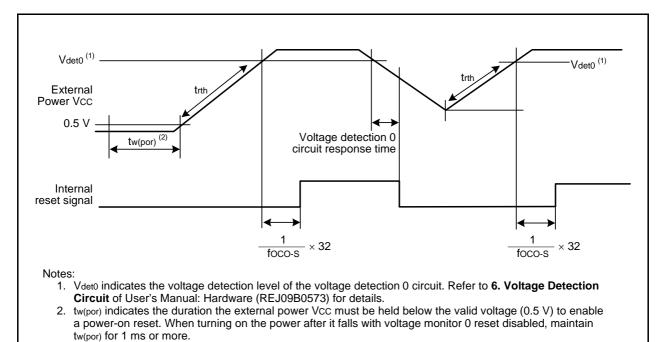
- 1. The measurement condition is Vcc = 1.8 V to 5.5 V and $T_{opr} = -20$ to 85°C (N version) / -40 to 85°C (D version).
- 2. Time until the voltage monitor 2 interrupt request is generated after the voltage passes Vdet2.
- 3. Necessary time until the voltage detection circuit operates after setting to 1 again after setting the VCA27 bit in the VCA2 register to 0.

Table 5.10 Power-on Reset Circuit ⁽²⁾

Symbol	Parameter	Condition		Standard			
	Falanetei	Condition	Min.	Тур.	Max.	Unit	
trth	External power Vcc rise gradient	(1)	0	-	50,000	mV/msec	

Notes:

- 1. The measurement condition is $T_{opr} = -20$ to $85^{\circ}C$ (N version) / -40 to $85^{\circ}C$ (D version), unless otherwise specified.
- 2. To use the power-on reset function, enable voltage monitor 0 reset by setting the LVDAS bit in the OFS register to 0.



Power-on Reset Circuit Electrical Characteristics

Figure 5.3



Symbol	bol Parameter		Condition		Standard			Unit
Symbol	F	rarameter	Condition	Condition		Тур.	Max.	Unit
Vон	Output "H"	Other than XOUT	Drive capacity High $Vcc = 5 V$	Iон = -20 mA	Vcc - 2.0	-	Vcc	V
	voltage		Drive capacity Low Vcc = 5 V	Iон = -5 mA	Vcc - 2.0	-	Vcc	V
		XOUT	Vcc = 5 V	Іон = -200 μА	1.0	-	Vcc	V
Vol	Output "L"	Other than XOUT	Drive capacity High $Vcc = 5 V$	IoL = 20 mA	-	-	2.0	V
	voltage		Drive capacity Low $Vcc = 5 V$	IoL = 5 mA	-	-	2.0	V
		XOUT	Vcc = 5 V	IoL = 200 μA	-	-	0.5	V
VT+-VT-	Hysteresis	INTO, INT1, INT3, KIO, KI1, KI2, KI3, TRAIO, TRBO, TRCIOA, TRCIOB, TRCIOC, TRCIOD, TRCTRG, TRCCLK, ADTRG, RXD0, RXD2, CLK0, CLK2, SSI, SCL, SDA, SSO RESET			0.1	1.2	_	V
Ін	Input "H" cur	rent	VI = 5 V, Vcc = 5.0 V		-	-	5.0	μΑ
lı∟	Input "L" current		VI = 0 V, Vcc = 5.0 V		-		-5.0	μΑ
Rpullup	Pull-up resistance		VI = 0 V, Vcc = 5.0 V		25	50	100	kΩ
Rfxin	Feedback resistance	XIN			-	0.3	_	MΩ
RfxCIN	Feedback resistance	XCIN			-	8	-	MΩ
Vram	RAM hold vo	oltage	During stop mode		1.8	-	-	V

Table 5.16	Electrical Characteristics (1) [4.2 V \leq Vcc \leq 5.5 V]
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Note:

1. $4.2 \text{ V} \le \text{Vcc} \le 5.5 \text{ V}$ and $\text{T}_{opr} = -20 \text{ to } 85^{\circ}\text{C}$ (N version) / -40 to 85°C (D version), f(XIN) = 20 MHz, unless otherwise specified.



Table 5.20 Serial Interface	Table 5.20	Serial Interface
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Symbol	Parameter		Standard		
	Falanlelei	Min.	Max.	Unit	
tc(CK)	CLKi input cycle time	200	-	ns	
tW(CKH)	CLKi input "H" width	100	-	ns	
tW(CKL)	CLKi input "L" width	100	-	ns	
td(C-Q)	TXDi output delay time	-	50	ns	
th(C-Q)	TXDi hold time	0	-	ns	
tsu(D-C)	RXDi input setup time		-	ns	
th(C-D)	RXDi input hold time	90	-	ns	

i = 0, 2

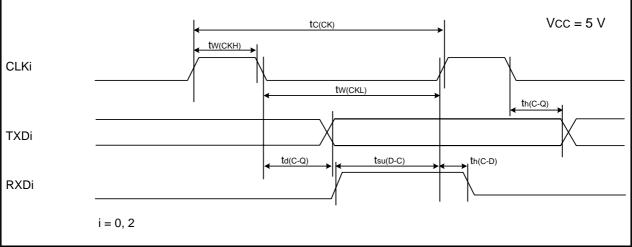


Figure 5.10 Serial Interface Timing Diagram when Vcc = 5 V

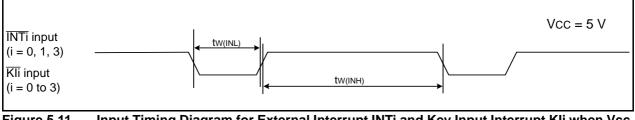
Table 5.21 External Interrupt INTi (i = 0, 1, 3) Input, Key Input Interrupt Kli (i = 0 to 3)

Symbol	Parameter		Standard		
Symbol			Max.	Unit	
tw(INH)	INTi input "H" width, Kli input "H" width	250 (1)	-	ns	
tw(INL)	INTi input "L" width, Kli input "L" width		-	ns	

Notes:

1. When selecting the digital filter by the INTi input filter select bit, use an INTi input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

2. When selecting the digital filter by the INTi input filter select bit, use an INTi input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.



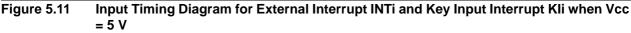


Table 5.23Electrical Characteristics (4) $[2.7 V \le Vcc < 3.3 V]$
(Topr = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter		Condition		Standar	d	Unit
Symbol				Min.	Тур.	Max.	Unit
lcc	Power supply current (Vcc = 2.7 to 3.3 V) Single-chip mode,	High-speed clock mode	XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	-	3.5	10	mA
	output pins are open, other pins are Vss		XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	-	1.5	7.5	mA
		High-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator on fOCO-F = 20 MHz Low-speed on-chip oscillator on = 125 kHz No division	-	7.0	15	mA
			XIN clock off High-speed on-chip oscillator on fOCO-F = 20 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	_	3.0	-	mA
			XIN clock off High-speed on-chip oscillator on fOCO-F = 10 MHz Low-speed on-chip oscillator on = 125 kHz No division	-	4.0	-	mA
			XIN clock off High-speed on-chip oscillator on fOCO-F = 10 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	-	1.5	-	mA
			XIN clock off High-speed on-chip oscillator on fOCO-F = 4 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-16 MSTIIC = MSTTRD = MSTTRC = 1	-	1	_	mA
		Low-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR27 = 1, VCA20 = 0	_	90	390	μA
		Low-speed clock mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz No division FMR27 = 1, VCA20 = 0	-	80	400	μA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz No division Program operation on RAM Flash memory off, FMSTP = 1, VCA20 = 0	-	40	_	μA
		Wait mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0, VCA20 = 1	-	15	90	μA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0, VCA20 = 1	-	4	80	μA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (peripheral clock off) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0, VCA20 = 1	-	3.5	-	μA
		Stop mode	XIN clock off, Topr = 25° C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	-	2.0	5.0	μA
			XIN clock off, Topr = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off	-	5.0	-	μA



Table 5.29Electrical Characteristics (6) [1.8 V \leq Vcc < 2.7 V]
(Topr = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter		Condition		Standar	b	Unit
Symbol				Min.	Тур.	Max.	Unit
Icc	Power supply current (Vcc = 1.8 to 2.7 V) Single-chip mode, output pins are open,	High-speed clock mode	XIN = 5 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	-	2.2	-	mA
	other pins are Vss		XIN = 5 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	-	0.8	-	mA
		High-speed on-chip oscillator	XIN clock off High-speed on-chip oscillator on fOCO-F = 5 MHz Low-speed on-chip oscillator on = 125 kHz No division	-	2.5	10	mA
		mode	XIN clock off High-speed on-chip oscillator on fOCO-F = 5 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	_	1.7	-	mA
			XIN clock off High-speed on-chip oscillator on fOCO-F = 4 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-16 MSTIIC = MSTTRD = MSTTRC = 1	-	1	-	mA
		Low-speed on- chip oscillator mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR27 = 1, VCA20 = 0	-	90	300	μA
		Low-speed clock mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz No division FMR27 = 1, VCA20 = 0	_	80	350	μΑ
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz No division Program operation on RAM Flash memory off, FMSTP = 1, VCA20 = 0	-	40	-	μΑ
		Wait mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	_	15	90	μA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	_	4	80	μA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (peripheral clock off) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	_	3.5	_	μA
		Stop mode	XIN clock off, Topr = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	_	2.0	5	μA
			XIN clock off, Topr = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	-	5.0	-	μA



REVISION HISTORY	R8C/32C Group Datasheet
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Rev.	Date		Description
	Dale	Page	Summary
0.10	Sep. 01, 2009	-	First Edition issued
1.00	Aug. 24, 2010	All	"Preliminary" and "Under development" deleted
		4	Table1.3 revised
		26 to 51	"5. Electrical Characteristics" added

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General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

- The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.
- 2. Processing at Power-on

The state of the product is undefined at the moment when power is supplied.

- The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
 - In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

Access to reserved addresses is prohibited.

- The reserved addresses are provided for the possible future expansion of functions. Do
 not access these addresses; the correct operation of LSI is not guaranteed if they are
 accessed.
- 4. Clock Signals

After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

- When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.
- 5. Differences between Products

Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

— The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.