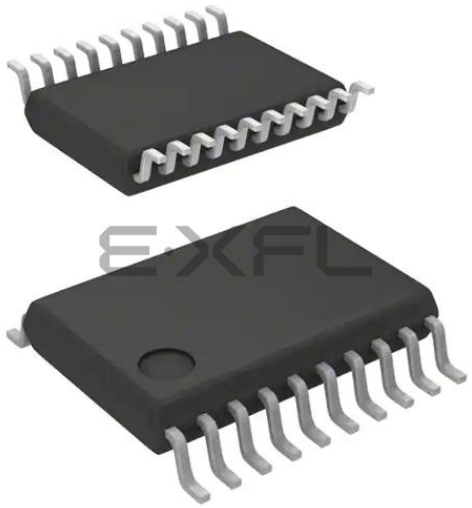
Renesas Electronics America Inc - R5F21322CNSP#U0 Datasheet



Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	I²C, LINbus, SIO, SSU, UART/USART
Peripherals	POR, PWM, Voltage Detect, WDT
Number of I/O	15
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-LSSOP (0.173", 4.40mm Width)
Supplier Device Package	20-LSSOP
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f21322cnsp-u0

1.5 Pin Functions

Tables 1.5 and 1.6 list Pin Functions.

Table 1.5 Pin Functions (1)

Item	Pin Name	I/O Type	Description
Power supply input	VCC, VSS	–	Apply 1.8 V to 5.5 V to the VCC pin. Apply 0 V to the VSS pin.
Analog power supply input	AVCC, AVSS	–	Power supply for the A/D converter. Connect a capacitor between AVCC and AVSS.
Reset input	$\overline{\text{RESET}}$	I	Input “L” on this pin resets the MCU.
MODE	MODE	I	Connect this pin to VCC via a resistor.
XIN clock input	XIN	I	These pins are provided for XIN clock generation circuit I/O. Connect a ceramic resonator or a crystal oscillator between the XIN and XOUT pins (1). To use an external clock, input it to the XOUT pin and leave the XIN pin open.
XIN clock output	XOUT	I/O	
XCIN clock input	XCIN	I	These pins are provided for XCIN clock generation circuit I/O. Connect a crystal oscillator between the XCIN and XCOUT pins (1). To use an external clock, input it to the XCIN pin and leave the XCOUT pin open.
XCIN clock output	XCOUT	O	
$\overline{\text{INT}}$ interrupt input	$\overline{\text{INT0}}$, $\overline{\text{INT1}}$, $\overline{\text{INT3}}$	I	$\overline{\text{INT}}$ interrupt input pins. $\overline{\text{INT0}}$ is timer RB, and RC input pin.
Key input interrupt	$\overline{\text{KI0}}$ to $\overline{\text{KI3}}$	I	Key input interrupt input pins
Timer RA	TRAIO	I/O	Timer RA I/O pin
	TRAO	O	Timer RA output pin
Timer RB	TRBO	O	Timer RB output pin
Timer RC	TRCCLK	I	External clock input pin
	TRCTRG	I	External trigger input pin
	TRCIOA, TRCIOB, TRCIOC, TRCIOD	I/O	Timer RC I/O pins
Serial interface	CLK0, CLK2	I/O	Transfer clock I/O pins
	RXD0, RXD2	I	Serial data input pins
	TXD0, TXD2	O	Serial data output pins
	$\overline{\text{CTS2}}$	I	Transmission control input pin
	$\overline{\text{RTS2}}$	O	Reception control output pin
	SCL2	I/O	I^2C mode clock I/O pin
	SDA2	I/O	I^2C mode data I/O pin
I^2C bus	SCL	I/O	Clock I/O pin
	SDA	I/O	Data I/O pin
SSU	SSI	I/O	Data I/O pin
	$\overline{\text{SCS}}$	I/O	Chip-select signal I/O pin
	SSCK	I/O	Clock I/O pin
	SSO	I/O	Data I/O pin

I: Input O: Output I/O: Input and output

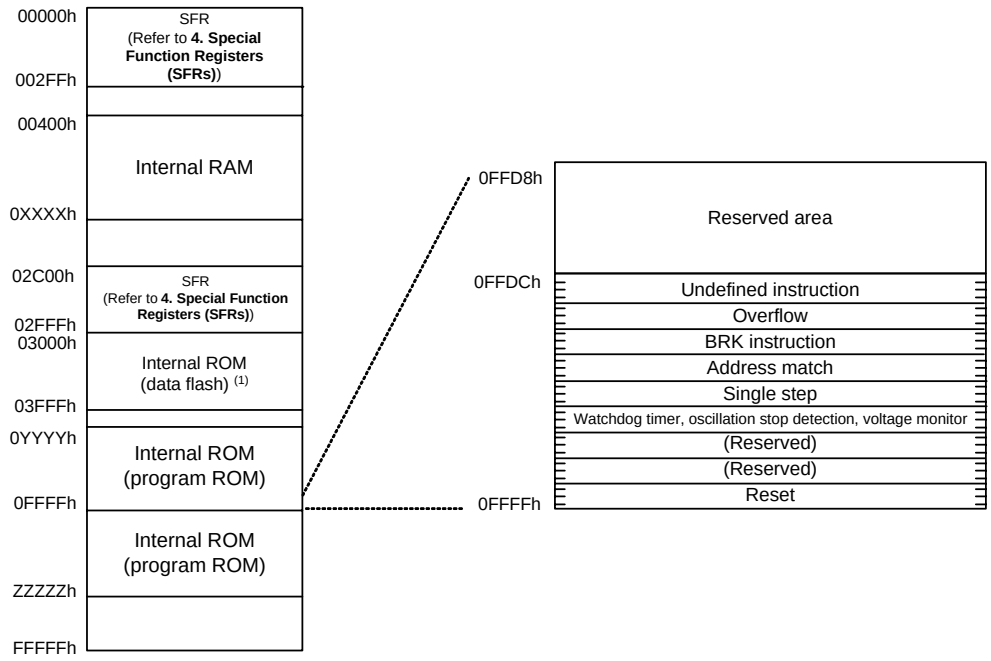
Note:

1. Refer to the oscillator manufacturer for oscillation characteristics.

3. Memory

3.1 R8C/32C Group

Figure 3.1 is a Memory Map of R8C/32C Group. The R8C/32C Group has a 1-Mbyte address space from addresses 00000h to FFFFFh. The internal ROM (program ROM) is allocated lower addresses, beginning with address 0FFFFh. For example, a 16-Kbyte internal ROM area is allocated addresses 0C000h to 0FFFFh.
The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. The starting address of each interrupt routine is stored here.
The internal ROM (data flash) is allocated addresses 03000h to 03FFFh.
The internal RAM is allocated higher addresses, beginning with address 00400h. For example, a 1.5-Kbyte internal RAM area is allocated addresses 00400h to 009FFh. The internal RAM is used not only for data storage but also as a stack area when a subroutine is called or when an interrupt request is acknowledged.
Special function registers (SFRs) are allocated addresses 00000h to 002FFh and 02C00h to 02FFFh. Peripheral function control registers are allocated here. All unallocated spaces within the SFRs are reserved and cannot be accessed by users.



Notes:
1. Data flash indicates block A (1 Kbyte), block B (1 Kbyte), block C (1 Kbyte), and block D (1 Kbyte).
2. The blank areas are reserved and cannot be accessed by users.

Part Number	Internal ROM			Internal RAM	
	Size	Address 0YYYYh	Address ZZZZZh	Size	Address 0XXXXh
R5F21321CNFP, R5F21321CDFP	4 Kbytes	0F000h	–	512 bytes	005FFh
R5F21322CNFP, R5F21322CDFP	8 Kbytes	0E000h	–	1 Kbyte	007FFh
R5F21324CNFP, R5F21324CDFP	16 Kbytes	0C000h	–	1.5 Kbytes	009FFh

Figure 3.1 Memory Map of R8C/32C Group

Table 4.2 SFR Information (2) (1)

Address	Register	Symbol	After Reset
003Ah	Voltage Monitor 2 Circuit Control Register	VW2C	10000010b
003Bh			
003Ch			
003Dh			
003Eh			
003Fh			
0040h			
0041h	Flash Memory Ready Interrupt Control Register	FMRDYIC	XXXXX000b
0042h			
0043h			
0044h			
0045h			
0046h			
0047h	Timer RC Interrupt Control Register	TRCIC	XXXXX000b
0048h			
0049h			
004Ah	Timer RE Interrupt Control Register	TREIC	XXXXX000b
004Bh	UART2 Transmit Interrupt Control Register	S2TIC	XXXXX000b
004Ch	UART2 Receive Interrupt Control Register	S2RIC	XXXXX000b
004Dh	Key Input Interrupt Control Register	KUPIC	XXXXX000b
004Eh	A/D Conversion Interrupt Control Register	ADIC	XXXXX000b
004Fh	SSU Interrupt Control Register / IIC bus Interrupt Control Register (2)	SSUIC / IICIC	XXXXX000b
0050h			
0051h	UART0 Transmit Interrupt Control Register	S0TIC	XXXXX000b
0052h	UART0 Receive Interrupt Control Register	S0RIC	XXXXX000b
0053h			
0054h			
0055h			
0056h	Timer RA Interrupt Control Register	TRAIC	XXXXX000b
0057h			
0058h	Timer RB Interrupt Control Register	TRBIC	XXXXX000b
0059h	INT1 Interrupt Control Register	INT1IC	XX00X000b
005Ah	INT3 Interrupt Control Register	INT3IC	XX00X000b
005Bh			
005Ch			
005Dh	INT0 Interrupt Control Register	INT0IC	XX00X000b
005Eh	UART2 Bus Collision Detection Interrupt Control Register	U2BCNIC	XXXXX000b
005Fh			
0060h			
0061h			
0062h			
0063h			
0064h			
0065h			
0066h			
0067h			
0068h			
0069h			
006Ah			
006Bh			
006Ch			
006Dh			
006Eh			
006Fh			
0070h			
0071h			
0072h	Voltage Monitor 1 Interrupt Control Register	VCMP1IC	XXXXX000b
0073h	Voltage Monitor 2 Interrupt Control Register	VCMP2IC	XXXXX000b
0074h			
0075h			
0076h			
0077h			
0078h			
0079h			
007Ah			
007Bh			
007Ch			
007Dh			
007Eh			
007Fh			

X: Undefined

Notes:
1. The blank areas are reserved and cannot be accessed by users.
2. Selectable by the IICSEL bit in the SSUIICSR register.

Table 4.3 SFR Information (3) (1)

Address	Register	Symbol	After Reset
0080h	DTC Activation Control Register	DTCTL	00h
0081h			
0082h			
0083h			
0084h			
0085h			
0086h			
0087h			
0088h	DTC Activation Enable Register 0	DTCEN0	00h
0089h	DTC Activation Enable Register 1	DTCEN1	00h
008Ah	DTC Activation Enable Register 2	DTCEN2	00h
008Bh	DTC Activation Enable Register 3	DTCEN3	00h
008Ch			
008Dh	DTC Activation Enable Register 5	DTCEN5	00h
008Eh	DTC Activation Enable Register 6	DTCEN6	00h
008Fh			
0090h			
0091h			
0092h			
0093h			
0094h			
0095h			
0096h			
0097h			
0098h			
0099h			
009Ah			
009Bh			
009Ch			
009Dh			
009Eh			
009Fh			
00A0h	UART0 Transmit / Receive Mode Register	U0MR	00h
00A1h	UART0 Bit Rate Register	U0BRG	XXh
00A2h	UART0 Transmit Buffer Register	U0TB	XXh
00A3h			XXh
00A4h	UART0 Transmit / Receive Control Register 0	U0C0	00001000b
00A5h	UART0 Transmit / Receive Control Register 1	U0C1	00000010b
00A6h	UART0 Receive Buffer Register	U0RB	XXh
00A7h			XXh
00A8h	UART2 Transmit / Receive Mode Register	U2MR	00h
00A9h	UART2 Bit Rate Register	U2BRG	XXh
00AAh	UART2 Transmit Buffer Register	U2TB	XXh
00ABh			XXh
00ACh	UART2 Transmit / Receive Control Register 0	U2C0	00001000b
00ADh	UART2 Transmit / Receive Control Register 1	U2C1	00000010b
00AEh	UART2 Receive Buffer Register	U2RB	XXh
00AFh			XXh
00B0h	UART2 Digital Filter Function Select Register	URXDF	00h
00B1h			
00B2h			
00B3h			
00B4h			
00B5h			
00B6h			
00B7h			
00B8h			
00B9h			
00BAh			
00BBh	UART2 Special Mode Register 5	U2SMR5	00h
00BCh	UART2 Special Mode Register 4	U2SMR4	00h
00BDh	UART2 Special Mode Register 3	U2SMR3	000X0X0Xb
00BEh	UART2 Special Mode Register 2	U2SMR2	X0000000b
00BFh	UART2 Special Mode Register	U2SMR	X0000000b

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.5 SFR Information (5) (1)

Address	Register	Symbol	After Reset
0100h	Timer RA Control Register	TRACR	00h
0101h	Timer RA I/O Control Register	TRAIOC	00h
0102h	Timer RA Mode Register	TRAMR	00h
0103h	Timer RA Prescaler Register	TRAPRE	FFh
0104h	Timer RA Register	TRA	FFh
0105h	LIN Control Register 2	LINCR2	00h
0106h	LIN Control Register	LINCR	00h
0107h	LIN Status Register	LINST	00h
0108h	Timer RB Control Register	TRBCR	00h
0109h	Timer RB One-Shot Control Register	TRBOCR	00h
010Ah	Timer RB I/O Control Register	TRBIOC	00h
010Bh	Timer RB Mode Register	TRBMR	00h
010Ch	Timer RB Prescaler Register	TRBPRE	FFh
010Dh	Timer RB Secondary Register	TRBSC	FFh
010Eh	Timer RB Primary Register	TRBPR	FFh
010Fh			
0110h			
0111h			
0112h			
0113h			
0114h			
0115h			
0116h			
0117h			
0118h	Timer RE Second Data Register / Counter Data Register	TRESEC	00h
0119h	Timer RE Minute Data Register / Compare Data Register	TREMIN	00h
011Ah	Timer RE Hour Data Register	TREHR	00h
011Bh	Timer RE Day of Week Data Register	TREWK	00h
011Ch	Timer RE Control Register 1	TRECR1	00h
011Dh	Timer RE Control Register 2	TRECR2	00h
011Eh	Timer RE Count Source Select Register	TRECSR	00001000b
011Fh			
0120h	Timer RC Mode Register	TRCMR	01001000b
0121h	Timer RC Control Register 1	TRCCR1	00h
0122h	Timer RC Interrupt Enable Register	TRCIER	01110000b
0123h	Timer RC Status Register	TRCSR	01110000b
0124h	Timer RC I/O Control Register 0	TRCIOR0	10001000b
0125h	Timer RC I/O Control Register 1	TRCIOR1	10001000b
0126h	Timer RC Counter	TRC	00h
0127h			00h
0128h	Timer RC General Register A	TRCGRA	FFh
0129h			FFh
012Ah	Timer RC General Register B	TRCGRB	FFh
012Bh			FFh
012Ch	Timer RC General Register C	TRCGRC	FFh
012Dh			FFh
012Eh	Timer RC General Register D	TRCGRD	FFh
012Fh			FFh
0130h	Timer RC Control Register 2	TRCCR2	00011000b
0131h	Timer RC Digital Filter Function Select Register	TRCDF	00h
0132h	Timer RC Output Master Enable Register	TRCOER	01111111b
0133h	Timer RC Trigger Control Register	TRCADCR	00h
0134h			
0135h			
0136h			
0137h			
0138h			
0139h			
013Ah			
013Bh			
013Ch			
013Dh			
013Eh			
013Fh			

Note:
1. The blank areas are reserved and cannot be accessed by users.

Table 4.6 SFR Information (6) (1)

Address	Register	Symbol	After Reset
0140h			
0141h			
0142h			
0143h			
0144h			
0145h			
0146h			
0147h			
0148h			
0149h			
014Ah			
014Bh			
014Ch			
014Dh			
014Eh			
014Fh			
0150h			
0151h			
0152h			
0153h			
0154h			
0155h			
0156h			
0157h			
0158h			
0159h			
015Ah			
015Bh			
015Ch			
015Dh			
015Eh			
015Fh			
0160h			
0161h			
0162h			
0163h			
0164h			
0165h			
0166h			
0167h			
0168h			
0169h			
016Ah			
016Bh			
016Ch			
016Dh			
016Eh			
016Fh			
0170h			
0171h			
0172h			
0173h			
0174h			
0175h			
0176h			
0177h			
0178h			
0179h			
017Ah			
017Bh			
017Ch			
017Dh			
017Eh			
017Fh			

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.8 SFR Information (8) (1)

Address	Register	Symbol	After Reset
01C0h	Address Match Interrupt Register 0	RMAD0	XXh
01C1h			XXh
01C2h			0000XXXXb
01C3h	Address Match Interrupt Enable Register 0	AIER0	00h
01C4h	Address Match Interrupt Register 1	RMAD1	XXh
01C5h			XXh
01C6h			0000XXXXb
01C7h	Address Match Interrupt Enable Register 1	AIER1	00h
01C8h			
01C9h			
01CAh			
01CBh			
01CCh			
01CDh			
01CEh			
01CFh			
01D0h			
01D1h			
01D2h			
01D3h			
01D4h			
01D5h			
01D6h			
01D7h			
01D8h			
01D9h			
01DAh			
01DBh			
01DCh			
01DDh			
01DEh			
01DFh			
01E0h	Pull-Up Control Register 0	PUR0	00h
01E1h	Pull-Up Control Register 1	PUR1	00h
01E2h			
01E3h			
01E4h			
01E5h			
01E6h			
01E7h			
01E8h			
01E9h			
01EAh			
01EBh			
01ECh			
01EDh			
01EEh			
01EFh			
01F0h	Port P1 Drive Capacity Control Register	P1DRR	00h
01F1h			
01F2h	Drive Capacity Control Register 0	DRR0	00h
01F3h	Drive Capacity Control Register 1	DRR1	00h
01F4h			
01F5h	Input Threshold Control Register 0	VLT0	00h
01F6h	Input Threshold Control Register 1	VLT1	00h
01F7h			
01F8h	Comparator B Control Register 0	INTCMP	00h
01F9h			
01FAh	External Input Enable Register 0	INTEN	00h
01FBh			
01FCh	INT Input Filter Select Register 0	INTF	00h
01FDh			
01FEh	Key Input Enable Register 0	KIEN	00h
01FFh			

X: Undefined
Note:
1. The blank areas are reserved and cannot be accessed by users.

Table 4.9 SFR Information (9) (1)

Address	Register	Symbol	After Reset
2C00h	DTC Transfer Vector Area		XXh
2C01h	DTC Transfer Vector Area		XXh
2C02h	DTC Transfer Vector Area		XXh
2C03h	DTC Transfer Vector Area		XXh
2C04h	DTC Transfer Vector Area		XXh
2C05h	DTC Transfer Vector Area		XXh
2C06h	DTC Transfer Vector Area		XXh
2C07h	DTC Transfer Vector Area		XXh
2C08h	DTC Transfer Vector Area		XXh
2C09h	DTC Transfer Vector Area		XXh
2C0Ah	DTC Transfer Vector Area		XXh
:	DTC Transfer Vector Area		XXh
:	DTC Transfer Vector Area		XXh
2C3Ah	DTC Transfer Vector Area		XXh
2C3Bh	DTC Transfer Vector Area		XXh
2C3Ch	DTC Transfer Vector Area		XXh
2C3Dh	DTC Transfer Vector Area		XXh
2C3Eh	DTC Transfer Vector Area		XXh
2C3Fh	DTC Transfer Vector Area		XXh
2C40h	DTC Control Data 0	DTCD0	XXh
2C41h			XXh
2C42h			XXh
2C43h			XXh
2C44h			XXh
2C45h			XXh
2C46h			XXh
2C47h			XXh
2C48h	DTC Control Data 1	DTCD1	XXh
2C49h			XXh
2C4Ah			XXh
2C4Bh			XXh
2C4Ch			XXh
2C4Dh			XXh
2C4Eh			XXh
2C4Fh			XXh
2C50h	DTC Control Data 2	DTCD2	XXh
2C51h			XXh
2C52h			XXh
2C53h			XXh
2C54h			XXh
2C55h			XXh
2C56h			XXh
2C57h			XXh
2C58h	DTC Control Data 3	DTCD3	XXh
2C59h			XXh
2C5Ah			XXh
2C5Bh			XXh
2C5Ch			XXh
2C5Dh			XXh
2C5Eh			XXh
2C5Fh			XXh
2C60h	DTC Control Data 4	DTCD4	XXh
2C61h			XXh
2C62h			XXh
2C63h			XXh
2C64h			XXh
2C65h			XXh
2C66h			XXh
2C67h			XXh
2C68h	DTC Control Data 5	DTCD5	XXh
2C69h			XXh
2C6Ah			XXh
2C6Bh			XXh
2C6Ch			XXh
2C6Dh			XXh
2C6Eh			XXh
2C6Fh			XXh

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.11 SFR Information (11) (1)

Address	Register	Symbol	After Reset
2CB0h	DTC Control Data 14	DTCD14	XXh
2CB1h			XXh
2CB2h			XXh
2CB3h			XXh
2CB4h			XXh
2CB5h			XXh
2CB6h			XXh
2CB7h			XXh
2CB8h	DTC Control Data 15	DTCD15	XXh
2CB9h			XXh
2CBAh			XXh
2CBBh			XXh
2CBCh			XXh
2CBDh			XXh
2CBEh			XXh
2CBFh			XXh
2CC0h	DTC Control Data 16	DTCD16	XXh
2CC1h			XXh
2CC2h			XXh
2CC3h			XXh
2CC4h			XXh
2CC5h			XXh
2CC6h			XXh
2CC7h			XXh
2CC8h	DTC Control Data 17	DTCD17	XXh
2CC9h			XXh
2CCAh			XXh
2CCBh			XXh
2CCCh			XXh
2CCDh			XXh
2CCEh			XXh
2CCFh			XXh
2CD0h	DTC Control Data 18	DTCD18	XXh
2CD1h			XXh
2CD2h			XXh
2CD3h			XXh
2CD4h			XXh
2CD5h			XXh
2CD6h			XXh
2CD7h			XXh
2CD8h	DTC Control Data 19	DTCD19	XXh
2CD9h			XXh
2CDAh			XXh
2CDBh			XXh
2CDCh			XXh
2CDDh			XXh
2CDEh			XXh
2CDFh			XXh
2CE0h	DTC Control Data 20	DTCD20	XXh
2CE1h			XXh
2CE2h			XXh
2CE3h			XXh
2CE4h			XXh
2CE5h			XXh
2CE6h			XXh
2CE7h			XXh
2CE8h	DTC Control Data 21	DTCD21	XXh
2CE9h			XXh
2CEAh			XXh
2CEBh			XXh
2CECh			XXh
2CEDh			XXh
2CEEh			XXh
2CEFh			XXh

X: Undefined
Note:
1. The blank areas are reserved and cannot be accessed by users.

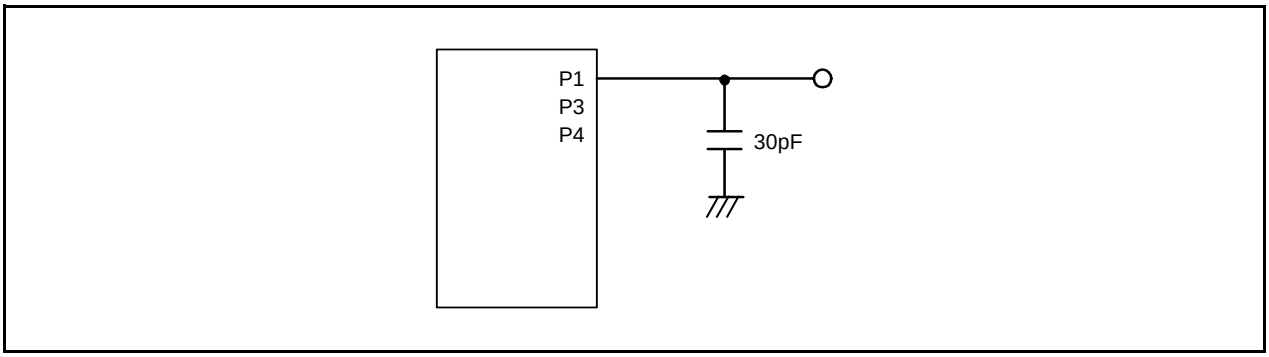


Figure 5.1 Ports P1, P3, P4 Timing Measurement Circuit

Table 5.3 A/D Converter Characteristics

Symbol	Parameter		Conditions		Standard			Unit
					Min.	Typ.	Max.	
–	Resolution		V_{ref} = AV_{CC}		–	–	10	Bit
–	Absolute accuracy	10-bit mode	V_{ref} = AV_{CC} = 5.0 V	AN8 to AN11 input	–	–	±3	LSB
			V_{ref} = AV_{CC} = 3.3 V	AN8 to AN11 input	–	–	±5	LSB
			V_{ref} = AV_{CC} = 3.0 V	AN8 to AN11 input	–	–	±5	LSB
			V_{ref} = AV_{CC} = 2.2 V	AN8 to AN11 input	–	–	±5	LSB
		8-bit mode	V_{ref} = AV_{CC} = 5.0 V	AN8 to AN11 input	–	–	±2	LSB
			V_{ref} = AV_{CC} = 3.3 V	AN8 to AN11 input	–	–	±2	LSB
			V_{ref} = AV_{CC} = 3.0 V	AN8 to AN11 input	–	–	±2	LSB
			V_{ref} = AV_{CC} = 2.2 V	AN8 to AN11 input	–	–	±2	LSB
ϕAD	A/D conversion clock		4.0 V ≤ V_{ref} = AV_{CC} ≤ 5.5 V (2)		2	–	20	MHz
			3.2 V ≤ V_{ref} = AV_{CC} ≤ 5.5 V (2)		2	–	16	MHz
			2.7 V ≤ V_{ref} = AV_{CC} ≤ 5.5 V (2)		2	–	10	MHz
			2.2 V ≤ V_{ref} = AV_{CC} ≤ 5.5 V (2)		2	–	5	MHz
–	Tolerance level impedance				–	3	–	kΩ
t_{CONV}	Conversion time	10-bit mode	V_{ref} = AV_{CC} = 5.0 V, ϕAD = 20 MHz		2.2	–	–	µs
		8-bit mode	V_{ref} = AV_{CC} = 5.0 V, ϕAD = 20 MHz		2.2	–	–	µs
t_{SAMP}	Sampling time		ϕAD = 20 MHz		0.8	–	–	µs
I_{Vref}	V_{ref} current		V_{CC} = 5 V, XIN = f1 = ϕAD = 20 MHz		–	45	–	µA
V_{ref}	Reference voltage				2.2	–	AV_{CC}	V
V_{IA}	Analog input voltage (3)				0	–	V_{ref}	V
OCVREF	On-chip reference voltage		2 MHz ≤ ϕAD ≤ 4 MHz		1.19	1.34	1.49	V

Notes:
1. V_{CC}/AV_{CC} = V_{ref} = 2.2 to 5.5 V, V_{SS} = 0 V and T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.
2. The A/D conversion result will be undefined in wait mode, stop mode, when the flash memory stops, and in low-current-consumption mode. Do not perform A/D conversion in these states or transition to these states during A/D conversion.
3. When the analog input voltage is over the reference voltage, the A/D conversion result will be 3FFh in 10-bit mode and FFh in 8-bit mode.

Table 5.4 Comparator B Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
Vref	IVREF1, IVREF3 input reference voltage		0	–	V_{CC} – 1.4	V
V_I	IVCMP1, IVCMP3 input voltage		–0.3	–	V_{CC} + 0.3	V
–	Offset		–	5	100	mV
t_d	Comparator output delay time (2)	V_I = Vref ± 100 mV	–	0.1	–	µs
I_{CMP}	Comparator operating current	V_{CC} = 5.0 V	–	17.5	–	µA

Notes:
1. V_{CC} = 2.7 to 5.5 V, T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.
2. When the digital filter is disabled.

Table 5.5 Flash Memory (Program ROM) Electrical Characteristics

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
–	Program/erase endurance (2)		1,000 (3)	–	–	times
–	Byte program time		–	80	500	µs
–	Block erase time		–	0.3	–	s
$t_{d(SR-SUS)}$	Time delay from suspend request until suspend		–	–	5 + CPU clock × 3 cycles	ms
–	Interval from erase start/restart until following suspend request		0	–	–	µs
–	Time from suspend until erase restart		–	–	30+CPU clock × 1 cycle	µs
$t_{d(CMDRST-READY)}$	Time from when command is forcibly terminated until reading is enabled		–	–	30+CPU clock × 1 cycle	µs
–	Program, erase voltage		2.7	–	5.5	V
–	Read voltage		1.8	–	5.5	V
–	Program, erase temperature		0	–	60	°C
–	Data hold time (7)	Ambient temperature = 55°C	20	–	–	year

Notes:
1. V_{CC} = 2.7 to 5.5 V and T_{opr} = 0 to 60°C, unless otherwise specified.
2. Definition of programming/erasure endurance
   The programming and erasure endurance is defined on a per-block basis.
   If the programming and erasure endurance is n (n = 1,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.
   However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
3. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
4. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
5. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
6. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
7. The data hold time includes time that the power supply is off or the clock is not supplied.

Table 5.6 Flash Memory (Data flash Block A to Block D) Electrical Characteristics

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
–	Program/erase endurance (2)		10,000 (3)	–	–	times
–	Byte program time (program/erase endurance ≤ 1,000 times)		–	160	1,500	µs
–	Byte program time (program/erase endurance > 1,000 times)		–	300	1,500	µs
–	Block erase time (program/erase endurance ≤ 1,000 times)		–	0.2	1	s
–	Block erase time (program/erase endurance > 1,000 times)		–	0.3	1	s
$t_{d(SR-SUS)}$	Time delay from suspend request until suspend		–	–	5 + CPU clock × 3 cycles	ms
–	Interval from erase start/restart until following suspend request		0	–	–	µs
–	Time from suspend until erase restart		–	–	30+CPU clock × 1 cycle	µs
$t_{d(CMDRST-READY)}$	Time from when command is forcibly terminated until reading is enabled		–	–	30+CPU clock × 1 cycle	µs
–	Program, erase voltage		2.7	–	5.5	V
–	Read voltage		1.8	–	5.5	V
–	Program, erase temperature		–20 (7)	–	85	°C
–	Data hold time (8)	Ambient temperature = 55 °C	20	–	–	year

Notes:
1. V_{CC} = 2.7 to 5.5 V and T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.
2. Definition of programming/erasure endurance
   The programming and erasure endurance is defined on a per-block basis.
   If the programming and erasure endurance is n (n = 10,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.
   However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
3. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
4. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. In addition, averaging the erasure endurance between blocks A to D can further reduce the actual erasure endurance. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
5. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
6. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
7. –40°C for D version.
8. The data hold time includes time that the power supply is off or the clock is not supplied.

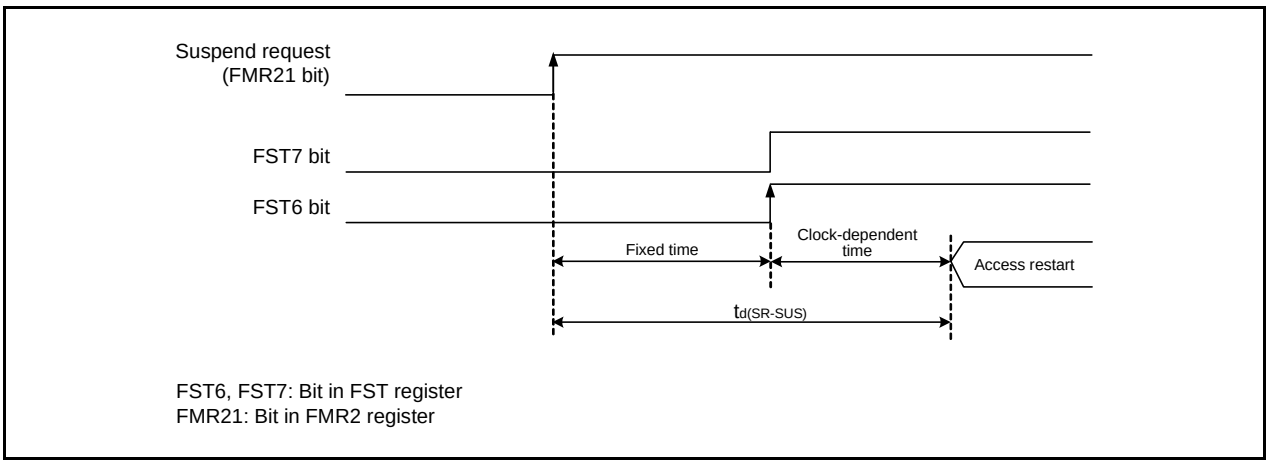


Figure 5.2 Time delay until Suspend

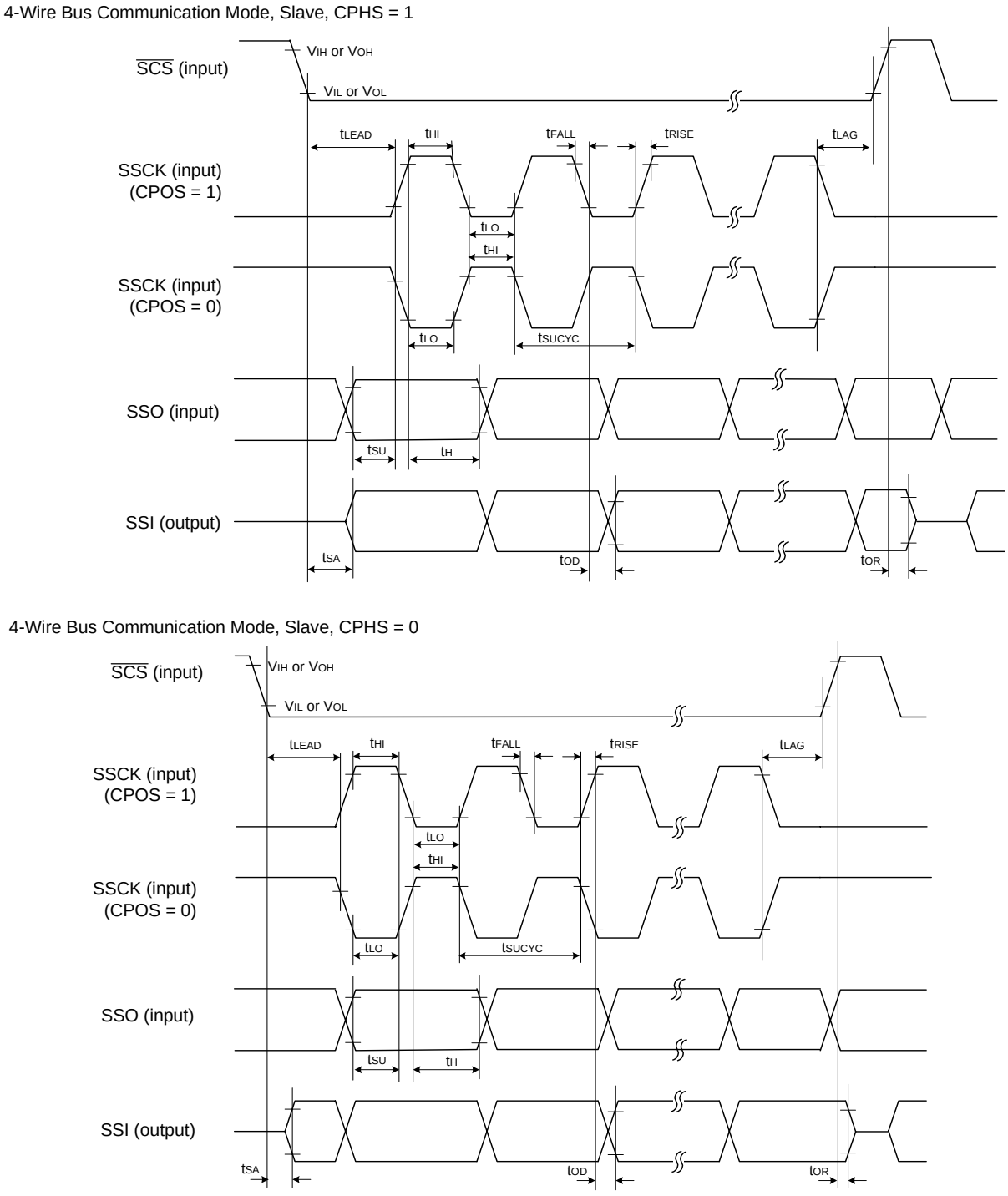


Figure 5.5 I/O Timing of Synchronous Serial Communication Unit (SSU) (Slave)

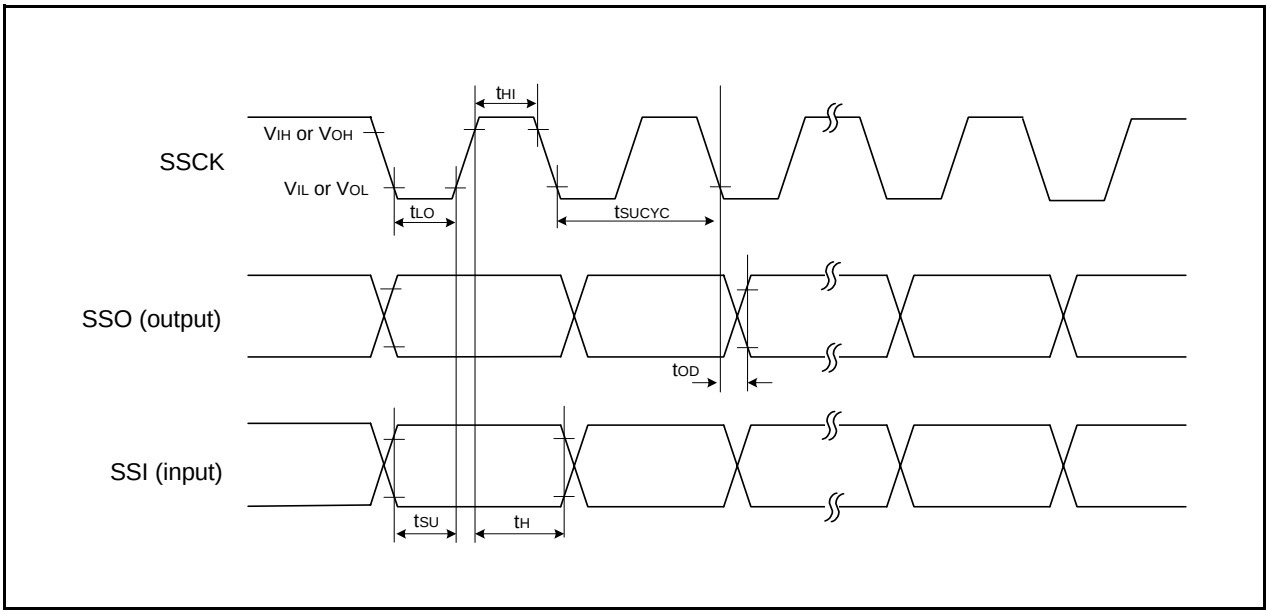


Figure 5.6 I/O Timing of Synchronous Serial Communication Unit (SSU) (Clock Synchronous Communication Mode)

Table 5.26 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	300	–	ns
$t_{W(CKH)}$	CLKi input “H” width	150	–	ns
$t_{W(CKL)}$	CLKi Input “L” width	150	–	ns
$t_{d(C-Q)}$	TXDi output delay time	–	80	ns
$t_{h(C-Q)}$	TXDi hold time	0	–	ns
$t_{su(D-C)}$	RXDi input setup time	70	–	ns
$t_{h(C-D)}$	RXDi input hold time	90	–	ns

i = 0, 2

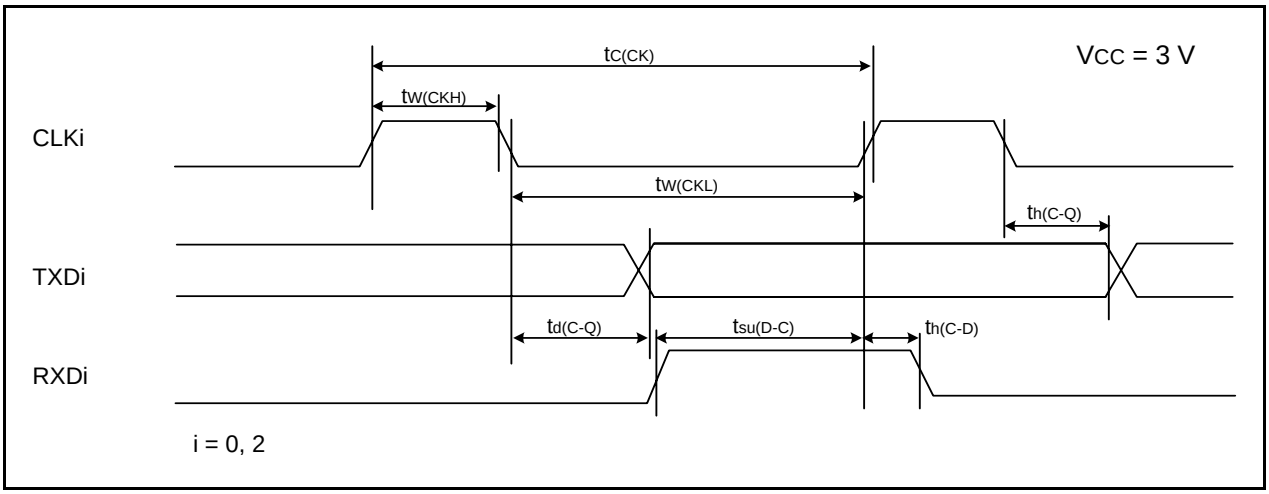


Figure 5.14 Serial Interface Timing Diagram when VCC = 3 V

Table 5.27 External Interrupt $\overline{INTi}$ (i = 0, 1, 3) Input, Key Input Interrupt $\overline{KIi}$ (i = 0 to 3)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{W(INH)}$	$\overline{INTi}$ input “H” width, $\overline{KIi}$ input “H” width	380 (1)	–	ns
$t_{W(INL)}$	$\overline{INTi}$ input “L” width, $\overline{KIi}$ input “L” width	380 (2)	–	ns

Notes:
1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

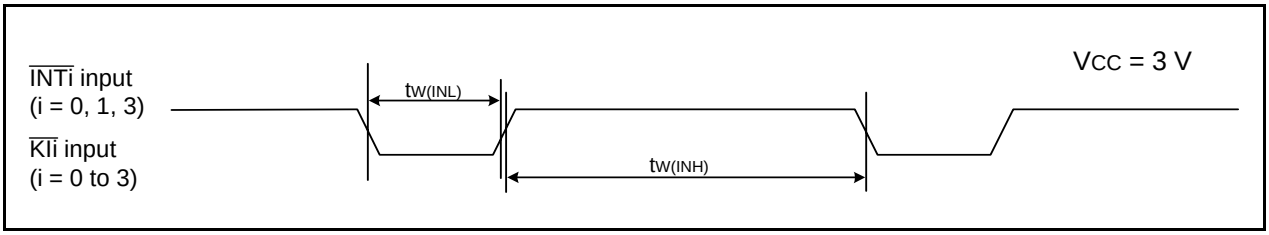


Figure 5.15 Input Timing Diagram for External Interrupt INTi and Key Input Interrupt KIi when Vcc = 3 V

Table 5.29 Electrical Characteristics (6) [1.8 V ≤ Vcc < 2.7 V]
(Topr = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition		Standard			Unit
				Min.	Typ.	Max.	
ICC	Power supply current (VCC = 1.8 to 2.7 V) Single-chip mode, output pins are open, other pins are VSS	High-speed clock mode	XIN = 5 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	2.2	–	mA
			XIN = 5 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	0.8	–	mA
		High-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator on fOCO-F = 5 MHz Low-speed on-chip oscillator on = 125 kHz No division	–	2.5	10	mA
			XIN clock off High-speed on-chip oscillator on fOCO-F = 5 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	1.7	–	mA
			XIN clock off High-speed on-chip oscillator on fOCO-F = 4 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-16 MSTIIC = MSTTRD = MSTTRC = 1	–	1	–	mA
		Low-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR27 = 1, VCA20 = 0	–	90	300	µA
		Low-speed clock mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz No division FMR27 = 1, VCA20 = 0	–	80	350	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz No division Program operation on RAM Flash memory off, FMSTP = 1, VCA20 = 0	–	40	–	µA
		Wait mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	15	90	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	4	80	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (peripheral clock off) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	3.5	–	µA
		Stop mode	XIN clock off, Topr = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	–	2.0	5	µA
			XIN clock off, Topr = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	–	5.0	–	µA

Table 5.32 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	800	–	ns
$t_{W(CKH)}$	CLKi input “H” width	400	–	ns
$t_{W(CKL)}$	CLKi input “L” width	400	–	ns
$t_{d(C-Q)}$	TXDi output delay time	–	200	ns
$t_{h(C-Q)}$	TXDi hold time	0	–	ns
$t_{su(D-C)}$	RXDi input setup time	150	–	ns
$t_{h(C-D)}$	RXDi input hold time	90	–	ns

i = 0, 2

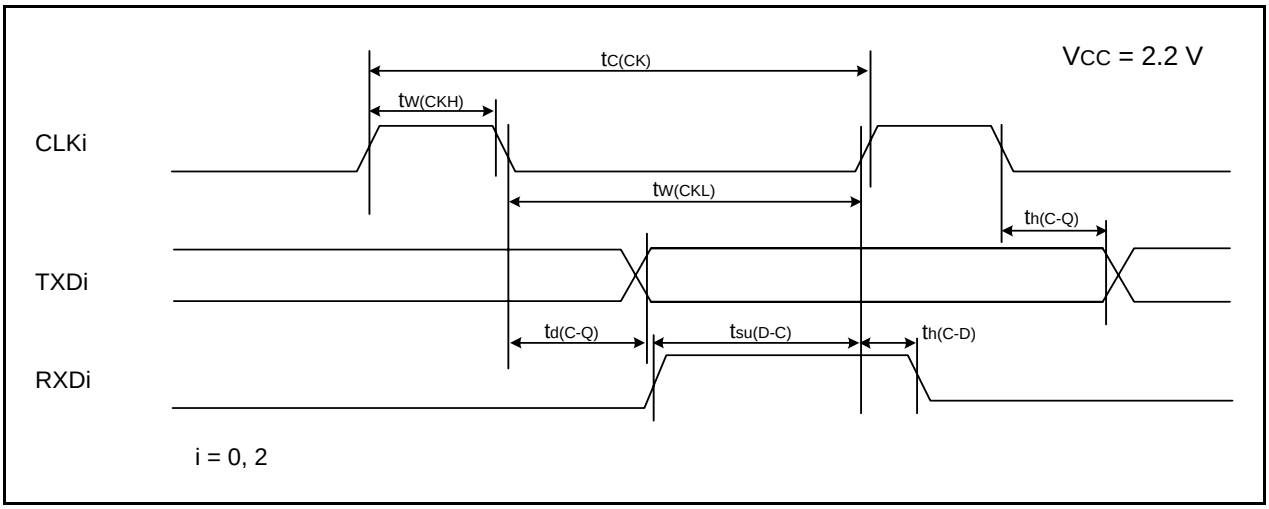


Figure 5.18 Serial Interface Timing Diagram when VCC = 2.2 V

Table 5.33 External Interrupt $\overline{INTi}$ (i = 0, 1, 3) Input, Key Input Interrupt $\overline{KIi}$ (i = 0 to 3)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{W(INH)}$	$\overline{INTi}$ input “H” width, $\overline{KIi}$ input “H” width	1000 (1)	–	ns
$t_{W(INL)}$	$\overline{INTi}$ input “L” width, $\overline{KIi}$ input “L” width	1000 (2)	–	ns

Notes:
1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

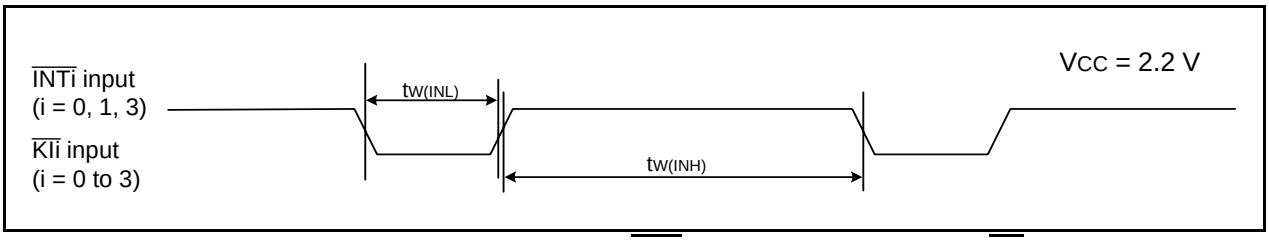


Figure 5.19 Input Timing for External Interrupt $\overline{INTi}$ and Key Input Interrupt $\overline{KIi}$ when Vcc = 2.2 V

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

Notice

1. All information included in this document is current as of the date this document is issued. Such information, however, is subject to change without any prior notice. Before purchasing or using any Renesas Electronics products listed herein, please confirm the latest product information with a Renesas Electronics sales office. Also, please pay regular and careful attention to additional and different information to be disclosed by Renesas Electronics such as that disclosed through our website.
2. Renesas Electronics does not assume any liability for infringement of patents, copyrights, or other intellectual property rights of third parties by or arising from the use of Renesas Electronics products or technical information described in this document. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
3. You should not alter, modify, copy, or otherwise misappropriate any Renesas Electronics product, whether in whole or in part.
4. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation of these circuits, software, and information in the design of your equipment. Renesas Electronics assumes no responsibility for any losses incurred by you or third parties arising from the use of these circuits, software, or information.
5. When exporting the products or technology described in this document, you should comply with the applicable export control laws and regulations and follow the procedures required by such laws and regulations. You should not use Renesas Electronics products or the technology described in this document for any purpose relating to military applications or use by the military, including but not limited to the development of weapons of mass destruction. Renesas Electronics products and technology may not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations.
6. Renesas Electronics has used reasonable care in preparing the information included in this document, but Renesas Electronics does not warrant that such information is error free. Renesas Electronics assumes no liability whatsoever for any damages incurred by you resulting from errors in or omissions from the information included herein.
7. Renesas Electronics products are classified according to the following three quality grades: "Standard", "High Quality", and "Specific". The recommended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below. You must check the quality grade of each Renesas Electronics product before using it in a particular application. You may not use any Renesas Electronics product for any application categorized as "Specific" without the prior written consent of Renesas Electronics. Further, you may not use any Renesas Electronics product for any application for which it is not intended without the prior written consent of Renesas Electronics. Renesas Electronics shall not be in any way liable for any damages or losses incurred by you or third parties arising from the use of any Renesas Electronics product for an application categorized as "Specific" or for which the product is not intended where you have failed to obtain the prior written consent of Renesas Electronics. The quality grade of each Renesas Electronics product is "Standard" unless otherwise expressly specified in a Renesas Electronics data sheets or data books, etc.
   - "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; and industrial robots.
   - "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control systems; anti-disaster systems; anti-crime systems; safety equipment; and medical equipment not specifically designed for life support.
   - "Specific": Aircraft; aerospace equipment; submersible repeaters; nuclear reactor control systems; medical equipment or systems for life support (e.g. artificial life support devices or systems), surgical implantations, or healthcare intervention (e.g. excision, etc.), and any other applications or purposes that pose a direct threat to human life.
8. You should use the Renesas Electronics products described in this document within the range specified by Renesas Electronics, especially with respect to the maximum rating, operating supply voltage range, movement power voltage range, heat radiation characteristics, installation and other product characteristics. Renesas Electronics shall have no liability for malfunctions or damages arising out of the use of Renesas Electronics products beyond such specified ranges.
9. Although Renesas Electronics endeavors to improve the quality and reliability of its products, semiconductor products have specific characteristics such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Further, Renesas Electronics products are not subject to radiation resistance design. Please be sure to implement safety measures to guard them against the possibility of physical injury, and injury or damage caused by fire in the event of the failure of a Renesas Electronics product, such as safety design for hardware and software including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult, please evaluate the safety of the final products or system manufactured by you.
10. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. Please use Renesas Electronics products in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. Renesas Electronics assumes no liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
11. This document may not be reproduced or duplicated, in any form, in whole or in part, without prior written consent of Renesas Electronics.
12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products, or if you have any other inquiries.

(Note 1) "Renesas Electronics" as used in this document means Renesas Electronics Corporation and also includes its majority-owned subsidiaries.

(Note 2) "Renesas Electronics product(s)" means any product developed or manufactured by or for Renesas Electronics.

RENESAS

SALES OFFICES Renesas Electronics Corporation http://www.renesas.com

Refer to "http://www.renesas.com/" for the latest and detailed information.

Renesas Electronics America Inc.
2880 Scott Boulevard Santa Clara, CA 95050-2554, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited
1101 Nicholson Road, Newmarket, Ontario L3Y 9C3, Canada
Tel: +1-905-898-5441, Fax: +1-905-898-3220

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-585-100, Fax: +44-1628-585-900

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-65030, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
7th Floor, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100083, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 204, 205, AZIA Center, No.1233 Lujiazui Ring Rd., Pudong District, Shanghai 200120, China
Tel: +86-21-5877-1818, Fax: +86-21-6887-7858 / -7898

Renesas Electronics Hong Kong Limited
Unit 1601-1613, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2886-9318, Fax: +852 2886-9022/9044

Renesas Electronics Taiwan Co., Ltd.
7F, No. 363 Fu Shing North Road Taipei, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
1 harbourFront Avenue, #06-10, keppel Bay Tower, Singapore 098632
Tel: +65-6213-0200, Fax: +65-6278-8001

Renesas Electronics Malaysia Sdn.Bhd.
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics Korea Co., Ltd.
11F., Samik Lavied' or Bldg., 720-2 Yeoksam-Dong, Kangnam-Ku, Seoul 135-080, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141

Colophon 1.0