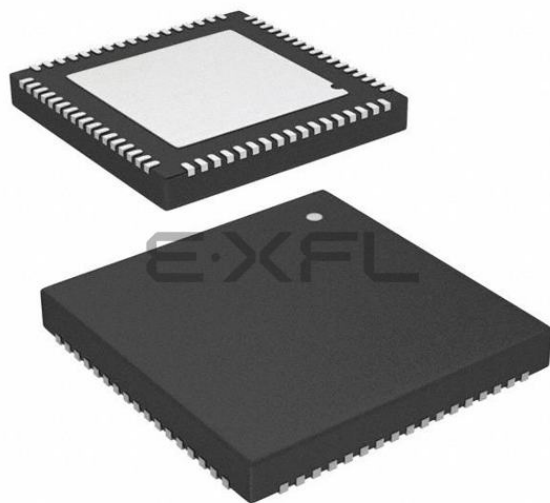




Welcome to [E-XFL.COM](#)

What is "[Embedded - Microcontrollers](#)"?

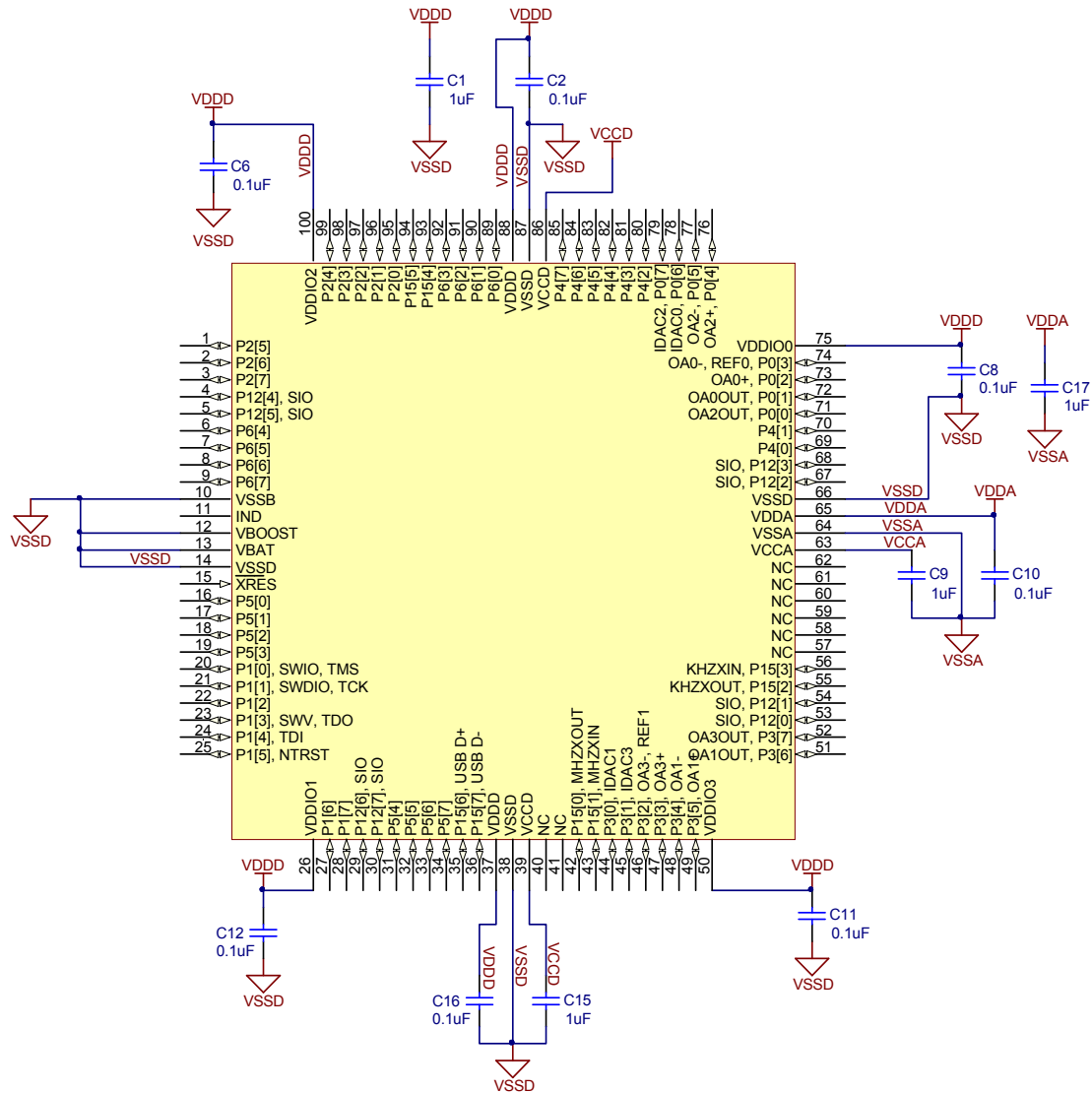
"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	67MHz
Connectivity	EBI/EMI, I ² C, LINbus, SPI, UART/USART, USB
Peripherals	CapSense, DMA, LCD, POR, PWM, WDT
Number of I/O	38
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 5.5V
Data Converters	A/D 16x20b; D/A 4x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	68-VFQFN Exposed Pad
Supplier Device Package	68-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c3865lti-014

Figure 2-7. Example Schematic for 100-pin TQFP Part with Power Connections



Note The two VCCD pins must be connected together with as short a trace as possible. A trace under the device is recommended, as shown in [Figure 2-8](#) on page 12.

For more information on pad layout, refer to <http://www.cypress.com/cad-resources/psoc-3-cad-libraries>.

4.3 Instruction Set

The 8051 instruction set is highly optimized for 8-bit handling and Boolean operations. The types of instructions supported include:

- Arithmetic instructions
- Logical instructions

- Data transfer instructions
- Boolean instructions
- Program branching instructions

4.3.1 Instruction Set Summary

4.3.1.1 Arithmetic Instructions

Arithmetic instructions support the direct, indirect, register, immediate constant, and register-specific instructions. Arithmetic modes are used for addition, subtraction, multiplication, division, increment, and decrement operations. [Table 4-1](#) lists the different arithmetic instructions.

Table 4-1. Arithmetic Instructions

Mnemonic	Description	Bytes	Cycles
ADD A,Rn	Add register to accumulator	1	1
ADD A,Direct	Add direct byte to accumulator	2	2
ADD A,@Ri	Add indirect RAM to accumulator	1	2
ADD A,#data	Add immediate data to accumulator	2	2
ADDC A,Rn	Add register to accumulator with carry	1	1
ADDC A,Direct	Add direct byte to accumulator with carry	2	2
ADDC A,@Ri	Add indirect RAM to accumulator with carry	1	2
ADDC A,#data	Add immediate data to accumulator with carry	2	2
SUBB A,Rn	Subtract register from accumulator with borrow	1	1
SUBB A,Direct	Subtract direct byte from accumulator with borrow	2	2
SUBB A,@Ri	Subtract indirect RAM from accumulator with borrow	1	2
SUBB A,#data	Subtract immediate data from accumulator with borrow	2	2
INC A	Increment accumulator	1	1
INC Rn	Increment register	1	2
INC Direct	Increment direct byte	2	3
INC @Ri	Increment indirect RAM	1	3
DEC A	Decrement accumulator	1	1
DEC Rn	Decrement register	1	2
DEC Direct	Decrement direct byte	2	3
DEC @Ri	Decrement indirect RAM	1	3
INC DPTR	Increment data pointer	1	1
MUL	Multiply accumulator and B	1	2
DIV	Divide accumulator by B	1	6
DAA	Decimal adjust accumulator	1	3

4.4 DMA and PHUB

The PHUB and the DMA controller are responsible for data transfer between the CPU and peripherals, and also data transfers between peripherals. The PHUB and DMA also control device configuration during boot. The PHUB consists of:

- A central hub that includes the DMA controller, arbiter, and router
- Multiple spokes that radiate outward from the hub to most peripherals

There are two PHUB masters: the CPU and the DMA controller. Both masters may initiate transactions on the bus. The DMA channels can handle peripheral communication without CPU intervention. The arbiter in the central hub determines which DMA channel is the highest priority if there are multiple requests.

4.4.1 PHUB Features

- CPU and DMA controller are both bus masters to the PHUB
- Eight multi-layer AHB bus parallel access paths (spokes) for peripheral access
- Simultaneous CPU and DMA access to peripherals located on different spokes
- Simultaneous DMA source and destination burst transactions on different spokes
- Supports 8-, 16-, 24-, and 32-bit addressing and data

Table 4-6. PHUB Spokes and Peripherals

PHUB Spokes	Peripherals
0	SRAM
1	IOs, PICU, EMIF
2	PHUB local configuration, Power manager, Clocks, IC, SWV, EEPROM, Flash programming interface
3	Analog interface and trim, Decimator
4	USB, CAN, I ² C, Timers, Counters, and PWMs
5	DFB
6	UDBs group 1
7	UDBs group 2

4.4.2 DMA Features

- 24 DMA channels
- Each channel has one or more transaction descriptors (TD) to configure channel behavior. Up to 128 total TDs can be defined
- TDs can be dynamically updated
- Eight levels of priority per channel
- Any digitally routable signal, the CPU, or another DMA channel, can trigger a transaction
- Each channel can generate up to two interrupts per transfer

- Transactions can be stalled or canceled
- Supports transaction size of infinite or 1 to 64 KB
- TDs may be nested and/or chained for complex transactions

4.4.3 Priority Levels

The CPU always has higher priority than the DMA controller when their accesses require the same bus resources. Due to the system architecture, the CPU can never starve the DMA. DMA channels of higher priority (lower priority number) may interrupt current DMA transfers. In the case of an interrupt, the current transfer is allowed to complete its current transaction. To ensure latency limits when multiple DMA accesses are requested simultaneously, a fairness algorithm guarantees an interleaved minimum percentage of bus bandwidth for priority levels 2 through 7. Priority levels 0 and 1 do not take part in the fairness algorithm and may use 100 percent of the bus bandwidth. If a tie occurs on two DMA requests of the same priority level, a simple round robin method is used to evenly share the allocated bandwidth. The round robin allocation can be disabled for each DMA channel, allowing it to always be at the head of the line. Priority levels 2 to 7 are guaranteed the minimum bus bandwidth shown in Table 4-7 after the CPU and DMA priority levels 0 and 1 have satisfied their requirements.

Table 4-7. Priority Levels

Priority Level	% Bus Bandwidth
0	100.0
1	100.0
2	50.0
3	25.0
4	12.5
5	6.2
6	3.1
7	1.5

When the fairness algorithm is disabled, DMA access is granted based solely on the priority level; no bus bandwidth guarantees are made.

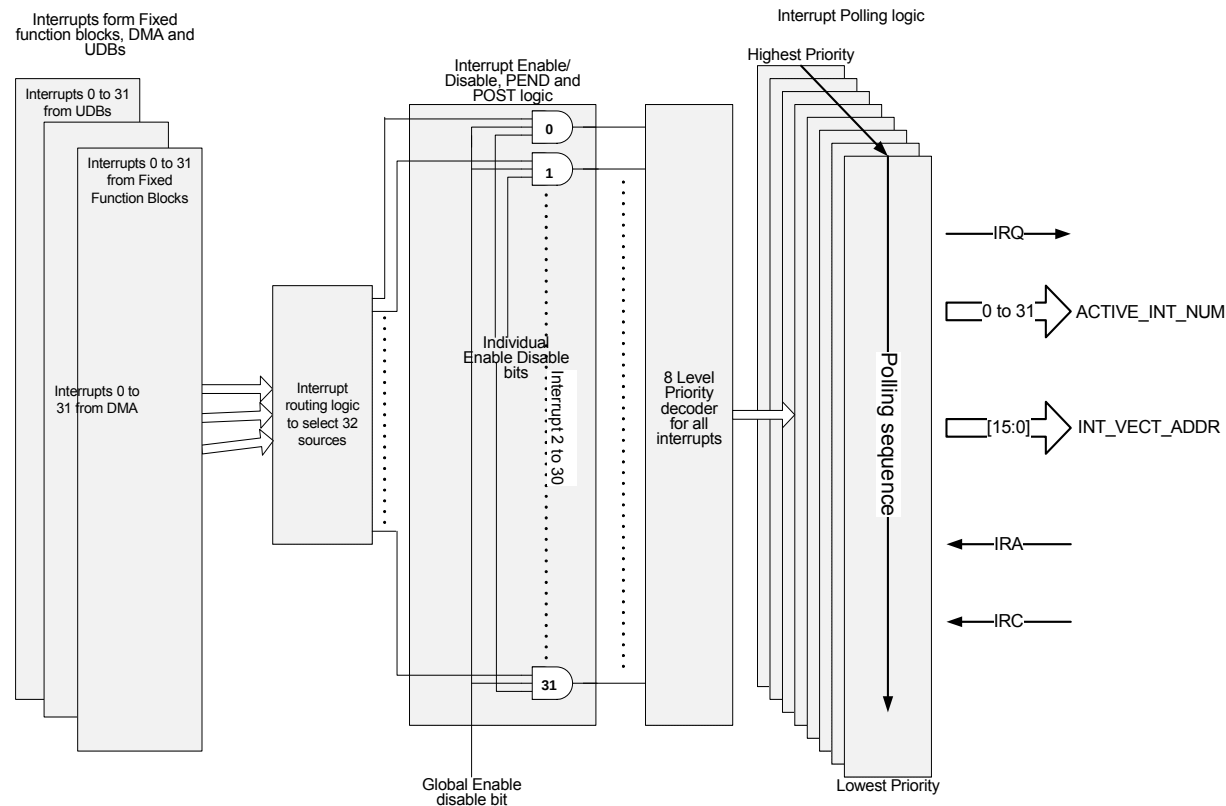
4.4.4 Transaction Modes Supported

The flexible configuration of each DMA channel and the ability to chain multiple channels allow the creation of both simple and complex use cases. General use cases include, but are not limited to:

4.4.4.1 Simple DMA

In a simple DMA case, a single TD transfers data between a source and sink (peripherals or memory location). The basic timing diagrams of DMA read and write cycles are shown in Figure 4-1. For more description on other transfer modes, refer to the Technical Reference Manual.

Figure 4-3. Interrupt Structure

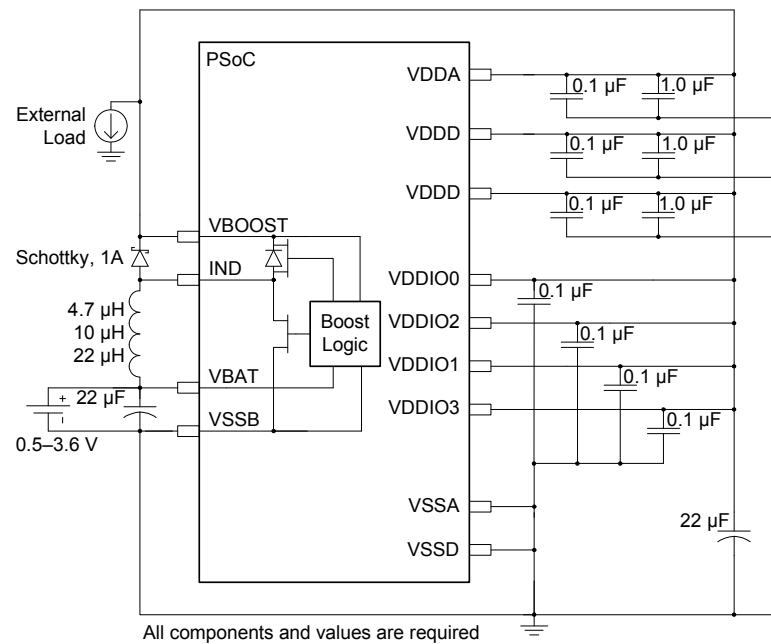


When an interrupt is pending, the current instruction is completed and the program counter is pushed onto the stack. Code execution then jumps to the program address provided by the vector. After the ISR is completed, a RETI instruction is executed and returns execution to the instruction following the previously interrupted instruction. To do this the RETI instruction pops the program counter from the stack.

If the same priority level is assigned to two or more interrupts, the interrupt with the lower vector number is executed first. Each interrupt vector may choose from three interrupt sources: Fixed Function, DMA, and UDB. The fixed function interrupts are

direct connections to the most common interrupt sources and provide the lowest resource cost connection. The DMA interrupt sources provide direct connections to the two DMA interrupt sources provided per DMA channel. The third interrupt source for vectors is from the UDB digital routing array. This allows any digital signal available to the UDB array to be used as an interrupt source. Fixed function interrupts and all interrupt sources may be routed to any interrupt vector using the UDB interrupt source connections.

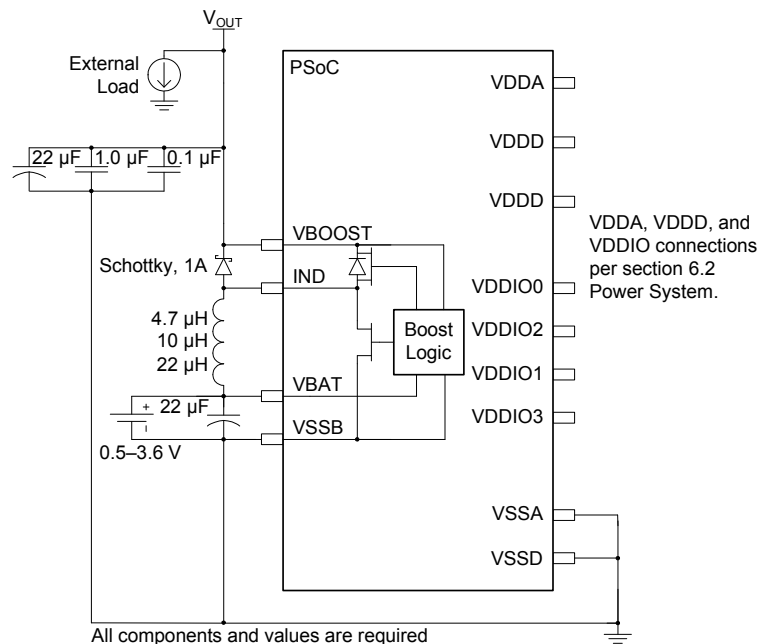
Figure 6-6. Application of Boost Converter powering PSoC device



The boost converter may also generate a supply that is not used directly by the PSoC device. An example of this use case is boosting a 1.8 V supply to 4.0 V to drive a white LED. If the boost converter is not supplying the PSoC devices V_{DDA} , V_{DDD} , and V_{DDIO} it must comply with the same design rules as supplying

the PSoC device, but with a change to the bulk capacitor requirements. A parallel arrangement 22 μF , 1.0 μF , and 0.1 μF capacitors are all required on the Vout supply and must be placed within 1 cm of the VBOOST pin to ensure regulator stability.

Figure 6-7. Application of Boost Converter not powering PSoC device



The switching frequency is set to 400 kHz using an oscillator integrated into the boost converter. The boost converter can be operated in two different modes: active and standby. Active mode is the normal mode of operation where the boost regulator

actively generates a regulated output voltage. In standby mode, most boost functions are disabled, thus reducing power consumption of the boost circuit. Only minimal power is provided, typically $< 5 \mu\text{A}$ to power the PSoC device in Sleep mode. The

The USBIO pins (P15[7] and P15[6]), when enabled for I/O mode, have limited drive mode control. The drive mode is set using the PRT15.DM0[7, 6] register. A resistive pull option is also available at the USBIO pins, which can be enabled using the PRT15.DM1[7, 6] register. When enabled for USB mode, the drive mode control has no impact on the configuration of the USB pins. Unlike the GPIO and SIO configurations, the port wide configuration registers do not configure the USB drive mode bits. Table 6-7 shows the drive mode configuration for the USBIO pins.

Table 6-7. USBIO Drive Modes (P15[7] and P15[6])

PRT15.DM1[7,6] Pull up enable	PRT15.DM0[7,6] Drive Mode enable	PRT15.DR[7,6] = 1	PRT15.DR[7,6] = 0	Description
0	0	High Z	Strong Low	Open Drain, Strong Low
0	1	Strong High	Strong Low	Strong Outputs
1	0	Res High (5k)	Strong Low	Resistive Pull Up, Strong Low
1	1	Strong High	Strong Low	Strong Outputs

■ High impedance analog

The default reset state with both the output driver and digital input buffer turned off. This prevents any current from flowing in the I/O's digital input buffer due to a floating voltage. This state is recommended for pins that are floating or that support an analog voltage. High impedance analog pins do not provide digital input functionality.

To achieve the lowest chip current in sleep modes, all I/Os must either be configured to the high impedance analog mode, or have their pins driven to a power supply rail by the PSoC device or by external circuitry.

■ High impedance digital

The input buffer is enabled for digital signal input. This is the standard high impedance (High Z) state recommended for digital inputs.

■ Resistive pull-up or resistive pull-down

Resistive pull-up or pull-down, respectively, provides a series resistance in one of the data states and strong drive in the other. Pins can be used for digital input and output in these modes. Interfacing to mechanical switches is a common application for these modes. Resistive pullup and pull-down are not available with SIO in regulated output mode.

■ Open drain, drives high and open drain, drives low

Open drain modes provide high impedance in one of the data states and strong drive in the other. Pins can be used for digital input and output in these modes. A common application for these modes is driving the I²C bus signal lines.

■ Strong drive

Provides a strong CMOS output drive in either high or low state. This is the standard output mode for pins. Strong Drive mode pins must not be used as inputs under normal circumstances. This mode is often used to drive digital output signals or external FETs.

■ Resistive pull-up and pull-down

Similar to the resistive pull-up and resistive pull-down modes except the pin is always in series with a resistor. The high data state is pull-up while the low data state is pull-down. This mode is most often used when other signals that may cause shorts can drive the bus. Resistive pullup and pull-down are not available with SIO in regulated output mode.

6.4.2 Pin Registers

Registers to configure and interact with pins come in two forms that may be used interchangeably.

All I/O registers are available in the standard port form, where each bit of the register corresponds to one of the port pins. This register form is efficient for quickly reconfiguring multiple port pins at the same time.

I/O registers are also available in pin form, which combines the eight most commonly used port register bits into a single register for each pin. This enables very fast configuration changes to individual pins with a single register write.

6.4.3 Bidirectional Mode

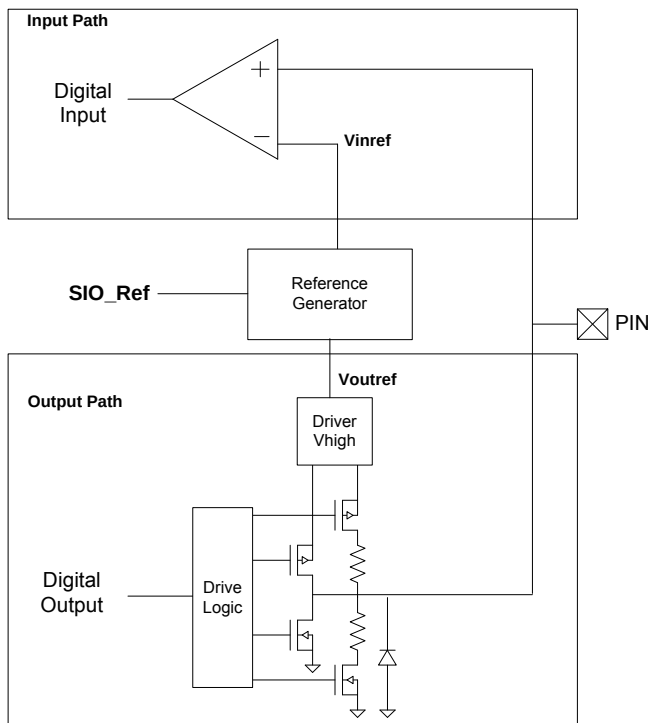
High speed bidirectional capability allows pins to provide both the high impedance digital drive mode for input signals and a second user selected drive mode such as strong drive (set using PRT×DM[2:0] registers) for output signals on the same pin, based on the state of an auxiliary control bus signal. The bidirectional capability is useful for processor busses and communications interfaces such as the SPI Slave MISO pin that requires dynamic hardware control of the output buffer.

The auxiliary control bus routes up to 16 UDB or digital peripheral generated output enable signals to one or more pins.

6.4.4 Slew Rate Limited Mode

GPIO and SIO pins have fast and slow output slew rate options for strong and open drain drive modes, not resistive drive modes. Because it results in reduced EMI, the slow edge rate option is recommended for signals that are not speed critical, generally less than 1 MHz. The fast slew rate is for signals between 1 MHz and 33 MHz. The slew rate is individually configurable for each pin, and is set by the PRT×SLW registers.

Figure 6-13. SIO Reference for Input and Output



6.4.13 SIO as Comparator

This section applies only to SIO pins. The adjustable input level feature of the SIOs as explained in the [Adjustable Input Level](#) section can be used to construct a comparator. The threshold for the comparator is provided by the SIO's reference generator. The reference generator has the option to set the analog signal routed through the analog global line as threshold for the comparator. Note that a pair of SIO pins share the same threshold. The digital input path in [Figure 6-10](#) on page 39 illustrates this functionality. In the figure, 'Reference level' is the analog signal routed through the analog global. The hysteresis feature can also be enabled for the input buffer of the SIO, which increases noise immunity for the comparator.

6.4.14 Hot Swap

This section applies only to SIO pins. SIO pins support 'hot swap' capability to plug into an application without loading the signals that are connected to the SIO pins even when no power is applied to the PSoC device. This allows the unpowered PSoC to maintain a high impedance load to the external device while also preventing the PSoC from being powered through a SIO pin's protection diode.

Powering the device up or down while connected to an operational I²C bus may cause transient states on the SIO pins. The overall I²C bus design should take this into account.

6.4.15 Over Voltage Tolerance

All I/O pins provide an over voltage tolerance feature at any operating V_{DD}.

- There are no current limitations for the SIO pins as they present a high impedance load to the external circuit where $V_{DDIO} \leq V_{IN} \leq 5.5\text{ V}$.
- The GPIO pins must be limited to 100 μA using a current limiting resistor. GPIO pins clamp the pin voltage to approximately one diode above the VDDIO supply where $V_{DDIO} \leq V_{IN} \leq V_{DDA}$.
- In case of a GPIO pin configured for analog input/output, the analog voltage on the pin must not exceed the VDDIO supply voltage to which the GPIO belongs.

A common application for this feature is connection to a bus such as I²C where different devices are running from different supply voltages. In the I²C case, the PSoC chip is configured into the Open Drain, Drives Low mode for the SIO pin. This allows an external pull-up to pull the I²C bus voltage above the PSoC pin supply. For example, the PSoC chip could operate at 1.8 V, and an external device could run from 5 V. Note that the SIO pin's V_{IH} and V_{IL} levels are determined by the associated VDDIO supply pin. The SIO pin must be in one of the following modes: 0 (high impedance analog), 1 (high impedance digital), or 4 (open drain drives low). See [Figure 6-12](#) for details. Absolute maximum ratings for the device must be observed for all I/O pins.

6.4.16 Reset Configuration

While reset is active all I/Os are reset to and held in the High Impedance Analog state. After reset is released, the state can be reprogrammed on a port-by-port basis to pull-down or pull-up. To ensure correct reset operation, the port reset configuration data is stored in special nonvolatile registers. The stored reset data is automatically transferred to the port reset configuration registers at reset release.

6.4.17 Low-Power Functionality

In all low-power modes the I/O pins retain their state until the part is awakened and changed or reset. To awaken the part, use a pin interrupt, because the port interrupt logic continues to function in all low-power modes.

6.4.18 Special Pin Functionality

Some pins on the device include additional special functionality in addition to their GPIO or SIO functionality. The specific special function pins are listed in [Pinouts](#) on page 6. The special features are:

- Digital
 - 4- to 25-MHz crystal oscillator
 - 32.768-kHz crystal oscillator
 - Wake from sleep on I²C address match. Any pin can be used for I²C if wake from sleep is not required.
 - JTAG interface pins
 - SWD interface pins
 - SWV interface pins
 - External reset
- Analog
 - Opamp inputs and outputs
 - High current IDAC outputs
 - External reference inputs

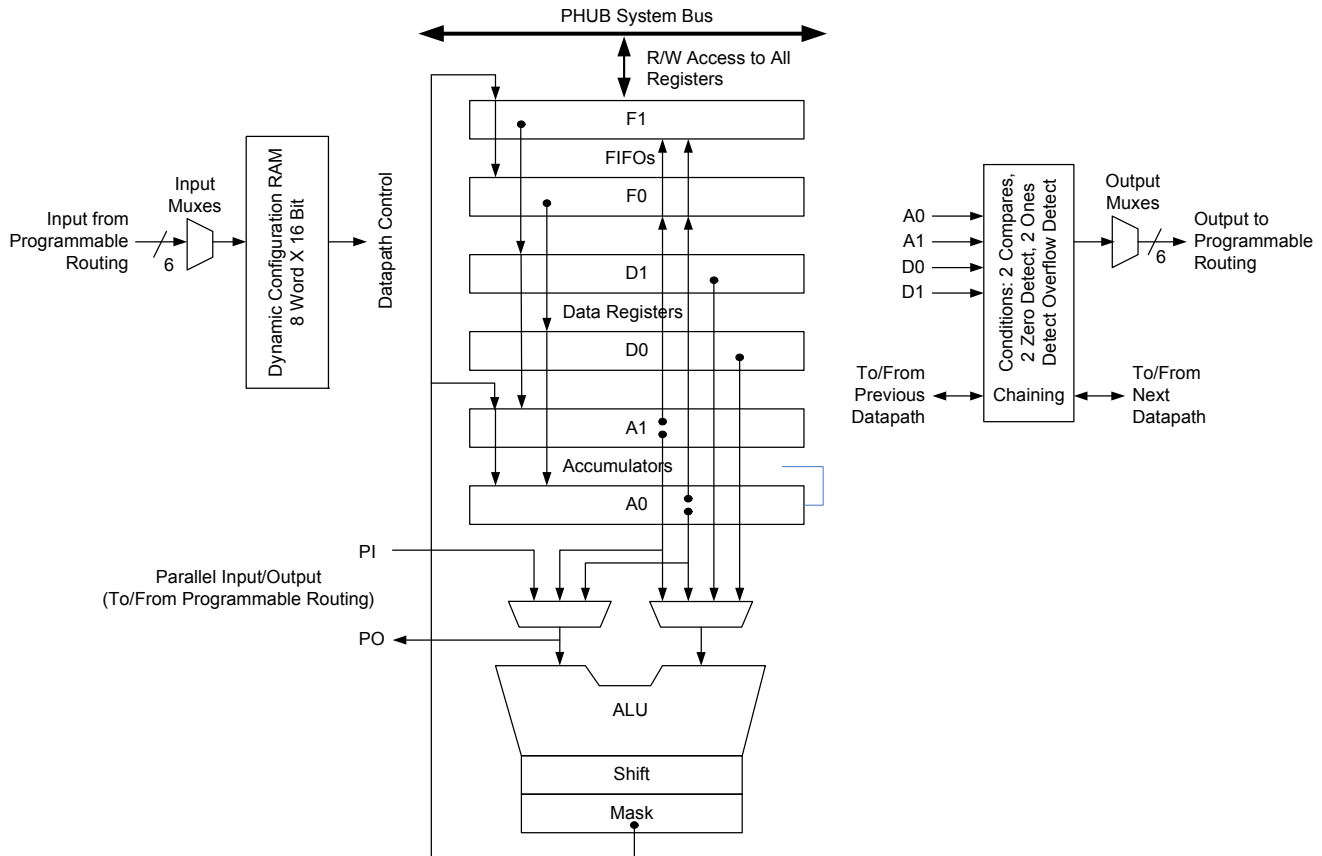
6.4.19 JTAG Boundary Scan

The device supports standard JTAG boundary scan chains on all I/O pins for board level test.

7.2.2 Datapath Module

The datapath contains an 8-bit single cycle ALU, with associated compare and condition generation logic. This datapath block is optimized to implement embedded functions, such as timers, counters, integrators, PWMs, PRS, CRC, shifters and dead band generators and many others.

Figure 7-4. Datapath Top Level



7.2.2.1 Working Registers

The datapath contains six primary working registers, which are accessed by CPU firmware or DMA during normal operation.

Table 7-1. Working Datapath Registers

Name	Function	Description
A0 and A1	Accumulators	These are sources and sinks for the ALU and also sources for the compares.
D0 and D1	Data Registers	These are sources for the ALU and sources for the compares.
F0 and F1	FIFOs	These are the primary interface to the system bus. They can be a data source for the data registers and accumulators or they can capture data from the accumulators or ALU. Each FIFO is four bytes deep.

7.2.2.2 Dynamic Configuration RAM

Dynamic configuration is the ability to change the datapath function and internal configuration on a cycle-by-cycle basis, under sequencer control. This is implemented using the 8-word $\times$ 16-bit configuration RAM, which stores eight unique 16-bit wide configurations. The address input to this RAM controls the sequence, and can be routed from any block connected to the UDB routing matrix, most typically PLD logic, I/O pins, or from the outputs of this or other datapath blocks.

ALU

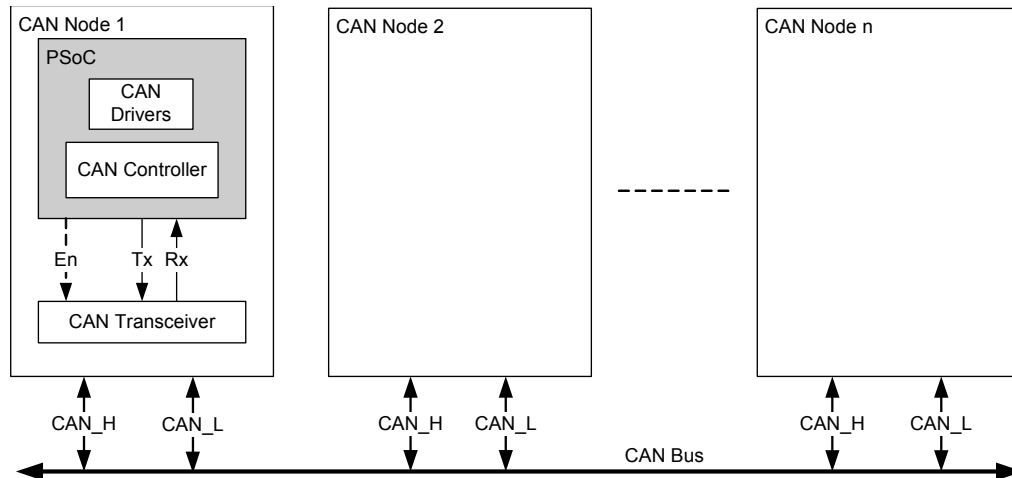
The ALU performs eight general purpose functions. They are:

- Increment
- Decrement
- Add
- Subtract
- Logical AND
- Logical OR
- Logical XOR
- Pass, used to pass a value through the ALU to the shift register, mask, or another UDB register.

7.5 CAN

The CAN peripheral is a fully functional controller area network (CAN) supporting communication baud rates up to 1 Mbps. The CAN controller implements the CAN2.0A and CAN2.0B specifications as defined in the Bosch specification and conforms to the ISO-11898-1 standard. The CAN protocol was originally designed for automotive applications with a focus on a high level of fault detection. This ensures high communication reliability at a low cost. Because of its success in automotive applications, CAN is used as a standard communication protocol for motion oriented machine control networks (CANOpen) and factory automation applications (DeviceNet). The CAN controller features allow the efficient implementation of higher level protocols without affecting the performance of the microcontroller CPU. Full configuration support is provided in PSoC Creator.

Figure 7-14. CAN Bus System Implementation



7.5.1 CAN Features

- CAN2.0A/B protocol implementation – ISO 11898 compliant
 - Standard and extended frames with up to 8 bytes of data per frame
 - Message filter capabilities
 - Remote Transmission Request (RTR) support
 - Programmable bit rate up to 1 Mbps
- Listen Only mode
- SW readable error counter and indicator
- Sleep mode: Wake the device from sleep with activity on the Rx pin
- Supports two or three wire interface to external transceiver (Tx, Rx, and Enable). The three-wire interface is compatible with the Philips PHY; the PHY is not included on-chip. The three wires can be routed to any I/O
- Enhanced interrupt controller
 - CAN receive and transmit buffers status
 - CAN controller error status including BusOff

■ Receive path

- 16 receive buffers each with its own message filter
- Enhanced hardware message filter implementation that covers the ID, IDE, and RTR
- DeviceNet addressing support
- Multiple receive buffers linkable to build a larger receive message array
- Automatic transmission request (RTR) response handler
- Lost received message notification

■ Transmit path

- Eight transmit buffers
- Programmable transmit priority
- Round robin
- Fixed priority
- Message transmissions abort capability

7.5.2 Software Tools Support

CAN Controller configuration integrated into PSoC Creator:

- CAN Configuration walkthrough with bit timing analyzer
- Receive filter setup

7.9 Digital Filter Block

Some devices in the CY8C38 family of devices have a dedicated HW accelerator block used for digital filtering. The DFB has a dedicated multiplier and accumulator that calculates a 24-bit by 24-bit multiply accumulate in one bus clock cycle. This enables the mapping of a direct form FIR filter that approaches a computation rate of one FIR tap for each clock cycle. The MCU can implement any of the functions performed by this block, but at a slower rate that consumes MCU bandwidth.

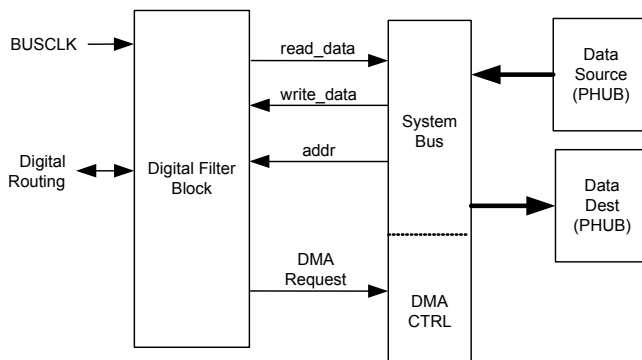
The heart of the DFB is a datapath (DP), which is the numerical calculation unit of the DFB. The DP is a 24-bit fixed-point numerical processor containing a 48-bit multiply and accumulate function (MAC), a multi-function ALU, sample and coefficient data RAMs as well as data routing, shifting, holding and rounding functions.

In the MAC, two 24-bit values can be multiplied and the result added to the 48-bit accumulator in each bus clock cycle. The MAC is the only portion of the DP that is wider than 24 bits. All results from the MAC are passed on to the ALU as 24-bit values representing the high-order 24 bits in the accumulator shifted by one (bits 46:23). The MAC assumes an implied binary point after the most significant bit.

The DP also contains an optimized ALU that supports add, subtract, comparison, threshold, absolute value, squelch, saturation, and other functions. The DP unit is controlled by seven control fields totaling 18 bits coming from the DFB Controller. For more information see the TRM.

The PSoC Creator interface provides a wizard to implement FIR and IIR digital filters with coefficients for LPF, BPF, HPF, Notch and arbitrary shape filters. 64 pairs of data and coefficients are stored. This enables a 64 tap FIR filter or up to 4 16 tap filters of either FIR or IIR formulation.

Figure 7-20. DFB Application Diagram (pwr/gnd not shown)



The typical use model is for data to be supplied to the DFB over the system bus from another on-chip system data source such as an ADC. The data typically passes through main memory or is directly transferred from another chip resource through DMA. The DFB processes this data and passes the result to another on chip resource such as a DAC or main memory through DMA on the system bus.

Data movement in or out of the DFB is typically controlled by the system DMA controller but can be moved directly by the MCU.

8. Analog Subsystem

The analog programmable system creates application specific combinations of both standard and advanced analog signal processing blocks. These blocks are then interconnected to each other and also to any pin on the device, providing a high level of design flexibility and IP security. The features of the analog subsystem are outlined here to provide an overview of capabilities and architecture.

- Flexible, configurable analog routing architecture provided by analog globals, analog mux bus, and analog local buses.
- High resolution delta-sigma ADC.
- Up to four 8-bit DACs that provide either voltage or current output.
- Four comparators with optional connection to configurable LUT outputs.
- Up to four configurable switched capacitor/continuous time (SC/CT) blocks for functions that include opamp, unity gain buffer, programmable gain amplifier, transimpedance amplifier, and mixer.
- Up to four opamps for internal use and connection to GPIO that can be used as high current output buffers.
- CapSense subsystem to enable capacitive touch sensing.
- Precision reference for generating an accurate analog voltage for internal analog blocks.

Analog local buses (abus) are routing resources located within the analog subsystem and are used to route signals between different analog blocks. There are eight abus routes in CY8C38, four in the left half (abusl [0:3]) and four in the right half (abusr [0:3]) as shown in Figure 8-2. Using the abus saves the analog globals and analog mux buses from being used for interconnecting the analog blocks.

Multiplexers and switches exist on the various buses to direct signals into and out of the analog blocks. A multiplexer can have only one connection on at a time, whereas a switch can have multiple connections on simultaneously. In Figure 8-2, multiplexers are indicated by grayed ovals and switches are indicated by transparent ovals.

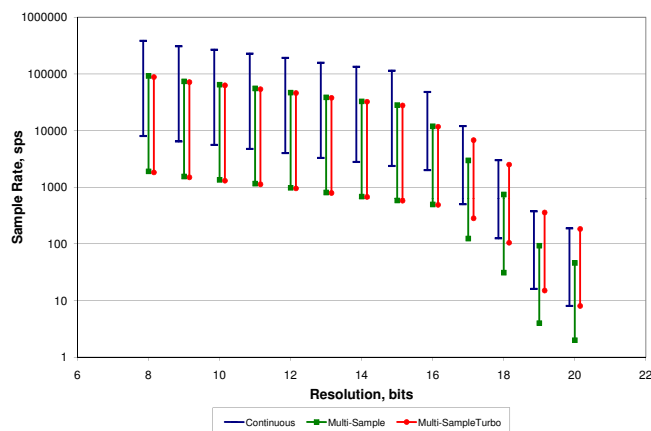
8.2 Delta-sigma ADC

The CY8C38 device contains one delta-sigma ADC. This ADC offers differential input, high resolution and excellent linearity, making it a good ADC choice for both audio signal processing and measurement applications. The converter's nominal operation is 16 bits at 48 ksp. The ADC can be configured to output 20-bit resolution at data rates of up to 187 sps. At a fixed clock rate, resolution can be traded for faster data rates as shown in Table 8-1 and Figure 8-3.

Table 8-1. Delta-sigma ADC Performance

Bits	Maximum Sample Rate (sps)	SINAD (dB)
20	187	—
16	48 k	84
12	192 k	66
8	384 k	43

Figure 8-3. Delta-sigma ADC Sample Rates, Range = ±1.024 V

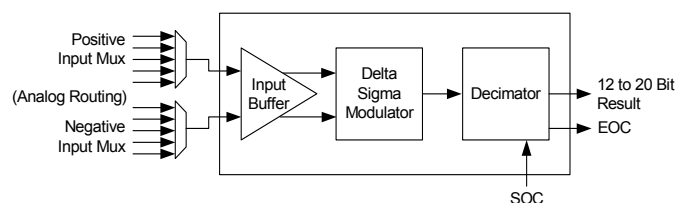


8.2.1 Functional Description

The ADC connects and configures three basic components, input buffer, delta-sigma modulator, and decimator. The basic

block diagram is shown in Figure 8-4. The signal from the input muxes is delivered to the delta-sigma modulator either directly or through the input buffer. The delta-sigma modulator performs the actual analog to digital conversion. The modulator over-samples the input and generates a serial data stream output. This high speed data stream is not useful for most applications without some type of post processing, and so is passed to the decimator through the Analog Interface block. The decimator converts the high speed serial data stream into parallel ADC results. The modulator/decimator frequency response is $[(\sin x)/x]^4$.

Figure 8-4. Delta-sigma ADC Block Diagram



Resolution and sample rate are controlled by the Decimator. Data is pipelined in the decimator; the output is a function of the last four samples. When the input multiplexer is switched, the output data is not valid until after the fourth sample after the switch.

8.2.2 Operational Modes

The ADC can be configured by the user to operate in one of four modes: Single Sample, Multi Sample, Continuous, or Multi Sample (Turbo). All four modes are started by either a write to the start bit in a control register or an assertion of the Start of Conversion (SoC) signal. When the conversion is complete, a status bit is set and the output signal End of Conversion (EoC) asserts high and remains high until the value is read by either the DMA controller or the CPU.

8.2.2.1 Single Sample

In Single Sample mode, the ADC performs one sample conversion on a trigger. In this mode, the ADC stays in standby state waiting for the SoC signal to be asserted. When SoC is signaled the ADC performs four successive conversions. The first three conversions prime the decimator. The ADC result is valid and available after the fourth conversion, at which time the EoC signal is generated. To detect the end of conversion, the system may poll a control register for status or configure the external EoC signal to generate an interrupt or invoke a DMA request. When the transfer is done the ADC reenters the standby state where it stays until another SoC event.

8.2.2.2 Continuous

Continuous sample mode is used to take multiple successive samples of a single input signal. Multiplexing multiple inputs should not be done with this mode. There is a latency of three conversion times before the first conversion result is available. This is the time required to prime the decimator. After the first result, successive conversions are available at the selected sample rate.

9.8 CSP Package Bootloader

A factory-installed bootloader program is included in all devices with CSP packages. The bootloader is compatible with PSoC Creator 3.0 bootloadable project files and has the following features:

- I²C-based
- SCLK and SDAT available at P1[6] and P1[7], respectively
- External pull-up resistors required
- I²C slave, address 4, data rate = 100 kbps
- Single application
- Wait two seconds for bootload command
- Other bootloader options are as set by the PSoC Creator 3.0 Bootloader Component default
- Occupies the bottom 9K of flash

For more information on this bootloader, see the following Cypress application notes:

- [AN89611](#) – PSoC® 3 AND PSoC 5LP - Getting Started With Chip Scale Packages (CSP)
- [AN73854](#) – PSoC 3 and PSoC 5 LP Introduction to Bootloaders
- [AN60317](#) – PSoC 3 and PSoC 5 LP I²C Bootloader

Note that a PSoC Creator bootloadable project must be associated with .hex and .elf files for a bootloader project that is configured for the target device. Bootloader .hex and .elf files can be found at www.cypress.com/go/PSoC3datasheet.

The factory-installed bootloader can be overwritten using JTAG or SWD programming.

Table 11-2. DC Specifications (continued)

Parameter	Description	Conditions	Min	Typ ^[25]	Max	Units	
	Sleep Mode^[28]						
	CPU = OFF RTC = ON (= ECO32K ON, in low-power mode) Sleep timer = ON (= ILO ON at 1 kHz) ^[29] WDT = OFF I ² C Wake = OFF Comparator = OFF POR = ON Boost = OFF SIO pins in single ended input, unregulated output mode	V _{DD} = V _{DDIO} = 4.5 V - 5.5 V	T = −40 °C	–	1.1	2.3	μA
			T = 25 °C	–	1.1	2.2	
			T = 85 °C	–	15	30	
		V _{DD} = V _{DDIO} = 2.7 V – 3.6 V	T = −40 °C	–	1	2.2	
			T = 25 °C	–	1	2.1	
			T = 85 °C	–	12	28	
	V _{DD} = V _{DDIO} = 1.71 V – 1.95 V ^[30]	T = 25 °C	–	2.2	4.2		
	Comparator = ON CPU = OFF RTC = OFF Sleep timer = OFF WDT = OFF I ² C Wake = OFF POR = ON Boost = OFF SIO pins in single ended input, unregulated output mode	V _{DD} = V _{DDIO} = 2.7 V – 3.6 V ^[31]	T = 25 °C	–	2.2	2.7	
I ² C Wake = ON CPU = OFF RTC = OFF Sleep timer = OFF WDT = OFF Comparator = OFF POR = ON Boost = OFF SIO pins in single ended input, unregulated output mode	V _{DD} = V _{DDIO} = 2.7 V – 3.6 V ^[31]	T = 25 °C	–	2.2	2.8		
Hibernate Mode^[28]							
Hibernate mode current All regulators and oscillators off SRAM retention GPIO interrupts are active Boost = OFF SIO pins in single ended input, unregulated output mode	V _{DD} = V _{DDIO} = 4.5 V - 5.5 V	T = −40 °C	–	0.2	1.5	μA	
		T = 25 °C	–	0.5	1.5		
		T = 85 °C	–	4.1	5.3		
	V _{DD} = V _{DDIO} = 2.7 V – 3.6 V	T = −40 °C	–	0.2	1.5		
		T = 25 °C	–	0.2	1.5		
		T = 85 °C	–	3.2	4.2		
	V _{DD} = V _{DDIO} = 1.71 V – 1.95 V ^[30]	T = −40 °C	–	0.2	1.5		
		T = 25 °C	–	0.3	1.5		
		T = 85 °C	–	3.3	4.3		
I _{DDAR}	Analog current consumption while device is reset ^[32]	V _{DDA} ≤ 3.6 V		–	0.3	0.6	mA
		V _{DDA} > 3.6 V		–	1.4	3.3	mA
I _{DDDR}	Digital current consumption while device is reset ^[32]	V _{DDD} ≤ 3.6 V		–	1.1	3.1	mA
		V _{DDD} > 3.6 V		–	0.7	3.1	mA

Notes

28. If V_{CCD} and V_{CCA} are externally regulated, the voltage difference between V_{CCD} and V_{CCA} must be less than 50 mV.
 29. Sleep timer generates periodic interrupts to wake up the CPU. This specification applies only to those times that the CPU is off.
 30. Externally regulated mode.
 31. Based on device characterization (not production tested).
 32. Based on device characterization (not production tested). USBIO pins tied to ground (VSSD).

11.4.4 XRES

Table 11-17. XRES DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
V _{IH}	Input voltage high threshold		$0.7 \times V_{DDIO}$	–	–	V
V _{IL}	Input voltage low threshold		–	–	$0.3 \times V_{DDIO}$	V
R _{pullup}	Pull-up resistor		3.5	5.6	8.5	kΩ
C _{IN}	Input capacitance ^[46]		–	3	–	pF
V _H	Input voltage hysteresis (Schmitt-Trigger) ^[46]		–	100	–	mV
I _{diode}	Current through protection diode to V _{DDIO} and V _{SSIO}		–	–	100	μA

Table 11-18. XRES AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
T _{RESET}	Reset pulse width		1	–	–	μs

11.5 Analog Peripherals

Specifications are valid for $-40\text{ °C} \leq T_A \leq 85\text{ °C}$ and $T_J \leq 100\text{ °C}$, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

11.5.1 Opamp

Table 11-19. Opamp DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
V _I	Input voltage range		V _{SSA}	–	V _{DDA}	V
V _{OS}	Input offset voltage		–	–	2.5	mV
		Operating temperature -40 °C to 70 °C	–	–	2	mV
TCV _{OS}	Input offset voltage drift with temperature	Power mode = high	–	–	±30	μV/°C
Ge1	Gain error, unity gain buffer mode	Rload = 1 kΩ	–	–	±0.1	%
C _{IN}	Input capacitance	Routing from pin	–	–	18	pF
V _O	Output voltage range	1 mA, source or sink, power mode = high	V _{SSA} + 0.05	–	V _{DDA} – 0.05	V
I _{OUT}	Output current capability, source or sink	V _{SSA} + 500 mV ≤ V _{out} ≤ V _{DDA} –500 mV, V _{DDA} > 2.7 V	25	–	–	mA
		V _{SSA} + 500 mV ≤ V _{out} ≤ V _{DDA} –500 mV, 1.7 V = V _{DDA} ≤ 2.7 V	16	–	–	mA
I _{DD}	Quiescent current	Power mode = min	–	250	400	uA
		Power mode = low	–	250	400	uA
		Power mode = med	–	330	950	uA
		Power mode = high	–	1000	2500	uA
CMRR	Common mode rejection ratio		80	–	–	dB
PSRR	Power supply rejection ratio	V _{DDA} ≥ 2.7 V	85	–	–	dB
		V _{DDA} < 2.7 V	70	–	–	dB
I _{IB}	Input bias current ^[46]	25 °C	–	10	–	pA

Note

46. Based on device characterization (Not production tested).

Figure 11-25. Opamp Voffset Histogram, 3388 samples/847 parts, 25 °C, $V_{DDA} = 5\text{ V}$

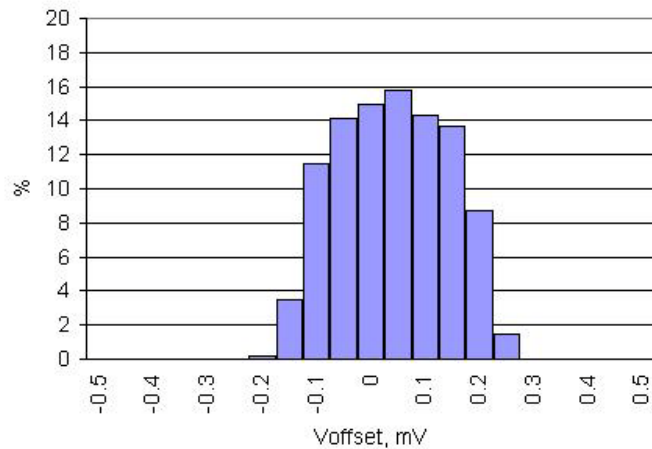


Figure 11-26. Opamp Voffset vs Temperature, $V_{DDA} = 5\text{ V}$

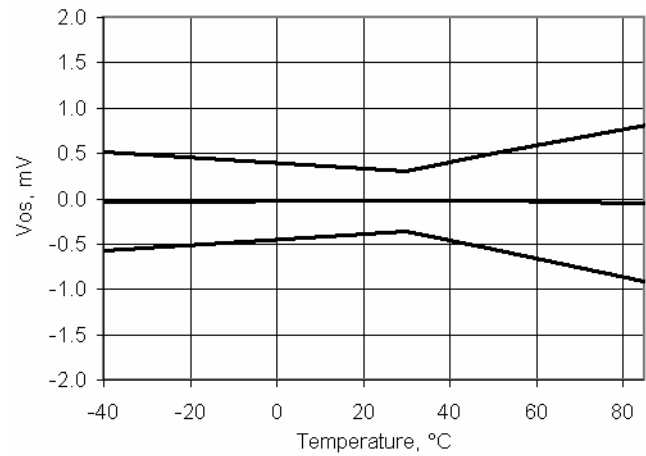


Figure 11-27. Opamp Voffset vs Vcommon and V_{DDA} , 25 °C

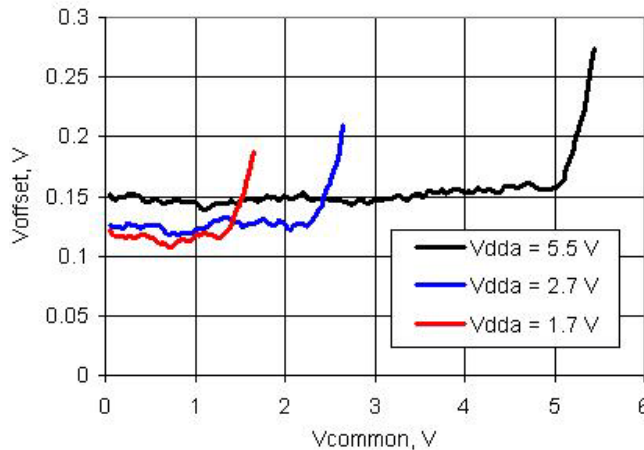


Figure 11-28. Opamp Output Voltage vs Load Current and Temperature, High Power Mode, 25 °C, $V_{DDA} = 2.7\text{ V}$

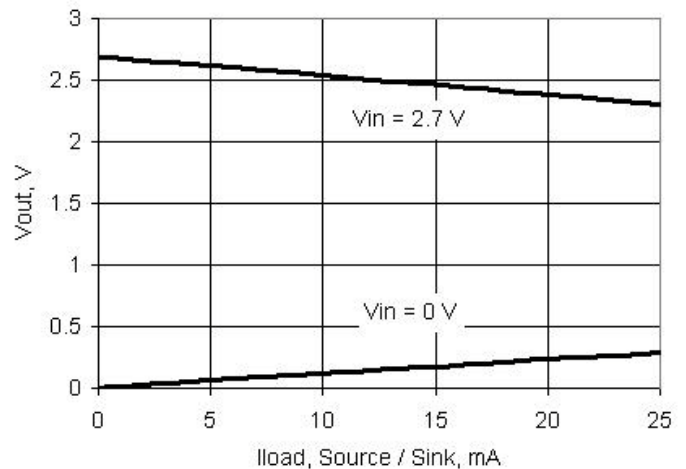


Figure 11-29. Opamp Operating Current vs V_{DDA} and Power Mode

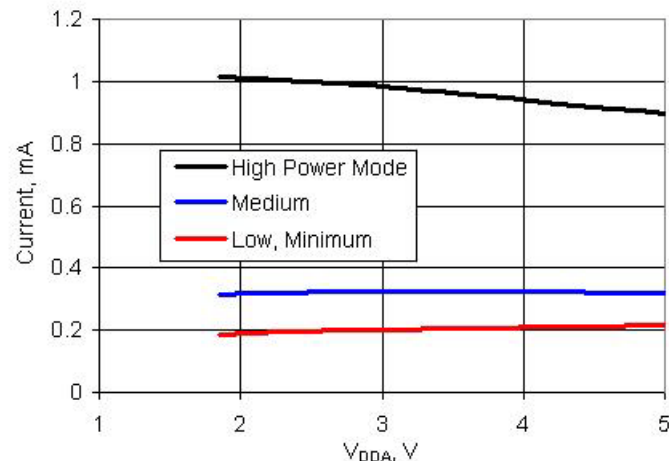


Figure 11-43. IDAC DNL vs Input Code, Range = 255 μ A, Source Mode

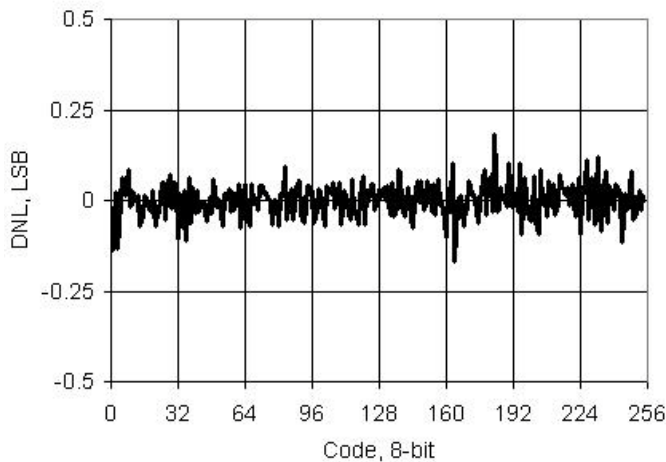


Figure 11-44. IDAC DNL vs Input Code, Range = 255 μ A, Sink Mode

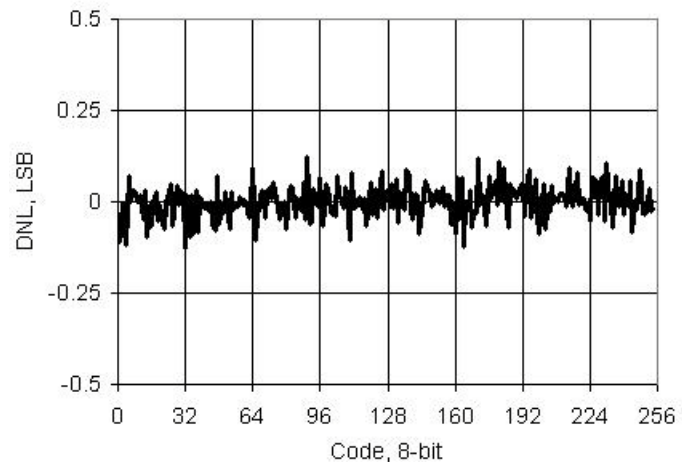


Figure 11-45. IDAC INL vs Temperature, Range = 255 μ A, High speed mode

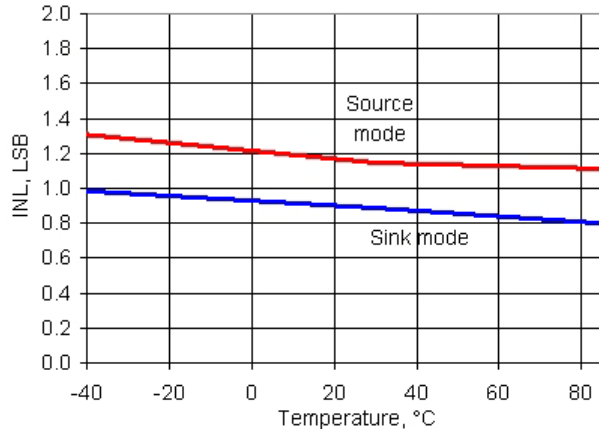


Figure 11-46. IDAC DNL vs Temperature, Range = 255 μ A, High speed mode

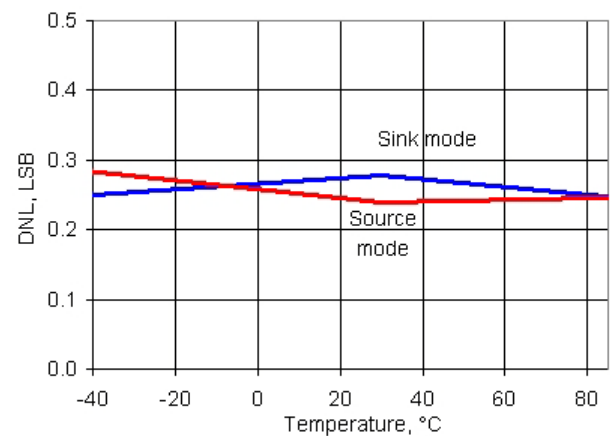


Figure 11-47. IDAC Full Scale Error vs Temperature, Range = 255 μ A, Source Mode

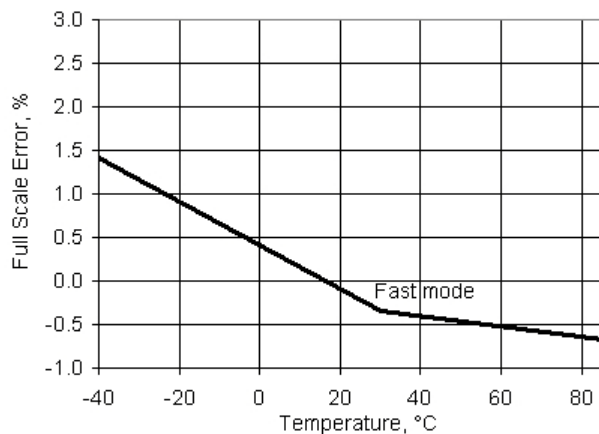


Figure 11-48. IDAC Full Scale Error vs Temperature, Range = 255 μ A, Sink Mode

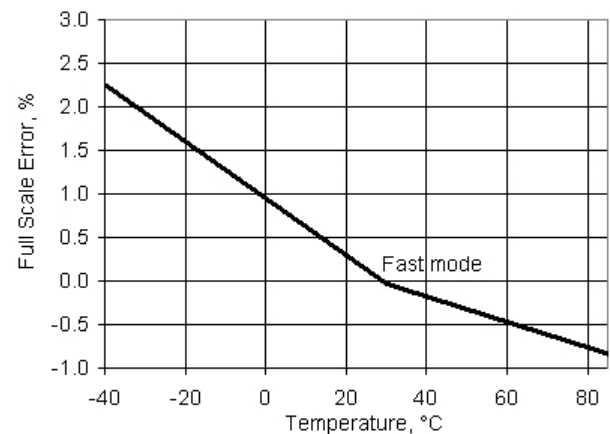


Table 11-41. PGA AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
BW1	–3 dB bandwidth	Power mode = high, gain = 1, input = 100 mV peak-to-peak	6.7	8	–	MHz
SR1	Slew rate	Power mode = high, gain = 1, 20% to 80%	3	–	–	V/μs
e _n	Input noise density	Power mode = high, V _{DDA} = 5 V, at 100 kHz	–	43	–	nV/sqrtHz

Figure 11-68. Bandwidth vs. Temperature, at Different Gain Settings, Power Mode = High

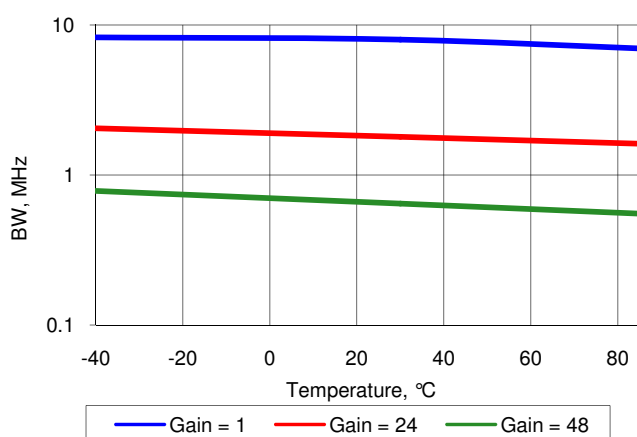
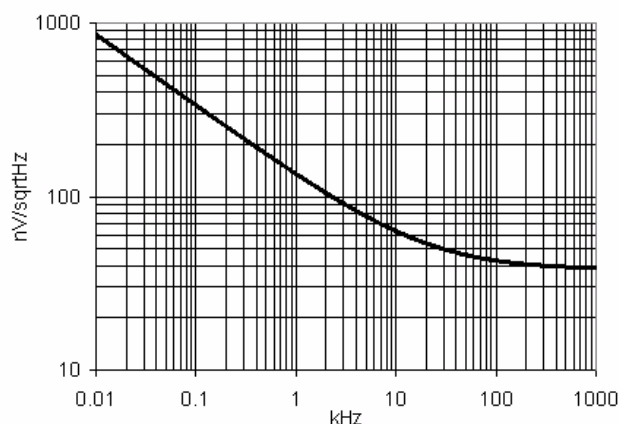


Figure 11-69. Noise vs. Frequency, V_{DDA} = 5 V, Power Mode = High



11.5.11 Temperature Sensor

Table 11-42. Temperature Sensor Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Temp sensor accuracy	Range: –40 °C to +85 °C	–	±5	–	°C

11.5.12 LCD Direct Drive

Table 11-43. LCD Direct Drive DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
I _{CC}	LCD system operating current	Device sleep mode with wakeup at 400-Hz rate to refresh LCDs, bus clock = 3 MHz, V _{DDIO} = V _{DDA} = 3 V, 4 commons, 16 segments, 1/4 duty cycle, 50 Hz frame rate, no glass connected	–	38	–	μA
I _{CC_SEG}	Current per segment driver	Strong drive mode	–	260	–	μA
V _{BIAS}	LCD bias range (V _{BIAS} refers to the main output voltage(V0) of LCD DAC)	V _{DDA} ≥ 3 V and V _{DDA} ≥ V _{BIAS}	2	–	5	V
	LCD bias step size	V _{DDA} ≥ 3 V and V _{DDA} ≥ V _{BIAS}	–	9.1 × V _{DDA}	–	mV
	LCD capacitance per segment/common driver	Drivers may be combined	–	500	5000	pF
	Long term segment offset		–	–	20	mV
I _{OUT}	Output drive current per segment driver)	V _{DDIO} = 5.5V, strong drive mode	355	–	710	μA

11.6.2 Counter

The following specifications apply to the Timer/Counter/PWM peripheral, in counter mode. Counters can also be implemented in UDBs; for more information, see the Counter component data sheet in PSoC Creator.

Table 11-47. Counter DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Block current consumption	16-bit counter, at listed input clock frequency	–	–	–	μA
	3 MHz		–	15	–	μA
	12 MHz		–	60	–	μA
	48 MHz		–	260	–	μA
	67 MHz		–	350	–	μA

Table 11-48. Counter AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Operating frequency		DC	–	67.01	MHz
	Capture pulse		15	–	–	ns
	Resolution		15	–	–	ns
	Pulse width		15	–	–	ns
	Pulse width (external)		30	–	–	ns
	Enable pulse width		15	–	–	ns
	Enable pulse width (external)		30	–	–	ns
	Reset pulse width		15	–	–	ns
	Reset pulse width (external)		30	–	–	ns

11.6.3 Pulse Width Modulation

The following specifications apply to the Timer/Counter/PWM peripheral, in PWM mode. PWM components can also be implemented in UDBs; for more information, see the PWM component data sheet in PSoC Creator.

Table 11-49. PWM DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Block current consumption	16-bit PWM, at listed input clock frequency	–	–	–	μA
	3 MHz		–	15	–	μA
	12 MHz		–	60	–	μA
	48 MHz		–	260	–	μA
	67 MHz		–	350	–	μA

Table 11-50. Pulse Width Modulation (PWM) AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Operating frequency		DC	–	67.01	MHz
	Pulse width		15	–	–	ns
	Pulse width (external)		30	–	–	ns
	Kill pulse width		15	–	–	ns
	Kill pulse width (external)		30	–	–	ns
	Enable pulse width		15	–	–	ns
	Enable pulse width (external)		30	–	–	ns
	Reset pulse width		15	–	–	ns
	Reset pulse width (external)		30	–	–	ns

16. Document Conventions

16.1 Units of Measure

Table 16-1. Units of Measure

Symbol	Unit of Measure
°C	degrees Celsius
dB	decibels
fF	femtofarads
Hz	hertz
KB	1024 bytes
kbps	kilobits per second
Khr	kilohours
kHz	kilohertz
kΩ	kilohms
ksps	kilosamples per second
LSB	least significant bit
Mbps	megabits per second
MHz	megahertz
MΩ	megaohms
Msps	megasamples per second
μA	microamperes
μF	microfarads
μH	microhenrys
μs	microseconds
μV	microvolts
μW	microwatts
mA	milliamperes
ms	milliseconds
mV	millivolts
nA	nanoamperes
ns	nanoseconds
nV	nanovolts
Ω	ohms
pF	picofarads
ppm	parts per million
ps	picoseconds
s	seconds
sps	samples per second
sqrtHz	square root of hertz
V	volts

Description Title: PSoC® 3: CY8C38 Family Datasheet Programmable System-on-Chip (PSoC®) (continued)
Document Number: 001-11729

Revision	ECN	Submission Date	Orig. of Change	Description of Change
*U	3645908	06/14/2012	MKEA	Section 2: Changed text and added figures describing Vddio source and sink. Corrected example PCB layout figure. Sections 3, 6.2: Added text about usage in externally regulated mode. Section 5.2 and elsewhere: Added text describing flash cache, and updated related text. Section 6.1, 11.91: Changed IMO startup time specification. Section 6.1.1.4: Removed text stating that FTW is a wakeup source. Section 6.2.1.4: Added paragraph clarifying limiting the frequency of IO input signals to achieve low hibernate current. Section 6.3: Changed reset status register description text. Sections 6.3.1.1, 6.3.1.2: Added text on XRES and PRES re-arm times Sections 6.3.1.1, 11.8.1: Revised description of IPOR and clarified PRES term. Added text on adjustability of buzz frequency. Section 6.4.14, 11.4: Deleted and updated text regarding SIO performance under certain power ramp conditions. Section 6.4.15: Changed text describing SIO modes for overvoltage tolerance. Section 7.8: Changed “compliant with I2C” to “compatible with I2C”. Section 7.9: Updated DFB description text. Sections 8.9, 11.5.6, 11.5.7: Changed DAC high and low speed/power mode descriptions and conditions. Section 9.1: Added a statement about support for JTAG programmers and file formats. Section 9.3: Deleted the text “debug operations are possible while the device is reset”. Section 11.1: Added specification for ESDHBM for when Vssa and Vssd are separate. Changed footnote to state that all GPIO input voltages must be less than Vddio. Changed supply ramp rate specification. Section 11.2.1: Added chip Idd specs for active and low-power modes, for multiple voltage, temperature and usage conditions. Section 11.3.3: Removed from boost mention of 22 µH inductors, and related graphs. Section 11.5.1: Changed load capacitor conditions in opamp specifications. Clarified description of opamp Iout specification. Section 11.5.3: Updated Vref temperature drift specifications. Added graphs and footnote. Section 11.5.4: Changed analog global specification descriptions and values. Section 11.5.5: Changed comparator specifications and conditions. Section 11.8.2: Voltage monitors response time specification is based on characterization. Section 13: Updated 48-QFN and 100-TQFP package drawings. Throughout document: updated terminology for “master” and “system” clock.
*V	3648803	06/18/2012	WKA/MKEA	Updated the description of changes for previous (*U) revision. No technical changes. EROS update.