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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	67MHz
Connectivity	EBI/EMI, I ² C, LINbus, SPI, UART/USART, USB
Peripherals	CapSense, DMA, LCD, POR, PWM, WDT
Number of I/O	38
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 5.5V
Data Converters	A/D 16x20b; D/A 4x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	68-VFQFN Exposed Pad
Supplier Device Package	68-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c3865lti-014t

More Information

Cypress provides a wealth of data at www.cypress.com to help you to select the right PSoC device for your design, and to help you to quickly and effectively integrate the device into your design. For a comprehensive list of resources, see the knowledge base article [KBA86521](#), [How to Design with PSoC 3](#), [PSoC 4](#), and [PSoC 5LP](#). Following is an abbreviated list for PSoC 3:

- Overview: [PSoC Portfolio](#), [PSoC Roadmap](#)
- Product Selectors: [PSoC 1](#), [PSoC 3](#), [PSoC 4](#), [PSoC 5LP](#)
In addition, PSoC Creator includes a device selection tool.
- Application notes: Cypress offers a large number of PSoC application notes and [code examples](#) covering a broad range of topics, from basic to advanced level. Recommended application notes for getting started with PSoC 3 are:
 - [AN54181](#): Getting Started With PSoC 3
 - [AN61290](#): Hardware Design Considerations
 - [AN57821](#): Mixed Signal Circuit Board Layout
 - [AN58304](#): Pin Selection for Analog Designs
 - [AN81623](#): Digital Design Best Practices
 - [AN73854](#): Introduction To Bootloaders
- Development Kits:
 - [CY8CKIT-030](#) is designed for analog performance, for developing high-precision analog, low-power, and low-voltage applications.
 - [CY8CKIT-001](#) provides a common development platform for any one of the PSoC 1, PSoC 3, PSoC 4, or PSoC 5LP families of devices.
 - The [MiniProg3](#) device provides an interface for flash programming and debug.
- Technical Reference Manuals (TRM)
 - [Architecture TRM](#)
 - [Registers TRM](#)
 - [Programming Specification](#)

PSoC Creator

[PSoC Creator](#) is a free Windows-based Integrated Design Environment (IDE). It enables concurrent hardware and firmware design of PSoC 3, PSoC 4, and PSoC 5LP based systems. Create designs using classic, familiar schematic capture supported by over 100 pre-verified, production-ready PSoC Components; see the [list of component datasheets](#). With PSoC Creator, you can:

1. Drag and drop component icons to build your hardware system design in the main design workspace
2. Codesign your application firmware with the PSoC hardware, using the PSoC Creator IDE C compiler
3. Configure components using the configuration tools
4. Explore the library of 100+ components
5. Review component datasheets

Figure 1. Multiple-Sensor Example Project in PSoC Creator

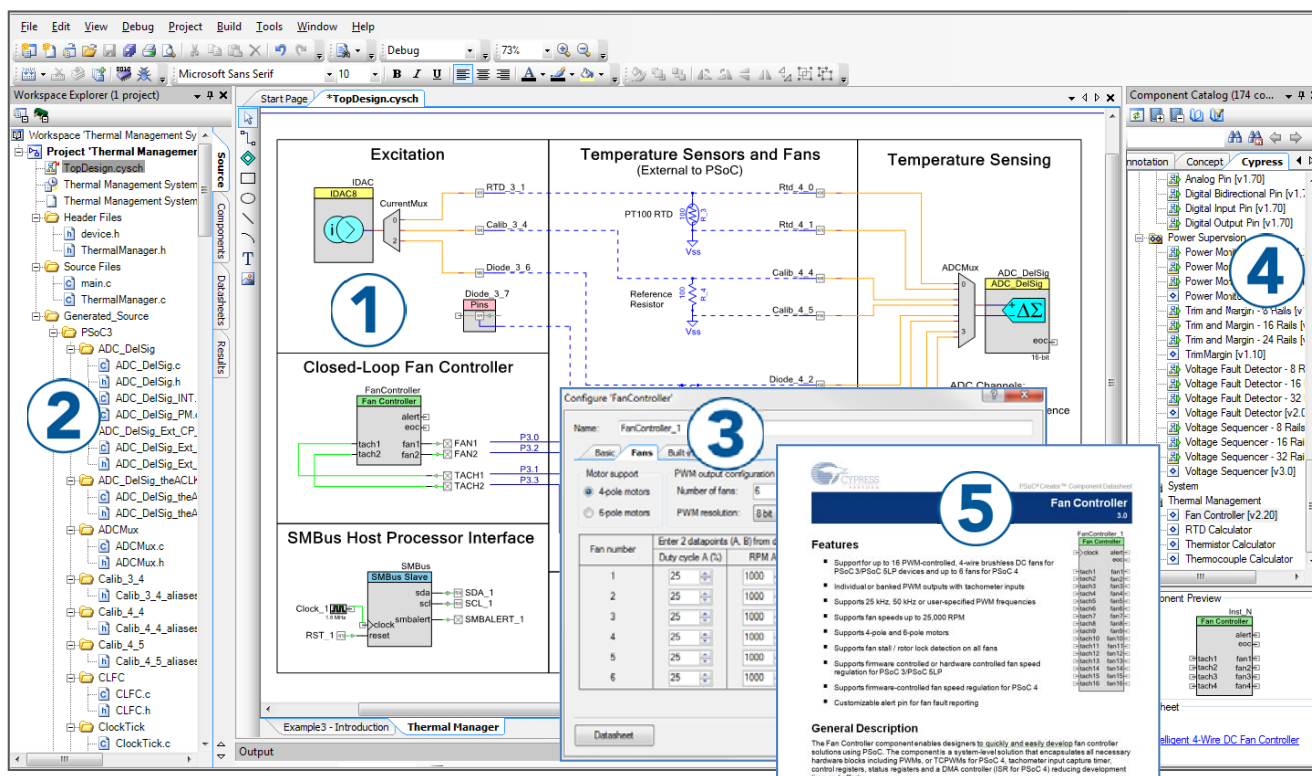


Figure 2-3. 48-pin SSOP Part Pinout

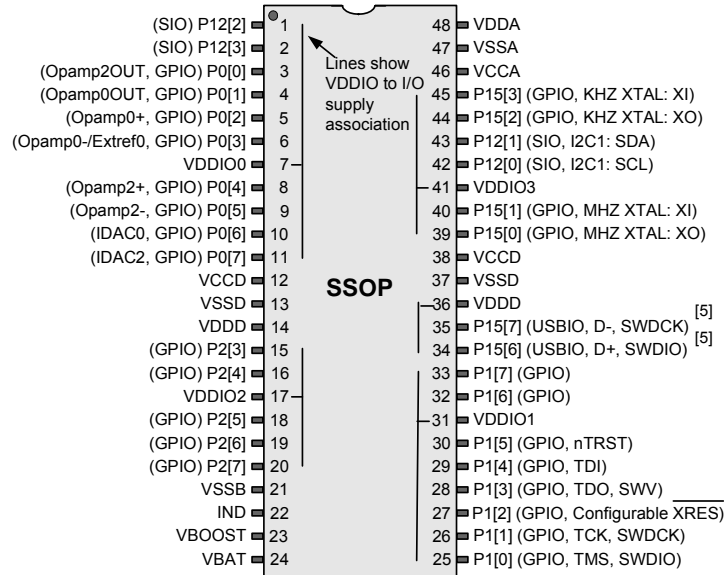
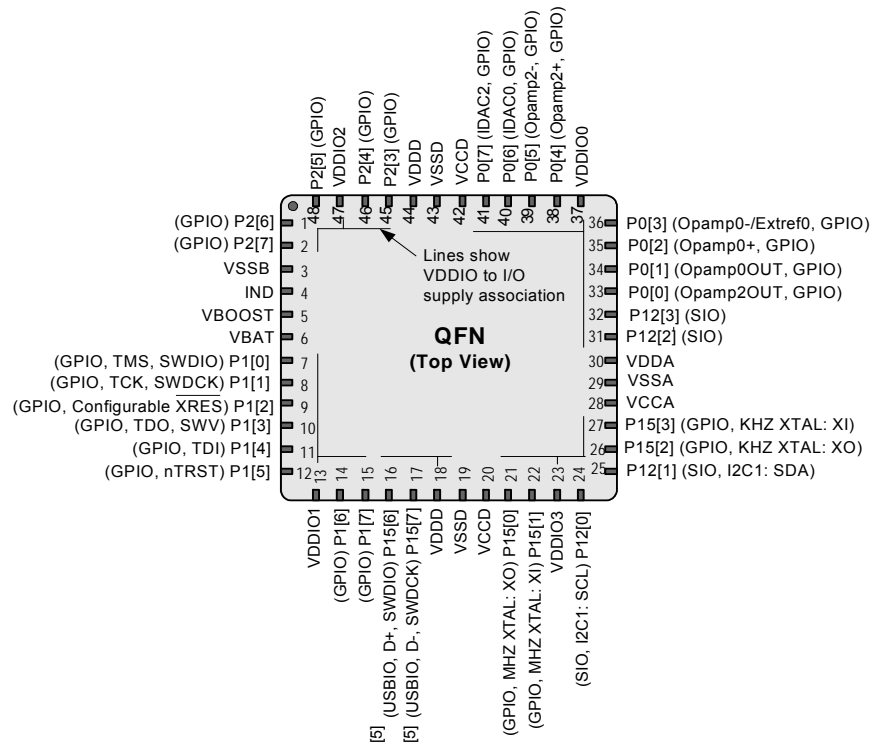


Figure 2-4. 48-pin QFN Part Pinout^[6]



Notes

5. Pins are Do Not Use (DNU) on devices without USB. The pin must be left floating.
6. The center pad on the QFN package should be connected to digital ground (VSSD) for best mechanical, thermal, and electrical performance. If not connected to ground, it should be electrically floated and not connected to any other signal. For more information, see [AN72845](#), Design Guidelines for QFN Devices.

Table 4-8. Interrupt Vector Table

#	Fixed Function	DMA	UDB
0	LVD	phub_termout0[0]	udb_intr[0]
1	Cache/ECC	phub_termout0[1]	udb_intr[1]
2	Reserved	phub_termout0[2]	udb_intr[2]
3	Sleep (Pwr Mgr)	phub_termout0[3]	udb_intr[3]
4	PICU[0]	phub_termout0[4]	udb_intr[4]
5	PICU[1]	phub_termout0[5]	udb_intr[5]
6	PICU[2]	phub_termout0[6]	udb_intr[6]
7	PICU[3]	phub_termout0[7]	udb_intr[7]
8	PICU[4]	phub_termout0[8]	udb_intr[8]
9	PICU[5]	phub_termout0[9]	udb_intr[9]
10	PICU[6]	phub_termout0[10]	udb_intr[10]
11	PICU[12]	phub_termout0[11]	udb_intr[11]
12	PICU[15]	phub_termout0[12]	udb_intr[12]
13	Comparators Combined	phub_termout0[13]	udb_intr[13]
14	Switched Caps Combined	phub_termout0[14]	udb_intr[14]
15	I ² C	phub_termout0[15]	udb_intr[15]
16	CAN	phub_termout1[0]	udb_intr[16]
17	Timer/Counter0	phub_termout1[1]	udb_intr[17]
18	Timer/Counter1	phub_termout1[2]	udb_intr[18]
19	Timer/Counter2	phub_termout1[3]	udb_intr[19]
20	Timer/Counter3	phub_termout1[4]	udb_intr[20]
21	USB SOF Int	phub_termout1[5]	udb_intr[21]
22	USB Arb Int	phub_termout1[6]	udb_intr[22]
23	USB Bus Int	phub_termout1[7]	udb_intr[23]
24	USB Endpoint[0]	phub_termout1[8]	udb_intr[24]
25	USB Endpoint Data	phub_termout1[9]	udb_intr[25]
26	Reserved	phub_termout1[10]	udb_intr[26]
27	LCD	phub_termout1[11]	udb_intr[27]
28	DFB Int	phub_termout1[12]	udb_intr[28]
29	Decimator Int	phub_termout1[13]	udb_intr[29]
30	PHUB Error Int	phub_termout1[14]	udb_intr[30]
31	EEPROM Fault Int	phub_termout1[15]	udb_intr[31]

5.7 Memory Map

The CY8C38 8051 memory map is very similar to the MCS-51 memory map.

5.7.1 Code Space

The CY8C38 8051 code space is 64 KB. Only main flash exists in this space. See the [Flash Program Memory](#) on page 23.

5.7.2 Internal Data Space

The CY8C38 8051 internal data space is 384 bytes, compressed within a 256-byte space. This space consists of 256 bytes of RAM (in addition to the SRAM mentioned in [Static RAM](#) on page 23) and a 128-byte space for special function registers (SFR). See [Figure 5-2](#). The lowest 32 bytes are used for 4 banks of registers R0-R7. The next 16 bytes are bit-addressable.

Figure 5-2. 8051 Internal Data Space

0x00 0x1F	4 Banks, R0-R7 Each	
0x20 0x2F	Bit-Addressable Area	
0x30 0x7F	Lower Core RAM Shared with Stack Space (direct and indirect addressing)	
0x80 0xFF	Upper Core RAM Shared with Stack Space (indirect addressing)	SFR Special Function Registers (direct addressing)

In addition to the register or bit address modes used with the lower 48 bytes, the lower 128 bytes can be accessed with direct or indirect addressing. With direct addressing mode, the upper 128 bytes map to the SFRs. With indirect addressing mode, the upper 128 bytes map to RAM. Stack operations use indirect addressing; the 8051 stack space is 256 bytes. See the [“Addressing Modes”](#) section on page 13.

5.7.3 SFRs

The SFR space provides access to frequently accessed registers. The memory map for the SFR memory space is shown in [Table 5-4](#).

Table 5-4. SFR Map

Address	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F
0xF8	SFRPRT15DR	SFRPRT15PS	SFRPRT15SEL	–	–	–	–	–
0xF0	B	–	SFRPRT12SEL	–	–	–	–	–
0xE8	SFRPRT12DR	SFRPRT12PS	MXAX	–	–	–	–	–
0xE0	ACC	–	–	–	–	–	–	–
0xD8	SFRPRT6DR	SFRPRT6PS	SFRPRT6SEL	–	–	–	–	–
0xD0	PSW	–	–	–	–	–	–	–
0xC8	SFRPRT5DR	SFRPRT5PS	SFRPRT5SEL	–	–	–	–	–
0xC0	SFRPRT4DR	SFRPRT4PS	SFRPRT4SEL	–	–	–	–	–
0xB8				–	–	–	–	–
0xB0	SFRPRT3DR	SFRPRT3PS	SFRPRT3SEL	–	–	–	–	–
0xA8	IE	–	–	–	–	–	–	–
0xA0	P2AX	–	SFRPRT1SEL	–	–	–	–	–
0x98	SFRPRT2DR	SFRPRT2PS	SFRPRT2SEL	–	–	–	–	–
0x90	SFRPRT1DR	SFRPRT1PS	–	DPX0	–	DPX1	–	–
0x88	–	SFRPRT0PS	SFRPRT0SEL	–	–	–	–	–
0x80	SFRPRT0DR	SP	DPL0	DPH0	DPL1	DPH1	DPS	–

The CY8C38 family provides the standard set of registers found on industry standard 8051 devices. In addition, the CY8C38 devices add SFRs to provide direct access to the I/O ports on the device. The following sections describe the SFRs added to the CY8C38 family.

5.7.4 XData Space Access SFRs

The 8051 core features dual DPTR registers for faster data transfer operations. The data pointer select SFR, DPS, selects which data pointer register, DPTR0 or DPTR1, is used for the following instructions:

- MOVX @DPTR, A
- MOVX A, @DPTR
- MOVC A, @A+DPTR
- JMP @A+DPTR
- INC DPTR
- MOV DPTR, #data16

The extended data pointer SFRs, DPX0, DPX1, MXAX, and P2AX, hold the most significant parts of memory addresses during access to the xdata space. These SFRs are used only with the MOVX instructions.

During a MOVX instruction using the DPTR0/DPTR1 register, the most significant byte of the address is always equal to the contents of DPX0/DPX1.

During a MOVX instruction using the R0 or R1 register, the most significant byte of the address is always equal to the contents of MXAX, and the next most significant byte is always equal to the contents of P2AX.

5.7.5 I/O Port SFRs

The I/O ports provide digital input sensing, output drive, pin interrupts, connectivity for analog inputs and outputs, LCD, and access to peripherals through the DSI. Full information on I/O ports is found in [I/O System and Routing](#) on page 37.

I/O ports are linked to the CPU through the PHUB and are also available in the SFRs. Using the SFRs allows faster access to a limited set of I/O port registers, while using the PHUB allows boot configuration and access to all I/O port registers.

Each SFR supported I/O port provides three SFRs:

- SFRPRTxDR sets the output data state of the port (where x is port number and includes ports 0–6, 12 and 15).
- The SFRPRTxSEL selects whether the PHUB PRTxDR register or the SFRPRTxDR controls each pin's output buffer within the port. If a SFRPRTxSEL[y] bit is high, the corresponding SFRPRTxDR[y] bit sets the output state for that pin. If a SFRPRTxSEL[y] bit is low, the corresponding PRTxDR[y] bit sets the output state of the pin (where y varies from 0 to 7).
- The SFRPRTxPS is a read only register that contains pin state values of the port pins.

5.7.5.1 xdata Space

The 8051 xdata space is 24-bit, or 16 MB in size. The majority of this space is not 'external'—it is used by on-chip components. See [Table 5-5](#). External, that is, off-chip, memory can be accessed using the EMIF. See [External Memory Interface](#) on page 25.

Table 5-5. XDATA Data Address Map

Address Range	Purpose
0x00 0000 – 0x00 1FFF	SRAM
0x00 4000 – 0x00 42FF	Clocking, PLLs, and oscillators
0x00 4300 – 0x00 43FF	Power management
0x00 4400 – 0x00 44FF	Interrupt controller
0x00 4500 – 0x00 45FF	Ports interrupt control
0x00 4700 – 0x00 47FF	Flash programming interface
0x00 4800 – 0x00 48FF	Cache controller
0x00 4900 – 0x00 49FF	I ² C controller
0x00 4E00 – 0x00 4EFF	Decimator
0x00 4F00 – 0x00 4FFF	Fixed timer/counter/PWMs
0x00 5000 – 0x00 51FF	I/O ports control
0x00 5400 – 0x00 54FF	EMIF control registers
0x00 5800 – 0x00 5FFF	Analog subsystem interface
0x00 6000 – 0x00 60FF	USB controller
0x00 6400 – 0x00 6FFF	UDB Working Registers
0x00 7000 – 0x00 7FFF	PHUB configuration
0x00 8000 – 0x00 8FFF	EEPROM
0x00 A000 – 0x00 A400	CAN
0x00 C000 – 0x00 C800	DFB
0x01 0000 – 0x01 FFFF	Digital Interconnect configuration
0x05 0220 – 0x05 02F0	Debug controller
0x08 0000 – 0x08 1FFF	Flash ECC bytes
0x80 0000 – 0xFF FFFF	External memory interface

6.4 I/O System and Routing

PSoC I/Os are extremely flexible. Every GPIO has analog and digital I/O capability. All I/Os have a large number of drive modes, which are set at POR. PSoC also provides up to four individual I/O voltage domains through the VDDIO pins.

There are two types of I/O pins on every device; those with USB provide a third type. Both GPIO and SIO provide similar digital functionality. The primary differences are their analog capability and drive strength. Devices that include USB also provide two USBIO pins that support specific USB functionality as well as limited GPIO capability.

All I/O pins are available for use as digital inputs and outputs for both the CPU and digital peripherals. In addition, all I/O pins can generate an interrupt. The flexible and advanced capabilities of the PSoC I/O, combined with any signal to any pin routability, greatly simplify circuit design and board layout. All GPIO pins can be used for analog input, CapSense^[13], and LCD segment drive, while SIO pins are used for voltages in excess of VDDA and for programmable output voltages.

- Features supported by both GPIO and SIO:
 - User programmable port reset state
 - Separate I/O supplies and voltages for up to four groups of I/O
 - Digital peripherals use DSI to connect the pins
 - Input or output or both for CPU and DMA
 - Eight drive modes
 - Every pin can be an interrupt source configured as rising edge, falling edge or both edges. If required, level sensitive interrupts are supported through the DSI
 - Dedicated port interrupt vector for each port

- Slew rate controlled digital output drive mode
- Access port control and configuration registers on either port basis or pin basis
- Separate port read (PS) and write (DR) data registers to avoid read modify write errors
- Special functionality on a pin by pin basis
- Additional features only provided on the GPIO pins:
 - LCD segment drive on LCD equipped devices
 - CapSense^[13]
 - Analog input and output capability
 - Continuous 100 µA clamp current capability
 - Standard drive strength down to 1.7 V
- Additional features only provided on SIO pins:
 - Higher drive strength than GPIO
 - Hot swap capability (5 V tolerance at any operating V_{DD})
 - Programmable and regulated high input and output drive levels down to 1.2 V
 - No analog input, CapSense, or LCD capability
 - Over voltage tolerance up to 5.5 V
 - SIO can act as a general purpose analog comparator
- USBIO features:
 - Full speed USB 2.0 compliant I/O
 - Highest drive strength for general purpose use
 - Input, output, or both for CPU and DMA
 - Input, output, or both for digital peripherals
 - Digital output (CMOS) drive mode
 - Each pin can be an interrupt source configured as rising edge, falling edge, or both edges

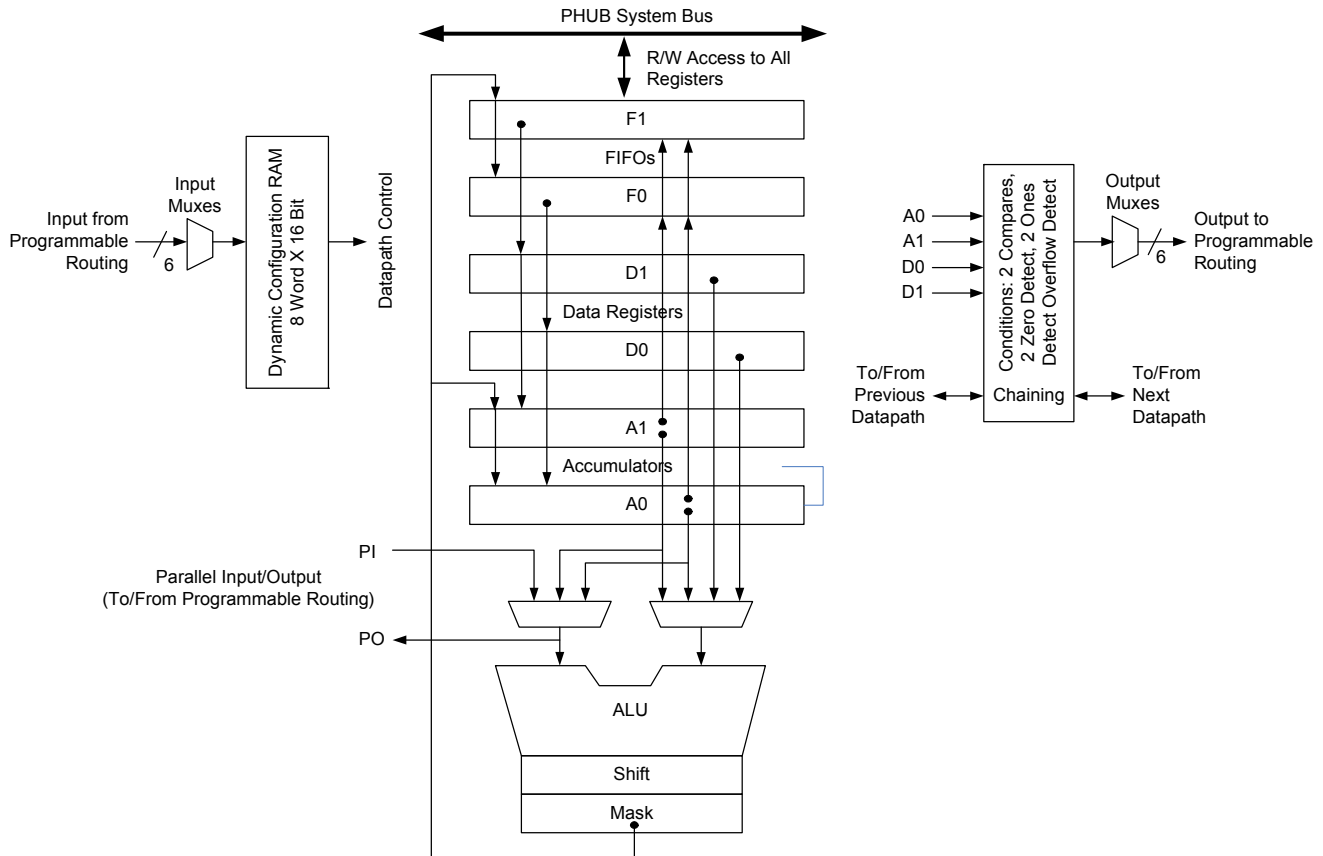
Note

13. GPIOs with opamp outputs are not recommended for use with CapSense.

7.2.2 Datapath Module

The datapath contains an 8-bit single cycle ALU, with associated compare and condition generation logic. This datapath block is optimized to implement embedded functions, such as timers, counters, integrators, PWMs, PRS, CRC, shifters and dead band generators and many others.

Figure 7-4. Datapath Top Level



7.2.2.1 Working Registers

The datapath contains six primary working registers, which are accessed by CPU firmware or DMA during normal operation.

Table 7-1. Working Datapath Registers

Name	Function	Description
A0 and A1	Accumulators	These are sources and sinks for the ALU and also sources for the compares.
D0 and D1	Data Registers	These are sources for the ALU and sources for the compares.
F0 and F1	FIFOs	These are the primary interface to the system bus. They can be a data source for the data registers and accumulators or they can capture data from the accumulators or ALU. Each FIFO is four bytes deep.

7.2.2.2 Dynamic Configuration RAM

Dynamic configuration is the ability to change the datapath function and internal configuration on a cycle-by-cycle basis, under sequencer control. This is implemented using the 8-word × 16-bit configuration RAM, which stores eight unique 16-bit wide configurations. The address input to this RAM controls the sequence, and can be routed from any block connected to the UDB routing matrix, most typically PLD logic, I/O pins, or from the outputs of this or other datapath blocks.

ALU

The ALU performs eight general purpose functions. They are:

- Increment
- Decrement
- Add
- Subtract
- Logical AND
- Logical OR
- Logical XOR
- Pass, used to pass a value through the ALU to the shift register, mask, or another UDB register.

8.3.2 LUT

The CY8C38 family of devices contains four LUTs. The LUT is a two input, one output lookup table that is driven by any one or two of the comparators in the chip. The output of any LUT is routed to the digital system interface of the UDB array. From the digital system interface of the UDB array, these signals can be connected to UDBs, DMA controller, I/O, or the interrupt controller.

The LUT control word written to a register sets the logic function on the output. The available LUT functions and the associated control word is shown in Table 8-2.

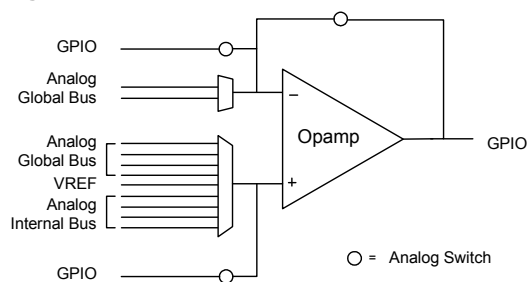
Table 8-2. LUT Function vs. Program Word and Inputs

Control Word	Output (A and B are LUT inputs)
0000b	FALSE ('0')
0001b	A AND B
0010b	A AND (NOT B)
0011b	A
0100b	(NOT A) AND B
0101b	B
0110b	A XOR B
0111b	A OR B
1000b	A NOR B
1001b	A XNOR B
1010b	NOT B
1011b	A OR (NOT B)
1100b	NOT A
1101b	(NOT A) OR B
1110b	A NAND B
1111b	TRUE ('1')

8.4 Opamps

The CY8C38 family of devices contain up to four general purpose opamps in a device.

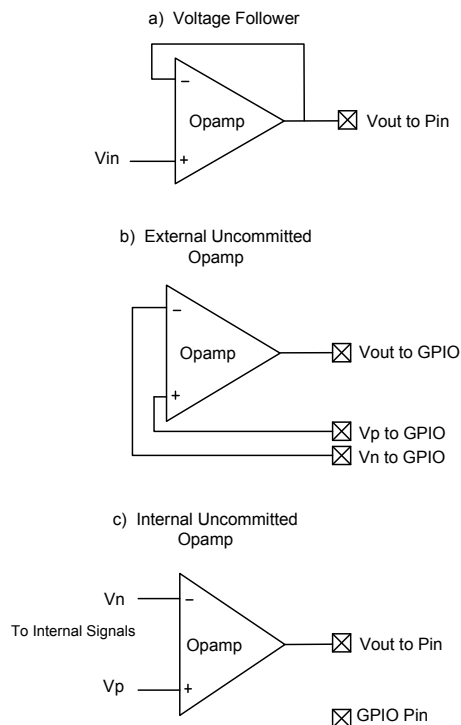
Figure 8-6. Opamp



The opamp is uncommitted and can be configured as a gain stage or voltage follower, or output buffer on external or internal signals.

See Figure 8-7. In any configuration, the input and output signals can all be connected to the internal global signals and monitored with an ADC, or comparator. The configurations are implemented with switches between the signals and GPIO pins.

Figure 8-7. Opamp Configurations



The opamp has three speed modes, slow, medium, and fast. The slow mode consumes the least amount of quiescent power and the fast mode consumes the most power. The inputs are able to swing rail-to-rail. The output swing is capable of rail-to-rail operation at low current output, within 50 mV of the rails. When driving high current loads (about 25 mA) the output voltage may only get within 500 mV of the rails.

8.5 Programmable SC/CT Blocks

The CY8C38 family of devices contains up to four switched capacitor/continuous time (SC/CT) blocks in a device. Each switched capacitor/continuous time block is built around a single rail-to-rail high bandwidth opamp.

Switched capacitor is a circuit design technique that uses capacitors plus switches instead of resistors to create analog functions. These circuits work by moving charge between capacitors by opening and closing different switches. Nonoverlapping in phase clock signals control the switches, so that not all switches are ON simultaneously.

The PSoC Creator tool offers a user friendly interface, which allows you to easily program the SC/CT blocks. Switch control and clock phase control configuration is done by PSoC Creator so users only need to determine the application use parameters such as gain, amplifier polarity, V_{REF} connection, and so on.

The same opamps and block interfaces are also connectable to an array of resistors which allows the construction of a variety of continuous time functions.

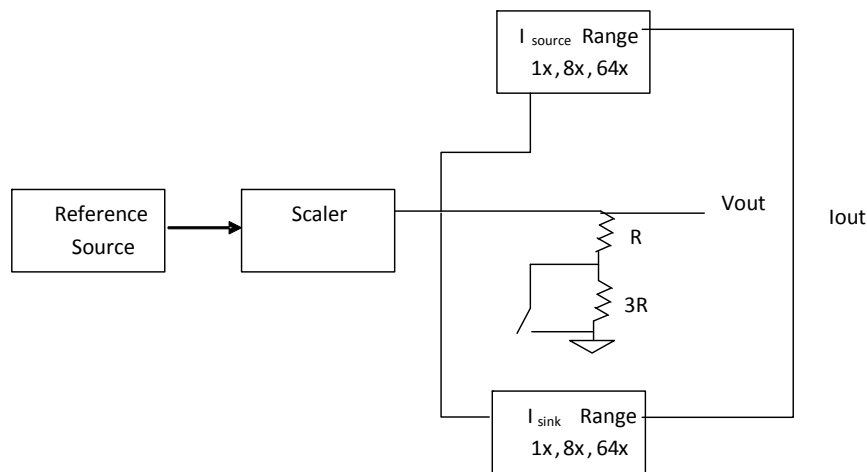
8.9 DAC

The CY8C38 parts contain up to four Digital to Analog Convertors (DACs). Each DAC is 8-bit and can be configured for either voltage or current output. The DACs support CapSense, power supply regulation, and waveform generation. Each DAC has the following features:

- Adjustable voltage or current output in 255 steps
- Programmable step size (range selection)
- Eight bits of calibration to correct ± 25 percent of gain error
- Source and sink option for current output

- High and low speed / power modes
- 8 Msps conversion rate for current output
- 1 Msps conversion rate for voltage output
- Monotonic in nature
- Data and strobe inputs can be provided by the CPU or DMA, or routed directly from the DSI
- Dedicated low-resistance output pin for high-current mode

Figure 8-11. DAC Block Diagram



8.9.1 Current DAC

The current DAC (IDAC) can be configured for the ranges 0 to 31.875 μ A, 0 to 255 μ A, and 0 to 2.04 mA. The IDAC can be configured to source or sink current.

8.9.2 Voltage DAC

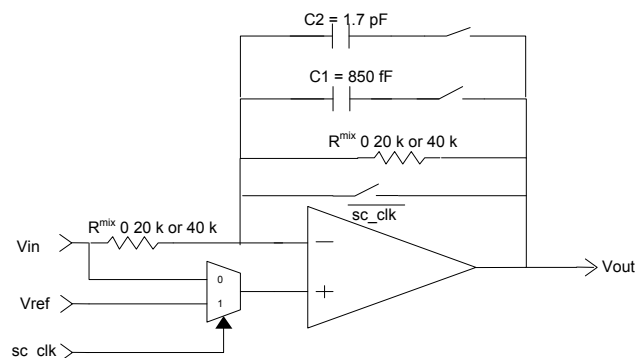
For the voltage DAC (VDAC), the current DAC output is routed through resistors. The two ranges available for the VDAC are 0 to 1.02 V and 0 to 4.08 V. In voltage mode any load connected to the output of a DAC should be purely capacitive (the output of the VDAC is not buffered).

8.10 Up/Down Mixer

In continuous time mode, the SC/CT block components are used to build an up or down mixer. Any mixing application contains an input signal frequency and a local oscillator frequency. The polarity of the clock, Fclk, switches the amplifier between inverting or noninverting gain. The output is the product of the input and the switching function from the local oscillator, with frequency components at the local oscillator plus and minus the signal frequency ($F_{clk} + F_{in}$ and $F_{clk} - F_{in}$) and reduced-level frequency components at odd integer multiples of the local oscillator frequency. The local oscillator frequency is provided by the selected clock source for the mixer.

Continuous time up and down mixing works for applications with input signals and local oscillator frequencies up to 1 MHz.

Figure 8-12. Mixer Configuration



8.11 Sample and Hold

The main application for a sample and hold, is to hold a value stable while an ADC is performing a conversion. Some applications require multiple signals to be sampled simultaneously, such as for power calculations (V and I).

11.3 Power Regulators

Specifications are valid for $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ and $T_J \leq 100^{\circ}\text{C}$, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

11.3.1 Digital Core Regulator

Table 11-4. Digital Core Regulator DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{DDD}	Input voltage		1.8	—	5.5	V
V_{CCD}	Output voltage		—	1.80	—	V
	Regulator output capacitor	$\pm 10\%$, X5R ceramic or better. The two V_{CCD} pins must be shorted together, with as short a trace as possible, see Power System on page 31	0.9	1	1.1	μF

Figure 11-5. Regulators V_{CC} vs V_{DD}

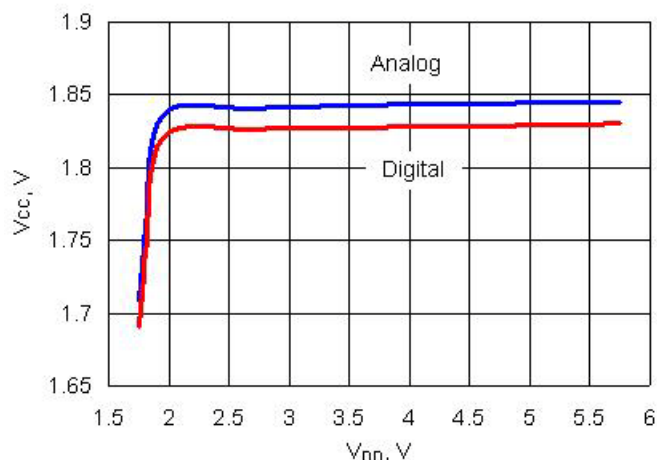
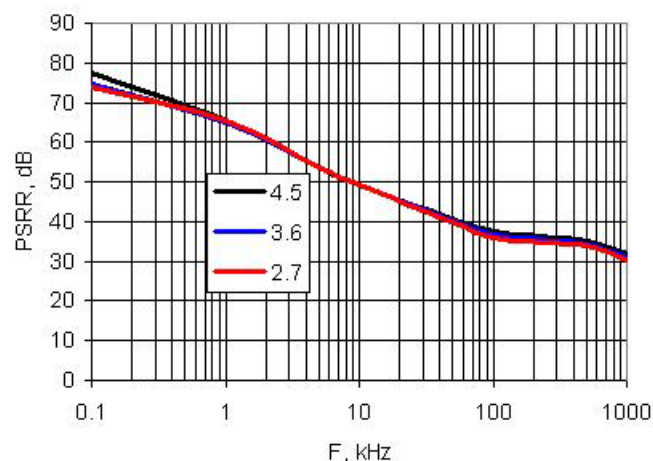


Figure 11-6. Digital Regulator PSRR vs Frequency and V_{DD}



11.3.2 Analog Core Regulator

Table 11-5. Analog Core Regulator DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{DDA}	Input voltage		1.8	—	5.5	V
V_{CCA}	Output voltage		—	1.80	—	V
	Regulator output capacitor	$\pm 10\%$, X5R ceramic or better	0.9	1	1.1	μF

Figure 11-7. Analog Regulator PSRR vs Frequency and V_{DD}

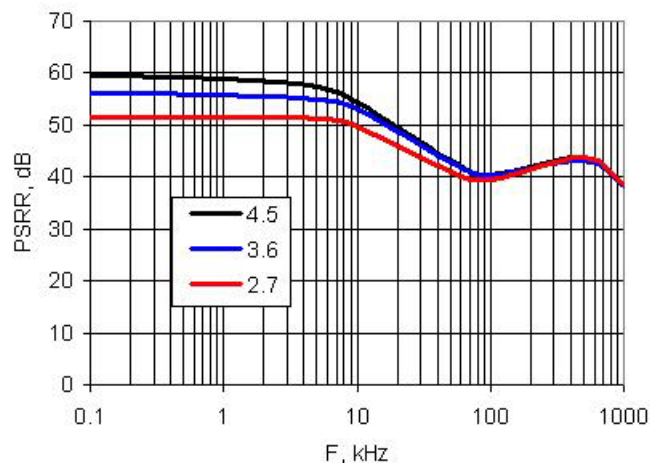


Figure 11-43. IDAC DNL vs Input Code, Range = 255 μ A, Source Mode

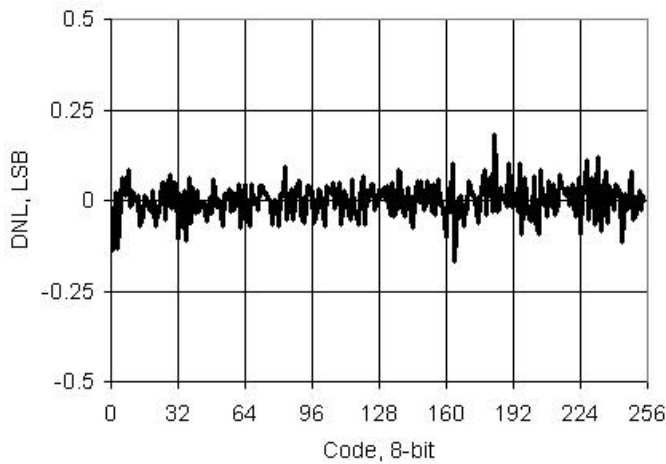


Figure 11-44. IDAC DNL vs Input Code, Range = 255 μ A, Sink Mode

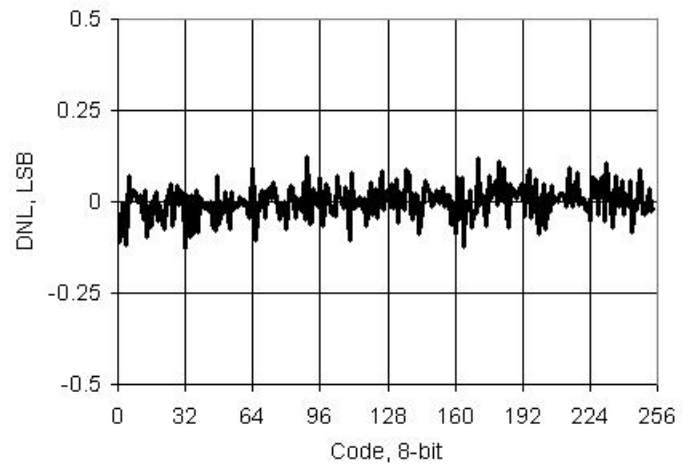


Figure 11-45. IDAC INL vs Temperature, Range = 255 μ A, High speed mode

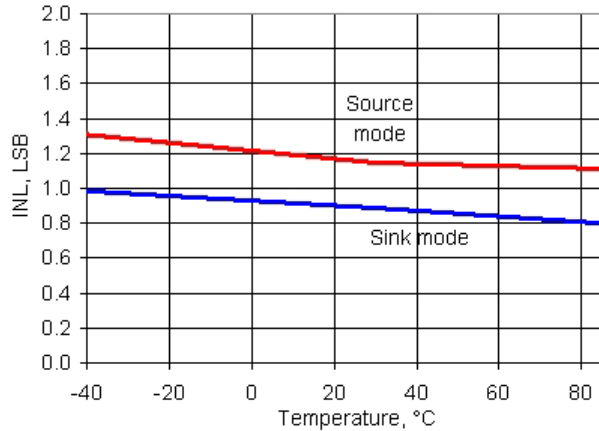


Figure 11-46. IDAC DNL vs Temperature, Range = 255 μ A, High speed mode

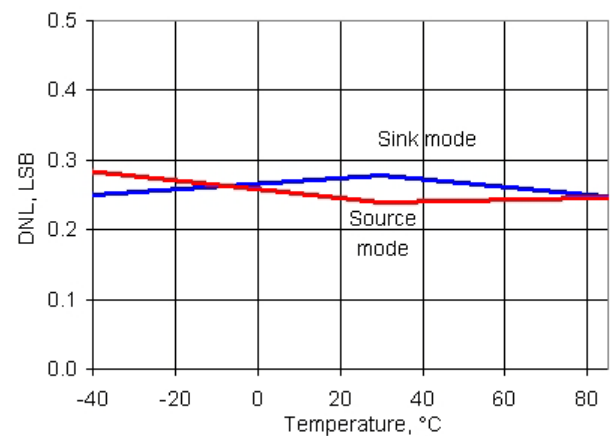


Figure 11-47. IDAC Full Scale Error vs Temperature, Range = 255 μ A, Source Mode

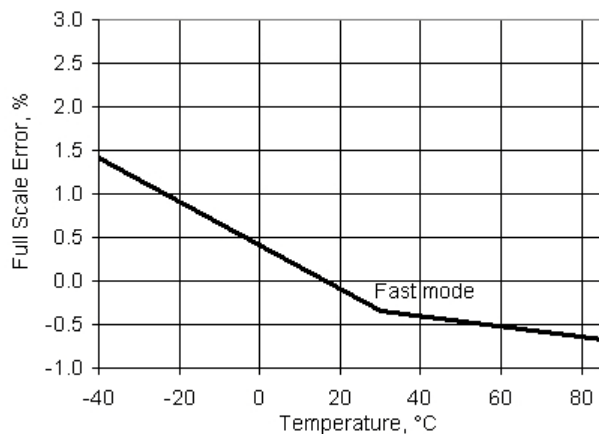


Figure 11-48. IDAC Full Scale Error vs Temperature, Range = 255 μ A, Sink Mode

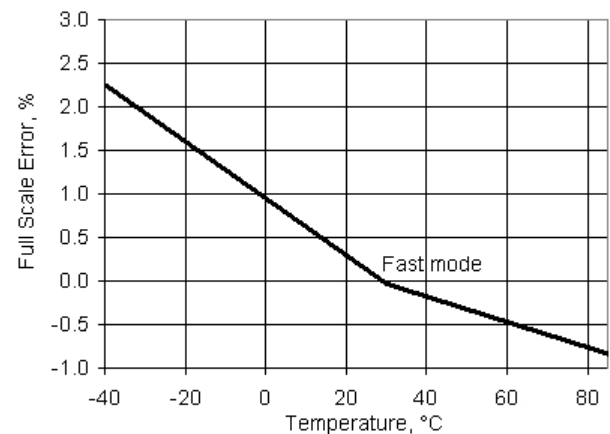


Figure 11-49. IDAC Operating Current vs Temperature, Range = 255 μ A, Code = 0, Source Mode

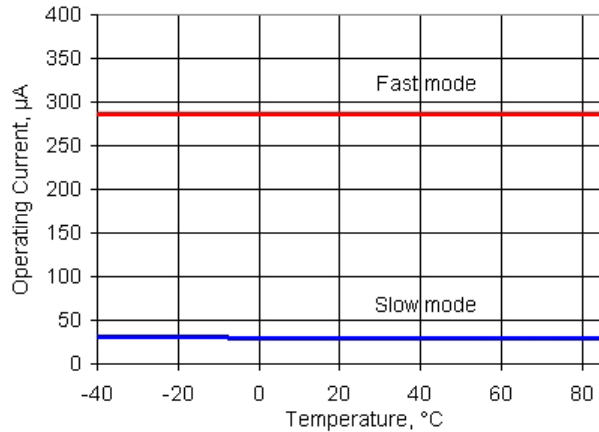


Figure 11-50. IDAC Operating Current vs Temperature, Range = 255 μ A, Code = 0, Sink Mode

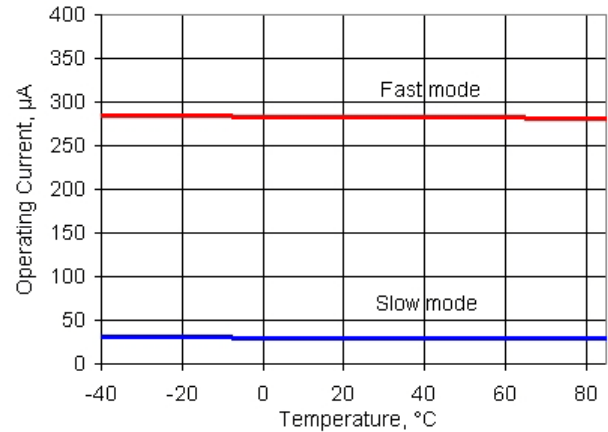


Table 11-33. IDAC AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
F_{DAC}	Update rate		–	–	8	Msp/s
T_{SETTLE}	Settling time to 0.5 LSB	Range = 31.875 μ A or 255 μ A, full scale transition, High speed mode, 600 Ω 15-pF load	–	–	125	ns
	Current noise	Range = 255 μ A, source mode, High speed mode, $V_{DDA} = 5$ V, 10 kHz	–	340	–	pA/sqrtHz

Figure 11-51. IDAC Step Response, Codes 0x40 - 0xC0, 255 μ A Mode, Source Mode, High speed mode, $V_{DDA} = 5$ V

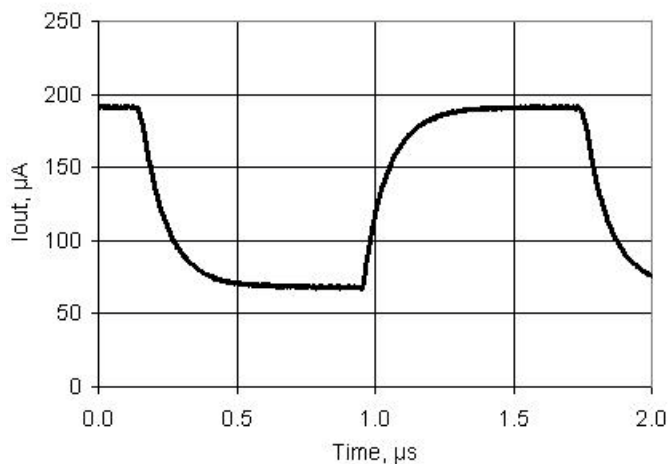
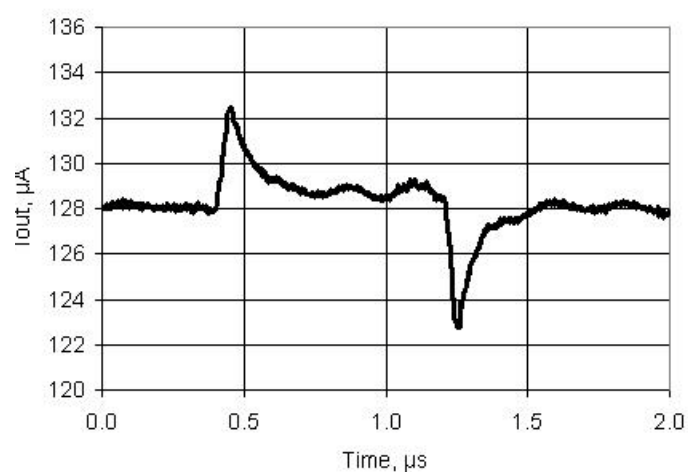


Figure 11-52. IDAC Glitch Response, Codes 0x7F - 0x80, 255 μ A Mode, Source Mode, High speed mode, $V_{DDA} = 5$ V



11.6.7 USB

Table 11-57. USB DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
V _{USB_5}	Device supply (V _{DD}) for USB operation	USB configured, USB regulator enabled	4.35	–	5.25	V
V _{USB_3.3}		USB configured, USB regulator bypassed	3.15	–	3.6	V
V _{USB_3}		USB configured, USB regulator bypassed ^[60]	2.85	–	3.6	V
I _{USB_Configured}	Device supply current in device active mode, bus clock and IMO = 24 MHz	V _{DD} = 5 V, F _{CPU} = 1.5 MHz	–	10	–	mA
		V _{DD} = 3.3 V, F _{CPU} = 1.5 MHz	–	8	–	mA
I _{USB_Suspended}	Device supply current in device sleep mode	V _{DD} = 5 V, connected to USB host, PICU configured to wake on USB resume signal	–	0.5	–	mA
		V _{DD} = 5 V, disconnected from USB host	–	0.3	–	mA
		V _{DD} = 3.3 V, connected to USB host, PICU configured to wake on USB resume signal	–	0.5	–	mA
		V _{DD} = 3.3 V, disconnected from USB host	–	0.3	–	mA

11.6.8 Universal Digital Blocks (UDBs)

PSoC Creator provides a library of prebuilt and tested standard digital peripherals (UART, SPI, LIN, PRS, CRC, timer, counter, PWM, AND, OR, and so on) that are mapped to the UDB array. See the component data sheets in PSoC Creator for full AC/DC specifications, APIs, and example code.

Table 11-58. UDB AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
Datapath Performance						
F _{MAX_TIMER}	Maximum frequency of 16-bit timer in a UDB pair		–	–	67.01	MHz
F _{MAX_ADDER}	Maximum frequency of 16-bit adder in a UDB pair		–	–	67.01	MHz
F _{MAX_CRC}	Maximum frequency of 16-bit CRC/PRS in a UDB pair		–	–	67.01	MHz
PLD Performance						
F _{MAX_PLD}	Maximum frequency of a two-pass PLD function in a UDB pair		–	–	67.01	MHz
Clock to Output Performance						
t _{CLK_OUT}	Propagation delay for clock in to data out, see Figure 11-70 .	25 °C, V _{DD} ≥ 2.7 V	–	20	25	ns
t _{CLK_OUT}	Propagation delay for clock in to data out, see Figure 11-70 .	Worst-case placement, routing, and pin selection	–	–	55	ns

Note

60. Rise/fall time matching (TR) not guaranteed, see [USB Driver AC Specifications](#) on page 87.

11.8.3 Interrupt Controller

Table 11-73. Interrupt Controller AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Delay from interrupt signal input to ISR code execution from ISR code	Includes worse case completion of longest instruction DIV with 6 cycles	–	–	25	Tcy CPU

11.8.4 JTAG Interface

Figure 11-73. JTAG Interface Timing

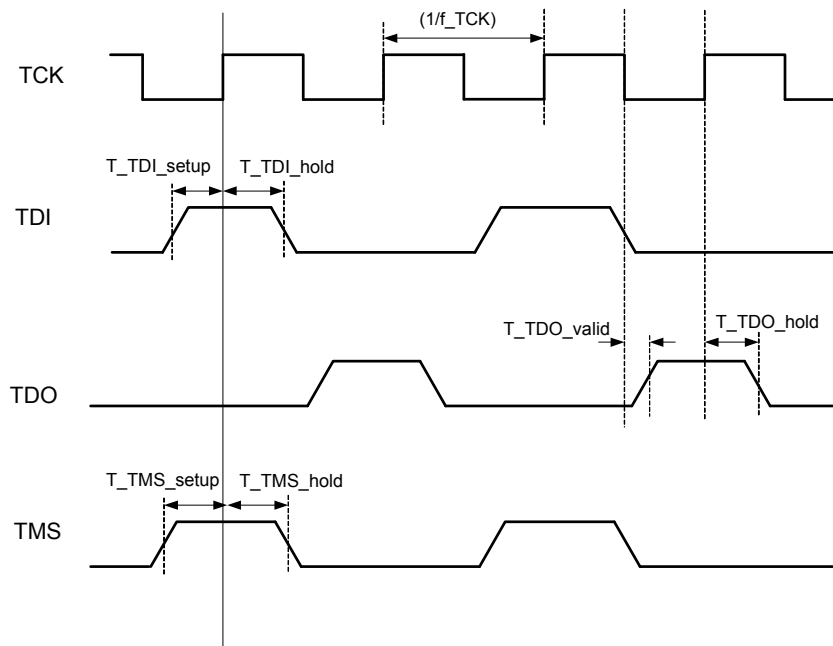


Table 11-74. JTAG Interface AC Specifications^[69]

Parameter	Description	Conditions	Min	Typ	Max	Units
f_TCK	TCK frequency	$3.3\text{ V} \leq V_{DD} \leq 5\text{ V}$	–	–	14 ^[70]	MHz
		$1.71\text{ V} \leq V_{DD} < 3.3\text{ V}$	–	–	7 ^[70]	MHz
T_TDI_setup	TDI setup before TCK high		$(T/10) - 5$	–	–	ns
T_TMS_setup	TMS setup before TCK high		T/4	–	–	
T_TDI_hold	TDI, TMS hold after TCK high	$T = 1/f_TCK$ max	T/4	–	–	
T_TDO_valid	TCK low to TDO valid	$T = 1/f_TCK$ max	–	–	2T/5	
T_TDO_hold	TDO hold after TCK high	$T = 1/f_TCK$ max	T/4	–	–	

Notes

69. Based on device characterization (Not production tested).
70. f_TCK must also be no more than 1/3 CPU clock frequency.

13. Packaging

Table 13-1. Package Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Units
T _A	Operating ambient temperature		–40	25.00	85	°C
T _J	Operating junction temperature		–40	–	100	°C
T _{JA}	Package θ_{JA} (48-pin SSOP)		–	49	–	°C/Watt
T _{JA}	Package θ_{JA} (48-pin QFN)		–	14	–	°C/Watt
T _{JA}	Package θ_{JA} (68-pin QFN)		–	15	–	°C/Watt
T _{JA}	Package θ_{JA} (100-pin TQFP)		–	34	–	°C/Watt
T _{JC}	Package θ_{JC} (48-pin SSOP)		–	24	–	°C/Watt
T _{JC}	Package θ_{JC} (48-pin QFN)		–	15	–	°C/Watt
T _{JC}	Package θ_{JC} (68-pin QFN)		–	13	–	°C/Watt
T _{JC}	Package θ_{JC} (100-pin TQFP)		–	10	–	°C/Watt
T _{JA}	Package θ_{JA} (72-pin CSP)		–	18	–	°C/Watt
T _{JC}	Package θ_{JC} (72-pin CSP)		–	0.13	–	°C/Watt

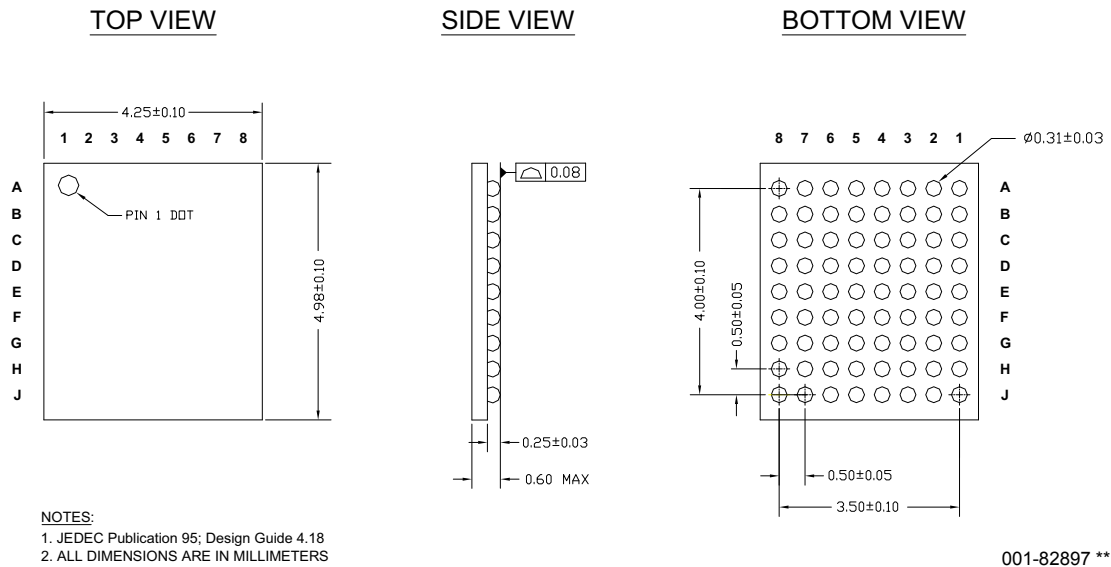
Table 13-2. Solder Reflow Peak Temperature

Package	Maximum Peak Temperature	Maximum Time at Peak Temperature
48-pin SSOP	260 °C	30 seconds
48-pin QFN	260 °C	30 seconds
68-pin QFN	260 °C	30 seconds
100-pin TQFP	260 °C	30 seconds
72-pin CSP	260 °C	30 seconds

Table 13-3. Package Moisture Sensitivity Level (MSL), IPC/JEDEC J-STD-2

Package	MSL
48-pin SSOP	MSL 3
48-pin QFN	MSL 3
68-pin QFN	MSL 3
100-pin TQFP	MSL 3
72-pin CSP	MSL 1

Figure 13-5. WLCSP Package (4.25 × 4.98 × 0.60 mm)



14. Acronyms

Table 14-1. Acronyms Used in this Document

Acronym	Description
abus	analog local bus
ADC	analog-to-digital converter
AG	analog global
AHB	AMBA (advanced microcontroller bus architecture) high-performance bus, an ARM data transfer bus
ALU	arithmetic logic unit
AMUXBUS	analog multiplexer bus
API	application programming interface
APSR	application program status register
ARM®	advanced RISC machine, a CPU architecture
ATM	automatic thump mode
BW	bandwidth
CAN	Controller Area Network, a communications protocol
CMRR	common-mode rejection ratio
CPU	central processing unit
CRC	cyclic redundancy check, an error-checking protocol
DAC	digital-to-analog converter, see also IDAC, VDAC
DFB	digital filter block
DIO	digital input/output, GPIO with only digital capabilities, no analog. See GPIO.
DMA	direct memory access, see also TD
DNL	differential nonlinearity, see also INL
DNU	do not use
DR	port write data registers
DSI	digital system interconnect
DWT	data watchpoint and trace
ECC	error correcting code
ECO	external crystal oscillator
EEPROM	electrically erasable programmable read-only memory
EMI	electromagnetic interference
EMIF	external memory interface
EOC	end of conversion
EOF	end of frame
EPSR	execution program status register
ESD	electrostatic discharge
ETM	embedded trace macrocell

Table 14-1. Acronyms Used in this Document (continued)

Acronym	Description
FIR	finite impulse response, see also IIR
FPB	flash patch and breakpoint
FS	full-speed
GPIO	general-purpose input/output, applies to a PSoC pin
HVI	high-voltage interrupt, see also LVI, LVD
IC	integrated circuit
IDAC	current DAC, see also DAC, VDAC
IDE	integrated development environment
I ² C, or IIC	Inter-Integrated Circuit, a communications protocol
IIR	infinite impulse response, see also FIR
ILO	internal low-speed oscillator, see also IMO
IMO	internal main oscillator, see also ILO
INL	integral nonlinearity, see also DNL
I/O	input/output, see also GPIO, DIO, SIO, USBIO
IPOR	initial power-on reset
IPSR	interrupt program status register
IRQ	interrupt request
ITM	instrumentation trace macrocell
LCD	liquid crystal display
LIN	Local Interconnect Network, a communications protocol.
LR	link register
LUT	lookup table
LVD	low-voltage detect, see also LVI
LVI	low-voltage interrupt, see also HVI
LVTTTL	low-voltage transistor-transistor logic
MAC	multiply-accumulate
MCU	microcontroller unit
MISO	master-in slave-out
NC	no connect
NMI	nonmaskable interrupt
NRZ	non-return-to-zero
NVIC	nested vectored interrupt controller
NVL	nonvolatile latch, see also WOL
opamp	operational amplifier
PAL	programmable array logic, see also PLD
PC	program counter
PCB	printed circuit board
PGA	programmable gain amplifier

Description Title: PSoC® 3: CY8C38 Family Datasheet Programmable System-on-Chip (PSoC®) (continued)
Document Number: 001-11729

Revision	ECN	Submission Date	Orig. of Change	Description of Change
*K	2903576	04/01/2010	MKEA	<p>Updated Vb pin in PCB Schematic.</p> <p>Updated Tstartup parameter in AC Specifications table.</p> <p>Added Load regulation and Line regulation parameters to Inductive Boost Regulator DC Specifications table.</p> <p>Updated I_{CC} parameter in LCD Direct Drive DC Specs table.</p> <p>In page 1, updated internal oscillator range under Precision programmable clocking to start from 3 MHz.</p> <p>Updated I_{OUT} parameter in LCD Direct Drive DC Specs table.</p> <p>Updated Table 6-2 and Table 6-3.</p> <p>Added bullets on CapSense in page 1; added CapSense column in Section 12.</p> <p>Removed some references to footnote [1].</p> <p>Changed INC_Rn cycles from 3 to 2 (Table 4-1).</p> <p>Added footnote in PLL AC Specification table.</p> <p>Added PLL intermediate frequency row with footnote in PLL AC Specs table.</p> <p>Added UDBs subsection under 11.6 Digital Peripherals.</p> <p>Updated Figure 2-6 (PCB Layout). Updated Pin Descriptions section and modified Figures 6-6, 6-8, 6-9.</p> <p>Updated LVD in Tables 6-2 and 6-3; modified Low-power modes bullet in page 1.</p> <p>Added note to Figures 2-5 and 6-2; Updated Figure 6-2 to add capacitors for V_{DDA} and V_{DDD} pins.</p> <p>Updated boost converter section (6.2.2).</p> <p>Updated Tstartup values in Table 11-3.</p> <p>Removed IPOR rows from Table 11-68.</p> <p>Updated 6.3.1.1, Power Voltage Level Monitors.</p> <p>Updated section 5.2 and Table 11-2 to correct suggestion of execution from flash.</p> <p>Updated V_{REF} specs in Table 11-21.</p> <p>Updated IDAC uncompensated gain error in Table 11-25.</p> <p>Updated Delay from Interrupt signal input to ISR code execution from ISR code in Table 11-72. Removed other line in table.</p> <p>Added sentence to last paragraph of section 6.1.1.3.</p> <p>Updated T_{RESP}, high and low-power modes, in Table 11-24.</p> <p>Updated f_{TCK} values in Table 11-73 and f_{SWDCK} values in Table 11-74.</p> <p>Updated SNR condition in Table 11-20.</p> <p>Corrected unit of measurement in Table 11-21.</p> <p>Updated sleep wakeup time in Table 6-3 and Tsleep in Table 11-3.</p> <p>Added 1.71 V ≤ V_{DDD} < 3.3 V, SWD over USBIO pins value to Table 11-74.</p> <p>Removed mention of hibernate reset (HRES) from page 1 features, Table 6-3, Section 6.2.1.4, Section 6.3, and Section 6.3.1.1.</p> <p>Changed PPOR/PRES to TBDs in Section 6.3.1.1, Section 6.4.1.6 (changed PPOR to reset), Table 11-3 (changed PPOR to PRES), Table 11-68 (changed title, values TBD), and Table 11-69 (changed PPOR_TR to PRES_TR).</p> <p>Added sentence saying that LVD circuits can generate a reset to Section 6.3.1.1.</p> <p>Changed I_{DD} values on page 1, page 5, and Table 11-2.</p> <p>Changed resume time value in Section 6.2.1.3.</p> <p>Changed ESD HBM value in Table 11-1.</p> <p>Changed SNR in 16-bit resolution mode value and sample rate row in Table 11-20.</p> <p>Removed V_{DDA} = 1.65 V rows and changed BWag value in Table 11-22.</p> <p>Changed V_{IOFF} values and changed CMRR value in Table 11-23.</p> <p>Changed INL max value in Table 11-27.</p> <p>Added max value to the Quiescent current specs in Tables 11-29 and 11-31.</p> <p>Changed occurrences of "Block" to "Row" and deleted the "ECC not included" footnote in Table 11-57.</p> <p>Changed max response time value in Tables 11-69 and 11-71.</p> <p>Changed the Startup time in Table 11-79.</p> <p>Added condition to intermediate frequency row in Table 11-85.</p> <p>Added row to Table 11-69.</p> <p>Added brown out note to Section 11.8.1.</p>

Description Title: PSoC® 3: CY8C38 Family Datasheet Programmable System-on-Chip (PSoC®) (continued)
Document Number: 001-11729

Revision	ECN	Submission Date	Orig. of Change	Description of Change
*U	3645908	06/14/2012	MKEA	<p>Section 2: Changed text and added figures describing Vddio source and sink. Corrected example PCB layout figure.</p> <p>Sections 3, 6.2: Added text about usage in externally regulated mode.</p> <p>Section 5.2 and elsewhere: Added text describing flash cache, and updated related text.</p> <p>Section 6.1, 11.91: Changed IMO startup time specification.</p> <p>Section 6.1.1.4: Removed text stating that FTW is a wakeup source.</p> <p>Section 6.2.1.4: Added paragraph clarifying limiting the frequency of IO input signals to achieve low hibernate current.</p> <p>Section 6.3: Changed reset status register description text.</p> <p>Sections 6.3.1.1, 6.3.1.2: Added text on XRES and PRES re-arm times</p> <p>Sections 6.3.1.1, 11.8.1: Revised description of IPOR and clarified PRES term. Added text on adjustability of buzz frequency.</p> <p>Section 6.4.14, 11.4: Deleted and updated text regarding SIO performance under certain power ramp conditions.</p> <p>Section 6.4.15: Changed text describing SIO modes for overvoltage tolerance.</p> <p>Section 7.8: Changed “compliant with I2C” to “compatible with I2C”.</p> <p>Section 7.9: Updated DFB description text.</p> <p>Sections 8.9, 11.5.6, 11.5.7: Changed DAC high and low speed/power mode descriptions and conditions.</p> <p>Section 9.1: Added a statement about support for JTAG programmers and file formats.</p> <p>Section 9.3: Deleted the text “debug operations are possible while the device is reset”.</p> <p>Section 11.1: Added specification for ESDHBM for when Vssa and Vssd are separate. Changed footnote to state that all GPIO input voltages must be less than Vddio. Changed supply ramp rate specification.</p> <p>Section 11.2.1: Added chip Idd specs for active and low-power modes, for multiple voltage, temperature and usage conditions.</p> <p>Section 11.3.3: Removed from boost mention of 22 µH inductors, and related graphs.</p> <p>Section 11.5.1: Changed load capacitor conditions in opamp specifications. Clarified description of opamp Iout specification.</p> <p>Section 11.5.3: Updated Vref temperature drift specifications. Added graphs and footnote.</p> <p>Section 11.5.4: Changed analog global specification descriptions and values.</p> <p>Section 11.5.5: Changed comparator specifications and conditions.</p> <p>Section 11.8.2: Voltage monitors response time specification is based on characterization.</p> <p>Section 13: Updated 48-QFN and 100-TQFP package drawings.</p> <p>Throughout document: updated terminology for “master” and “system” clock.</p>
*V	3648803	06/18/2012	WKA/MKEA	<p>Updated the description of changes for previous (*U) revision.</p> <p>No technical changes. EROS update.</p>

Description Title: PSoC® 3: CY8C38 Family Datasheet Programmable System-on-Chip (PSoC®) (continued)
Document Number: 001-11729

Revision	ECN	Submission Date	Orig. of Change	Description of Change
AA	4188568	11/14/2013	MKEA	Added SIO Comparator Specifications. Corrected typo in the V_{REF} parameter in the Voltage Reference Specifications. Added CSP information in Packaging and Ordering Information sections. Updated delta-sigma V_{OS} spec conditions.
AB	4385782	05/21/2014	MKEA	Updated General Description and Features . Added More Information and PSoC Creator sections. Updated 100-pin TQFP package diagram. Corrected number of I/O pins for CY8C3866FNI-210.
AC	4708125	03/31/2015	MKEA	Added INL4 and DNL4 specs in VDAC DC Specifications . Updated Figure 6-11 . Added second note after Figure 6-4 . Added a reference to Fig 6-1 in Section 6.1.1 and Section 6.1.2 . Updated Section 6.2.2 . Added Section 7.8.1 . Updated Boost specifications.
AD	4807497	06/23/2015	MKEA	Added reference to code examples in More Information. Updated typ value of TWRITE from 2 to 10 in EEPROM AC specs table. Changed "Device supply for USB operation" to "Device supply (VDDD) for USB operation" in USB DC Specifications. Clarified power supply sequencing and margin for VDDA and VDDD. Updated Serial Wire Debug Interface with limitations of debugging on Port 15. Updated Section 11.7.5. Updated Delta-sigma ADC DC Specifications
AE	4932879	09/24/2015	MKEA	Changed the Regulator Output Capacitor min and max from "-" to 0.9 and 1.1, respectively. Added reference to AN54439 in Section 11.9.3. Added MHz ECO DC specs table. Removed references to IPOR rearm issues in Section 6.3.1.1. Table 6-1: Changed DSI Fmax to 33 MHz Figure 6-1: Changed External I/O or DSI to 0-33 MHz. Table 11-10: Changed Fgpoin Max to 33 MHz Table 11-12: Changed Fsioin Max to 33 MHz.
AF	5322536	06/27/2016	MKEA	Updated More Information . Corrected typos in External Electrical Connections . Added links to CAD Libraries in Section 2.