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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	67MHz
Connectivity	EBI/EMI, I²C, LINbus, SPI, UART/USART, USB
Peripherals	CapSense, DMA, LCD, POR, PWM, WDT
Number of I/O	62
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 5.5V
Data Converters	A/D 16x20b; D/A 4x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c3866axi-039t

Contents

For more details on the peripherals see the "Example Peripherals" section on page 44 of this data sheet. For information on UDBs, DSI, and other digital blocks, see the "Digital Subsystem" section on page 44 of this data sheet.

PSoC's analog subsystem is the second half of its unique configurability. All analog performance is based on a highly accurate absolute voltage reference with less than 0.1-percent error over temperature and voltage. The configurable analog subsystem includes:

- Analog muxes
- Comparators
- Voltage references
- Analog-to-digital converter (ADC)
- Digital-to-analog converters (DACs)
- Digital filter block (DFB)

All GPIO pins can route analog signals into and out of the device using the internal analog bus. This allows the device to interface up to 62 discrete analog signals. The heart of the analog subsystem is a fast, accurate, configurable delta-sigma ADC with these features:

- Less than 100 µV offset
- A gain error of 0.2 percent
- INL less than ±2 LSB
- DNL less than ±1 LSB
- SINAD better than 84 dB in 16-bit mode

This converter addresses a wide variety of precision analog applications, including some of the most demanding sensors. The output of the ADC can optionally feed the programmable DFB through the DMA without CPU intervention. You can configure the DFB to perform IIR and FIR digital filters and several user-defined custom functions. The DFB can implement filters with up to 64 taps. It can perform a 48-bit multiply-accumulate (MAC) operation in one clock cycle.

Four high-speed voltage or current DACs support 8-bit output signals at an update rate of up to 8 Msps. They can be routed out of any GPIO pin. You can create higher resolution voltage PWM DAC outputs using the UDB array. This can be used to create a pulse width modulated (PWM) DAC of up to 10 bits, at up to 48 kHz. The digital DACs in each UDB support PWM, PRS, or delta-sigma algorithms with programmable widths. In addition to the ADC, DACs, and DFB, the analog subsystem provides multiple:

- Uncommitted opamps
- Configurable switched capacitor/continuous time (SC/CT) blocks. These support:
  - Transimpedance amplifiers
  - Programmable gain amplifiers
  - Mixers
  - Other similar analog components

See the "Analog Subsystem" section on page 56 of this data sheet for more details.

PSoC's 8051 CPU subsystem is built around a single cycle pipelined 8051 8-bit processor running at up to 67 MHz. The CPU subsystem includes a programmable nested vector interrupt controller, DMA controller, and RAM. PSoC's nested vector interrupt controller provides low latency by allowing the CPU to vector directly to the first address of the interrupt service routine, bypassing the jump instruction required by other architectures. The DMA controller enables peripherals to exchange data without CPU involvement. This allows the CPU to run slower (saving power) or use those CPU cycles to improve the performance of firmware algorithms. The single cycle 8051 CPU runs ten times faster than a standard 8051 processor. The processor speed itself is configurable, allowing you to tune active power consumption for specific applications.

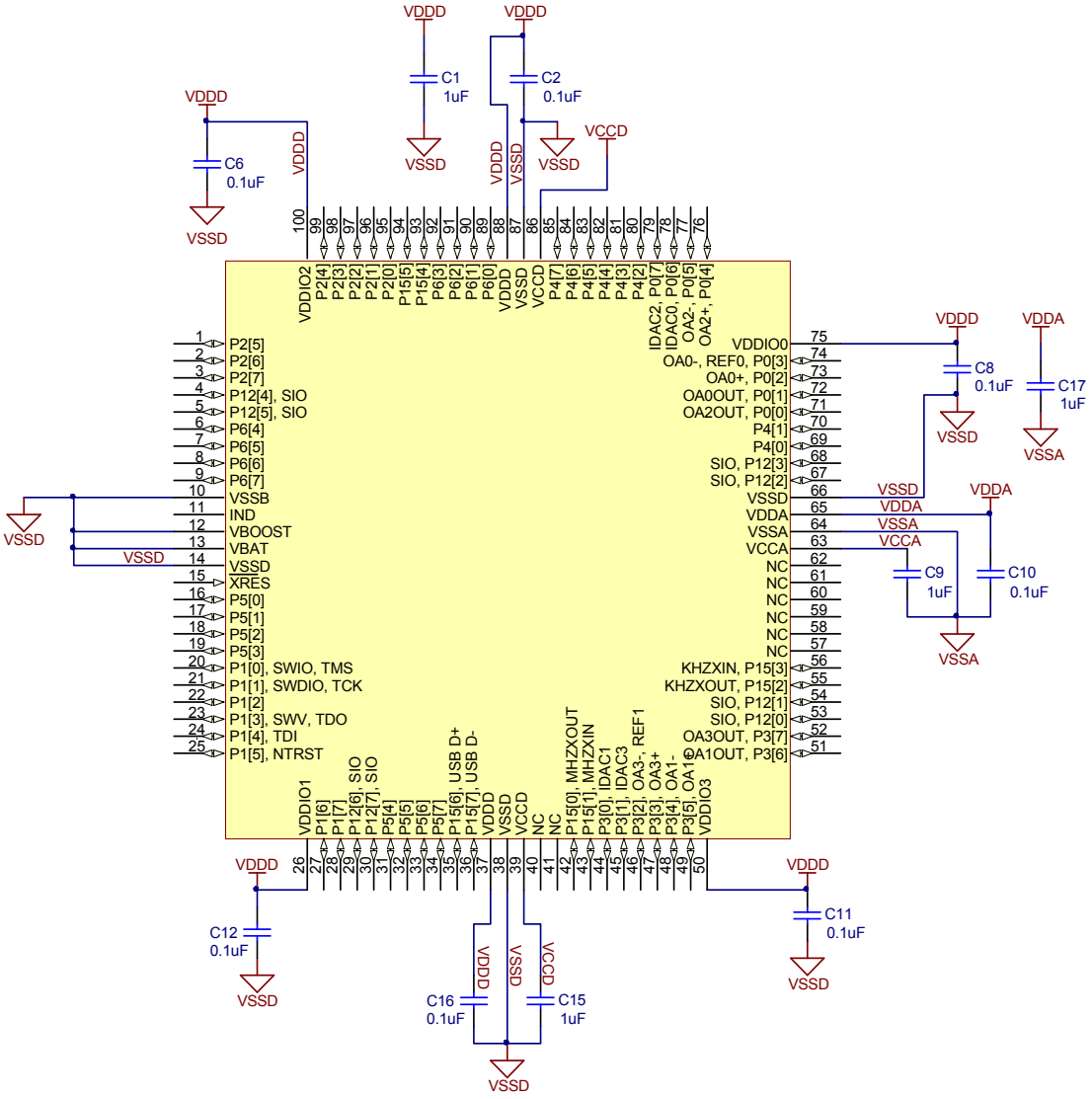
PSoC's nonvolatile subsystem consists of flash, byte-writeable EEPROM, and nonvolatile configuration options. It provides up to 64 KB of on-chip flash. The CPU can reprogram individual blocks of flash, enabling bootloaders. You can enable an error correcting code (ECC) for high reliability applications. A powerful and flexible protection model secures the user's sensitive information, allowing selective memory block locking for read and write protection. Up to 2 KB of byte-writeable EEPROM is available on-chip to store application data. Additionally, selected configuration options such as boot speed and pin drive mode are stored in nonvolatile memory. This allows settings to activate immediately after POR.

The three types of PSoC I/O are extremely flexible. All I/Os have many drive modes that are set at POR. PSoC also provides up to four I/O voltage domains through the VDDIO pins. Every GPIO has analog I/O, LCD drive[3], CapSense[4], flexible interrupt generation, slew rate control, and digital I/O capability. The SIOs on PSoC allow V_{OH} to be set independently of Vddio when used as outputs. When SIOs are in input mode they are high impedance. This is true even when the device is not powered or when the pin voltage goes above the supply voltage. This makes the SIO ideally suited for use on an I^2C bus where the PSoC may not be powered when other devices on the bus are. The SIO pins also have high current sink capability for applications such as LED drives. The programmable input threshold feature of the SIO can be used to make the SIO function as a general purpose analog comparator. For devices with Full-Speed USB the USB physical interface is also provided (USBIO). When not using USB these pins may also be used for limited digital functionality and device programming. All of the features of the PSoC I/Os are covered in detail in the "I/O System and Routing" section on page 37 of this data sheet.

The PSoC device incorporates flexible internal clock generators, designed for high stability and factory trimmed for high accuracy. The internal main oscillator (IMO) is the clock base for the system, and has 1-percent accuracy at 3 MHz. The IMO can be configured to run from 3 MHz up to 62 MHz. Multiple clock derivatives can be generated from the main clock frequency to meet application needs. The device provides a PLL to generate clock frequencies up to 67 MHz from the IMO, external crystal, or external reference clock.

Notes
3. This feature on select devices only. See Ordering Information on page 123 for details.
4. GPIOs with opamp outputs are not recommended for use with CapSense.

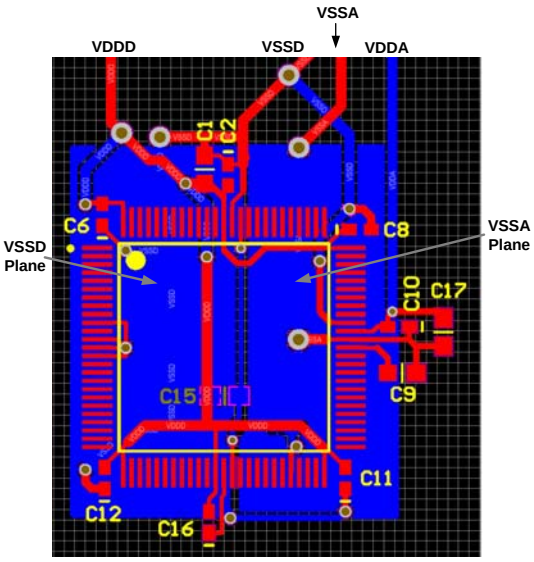
Figure 2-7. Example Schematic for 100-pin TQFP Part with Power Connections



Note The two VCCD pins must be connected together with as short a trace as possible. A trace under the device is recommended, as shown in Figure 2-8 on page 12.

For more information on pad layout, refer to http://www.cypress.com/cad-resources/psoc-3-cad-libraries.

Figure 2-8. Example PCB Layout for 100-pin TQFP Part for Optimal Analog Performance



3. Pin Descriptions

IDAC0, IDAC1, IDAC2, IDAC3

Low resistance output pin for high current DACs (IDAC).

Opamp0OUT, Opamp1OUT, Opamp2OUT, Opamp3OUT

High current output of uncommitted opamp[11].

Extref0, Extref1

External reference input to the analog system.

Opamp0–, Opamp1–, Opamp2–, Opamp3–

Inverting input to uncommitted opamp.

Opamp0+, Opamp1+, Opamp2+, Opamp3+

Noninverting input to uncommitted opamp.

GPIO

General purpose I/O pin provides interfaces to the CPU, digital peripherals, analog peripherals, interrupts, LCD segment drive, and CapSense[11].

I2C0: SCL, I2C1: SCL

I^2C SCL line providing wake from sleep on an address match. Any I/O pin can be used for I^2C SCL if wake from sleep is not required.

I2C0: SDA, I2C1: SDA

I^2C SDA line providing wake from sleep on an address match. Any I/O pin can be used for I^2C SDA if wake from sleep is not required.

IND

Inductor connection to boost pump.

kHz XTAL: Xo, kHz XTAL: Xi

32.768-kHz crystal oscillator pin.

MHz XTAL: Xo, MHz XTAL: Xi

4- to 25-MHz crystal oscillator pin.

nTRST

Optional JTAG test reset programming and debug port connection to reset the JTAG connection.

SIO

Special I/O provides interfaces to the CPU, digital peripherals and interrupts with a programmable high threshold voltage, analog comparator, high sink current, and high impedance state when the device is unpowered.

SWDCK

Serial wire debug clock programming and debug port connection.

SWDIO

Serial wire debug input and output programming and debug port connection.

SWV

Single wire viewer debug output.

TCK

JTAG test clock programming and debug port connection.

TDI

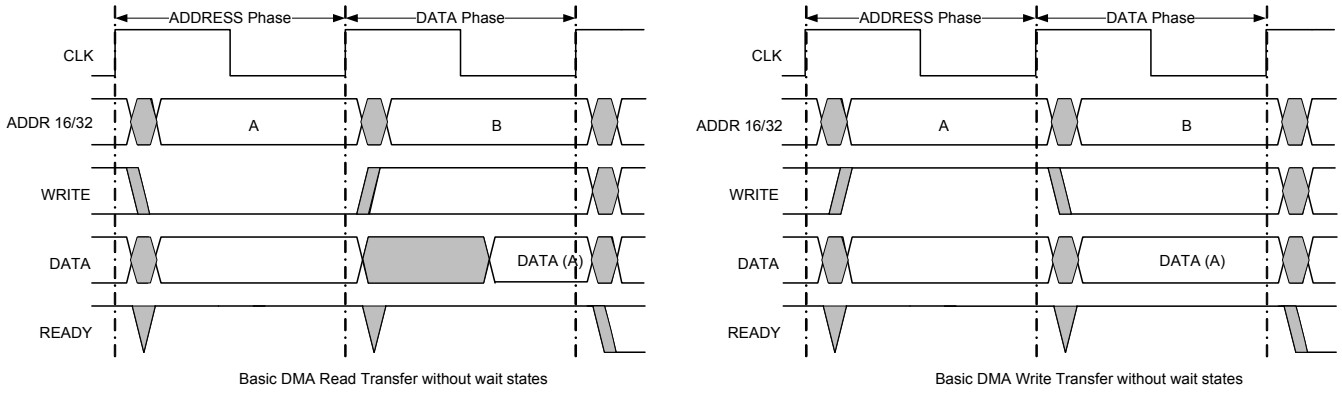
JTAG test data in programming and debug port connection.

TDO

JTAG test data out programming and debug port connection.

Note
11. GPIOs with opamp outputs are not recommended for use with CapSense.

Figure 4-1. DMA Timing Diagram



4.4.4.2 Auto Repeat DMA

Auto repeat DMA is typically used when a static pattern is repetitively read from system memory and written to a peripheral. This is done with a single TD that chains to itself.

4.4.4.3 Ping Pong DMA

A ping pong DMA case uses double buffering to allow one buffer to be filled by one client while another client is consuming the data previously received in the other buffer. In its simplest form, this is done by chaining two TDs together so that each TD calls the opposite TD when complete.

4.4.4.4 Circular DMA

Circular DMA is similar to ping pong DMA except it contains more than two buffers. In this case there are multiple TDs; after the last TD is complete it chains back to the first TD.

4.4.4.5 Scatter Gather DMA

In the case of scatter gather DMA, there are multiple noncontiguous sources or destinations that are required to effectively carry out an overall DMA transaction. For example, a packet may need to be transmitted off of the device and the packet elements, including the header, payload, and trailer, exist in various noncontiguous locations in memory. Scatter gather DMA allows the segments to be concatenated together by using multiple TDs in a chain. The chain gathers the data from the multiple locations. A similar concept applies for the reception of data onto the device. Certain parts of the received data may need to be scattered to various locations in memory for software processing convenience. Each TD in the chain specifies the location for each discrete element in the chain.

4.4.4.6 Packet Queuing DMA

Packet queuing DMA is similar to scatter gather DMA but specifically refers to packet protocols. With these protocols, there may be separate configuration, data, and status phases associated with sending or receiving a packet.

For instance, to transmit a packet, a memory mapped configuration register can be written inside a peripheral, specifying the overall length of the ensuing data phase. The CPU can set up this configuration information anywhere in system memory and copy it with a simple TD to the peripheral. After the configuration phase, a data phase TD (or a series of data phase TDs) can begin (potentially using scatter gather). When the data phase TD(s) finish, a status phase TD can be invoked that reads some memory mapped status information from the peripheral and copies it to a location in system memory specified by the CPU for later inspection. Multiple sets of configuration, data, and status phase ‘subchains’ can be strung together to create larger chains that transmit multiple packets in this way. A similar concept exists in the opposite direction to receive the packets.

4.4.4.7 Nested DMA

One TD may modify another TD, as the TD configuration space is memory mapped similar to any other peripheral. For example, a first TD loads a second TD’s configuration and then calls the second TD. The second TD moves data as required by the application. When complete, the second TD calls the first TD, which again updates the second TD’s configuration. This process repeats as often as necessary.

4.5 Interrupt Controller

The interrupt controller provides a mechanism for hardware resources to change program execution to a new address, independent of the current task being executed by the main code. The interrupt controller provides enhanced features not found on original 8051 interrupt controllers:

- Thirty-two interrupt vectors
- Jumps directly to ISR anywhere in code space with dynamic vector addresses
- Multiple sources for each vector
- Flexible interrupt to vector matching
- Each interrupt vector is independently enabled or disabled
- Each interrupt can be dynamically assigned one of eight priorities
- Eight level nestable interrupts
- Multiple I/O interrupt vectors
- Software can send interrupts
- Software can clear pending interrupts

Figure 4-2 on page 20 represents typical flow of events when an interrupt triggered. Figure 4-3 on page 21 shows the interrupt structure and priority polling.

Table 4-8. Interrupt Vector Table

#	Fixed Function	DMA	UDB
0	LVD	phub_termout0[0]	udb_intr[0]
1	Cache/ECC	phub_termout0[1]	udb_intr[1]
2	Reserved	phub_termout0[2]	udb_intr[2]
3	Sleep (Pwr Mgr)	phub_termout0[3]	udb_intr[3]
4	PICU[0]	phub_termout0[4]	udb_intr[4]
5	PICU[1]	phub_termout0[5]	udb_intr[5]
6	PICU[2]	phub_termout0[6]	udb_intr[6]
7	PICU[3]	phub_termout0[7]	udb_intr[7]
8	PICU[4]	phub_termout0[8]	udb_intr[8]
9	PICU[5]	phub_termout0[9]	udb_intr[9]
10	PICU[6]	phub_termout0[10]	udb_intr[10]
11	PICU[12]	phub_termout0[11]	udb_intr[11]
12	PICU[15]	phub_termout0[12]	udb_intr[12]
13	Comparators Combined	phub_termout0[13]	udb_intr[13]
14	Switched Caps Combined	phub_termout0[14]	udb_intr[14]
15	I^2C	phub_termout0[15]	udb_intr[15]
16	CAN	phub_termout1[0]	udb_intr[16]
17	Timer/Counter0	phub_termout1[1]	udb_intr[17]
18	Timer/Counter1	phub_termout1[2]	udb_intr[18]
19	Timer/Counter2	phub_termout1[3]	udb_intr[19]
20	Timer/Counter3	phub_termout1[4]	udb_intr[20]
21	USB SOF Int	phub_termout1[5]	udb_intr[21]
22	USB Arb Int	phub_termout1[6]	udb_intr[22]
23	USB Bus Int	phub_termout1[7]	udb_intr[23]
24	USB Endpoint[0]	phub_termout1[8]	udb_intr[24]
25	USB Endpoint Data	phub_termout1[9]	udb_intr[25]
26	Reserved	phub_termout1[10]	udb_intr[26]
27	LCD	phub_termout1[11]	udb_intr[27]
28	DFB Int	phub_termout1[12]	udb_intr[28]
29	Decimator Int	phub_termout1[13]	udb_intr[29]
30	PHUB Error Int	phub_termout1[14]	udb_intr[30]
31	EEPROM Fault Int	phub_termout1[15]	udb_intr[31]

6.1.1 Internal Oscillators

Figure 6-1 shows that there are two internal oscillators. They can be routed directly or divided. The direct routes may not have a 50% duty cycle. Divided clocks have a 50% duty cycle.

6.1.1.1 Internal Main Oscillator

In most designs the IMO is the only clock source required, due to its ±1-percent accuracy. The IMO operates with no external components and outputs a stable clock. A factory trim for each frequency range is stored in the device. With the factory trim, tolerance varies from ±1 percent at 3 MHz, up to ±7 percent at 62 MHz. The IMO, in conjunction with the PLL, allows generation of other clocks up to the device's maximum frequency (see PLL). The IMO provides clock outputs at 3, 6, 12, 24, 48, and 62 MHz.

6.1.1.2 Clock Doubler

The clock doubler outputs a clock at twice the frequency of the input clock. The doubler works at input frequency of 24 MHz, providing 48 MHz for the USB. It can be configured to use a clock from the IMO, MHzECO, or the DSI (external pin).

6.1.1.3 PLL

The PLL allows low-frequency, high-accuracy clocks to be multiplied to higher frequencies. This is a trade off between higher clock frequency and accuracy and, higher power consumption and increased startup time.

The PLL block provides a mechanism for generating clock frequencies based upon a variety of input sources. The PLL outputs clock frequencies in the range of 24 to 67 MHz. Its input and feedback dividers supply 4032 discrete ratios to create almost any desired clock frequency. The accuracy of the PLL output depends on the accuracy of the PLL input source. The most common PLL use is to multiply the IMO clock at 3 MHz, where it is most accurate, to generate the other clocks up to the device's maximum frequency.

The PLL achieves phase lock within 250 µs (verified by bit setting). It can be configured to use a clock from the IMO, MHzECO or DSI (external pin). The PLL clock source can be used until lock is complete and signaled with a lock bit. The lock signal can be routed through the DSI to generate an interrupt. Disable the PLL before entering low-power modes.

6.1.1.4 Internal Low-Speed Oscillator

The ILO provides clock frequencies for low-power consumption, including the watchdog timer, and sleep timer. The ILO generates up to three different clocks: 1 kHz, 33 kHz, and 100 kHz. The 1-kHz clock (CLK1K) is typically used for a background 'heartbeat' timer. This clock inherently lends itself to low-power supervisory operations such as the watchdog timer and long sleep intervals using the central timewheel (CTW).

The central timewheel is a 1-kHz, free running, 13-bit counter clocked by the ILO. The central timewheel is always enabled, except in hibernate mode and when the CPU is stopped during debug on chip mode. It can be used to generate periodic interrupts for timing purposes or to wake the system from a low-power mode. Firmware can reset the central timewheel. Systems that require accurate timing should use the RTC capability instead of the central timewheel.

The 100-kHz clock (CLK100K) can be used as a low power master clock. It can also generate time intervals using the fast timewheel.

The fast timewheel is a 5-bit counter, clocked by the 100-kHz clock. It features programmable settings and automatically resets when the terminal count is reached. An optional interrupt can be generated each time the terminal count is reached. This enables flexible, periodic interrupts of the CPU at a higher rate than is allowed using the central timewheel.

The 33-kHz clock (CLK33K) comes from a divide-by-3 operation on CLK100K. This output can be used as a reduced accuracy version of the 32.768-kHz ECO clock with no need for a crystal.

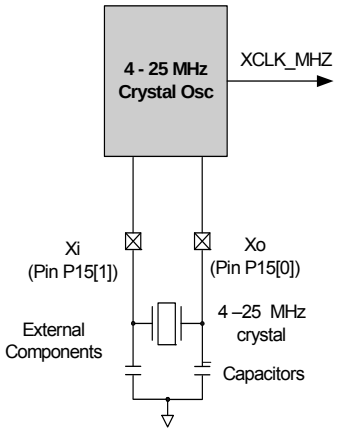
6.1.2 External Oscillators

Figure 6-1 shows that there are two external oscillators. They can be routed directly or divided. The direct routes may not have a 50% duty cycle. Divided clocks have a 50% duty cycle.

6.1.2.1 MHz External Crystal Oscillator

The MHzECO provides high frequency, high precision clocking using an external crystal (see Figure 6-2). It supports a wide variety of crystal types, in the range of 4 to 25 MHz. When used in conjunction with the PLL, it can generate other clocks up to the device's maximum frequency (see PLL). The GPIO pins connecting to the external crystal and capacitors are fixed. MHzECO accuracy depends on the crystal chosen.

Figure 6-2. MHzECO Block Diagram



6.1.2.2 32.768-kHz ECO

The 32.768-kHz external crystal oscillator (32kHzECO) provides precision timing with minimal power consumption using an external 32.768-kHz watch crystal (see Figure 6-3). The 32kHzECO also connects directly to the sleep timer and provides the source for the RTC. The RTC uses a 1-second interrupt to implement the RTC functionality in firmware.

The oscillator works in two distinct power modes. This allows users to trade off power consumption with noise immunity from neighboring circuits. The GPIO pins connected to the external crystal and capacitors are fixed.

6.2.1 Power Modes

PSoC 3 devices have four different power modes, as shown in Table 6-2 and Table 6-3. The power modes allow a design to easily provide required functionality and processing power while simultaneously minimizing power consumption and maximizing battery life in low-power and portable devices.

PSoC 3 power modes, in order of decreasing power consumption are:

- Active
- Alternate Active
- Sleep
- Hibernate

Active is the main processing mode. Its functionality is configurable. Each power controllable subsystem is enabled or disabled by using separate power configuration template registers. In alternate active mode, fewer subsystems are enabled, reducing power. In sleep mode most resources are disabled regardless of the template settings. Sleep mode is optimized to provide timed sleep intervals and Real Time Clock functionality. The lowest power mode is hibernate, which retains register and SRAM state, but no clocks, and allows wakeup only from I/O pins. Figure 6-5 on page 33 illustrates the allowable transitions between power modes. Sleep and hibernate modes should not be entered until all VDDIO supplies are at valid voltage levels.

Table 6-2. Power Modes

Power Modes	Description	Entry Condition	Wakeup Source	Active Clocks	Regulator
Active	Primary mode of operation, all peripherals available (programmable)	Wakeup, reset, manual register entry	Any interrupt	Any (programmable)	All regulators available. Digital and analog regulators can be disabled if external regulation used.
Alternate Active	Similar to Active mode, and is typically configured to have fewer peripherals active to reduce power. One possible configuration is to use the UDBs for processing, with the CPU turned off	Manual register entry	Any interrupt	Any (programmable)	All regulators available. Digital and analog regulators can be disabled if external regulation used.
Sleep	All subsystems automatically disabled	Manual register entry	Comparator, PICU, I^2C, RTC, CTW, LVD	ILO/kHzECO	Both digital and analog regulators buzzed. Digital and analog regulators can be disabled if external regulation used.
Hibernate	All subsystems automatically disabled Lowest power consuming mode with all peripherals and internal regulators disabled, except hibernate regulator is enabled Configuration and memory contents retained	Manual register entry	PICU		Only hibernate regulator active.

Table 6-3. Power Modes Wakeup Time and Power Consumption

Sleep Modes	Wakeup Time	Current (typ)	Code Execution	Digital Resources	Analog Resources	Clock Sources Available	Wakeup Sources	Reset Sources
Active	–	1.2 mA[12]	Yes	All	All	All	–	All
Alternate Active	–	–	User defined	All	All	All	–	All
Sleep	<15 µs	1 µA	No	I^2C	Comparator	ILO/kHzECO	Comparator, PICU, I^2C, RTC, CTW, LVD	XRES, LVD, WDR
Hibernate	<100 µs	200 nA	No	None	None	None	PICU	XRES

Note
12. Bus clock off. Execute from cache at 6 MHz. See Table 11-2 on page 72.

boost typically draws 250 µA in active mode and 25 µA in standby mode. The boost operating modes must be used in conjunction with chip power modes to minimize total power consumption. Table 6-4 lists the boost power modes available in different chip power modes.

Table 6-4. Chip and Boost Power Modes Compatibility

Chip Power Modes	Boost Power Modes
Chip-active or alternate active mode	Boost must be operated in its active mode.
Chip-sleep mode	Boost can be operated in either active or standby mode. In boost standby mode, the chip must wake up periodically for boost active-mode refresh.
Chip-hibernate mode	Boost can be operated in its active mode. However, it is recommended not to use the boost in chip hibernate mode due to the higher current consumption in boost active mode.

6.2.2.1 Boost Firmware Requirements

To ensure boost inrush current is within specification at startup, the **Enable Fast IMO During Startup** value must be unchecked in the PSoC Creator IDE. The **Enable Fast IMO During Startup** option is found in PSoC Creator in the design wide resources (cydwr) file **System** tab. Un-checking this option configures the device to run at 12 MHz vs 48 MHz during startup while configuring the device. The slower clock speed results in reduced current draw through the boost circuit.

6.2.2.2 Boost Design Process

Correct operation of the boost converter requires specific component values determined for each designs unique operating conditions. The C_{BAT} capacitor, Inductor, Schottky diode, and C_{BOOST} capacitor components are required with the values specified in the electrical specifications, Table 11-7 on page 78. The only variable component value is the inductor L_{BOOST} which is primarily sized for correct operation of the boost across operating conditions and secondarily for efficiency. Additional operating region constraints exist for V_{OUT}, V_{BAT}, I_{OUT}, and T_A.

The following steps must be followed to determine boost converter operating parameters and L_{BOOST} value.

1. Choose desired V_{BAT}, V_{OUT}, T_A, and I_{OUT} operating condition ranges for the application.
2. Determine if V_{BAT} and V_{OUT} ranges fit the boost operating range based on the **T_A range over V_{BAT} and V_{OUT}** chart, Figure 11-8 on page 78. If the operating ranges are not met, modify the operating conditions or use an external boost regulator.
3. Determine if the desired ambient temperature (T_A) range fits the ambient temperature operating range based on the **T_A range over V_{BAT} and V_{OUT}** chart, Figure 11-8 on page 78. If the temperature range is not met, modify the operating conditions and return to step 2, or use an external boost regulator.
4. Determine if the desired output current (I_{OUT}) range fits the output current operating range based on the **I_{OUT} range over V_{BAT} and V_{OUT}** chart, Figure 11-9 on page 78. If the output current range is not met, modify the operating conditions and return to step 2, or use an external boost regulator.
5. Find the allowed inductor values based on the **L_{BOOST} values over V_{BAT} and V_{OUT}** chart, Figure 11-10 on page 78.
6. Based on the allowed inductor values, inductor dimensions, inductor cost, boost efficiency, and V_{RIPPLE} choose the optimum inductor value for the system. Boost efficiency and V_{RIPPLE} typical values are provided in the **Efficiency vs V_{BAT}** and **V_{RIPPLE} vs V_{BAT}** charts, Figure 11-11 on page 79 through Figure 11-14 on page 79. In general, if high efficiency and low V_{RIPPLE} are most important, then the highest allowed inductor value should be used. If low inductor cost or small inductor size are most important, then one of the smaller allowed inductor values should be used. If the allowed inductor(s) efficiency, V_{RIPPLE}, cost or dimensions are not acceptable for the application than an external boost regulator should be used.

6.3 Reset

CY8C38 has multiple internal and external reset sources available. The reset sources are:

- Power source monitoring – The analog and digital power voltages, VDDA, VDDD, VCCA, and VCCD are monitored in several different modes during power up, active mode, and sleep mode (buzzing). If any of the voltages goes outside predetermined ranges then a reset is generated. The monitors are programmable to generate an interrupt to the processor under certain conditions before reaching the reset thresholds.
- External – The device can be reset from an external source by pulling the reset pin (XRES) low. The XRES pin includes an internal pull-up to VDDIO1. VDDD, VDDA, and VDDIO1 must all have voltage applied before the part comes out of reset.
- Watchdog timer – A watchdog timer monitors the execution of instructions by the processor. If the watchdog timer is not reset by firmware within a certain period of time, the watchdog timer generates a reset.
- Software – The device can be reset under program control.

8.3.2 LUT

The CY8C38 family of devices contains four LUTs. The LUT is a two input, one output lookup table that is driven by any one or two of the comparators in the chip. The output of any LUT is routed to the digital system interface of the UDB array. From the digital system interface of the UDB array, these signals can be connected to UDBs, DMA controller, I/O, or the interrupt controller.

The LUT control word written to a register sets the logic function on the output. The available LUT functions and the associated control word is shown in Table 8-2.

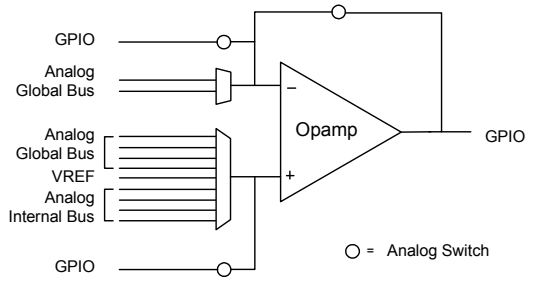
Table 8-2. LUT Function vs. Program Word and Inputs

Control Word	Output (A and B are LUT inputs)
0000b	**FALSE** (‘0’)
0001b	**A** AND **B**
0010b	**A** AND (NOT **B**)
0011b	A
0100b	(NOT **A**) AND **B**
0101b	B
0110b	**A** XOR **B**
0111b	**A** OR **B**
1000b	**A** NOR **B**
1001b	**A** XNOR **B**
1010b	NOT **B**
1011b	**A** OR (NOT **B**)
1100b	NOT **A**
1101b	(NOT **A**) OR **B**
1110b	**A** NAND **B**
1111b	**TRUE** (‘1’)

8.4 Opamps

The CY8C38 family of devices contain up to four general purpose opamps in a device.

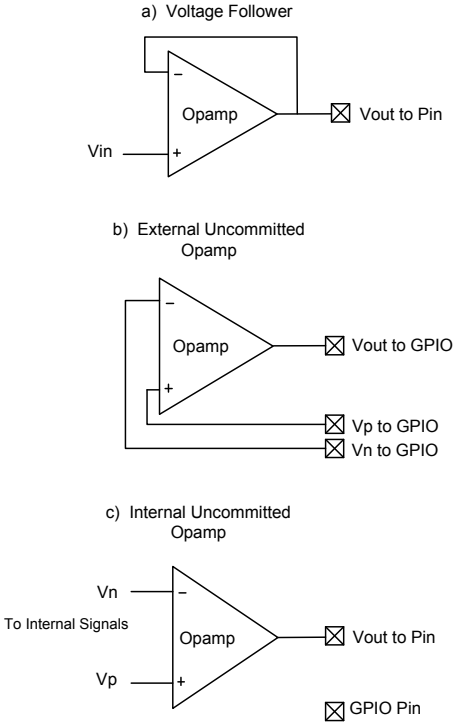
Figure 8-6. Opamp



The opamp is uncommitted and can be configured as a gain stage or voltage follower, or output buffer on external or internal signals.

See Figure 8-7. In any configuration, the input and output signals can all be connected to the internal global signals and monitored with an ADC, or comparator. The configurations are implemented with switches between the signals and GPIO pins.

Figure 8-7. Opamp Configurations



The opamp has three speed modes, slow, medium, and fast. The slow mode consumes the least amount of quiescent power and the fast mode consumes the most power. The inputs are able to swing rail-to-rail. The output swing is capable of rail-to-rail operation at low current output, within 50 mV of the rails. When driving high current loads (about 25 mA) the output voltage may only get within 500 mV of the rails.

8.5 Programmable SC/CT Blocks

The CY8C38 family of devices contains up to four switched capacitor/continuous time (SC/CT) blocks in a device. Each switched capacitor/continuous time block is built around a single rail-to-rail high bandwidth opamp.

Switched capacitor is a circuit design technique that uses capacitors plus switches instead of resistors to create analog functions. These circuits work by moving charge between capacitors by opening and closing different switches. Nonoverlapping in phase clock signals control the switches, so that not all switches are ON simultaneously.

The PSoC Creator tool offers a user friendly interface, which allows you to easily program the SC/CT blocks. Switch control and clock phase control configuration is done by PSoC Creator so users only need to determine the application use parameters such as gain, amplifier polarity, V_{REF} connection, and so on.

The same opamps and block interfaces are also connectable to an array of resistors which allows the construction of a variety of continuous time functions.

9.3 Debug Features

Using the JTAG or SWD interface, the CY8C38 supports the following debug features:

- Halt and single-step the CPU
- View and change CPU and peripheral registers, and RAM addresses
- Eight program address breakpoints
- One memory access breakpoint—break on reading or writing any memory address and data value
- Break on a sequence of breakpoints (non recursive)
- Debugging at the full speed of the CPU
- Compatible with PSoC Creator and MiniProg3 programmer and debugger
- Standard JTAG programming and debugging interfaces make CY8C38 compatible with other popular third-party tools (for example, ARM / Keil)

9.4 Trace Features

The CY8C38 supports the following trace features when using JTAG or SWD:

- Trace the 8051 program counter (PC), accumulator register (ACC), and one SFR / 8051 core RAM register
- Trace depth up to 1000 instructions if all registers are traced, or 2000 instructions if only the PC is traced (on devices that include trace memory)
- Program address trigger to start tracing
- Trace windowing, that is, only trace when the PC is within a given range
- Two modes for handling trace buffer full: continuous (overwriting the oldest trace data) or break when trace buffer is full

9.5 Single Wire Viewer Interface

The SWV interface is closely associated with SWD but can also be used independently. SWV data is output on the JTAG interface's TDO pin. If using SWV, you must configure the device for SWD, not JTAG. SWV is not supported with the JTAG interface.

SWV is ideal for application debug where it is helpful for the firmware to output data similar to 'printf' debugging on PCs. The SWV is ideal for data monitoring, because it requires only a single pin and can output data in standard UART format or Manchester encoded format. For example, it can be used to tune a PID control loop in which the output and graphing of the three error terms greatly simplifies coefficient tuning.

The following features are supported in SWV:

- 32 virtual channels, each 32 bits long
- Simple, efficient packing and serializing protocol
- Supports standard UART format (N81)

9.6 Programming Features

The JTAG and SWD interfaces provide full programming support. The entire device can be erased, programmed, and verified. You can increase flash protection levels to protect firmware IP. Flash protection can only be reset after a full device erase. Individual flash blocks can be erased, programmed, and verified, if block security settings permit.

9.7 Device Security

PSoC 3 offers an advanced security feature called device security, which permanently disables all test, programming, and debug ports, protecting your application from external access. The device security is activated by programming a 32-bit key (0×50536F43) to a Write Once Latch (WOL).

The Write Once Latch is a type of nonvolatile latch (NVL). The cell itself is an NVL with additional logic wrapped around it. Each WOL device contains four bytes (32 bits) of data. The wrapper outputs a '1' if a super-majority (28 of 32) of its bits match a pre-determined pattern (0×50536F43); it outputs a '0' if this majority is not reached. When the output is 1, the Write Once NV latch locks the part out of Debug and Test modes; it also permanently gates off the ability to erase or alter the contents of the latch. Matching all bits is intentionally not required, so that single (or few) bit failures do not deassert the WOL output. The state of the NVL bits after wafer processing is truly random with no tendency toward 1 or 0.

The WOL only locks the part after the correct 32-bit key (0×50536F43) is loaded into the NVL's volatile memory, programmed into the NVL's nonvolatile cells, and the part is reset. The output of the WOL is only sampled on reset and used to disable the access. This precaution prevents anyone from reading, erasing, or altering the contents of the internal memory.

The user can write the key into the WOL to lock out external access only if no flash protection is set (see "Flash Security" on page 23). However, after setting the values in the WOL, a user still has access to the part until it is reset. Therefore, a user can write the key into the WOL, program the flash protection data, and then reset the part to lock it.

If the device is protected with a WOL setting, Cypress cannot perform failure analysis and, therefore, cannot accept RMAs from customers. The WOL can be read out through the SWD port to electrically identify protected parts. The user can write the key in WOL to lock out external access only if no flash protection is set. For more information on how to take full advantage of the security features in PSoC see the PSoC 3 TRM.

Disclaimer

Note the following details of the flash code protection features on Cypress devices.

Cypress products meet the specifications contained in their particular Cypress data sheets. Cypress believes that its family of products is one of the most secure families of its kind on the market today, regardless of how they are used. There may be methods, unknown to Cypress, that can breach the code protection features. Any of these methods, to our knowledge, would be dishonest and possibly illegal. Neither Cypress nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Cypress is willing to work with the customer who is concerned about the integrity of their code. Code protection is constantly evolving. We at Cypress are committed to continuously improving the code protection features of our products.

11.3.3 Inductive Boost Regulator

Unless otherwise specified, operating conditions are: V_{BAT} = 0.5 V–3.6 V, V_{OUT} = 1.8 V–5.0 V, I_{OUT} = 0 mA–50 mA, L_{BOOST} = 4.7 µH–22 µH, C_{BOOST} = 22 µF || 3 × 1.0 µF || 3 × 0.1 µF, C_{BAT} = 22 µF, I_F = 1.0 A. Unless otherwise specified, all charts and graphs show typical values.

Table 11-6. Inductive Boost Regulator DC Specifications

Parameter	Description	Conditions		Min	Typ	Max	Units
V_{OUT}	Boost output voltage[34]	vsel = 1.8 V in register BOOST_CR0		1.71	1.8	1.89	V
		vsel = 1.9 V in register BOOST_CR0		1.81	1.90	2.00	V
		vsel = 2.0 V in register BOOST_CR0		1.90	2.00	2.10	V
		vsel = 2.4 V in register BOOST_CR0		2.16	2.40	2.64	V
		vsel = 2.7 V in register BOOST_CR0		2.43	2.70	2.97	V
		vsel = 3.0 V in register BOOST_CR0		2.70	3.00	3.30	V
		vsel = 3.3 V in register BOOST_CR0		2.97	3.30	3.63	V
		vsel = 3.6 V in register BOOST_CR0		3.24	3.60	3.96	V
		vsel = 5.0 V in register BOOST_CR0		4.50	5.00	5.50	V
V_{BAT}	Input voltage to boost[35]	I_{OUT} = 0 mA–5 mA	vsel = 1.8 V–2.0 V, T_A = 0 °C–70 °C	0.5	–	0.8	V
		I_{OUT} = 0 mA–15 mA	vsel = 1.8 V–5.0 V[36], T_A = –10 °C–85 °C	1.6	–	3.6	V
		I_{OUT} = 0 mA–25 mA	vsel = 1.8 V–2.7 V, T_A = –10 °C–85 °C	0.8	–	1.6	V
		I_{OUT} = 0 mA–50 mA	vsel = 1.8 V–3.3 V[36], T_A = –40 °C–85 °C	1.8	–	2.5	V
			vsel = 1.8 V–3.3 V[36], T_A = –10 °C–85 °C	1.3	–	2.5	V
			vsel = 2.5 V–5.0 V[36], T_A = –10 °C–85 °C	2.5	–	3.6	V
I_{OUT}	Output current	T_A = 0 °C–70 °C	V_{BAT} = 0.5 V–0.8 V	0	–	5	mA
		T_A = –10 °C–85 °C	V_{BAT} = 1.6 V–3.6 V	0	–	15	mA
			V_{BAT} = 0.8 V–1.6 V	0	–	25	mA
			V_{BAT} = 1.3 V–2.5 V	0	–	50	mA
			V_{BAT} = 2.5 V–3.6 V	0	–	50	mA
		T_A = –40 °C–85 °C	V_{BAT} = 1.8 V–2.5 V	0	–	50	mA
I_{LPK}	Inductor peak current			–	–	700	mA
I_Q	Quiescent current	Boost active mode		–	250	–	µA
		Boost sleep mode, I_{OUT} < 1 µA		–	25	–	µA
Reg_{LOAD}	Load regulation			–	–	10	%
Reg_{LINE}	Line regulation			–	–	10	%

Notes
34. Listed vsel options are characterized. Additional vsel options are valid and guaranteed by design.
35. The boost will start at all valid V_{BAT} conditions including down to V_{BAT} = 0.5 V.
36. If V_{BAT} is greater than or equal to V_{OUT} boost setting, then V_{OUT} will be less than V_{BAT} due to resistive losses in the boost circuit.

Figure 11-22. USBIO Output High Voltage and Current, GPIO Mode

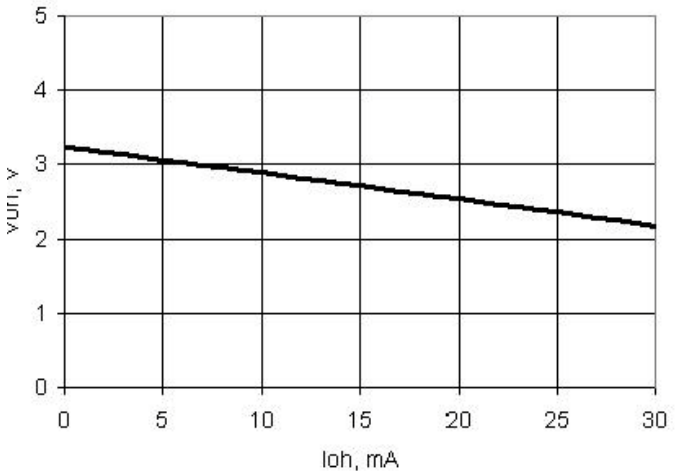


Figure 11-23. USBIO Output Low Voltage and Current, GPIO Mode

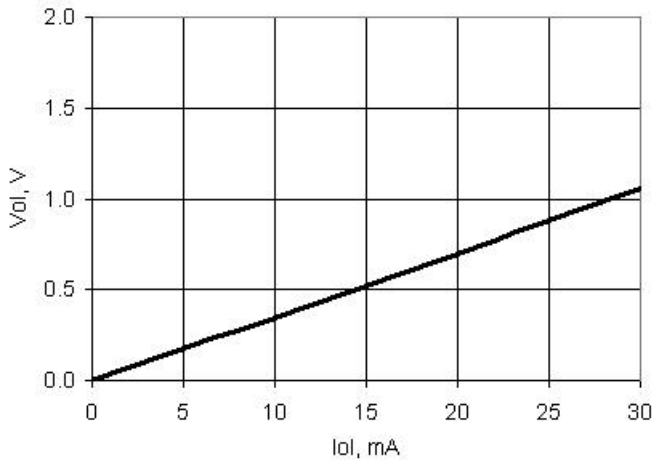


Table 11-15. USBIO AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
Tdrate	Full-speed data rate average bit rate		12 – 0.25%	12	12 + 0.25%	MHz
Tjr1	Receiver data jitter tolerance to next transition		–8	–	8	ns
Tjr2	Receiver data jitter tolerance to pair transition		–5	–	5	ns
Tdj1	Driver differential jitter to next transition		–3.5	–	3.5	ns
Tdj2	Driver differential jitter to pair transition		–4	–	4	ns
Tfdeop	Source jitter for differential transition to SE0 transition		–2	–	5	ns
Tfeopt	Source SE0 interval of EOP		160	–	175	ns
Tfeopr	Receiver SE0 interval of EOP		82	–	–	ns
Tfst	Width of SE0 interval during differential transition		–	–	14	ns
Fgpio_out	GPIO mode output operating frequency	$3\ V \le V_{DDD} \le 5.5\ V$	–	–	20	MHz
		$V_{DDD} = 1.71\ V$	–	–	6	MHz
Tr_gpio	Rise time, GPIO mode, 10%/90% V_{DDD}	$V_{DDD} > 3\ V$, 25 pF load	–	–	12	ns
		$V_{DDD} = 1.71\ V$, 25 pF load	–	–	40	ns
Tf_gpio	Fall time, GPIO mode, 90%/10% V_{DDD}	$V_{DDD} > 3\ V$, 25 pF load	–	–	12	ns
		$V_{DDD} = 1.71\ V$, 25 pF load	–	–	40	ns

Table 11-23. Delta-sigma ADC Sample Rates, Range = ±1.024 V

Resolution, Bits	Continuous		Multi-Sample		Multi-Sample Turbo	
	Min	Max	Min	Max	Min	Max
8	8000	384000	1911	91701	1829	87771
9	6400	307200	1543	74024	1489	71441
10	5566	267130	1348	64673	1307	62693
11	4741	227555	1154	55351	1123	53894
12	4000	192000	978	46900	956	45850
13	3283	157538	806	38641	791	37925
14	2783	133565	685	32855	674	32336
15	2371	113777	585	28054	577	27675
16	2000	48000	495	11861	489	11725
17	500	12000	124	2965	282	6766
18	125	3000	31	741	105	2513
19	16	375	4	93	15	357
20	8	187.5	2	46	8	183

Figure 11-33. Delta-sigma ADC IDD vs sps, Range = ±1.024 V, Continuous Sample Mode, Input Buffer Bypassed

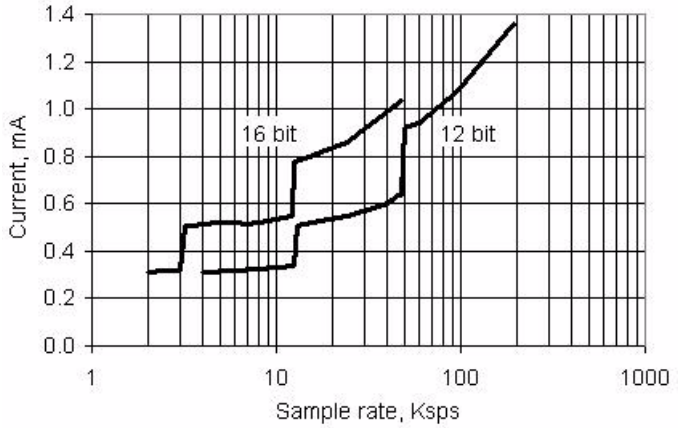


Figure 11-34. Delta-sigma ADC Noise Histogram, 1000 Samples, 20-Bit, 187 sps, Ext Ref, $V_{IN} = V_{REF}/2$, Range = ±1.024 V

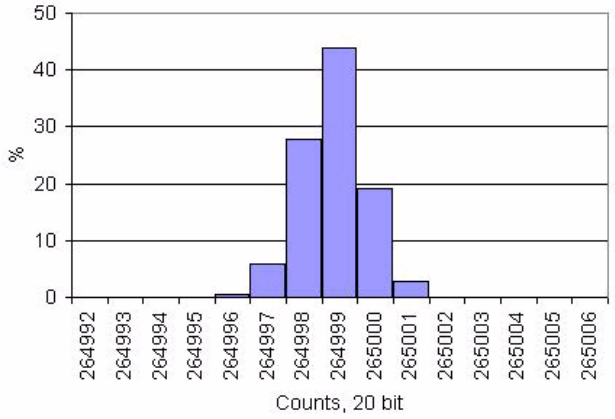


Figure 11-35. Delta-sigma ADC Noise Histogram, 1000 Samples, 16-bit, 48 ksps, Ext Ref, $V_{IN} = V_{REF}/2$, Range = ±1.024 V

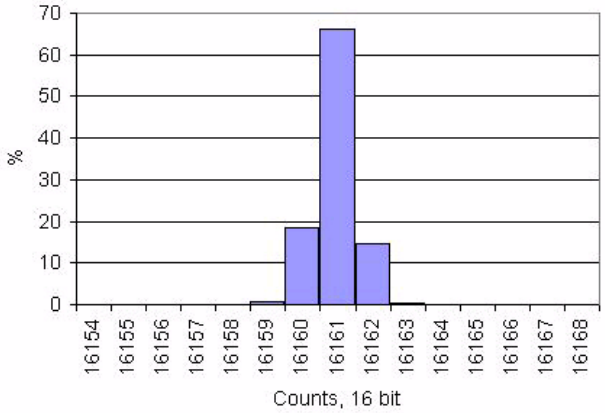


Figure 11-36. Delta-sigma ADC Noise Histogram, 1000 Samples, 16-bit, 48 ksps, Int Ref, $V_{IN} = V_{REF}/2$, Range = ±1.024 V

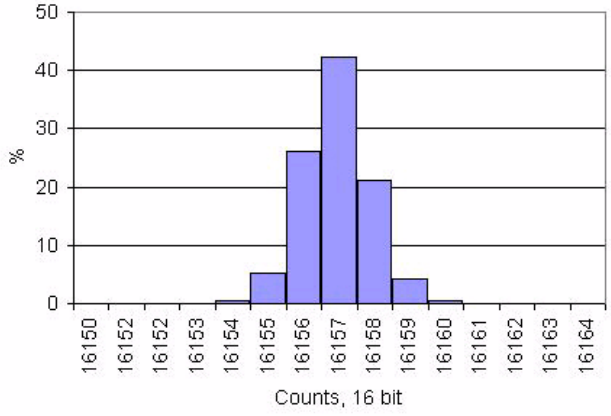


Table 11-32. IDAC DC Specifications *(continued)*

Parameter	Description	Conditions	Min	Typ	Max	Units
I_{DD}	Operating current, code = 0	Low speed mode, source mode, range = 31.875 µA	–	44	100	µA
		Low speed mode, source mode, range = 255 µA,	–	33	100	µA
		Low speed mode, source mode, range = 2.04 mA	–	33	100	µA
		Low speed mode, sink mode, range = 31.875 µA	–	36	100	µA
		Low speed mode, sink mode, range = 255 µA	–	33	100	µA
		Low speed mode, sink mode, range = 2.04 mA	–	33	100	µA
		High speed mode, source mode, range = 31.875 µA	–	310	500	µA
		High speed mode, source mode, range = 255 µA	–	305	500	µA
		High speed mode, source mode, range = 2.04 mA	–	305	500	µA
		High speed mode, sink mode, range = 31.875 µA	–	310	500	µA
		High speed mode, sink mode, range = 255 µA	–	300	500	µA
		High speed mode, sink mode, range = 2.04 mA	–	300	500	µA

Figure 11-41. IDAC INL vs Input Code, Range = 255 µA, Source Mode

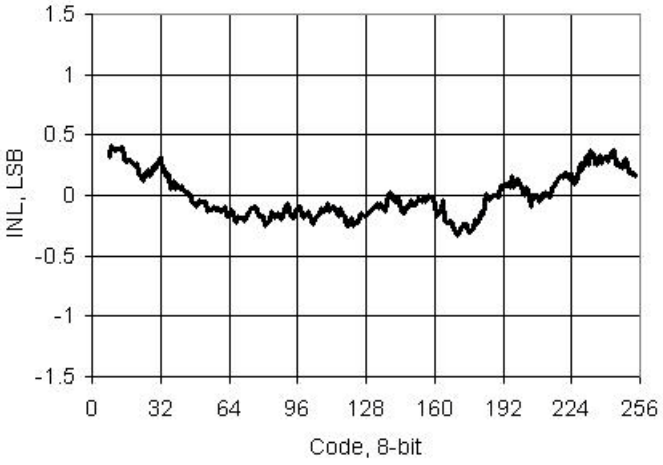
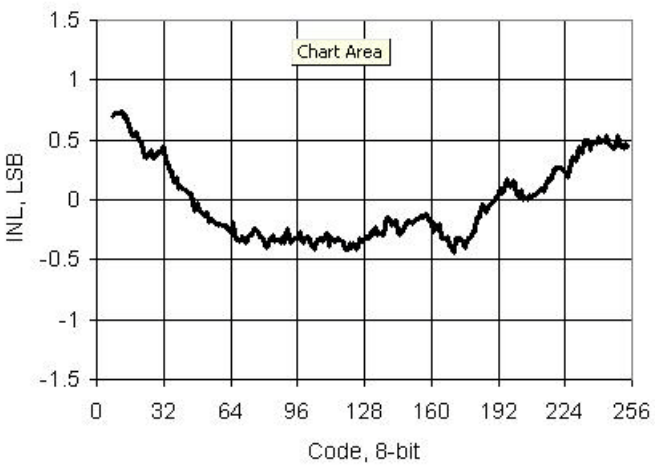


Figure 11-42. IDAC INL vs Input Code, Range = 255 µA, Sink Mode



11.6.7 USB

Table 11-57. USB DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{USB_5}	Device supply (V_{DDD}) for USB operation	USB configured, USB regulator enabled	4.35	–	5.25	V
$V_{USB\_3.3}$		USB configured, USB regulator bypassed	3.15	–	3.6	V
V_{USB_3}		USB configured, USB regulator bypassed[60]	2.85	–	3.6	V
$I_{USB\_Configured}$	Device supply current in device active mode, bus clock and IMO = 24 MHz	V_{DDD} = 5 V, F_{CPU} = 1.5 MHz	–	10	–	mA
		V_{DDD} = 3.3 V, F_{CPU} = 1.5 MHz	–	8	–	mA
$I_{USB\_Suspended}$	Device supply current in device sleep mode	V_{DDD} = 5 V, connected to USB host, PICU configured to wake on USB resume signal	–	0.5	–	mA
		V_{DDD} = 5 V, disconnected from USB host	–	0.3	–	mA
		V_{DDD} = 3.3 V, connected to USB host, PICU configured to wake on USB resume signal	–	0.5	–	mA
		V_{DDD} = 3.3 V, disconnected from USB host	–	0.3	–	mA

11.6.8 Universal Digital Blocks (UDBs)

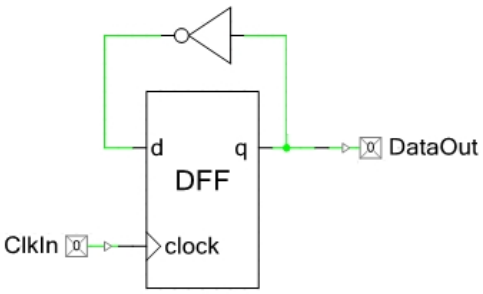
PSoC Creator provides a library of prebuilt and tested standard digital peripherals (UART, SPI, LIN, PRS, CRC, timer, counter, PWM, AND, OR, and so on) that are mapped to the UDB array. See the component data sheets in PSoC Creator for full AC/DC specifications, APIs, and example code.

Table 11-58. UDB AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
Datapath Performance						
F_{MAX_TIMER}	Maximum frequency of 16-bit timer in a UDB pair		–	–	67.01	MHz
F_{MAX_ADDER}	Maximum frequency of 16-bit adder in a UDB pair		–	–	67.01	MHz
F_{MAX_CRC}	Maximum frequency of 16-bit CRC/PRS in a UDB pair		–	–	67.01	MHz
PLD Performance						
F_{MAX_PLD}	Maximum frequency of a two-pass PLD function in a UDB pair		–	–	67.01	MHz
Clock to Output Performance						
t_{CLK_OUT}	Propagation delay for clock in to data out, see Figure 11-70.	25 °C, $V_{DDD} \geq 2.7$ V	–	20	25	ns
t_{CLK_OUT}	Propagation delay for clock in to data out, see Figure 11-70.	Worst-case placement, routing, and pin selection	–	–	55	ns

Note
60. Rise/fall time matching (TR) not guaranteed, see USB Driver AC Specifications on page 87.

Figure 11-70. Clock to Output Performance



11.7 Memory

Specifications are valid for –40 °C ≤ T_A ≤ 85 °C and T_J ≤ 100 °C, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

11.7.1 Flash

Table 11-59. Flash DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Erase and program voltage	V_{DDD} pin	1.71	–	5.5	V

Table 11-60. Flash AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
T_{WRITE}	Row write time (erase + program)		–	15	20	ms
T_{ERASE}	Row erase time		–	10	13	ms
	Row program time		–	5	7	ms
T_{BULK}	Bulk erase time (16 KB to 64 KB)		–	–	35	ms
	Sector erase time (8 KB to 16 KB)		–	–	15	ms
T_{PROG}	Total device programming time	No overhead[61]	–	1.5	2	seconds
	Flash data retention time, retention period measured from last erase cycle	Average ambient temp. T_A ≤ 55 °C, 100 K erase/program cycles	20	–	–	years
		Average ambient temp. T_A ≤ 85 °C, 10 K erase/program cycles	10	–	–	

Note
61. See PSoC® 3 Device Programming Specifications for a description of a low-overhead method of programming PSoC 3 flash.

11.8 PSoC System Resources

Specifications are valid for –40 °C ≤ T_A ≤ 85 °C and T_J ≤ 100 °C, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

11.8.1 POR with Brown Out

For brown out detect in regulated mode, V_{DDD} and V_{DDA} must be ≥ 2.0 V. Brown out detect is not available in externally regulated mode.

Table 11-69. Precise Low-Voltage Reset (PRES) with Brown Out DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
PRESR	Rising trip voltage	Factory trim	1.64	–	1.68	V
PRESF	Falling trip voltage		1.62	–	1.66	V

Table 11-70. Power On Reset (POR) with Brown Out AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
PRES_TR	Response time		–	–	0.5	µs
	V_{DDD}/V_{DDA} droop rate	Sleep mode	–	5	–	V/sec

11.8.2 Voltage Monitors

Table 11-71. Voltage Monitors DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
LVI	Trip voltage					
	LVI_A/D_SEL[3:0] = 0000b		1.68	1.73	1.77	V
	LVI_A/D_SEL[3:0] = 0001b		1.89	1.95	2.01	V
	LVI_A/D_SEL[3:0] = 0010b		2.14	2.20	2.27	V
	LVI_A/D_SEL[3:0] = 0011b		2.38	2.45	2.53	V
	LVI_A/D_SEL[3:0] = 0100b		2.62	2.71	2.79	V
	LVI_A/D_SEL[3:0] = 0101b		2.87	2.95	3.04	V
	LVI_A/D_SEL[3:0] = 0110b		3.11	3.21	3.31	V
	LVI_A/D_SEL[3:0] = 0111b		3.35	3.46	3.56	V
	LVI_A/D_SEL[3:0] = 1000b		3.59	3.70	3.81	V
	LVI_A/D_SEL[3:0] = 1001b		3.84	3.95	4.07	V
	LVI_A/D_SEL[3:0] = 1010b		4.08	4.20	4.33	V
	LVI_A/D_SEL[3:0] = 1011b		4.32	4.45	4.59	V
	LVI_A/D_SEL[3:0] = 1100b		4.56	4.70	4.84	V
	LVI_A/D_SEL[3:0] = 1101b		4.83	4.98	5.13	V
	LVI_A/D_SEL[3:0] = 1110b		5.05	5.21	5.37	V
	LVI_A/D_SEL[3:0] = 1111b		5.30	5.47	5.63	V
HVI	Trip voltage		5.57	5.75	5.92	V

Table 11-72. Voltage Monitors AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Response time[68]		–	–	1	µs

Note
68. Based on device characterization (Not production tested).

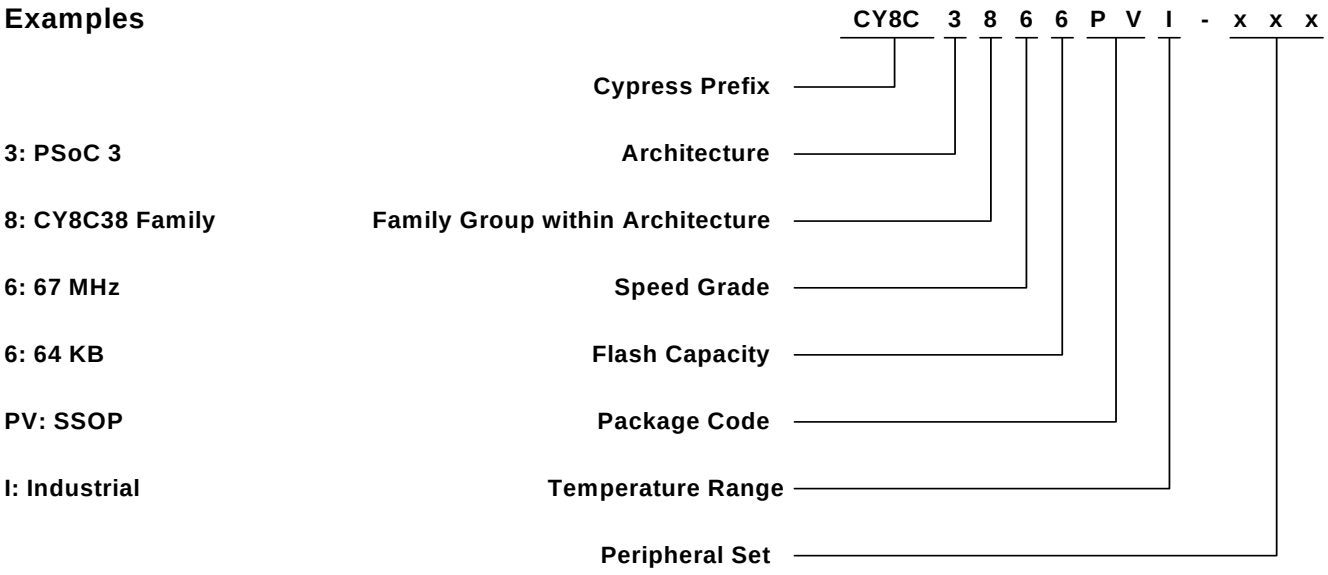
12.1 Part Numbering Conventions

PSoC 3 devices follow the part numbering convention described here. All fields are single character alphanumeric (0, 1, 2, …, 9, A, B, …, Z) unless stated otherwise.

CY8Cabcdefg-xxx

- a: Architecture
  - 3: PSoC 3
  - 5: PSoC 5
- b: Family group within architecture
  - 4: CY8C34 family
  - 6: CY8C36 family
  - 8: CY8C38 family
- c: Speed grade
  - 4: 48 MHz
  - 6: 67 MHz
- d: Flash capacity
  - 4: 16 KB
  - 5: 32 KB
  - 6: 64 KB
- ef: Package code
  - Two character alphanumeric
  - AX: TQFP
  - LT: QFN
  - PV: SSOP
  - FN: CSP
- g: Temperature range
  - C: commercial
  - I: industrial
  - A: automotive
- xxx: Peripheral set
  - Three character numeric
  - No meaning is associated with these three characters.

Examples



Tape and reel versions of these devices are available and are marked with a "T" at the end of the part number.

All devices in the PSoC 3 CY8C38 family comply to RoHS-6 specifications, demonstrating the commitment by Cypress to lead-free products. Lead (Pb) is an alloying element in solders that has resulted in environmental concerns due to potential toxicity. Cypress uses nickel-palladium-gold (NiPdAu) technology for the majority of leadframe-based packages.

A high-level review of the Cypress Pb-free position is available on our website. Specific package information is also available. Package Material Declaration data sheets (PMDDs) identify all substances contained within Cypress packages. PMDDs also confirm the absence of many banned substances. The information in the PMDDs will help Cypress customers plan for recycling or other “end of life” requirements.

Description Title: PSoC® 3: CY8C38 Family Datasheet Programmable System-on-Chip (PSoC®) *(continued)* Document Number: 001-11729				
Revision	**ECN**	**Submission Date**	**Orig. of Change**	**Description of Change**
*S	3259185	05/17/2011	MKEA	Added JTAG and SWD interface connection diagrams Updated $T_{JA}$and T_{JC} values in Table 13-1 Changed typ and max values for the TCVos parameter in Opamp DC specifications table. Updated Clocking subsystem diagram. Changed Vssd to V_{SSB} in the PSoC Power System diagram Updated Ordering information.
*T	3464258	12/14/2011	MKEA	Updated Analog Global specs Updated IDAC range Updated TIA section Modified VDDIO description in Section 3 Added note on Sleep and Hibernate modes in the Power Modes section Updated Boost Converter section Updated conditions for Inductive boost AC specs Added VDAC/IDAC noise graphs and specs Added pin capacitance specs for ECO pins Removed C_L from 32 kHz External Crystal DC Specs table. Added reference to AN54439 in Section 6.1.2.2 Deleted T_SWDO_hold row from the SWD Interface AC Specifications table Removed Pin 46 connections in "Example Schematic for 100-pin TQFP Part with Power Connections” Updated Active Mode IDD description in Table 11-2. Added I_{DDDR} and I_{DDAR} specs in Table 11-2. Replaced “total device program time” with T_{PROG} in Flash AC specs table Added I_{GPIO}, I_{SIO} and I_{USBIO} specs in Absolute Maximum Ratings Added conditions to I_{CC} spec in 32 kHz External Crystal DC Specs table. Updated TCV_{OS} value Removed Boost Efficiency vs V_{OUT} graph Updated boost graphs Updated min value of GPIO input edge rate Removed 3.4 Mbps in UDBs from I2C section Updated USBIO Block diagram; added USBIO drive mode description Updated Analog Interconnect diagram Changed max IMO startup time to 12 µs Added note for I_{IL} spec in USBIO DC specs table Updated GPIO Block diagram Updated voltage reference specs Added text explaining power supply ramp up in Section 11-4.