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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	67MHz
Connectivity	EBI/EMI, I ² C, LINbus, SPI, UART/USART
Peripherals	CapSense, DMA, LCD, POR, PWM, WDT
Number of I/O	62
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 5.5V
Data Converters	A/D 16x20b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c3866axi-206t

1. Architectural Overview

Introducing the CY8C38 family of ultra low-power, flash Programmable System-on-Chip (PSoC®) devices, part of a scalable 8-bit PSoC 3 and 32-bit PSoC 5 platform. The CY8C38 family provides configurable blocks of analog, digital, and interconnect circuitry around a CPU subsystem. The combination of a CPU with a flexible analog subsystem, digital subsystem, routing, and I/O enables a high level of integration in a wide variety of consumer, industrial, and medical applications.

Figure 1-1. Simplified Block Diagram

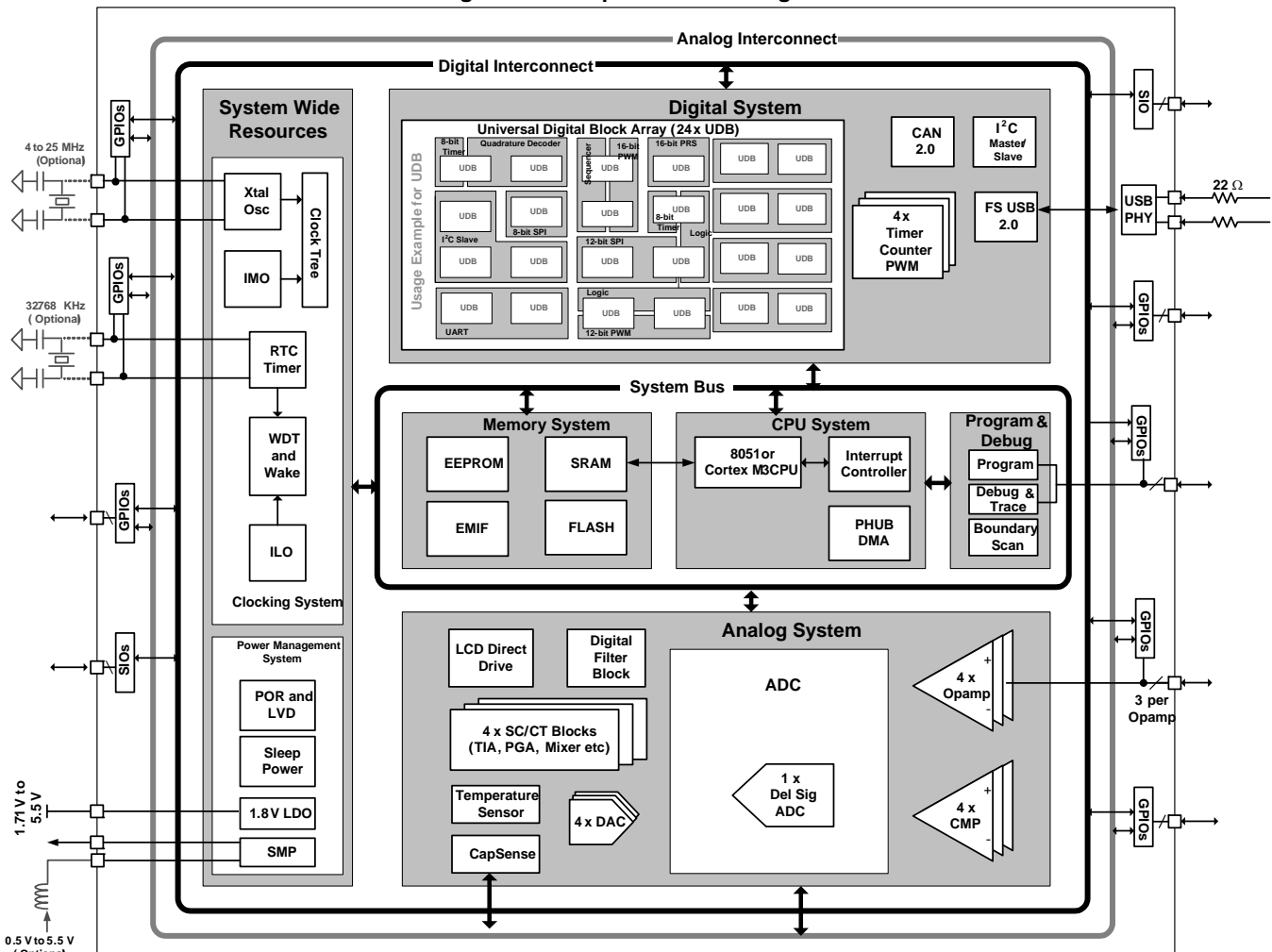


Figure 1-1 illustrates the major components of the CY8C38 family. They are:

- 8051 CPU subsystem
- Nonvolatile subsystem
- Programming, debug, and test subsystem
- Inputs and outputs
- Clocking
- Power
- Digital subsystem
- Analog subsystem

PSoC's digital subsystem provides half of its unique configurability. It connects a digital signal from any peripheral to any pin through the digital system interconnect (DSI). It also provides functional flexibility through an array of small, fast, low-power UDBs. PSoC Creator provides a library of prebuilt and tested standard digital peripherals (UART, SPI, LIN, PRS, CRC, timer, counter, PWM, AND, OR, and so on) that are mapped to the UDB array. You can also easily create a digital circuit using boolean primitives by means of graphical design entry. Each UDB contains programmable array logic (PAL)/programmable logic device (PLD) functionality, together with a small state machine engine to support a wide variety of peripherals.

In addition to the flexibility of the UDB array, PSoC also provides configurable digital blocks targeted at specific functions. For the CY8C38 family these blocks can include four 16-bit timers, counters, and PWM blocks; I²C slave, master, and multimaster; FS USB; and Full CAN 2.0b.

Figure 2-3. 48-pin SSOP Part Pinout

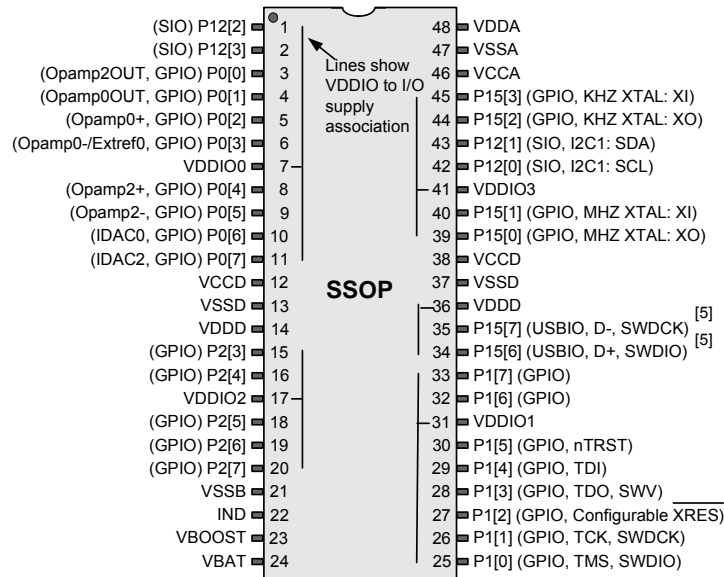
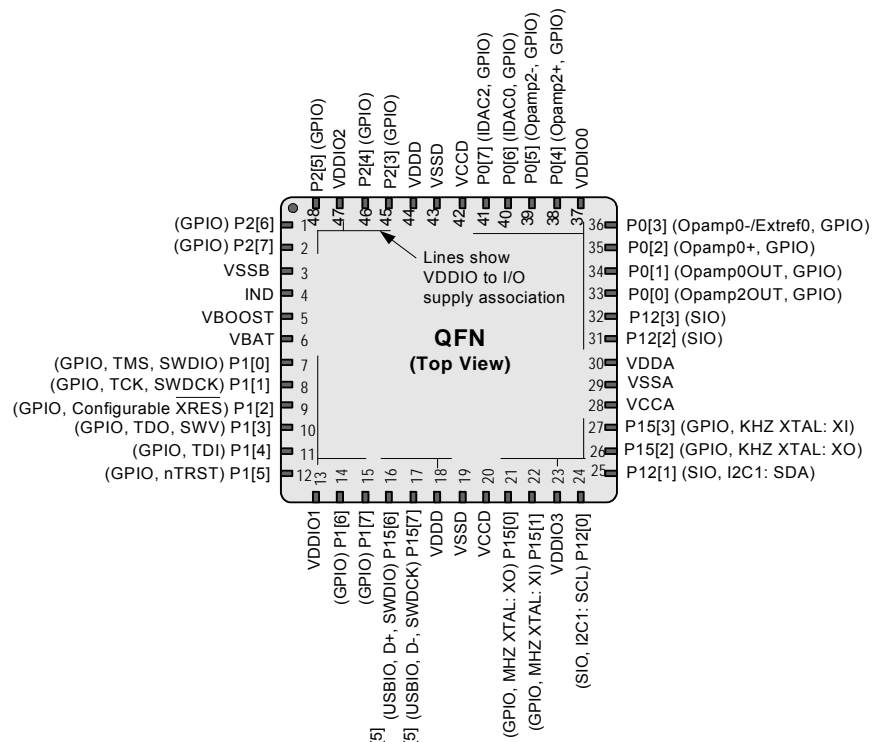


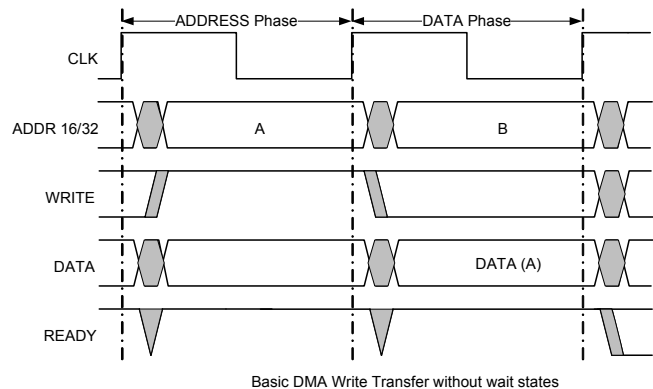
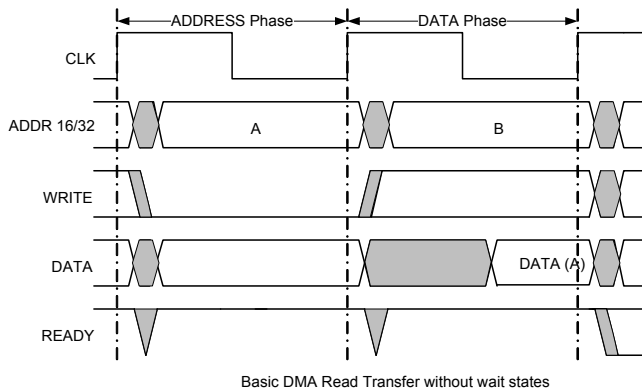
Figure 2-4. 48-pin QFN Part Pinout^[6]



Notes

5. Pins are Do Not Use (DNU) on devices without USB. The pin must be left floating.
6. The center pad on the QFN package should be connected to digital ground (VSSD) for best mechanical, thermal, and electrical performance. If not connected to ground, it should be electrically floated and not connected to any other signal. For more information, see [AN72845](#), Design Guidelines for QFN Devices.

Figure 4-1. DMA Timing Diagram



4.4.4.2 Auto Repeat DMA

Auto repeat DMA is typically used when a static pattern is repetitively read from system memory and written to a peripheral. This is done with a single TD that chains to itself.

4.4.4.3 Ping Pong DMA

A ping pong DMA case uses double buffering to allow one buffer to be filled by one client while another client is consuming the data previously received in the other buffer. In its simplest form, this is done by chaining two TDs together so that each TD calls the opposite TD when complete.

4.4.4.4 Circular DMA

Circular DMA is similar to ping pong DMA except it contains more than two buffers. In this case there are multiple TDs; after the last TD is complete it chains back to the first TD.

4.4.4.5 Scatter Gather DMA

In the case of scatter gather DMA, there are multiple noncontiguous sources or destinations that are required to effectively carry out an overall DMA transaction. For example, a packet may need to be transmitted off of the device and the packet elements, including the header, payload, and trailer, exist in various noncontiguous locations in memory. Scatter gather DMA allows the segments to be concatenated together by using multiple TDs in a chain. The chain gathers the data from the multiple locations. A similar concept applies for the reception of data onto the device. Certain parts of the received data may need to be scattered to various locations in memory for software processing convenience. Each TD in the chain specifies the location for each discrete element in the chain.

4.4.4.6 Packet Queuing DMA

Packet queuing DMA is similar to scatter gather DMA but specifically refers to packet protocols. With these protocols, there may be separate configuration, data, and status phases associated with sending or receiving a packet.

For instance, to transmit a packet, a memory mapped configuration register can be written inside a peripheral, specifying the overall length of the ensuing data phase. The CPU can set up this configuration information anywhere in system memory and copy it with a simple TD to the peripheral. After the configuration phase, a data phase TD (or a series of data phase TDs) can begin (potentially using scatter gather). When the data

phase TD(s) finish, a status phase TD can be invoked that reads some memory mapped status information from the peripheral and copies it to a location in system memory specified by the CPU for later inspection. Multiple sets of configuration, data, and status phase 'subchains' can be strung together to create larger chains that transmit multiple packets in this way. A similar concept exists in the opposite direction to receive the packets.

4.4.4.7 Nested DMA

One TD may modify another TD, as the TD configuration space is memory mapped similar to any other peripheral. For example, a first TD loads a second TD's configuration and then calls the second TD. The second TD moves data as required by the application. When complete, the second TD calls the first TD, which again updates the second TD's configuration. This process repeats as often as necessary.

4.5 Interrupt Controller

The interrupt controller provides a mechanism for hardware resources to change program execution to a new address, independent of the current task being executed by the main code. The interrupt controller provides enhanced features not found on original 8051 interrupt controllers:

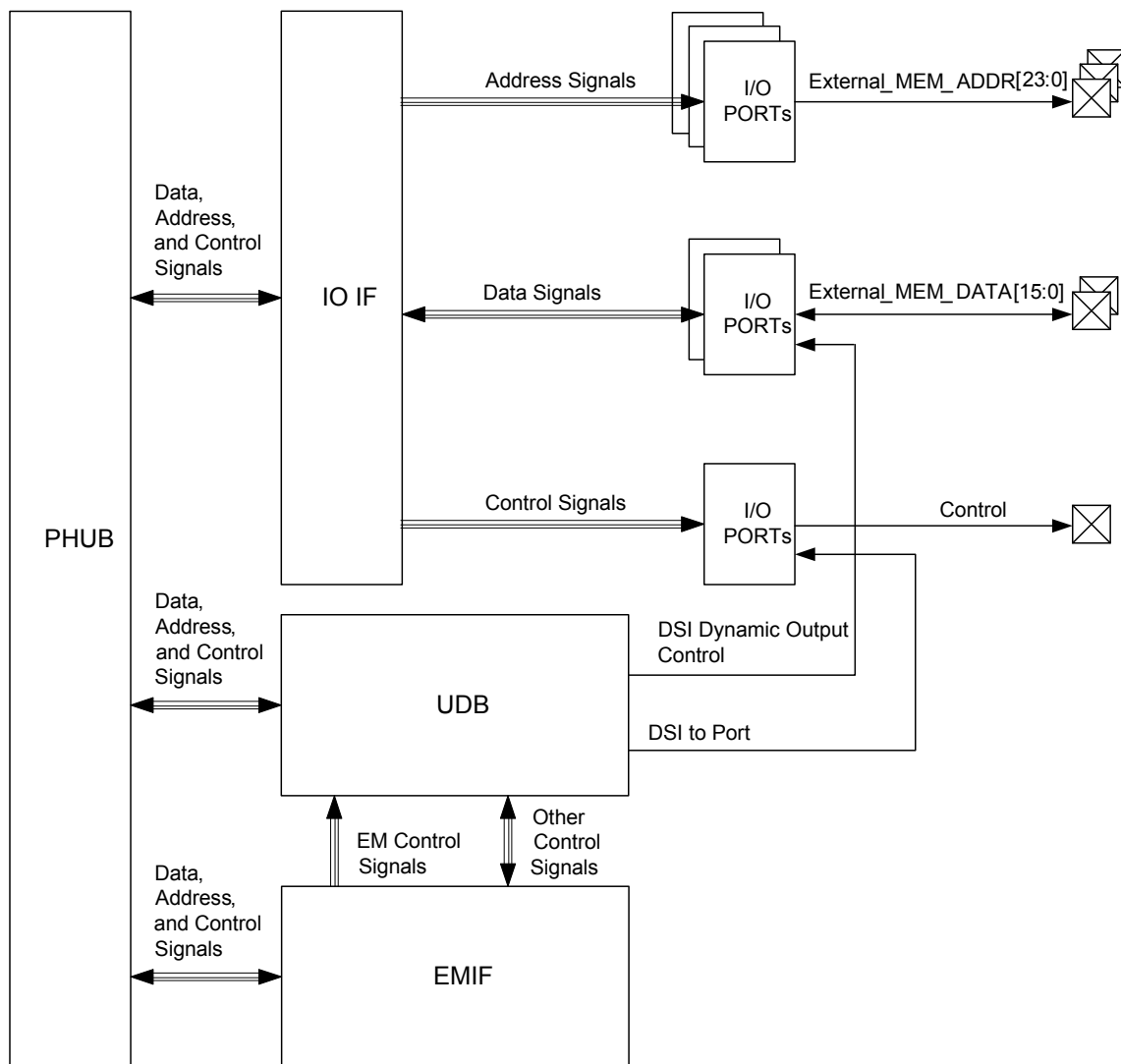
- Thirty-two interrupt vectors
- Jumps directly to ISR anywhere in code space with dynamic vector addresses
- Multiple sources for each vector
- Flexible interrupt to vector matching
- Each interrupt vector is independently enabled or disabled
- Each interrupt can be dynamically assigned one of eight priorities
- Eight level nestable interrupts
- Multiple I/O interrupt vectors
- Software can send interrupts
- Software can clear pending interrupts

Figure 4-2 on page 20 represents typical flow of events when an interrupt triggered. Figure 4-3 on page 21 shows the interrupt structure and priority polling.

5.6 External Memory Interface

CY8C38 provides an EMIF for connecting to external memory devices. The connection allows read and write accesses to external memories. The EMIF operates in conjunction with UDBs, I/O ports, and other hardware to generate external memory address and control signals. At 33 MHz, each memory access cycle takes four bus clock cycles. Figure 5-1 is the EMIF block diagram. The EMIF supports synchronous and asynchronous memories. The CY8C38 supports only one type of external memory device at a time. External memory can be accessed through the 8051 xdata space; up to 24 address bits can be used. See “xdata Space” section on page 27. The memory can be 8 or 16 bits wide.

Figure 5-1. EMIF Block Diagram



6.4 I/O System and Routing

PSoC I/Os are extremely flexible. Every GPIO has analog and digital I/O capability. All I/Os have a large number of drive modes, which are set at POR. PSoC also provides up to four individual I/O voltage domains through the VDDIO pins.

There are two types of I/O pins on every device; those with USB provide a third type. Both GPIO and SIO provide similar digital functionality. The primary differences are their analog capability and drive strength. Devices that include USB also provide two USBIO pins that support specific USB functionality as well as limited GPIO capability.

All I/O pins are available for use as digital inputs and outputs for both the CPU and digital peripherals. In addition, all I/O pins can generate an interrupt. The flexible and advanced capabilities of the PSoC I/O, combined with any signal to any pin routability, greatly simplify circuit design and board layout. All GPIO pins can be used for analog input, CapSense^[13], and LCD segment drive, while SIO pins are used for voltages in excess of VDDA and for programmable output voltages.

- Features supported by both GPIO and SIO:
 - User programmable port reset state
 - Separate I/O supplies and voltages for up to four groups of I/O
 - Digital peripherals use DSI to connect the pins
 - Input or output or both for CPU and DMA
 - Eight drive modes
 - Every pin can be an interrupt source configured as rising edge, falling edge or both edges. If required, level sensitive interrupts are supported through the DSI
 - Dedicated port interrupt vector for each port

- Slew rate controlled digital output drive mode
- Access port control and configuration registers on either port basis or pin basis
- Separate port read (PS) and write (DR) data registers to avoid read modify write errors
- Special functionality on a pin by pin basis
- Additional features only provided on the GPIO pins:
 - LCD segment drive on LCD equipped devices
 - CapSense^[13]
 - Analog input and output capability
 - Continuous 100 μ A clamp current capability
 - Standard drive strength down to 1.7 V
- Additional features only provided on SIO pins:
 - Higher drive strength than GPIO
 - Hot swap capability (5 V tolerance at any operating V_{DD})
 - Programmable and regulated high input and output drive levels down to 1.2 V
 - No analog input, CapSense, or LCD capability
 - Over voltage tolerance up to 5.5 V
 - SIO can act as a general purpose analog comparator
- USBIO features:
 - Full speed USB 2.0 compliant I/O
 - Highest drive strength for general purpose use
 - Input, output, or both for CPU and DMA
 - Input, output, or both for digital peripherals
 - Digital output (CMOS) drive mode
 - Each pin can be an interrupt source configured as rising edge, falling edge, or both edges

Note

13. GPIOs with opamp outputs are not recommended for use with CapSense.

6.4.5 Pin Interrupts

All GPIO and SIO pins are able to generate interrupts to the system. All eight pins in each port interface to their own Port Interrupt Control Unit (PICU) and associated interrupt vector. Each pin of the port is independently configurable to detect rising edge, falling edge, both edge interrupts, or to not generate an interrupt.

Depending on the configured mode for each pin, each time an interrupt event occurs on a pin, its corresponding status bit of the interrupt status register is set to '1' and an interrupt request is sent to the interrupt controller. Each PICU has its own interrupt vector in the interrupt controller and the pin status register providing easy determination of the interrupt source down to the pin level.

Port pin interrupts remain active in all sleep modes allowing the PSoC device to wake from an externally generated interrupt. While level sensitive interrupts are not directly supported; UDB provide this functionality to the system when needed.

6.4.6 Input Buffer Mode

GPIO and SIO input buffers can be configured at the port level for the default CMOS input thresholds or the optional LVTTTL input thresholds. All input buffers incorporate Schmitt triggers for input hysteresis. Additionally, individual pin input buffers can be disabled in any drive mode.

6.4.7 I/O Power Supplies

Up to four I/O pin power supplies are provided depending on the device and package. Each I/O supply must be less than or equal to the voltage on the chip's analog (VDDA) pin. This feature allows users to provide different I/O voltage levels for different pins on the device. Refer to the specific device package pinout to determine VDDIO capability for a given port and pin. The SIO port pins support an additional regulated high output capability, as described in [Adjustable Output Level](#).

6.4.8 Analog Connections

These connections apply only to GPIO pins. All GPIO pins may be used as analog inputs or outputs. The analog voltage present on the pin must not exceed the VDDIO supply voltage to which the GPIO belongs. Each GPIO may connect to one of the analog global busses or to one of the analog mux buses to connect any pin to any internal analog resource such as ADC or comparators. In addition, select pins provide direct connections to specific analog features such as the high current DACs or uncommitted opamps.

6.4.9 CapSense

This section applies only to GPIO pins. All GPIO pins may be used to create CapSense buttons and sliders^[15]. See the ["CapSense"](#) section on page 63 for more information.

6.4.10 LCD Segment Drive

This section applies only to GPIO pins. All GPIO pins may be used to generate Segment and Common drive signals for direct glass drive of LCD glass. See the ["LCD Direct Drive"](#) section on page 62 for details.

6.4.11 Adjustable Output Level

This section applies only to SIO pins. SIO port pins support the ability to provide a regulated high output level for interface to external signals that are lower in voltage than the SIO's respective VDDIO. SIO pins are individually configurable to output either the standard VDDIO level or the regulated output, which is based on an internally generated reference. Typically a voltage DAC (VDAC) is used to generate the reference (see [Figure 6-13](#)). The ["DAC"](#) section on page 64 has more details on VDAC use and reference routing to the SIO pins. Resistive pullup and pull-down drive modes are not available with SIO in regulated output mode.

6.4.12 Adjustable Input Level

This section applies only to SIO pins. SIO pins by default support the standard CMOS and LVTTTL input levels but also support a differential mode with programmable levels. SIO pins are grouped into pairs. Each pair shares a reference generator block which is used to set the digital input buffer reference level for interface to external signals that differ in voltage from VDDIO. The reference sets the pins voltage threshold for a high logic level (see [Figure 6-13](#)). Available input thresholds are:

- $0.5 \times \text{VDDIO}$
- $0.4 \times \text{VDDIO}$
- $0.5 \times V_{\text{REF}}$
- V_{REF}

Typically a voltage DAC (VDAC) generates the V_{REF} reference. ["DAC"](#) section on page 64 has more details on VDAC use and reference routing to the SIO pins.

Note

15. GPIOs with opamp outputs are not recommended for use with CapSense.

7. Digital Subsystem

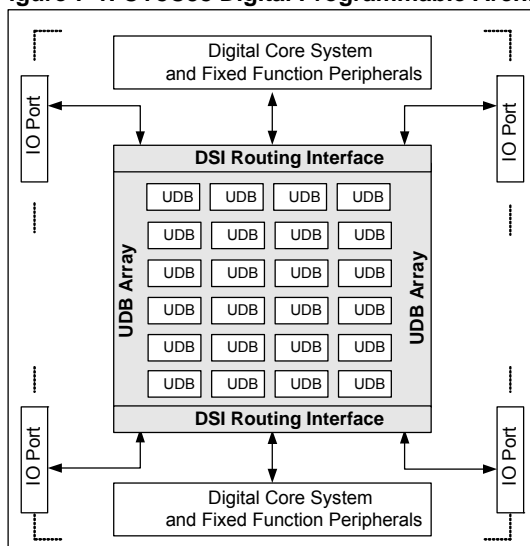
The digital programmable system creates application specific combinations of both standard and advanced digital peripherals and custom logic functions. These peripherals and logic are then interconnected to each other and to any pin on the device, providing a high level of design flexibility and IP security.

The features of the digital programmable system are outlined here to provide an overview of capabilities and architecture. You do not need to interact directly with the programmable digital system at the hardware and register level. PSoC Creator provides a high level schematic capture graphical interface to automatically place and route resources similar to PLDs.

The main components of the digital programmable system are:

- **UDB** – These form the core functionality of the digital programmable system. UDBs are a collection of uncommitted logic (PLD) and structural logic (Datapath) optimized to create all common embedded peripherals and customized functionality that are application or design specific.
- **Universal digital block array** – UDB blocks are arrayed within a matrix of programmable interconnect. The UDB array structure is homogeneous and allows for flexible mapping of digital functions onto the array. The array supports extensive and flexible routing interconnects between UDBs and the Digital System Interconnect.
- **Digital system interconnect (DSI)** – Digital signals from UDBs, fixed function peripherals, I/O pins, interrupts, DMA, and other system core signals are attached to the digital system interconnect to implement full featured device connectivity. The DSI allows any digital function to any pin or other feature routability when used with the universal digital block array.

Figure 7-1. CY8C38 Digital Programmable Architecture



7.1 Example Peripherals

The flexibility of the CY8C38 family's UDBs and analog blocks allow the user to create a wide range of components (peripherals). The most common peripherals were built and characterized by Cypress and are shown in the PSoC Creator component catalog, however, users may also create their own custom components using PSoC Creator. Using PSoC Creator, users may also create their own components for reuse within their organization, for example sensor interfaces, proprietary algorithms, and display interfaces.

The number of components available through PSoC Creator is too numerous to list in the data sheet, and the list is always growing. An example of a component available for use in CY8C38 family, but, not explicitly called out in this data sheet is the UART component.

7.1.1 Example Digital Components

The following is a sample of the digital components available in PSoC Creator for the CY8C38 family. The exact amount of hardware resources (UDBs, routing, RAM, flash) used by a component varies with the features selected in PSoC Creator for the component.

- **Communications**
 - I²C
 - UART
 - SPI
- **Functions**
 - EMIF
 - PWMs
 - Timers
 - Counters
- **Logic**
 - NOT
 - OR
 - XOR
 - AND

7.1.2 Example Analog Components

The following is a sample of the analog components available in PSoC Creator for the CY8C38 family. The exact amount of hardware resources (SC/CT blocks, routing, RAM, flash) used by a component varies with the features selected in PSoC Creator for the component.

- **Amplifiers**
 - TIA
 - PGA
 - opamp
- **ADC**
 - Delta-sigma
- **DACs**
 - Current
 - Voltage
 - PWM
- **Comparators**
- **Mixers**

7.8 I²C

PSoC includes a single fixed-function I²C peripheral. Additional I²C interfaces can be instantiated using Universal Digital Blocks (UDBs) in PSoC Creator, as required.

The I²C peripheral provides a synchronous two-wire interface designed to interface the PSoC device with a two-wire I²C serial communication bus. It is compatible^[16] with I²C Standard-mode, Fast-mode, and Fast-mode Plus devices as defined in the NXP I²C-bus specification and user manual (UM10204). The I²C bus I/O may be implemented with GPIO or SIO in open-drain modes.

To eliminate the need for excessive CPU intervention and overhead, I²C specific support is provided for status detection and generation of framing bits. I²C operates as a slave, a master, or multimaster (Slave and Master)^[17]. In slave mode, the unit always listens for a start condition to begin sending or receiving data. Master mode supplies the ability to generate the Start and Stop conditions and initiate transactions. Multimaster mode provides clock synchronization and arbitration to allow multiple masters on the same bus. If Master mode is enabled and Slave mode is not enabled, the block does not generate interrupts on externally generated Start conditions. I²C interfaces through DSI routing and allows direct connections to any GPIO or SIO pins.

I²C provides hardware address detect of a 7-bit address without CPU intervention. Additionally the device can wake from low-power modes on a 7-bit hardware address match. If wakeup

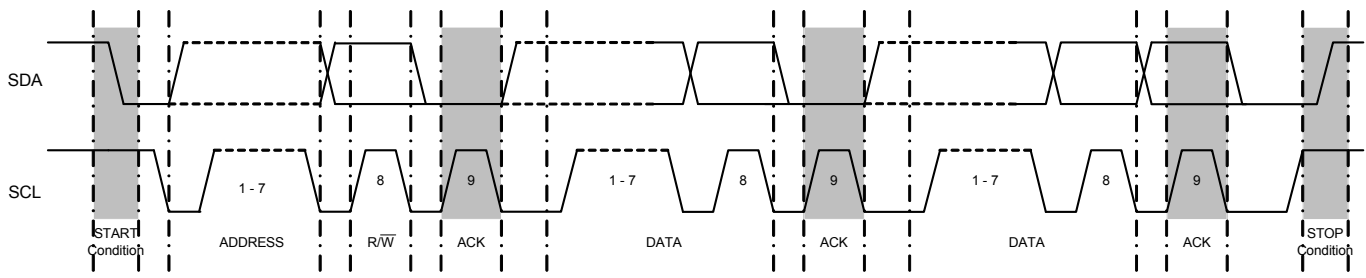
functionality is required, I²C pin connections are limited to one of two specific pairs of SIO pins. See descriptions of SCL and SDA pins in [Pin Descriptions](#) on page 12.

I²C features include:

- Slave and master, transmitter, and receiver operation
- Byte processing for low CPU overhead
- Interrupt or polling CPU interface
- Support for bus speeds up to 1 Mbps
- 7 or 10-bit addressing (10-bit addressing requires firmware support)
- SMBus operation (through firmware support - SMBus supported in hardware in UDBs)
- 7-bit hardware address compare
- Wake from low-power modes on address match
- Glitch filtering (active and alternate-active modes only)

Data transfers follow the format shown in [Figure 7-18](#). After the START condition (S), a slave address is sent. This address is 7 bits long followed by an eighth bit which is a data direction bit (R/W) - a 'zero' indicates a transmission (WRITE), a 'one' indicates a request for data (READ). A data transfer is always terminated by a STOP condition (P) generated by the master.

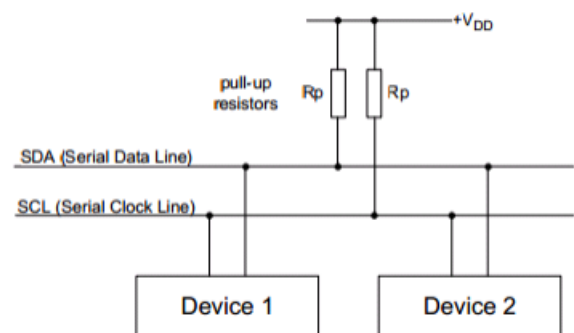
Figure 7-18. I²C Complete Transfer Timing



7.8.1 External Electrical Connections

As [Figure 7-19](#) shows, the I²C bus requires external pull-up resistors (R_p). These resistors are primarily determined by the supply voltage, bus speed, and bus capacitance. For detailed information on how to calculate the optimum pull-up resistor value for your design, we recommend using the UM10204 I²C-bus specification and user manual Rev 6, or newer, available from the NXP website at www.nxp.com.

Figure 7-19. Connection of Devices to the I²C Bus



Notes

16. The I²C peripheral is non-compliant with the NXP I²C specification in the following areas: analog glitch filter, I/O V_{OL}/I_{OL} , I/O hysteresis. The I²C Block has a digital glitch filter (not available in sleep mode). The Fast-mode minimum fall-time specification can be met by setting the I/Os to slow speed mode. See the I/O Electrical Specifications in "Inputs and Outputs" section on page 80 for details.
17. Fixed-block I²C does not support undefined bus conditions, nor does it support Repeated Start in Slave mode. These conditions should be avoided, or the UDB-based I²C component should be used instead.

The opamp and resistor array is programmable to perform various analog functions including

- Naked operational amplifier – Continuous mode
- Unity-gain buffer – Continuous mode
- PGA – Continuous mode
- Transimpedance amplifier (TIA) – Continuous mode
- Up/down mixer – Continuous mode
- Sample and hold mixer (NRZ S/H) – Switched cap mode
- First order analog to digital modulator – Switched cap mode

8.5.1 Naked Opamp

The Naked Opamp presents both inputs and the output for connection to internal or external signals. The opamp has a unity gain bandwidth greater than 6.0 MHz and output drive current up to 650 μ A. This is sufficient for buffering internal signals (such as DAC outputs) and driving external loads greater than 7.5 kohms.

8.5.2 Unity Gain

The Unity Gain buffer is a Naked Opamp with the output directly connected to the inverting input for a gain of 1.00. It has a –3 dB bandwidth greater than 6.0 MHz.

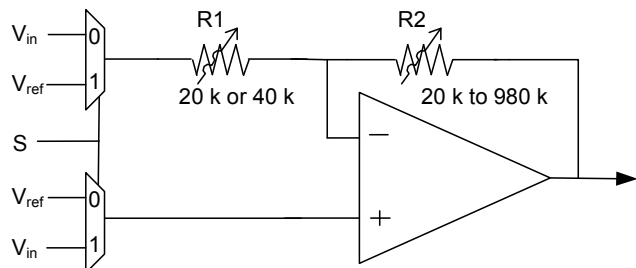
8.5.3 PGA

The PGA amplifies an external or internal signal. The PGA can be configured to operate in inverting mode or noninverting mode. The PGA function may be configured for both positive and negative gains as high as 50 and 49 respectively. The gain is adjusted by changing the values of R1 and R2 as illustrated in Figure 8-8. The schematic in Figure 8-8 shows the configuration and possible resistor settings for the PGA. The gain is switched from inverting and non inverting by changing the shared select value of the both the input muxes. The bandwidth for each gain case is listed in Table 8-3.

Table 8-3. Bandwidth

Gain	Bandwidth
1	6.0 MHz
24	340 kHz
48	220 kHz
50	215 kHz

Figure 8-8. PGA Resistor Settings



The PGA is used in applications where the input signal may not be large enough to achieve the desired resolution in the ADC, or dynamic range of another SC/CT block such as a mixer. The gain is adjustable at runtime, including changing the gain of the PGA prior to each ADC sample.

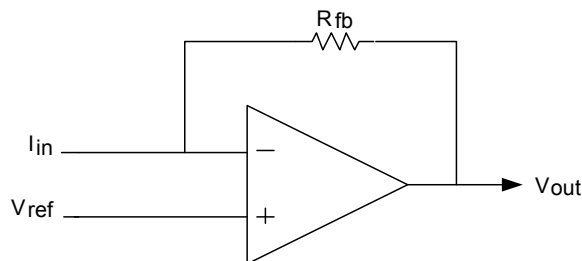
8.5.4 TIA

The Transimpedance Amplifier (TIA) converts an internal or external current to an output voltage. The TIA uses an internal feedback resistor in a continuous time configuration to convert input current to output voltage. For an input current I_{in} , the output voltage is $V_{REF} - I_{in} \times R_{fb}$, where V_{REF} is the value placed on the non inverting input. The feedback resistor R_{fb} is programmable between 20 K Ω and 1 M Ω through a configuration register. Table 8-4 shows the possible values of R_{fb} and associated configuration settings.

Table 8-4. Feedback Resistor Settings

Configuration Word	Nominal R_{fb} (K Ω)
000b	20
001b	30
010b	40
011b	60
100b	120
101b	250
110b	500
111b	1000

Figure 8-9. Continuous Time TIA Schematic



The TIA configuration is used for applications where an external sensor's output is current as a function of some type of stimulus such as temperature, light, magnetic flux etc. In a common application, the voltage DAC output can be connected to the V_{REF} TIA input to allow calibration of the external sensor bias current by adjusting the voltage DAC output voltage.

8.6 LCD Direct Drive

The PSoC LCD driver system is a highly configurable peripheral designed to allow PSoC to directly drive a broad range of LCD glass. All voltages are generated on chip, eliminating the need for external components. With a high multiplex ratio of up to 1/16, the CY8C38 family LCD driver system can drive a maximum of 736 segments. The PSoC LCD driver module was also designed with the conservative power budget of portable devices in mind, enabling different LCD drive modes and power down modes to conserve power.

Table 11-7. Recommended External Components for Boost Circuit

Parameter	Description	Conditions	Min	Typ	Max	Units
L _{BOOST}	Boost inductor	4.7 μ H nominal	3.7	4.7	5.7	μ H
		10 μ H nominal	8.0	10.0	12.0	μ H
		22 μ H nominal	17.0	22.0	27.0	μ H
C _{BOOST}	Total capacitance sum of V _{DD} , V _{DDA} , V _{DDIO} ^[37]		17.0	26.0	31.0	μ F
C _{BAT}	Battery filter capacitor		17.0	22.0	27.0	μ F
I _F	Schottky diode average forward current		1.0	–	–	A
V _R	Schottky reverse voltage		20.0	–	–	V

Figure 11-8. T_A range over V_{BAT} and V_{OUT}

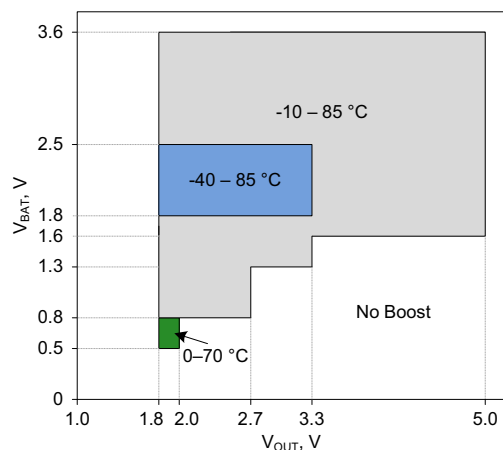


Figure 11-9. I_{OUT} range over V_{BAT} and V_{OUT}

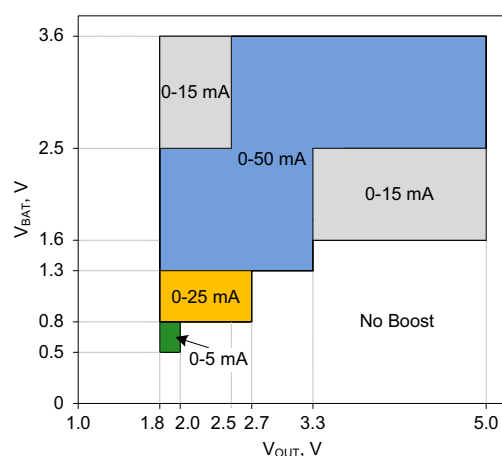
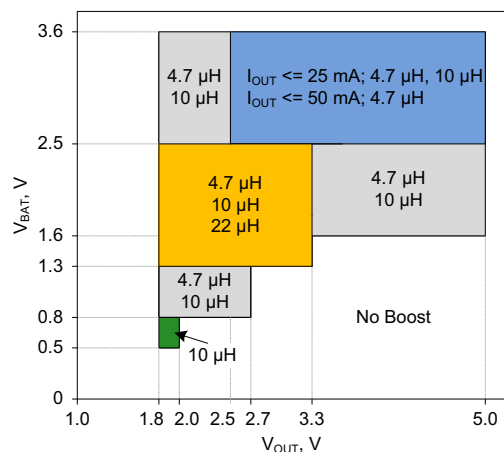


Figure 11-10. L_{BOOST} values over V_{BAT} and V_{OUT}



Note

37. Based on device characterization (Not production tested).

Figure 11-25. Opamp Voffset Histogram, 3388 samples/847 parts, 25 °C, $V_{DDA} = 5\text{ V}$

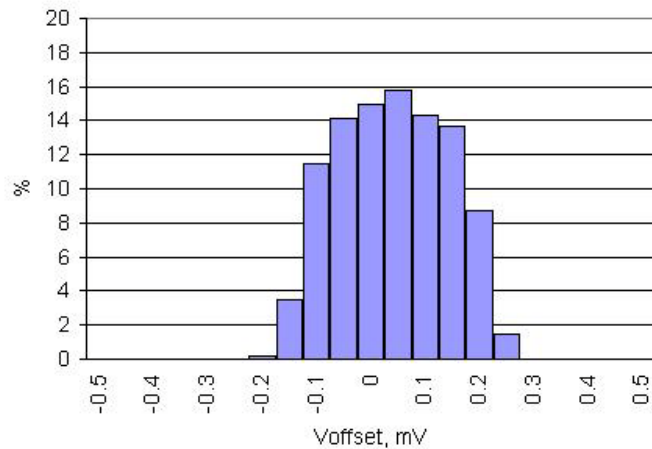


Figure 11-26. Opamp Voffset vs Temperature, $V_{DDA} = 5\text{ V}$

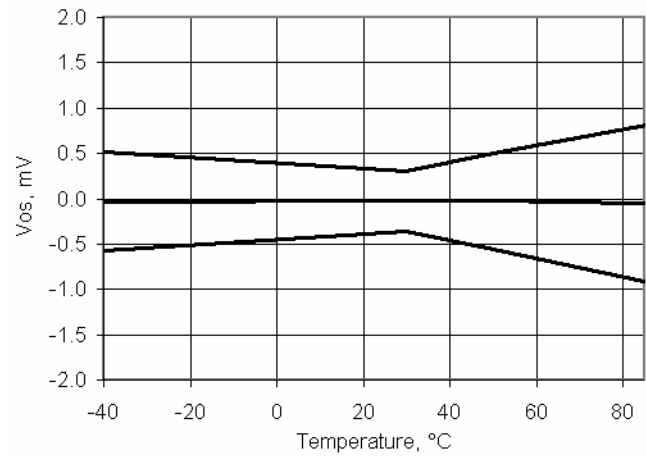


Figure 11-27. Opamp Voffset vs Vcommon and V_{DDA} , 25 °C

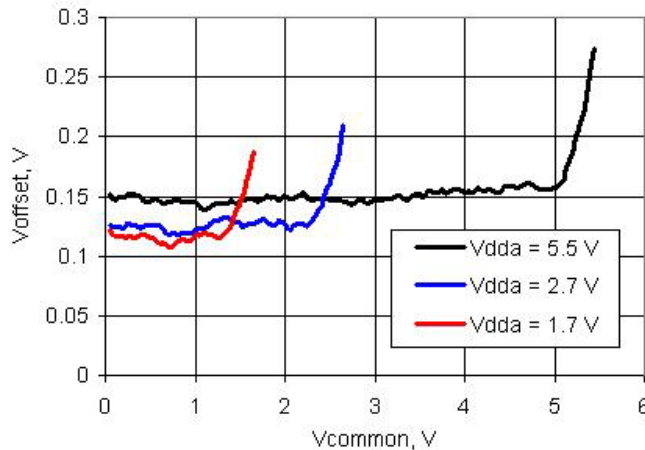


Figure 11-28. Opamp Output Voltage vs Load Current and Temperature, High Power Mode, 25 °C, $V_{DDA} = 2.7\text{ V}$

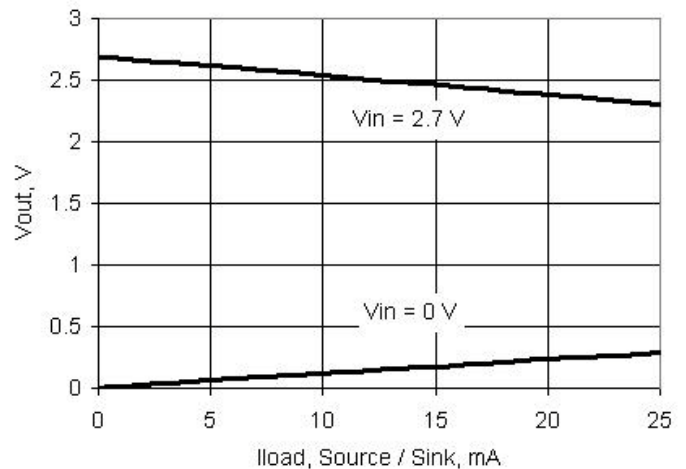


Figure 11-29. Opamp Operating Current vs V_{DDA} and Power Mode

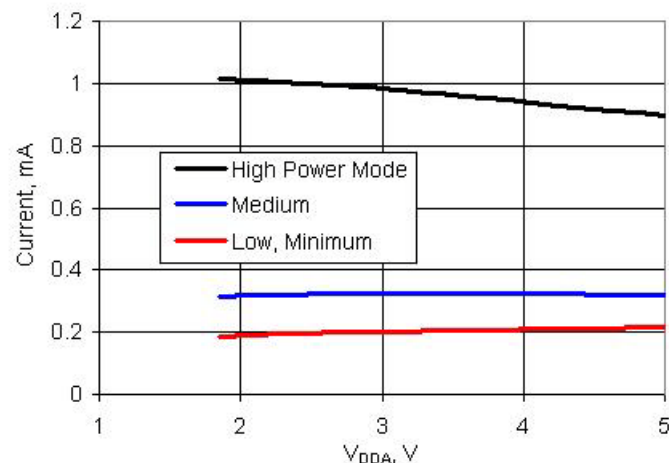


Table 11-20. Opamp AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
GBW	Gain-bandwidth product	Power mode = minimum, 15 pF load	1	–	–	MHz
		Power mode = low, 15 pF load	2	–	–	MHz
		Power mode = medium, 200 pF load	1	–	–	MHz
		Power mode = high, 200 pF load	3	–	–	MHz
SR	Slew rate, 20% - 80%	Power mode = low, 15 pF load	1.1	–	–	V/μs
		Power mode = medium, 200 pF load	0.9	–	–	V/μs
		Power mode = high, 200 pF load	3	–	–	V/μs
e_n	Input noise density	Power mode = high, $V_{DDA} = 5\text{ V}$, at 100 kHz	–	45	–	nV/sqrtHz

Figure 11-30. Opamp Noise vs Frequency, Power Mode = High, $V_{DDA} = 5\text{ V}$

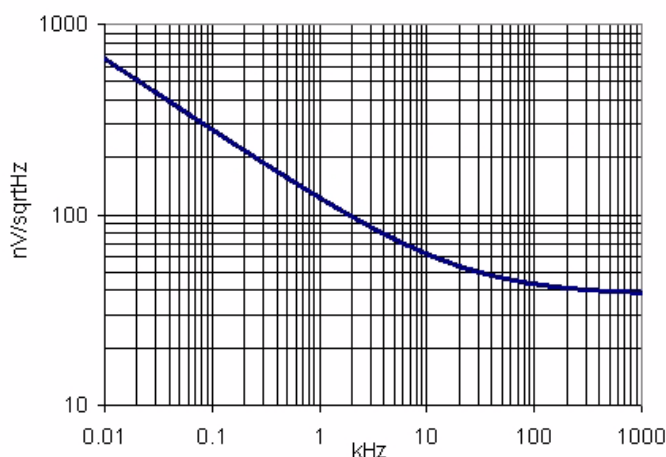


Figure 11-31. Opamp Step Response, Rising

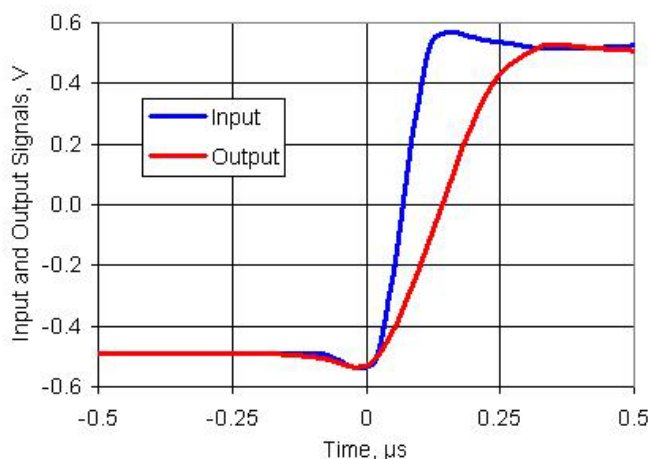
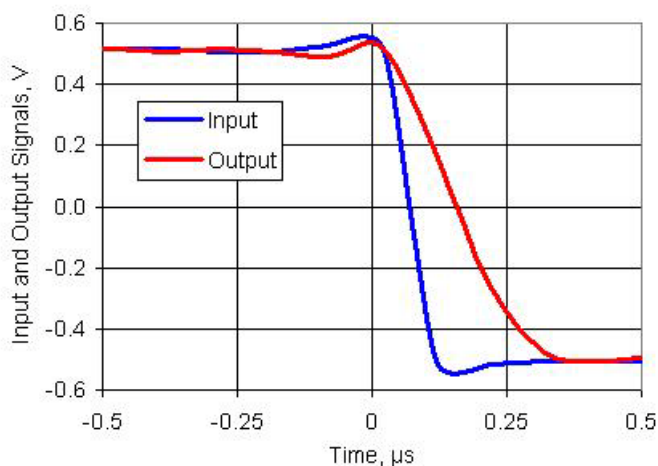


Figure 11-32. Opamp Step Response, Falling



11.5.4 Analog Globals

Table 11-29. Analog Globals Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
Rppag	Resistance pin-to-pin through P2[4], AGL0, DSM INP, AGL1, P2[5] ^[54]	$V_{DDA} = 3\text{ V}$	–	1472	2200	Ω
Rppmuxbus	Resistance pin-to-pin through P2[3], amuxbusL, P2[4] ^[54]	$V_{DDA} = 3\text{ V}$	–	706	1100	Ω

11.5.5 Comparator

Table 11-30. Comparator DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{OS}	Input offset voltage in fast mode	Factory trim, $V_{DDA} > 2.7\text{ V}$, $V_{IN} \geq 0.5\text{ V}$	–		10	mV
	Input offset voltage in slow mode	Factory trim, $V_{IN} \geq 0.5\text{ V}$	–		9	mV
	Input offset voltage in fast mode ^[55]	Custom trim	–	–	4	mV
	Input offset voltage in slow mode ^[55]	Custom trim	–	–	4	mV
	Input offset voltage in ultra low-power mode	$V_{DDA} \leq 4.6\text{ V}$	–	± 12	–	mV
V_{HYST}	Hysteresis	Hysteresis enable mode	–	10	32	mV
V_{ICM}	Input common mode voltage	High current / fast mode	V_{SSA}	–	V_{DDA}	V
		Low current / slow mode	V_{SSA}	–	V_{DDA}	V
		Ultra low-power mode $V_{DDA} \leq 4.6\text{ V}$	V_{SSA}	–	$V_{DDA} - 1.15$	V
CMRR	Common mode rejection ratio		–	50	–	dB
I_{CMP}	High current mode/fast mode ^[56]		–	–	400	μA
	Low current mode/slow mode ^[56]		–	–	100	μA
	Ultra low-power mode ^[56]	$V_{DDA} \leq 4.6\text{ V}$	–	6	–	μA

Table 11-31. Comparator AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
T_{RESP}	Response time, high current mode ^[56]	50 mV overdrive, measured pin-to-pin	–	75	110	ns
	Response time, low current mode ^[56]	50 mV overdrive, measured pin-to-pin	–	155	200	ns
	Response time, ultra low-power mode ^[56]	50 mV overdrive, measured pin-to-pin, $V_{DDA} \leq 4.6\text{ V}$	–	55	–	μs

Notes

54. The resistance of the analog global and analog mux bus is high if $V_{DDA} \leq 2.7\text{ V}$, and the chip is in either sleep or hibernate mode. Use of analog global and analog mux bus under these conditions is not recommended.

55. The recommended procedure for using a custom trim value for the on-chip comparators can be found in the TRM.

56. Based on device characterization (Not production tested).

11.6.2 Counter

The following specifications apply to the Timer/Counter/PWM peripheral, in counter mode. Counters can also be implemented in UDBs; for more information, see the Counter component data sheet in PSoC Creator.

Table 11-47. Counter DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Block current consumption	16-bit counter, at listed input clock frequency	–	–	–	μA
	3 MHz		–	15	–	μA
	12 MHz		–	60	–	μA
	48 MHz		–	260	–	μA
	67 MHz		–	350	–	μA

Table 11-48. Counter AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Operating frequency		DC	–	67.01	MHz
	Capture pulse		15	–	–	ns
	Resolution		15	–	–	ns
	Pulse width		15	–	–	ns
	Pulse width (external)		30	–	–	ns
	Enable pulse width		15	–	–	ns
	Enable pulse width (external)		30	–	–	ns
	Reset pulse width		15	–	–	ns
	Reset pulse width (external)		30	–	–	ns

11.6.3 Pulse Width Modulation

The following specifications apply to the Timer/Counter/PWM peripheral, in PWM mode. PWM components can also be implemented in UDBs; for more information, see the PWM component data sheet in PSoC Creator.

Table 11-49. PWM DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Block current consumption	16-bit PWM, at listed input clock frequency	–	–	–	μA
	3 MHz		–	15	–	μA
	12 MHz		–	60	–	μA
	48 MHz		–	260	–	μA
	67 MHz		–	350	–	μA

Table 11-50. Pulse Width Modulation (PWM) AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Operating frequency		DC	–	67.01	MHz
	Pulse width		15	–	–	ns
	Pulse width (external)		30	–	–	ns
	Kill pulse width		15	–	–	ns
	Kill pulse width (external)		30	–	–	ns
	Enable pulse width		15	–	–	ns
	Enable pulse width (external)		30	–	–	ns
	Reset pulse width		15	–	–	ns
	Reset pulse width (external)		30	–	–	ns

Figure 11-72. Synchronous Write and Read Cycle Timing, No Wait States

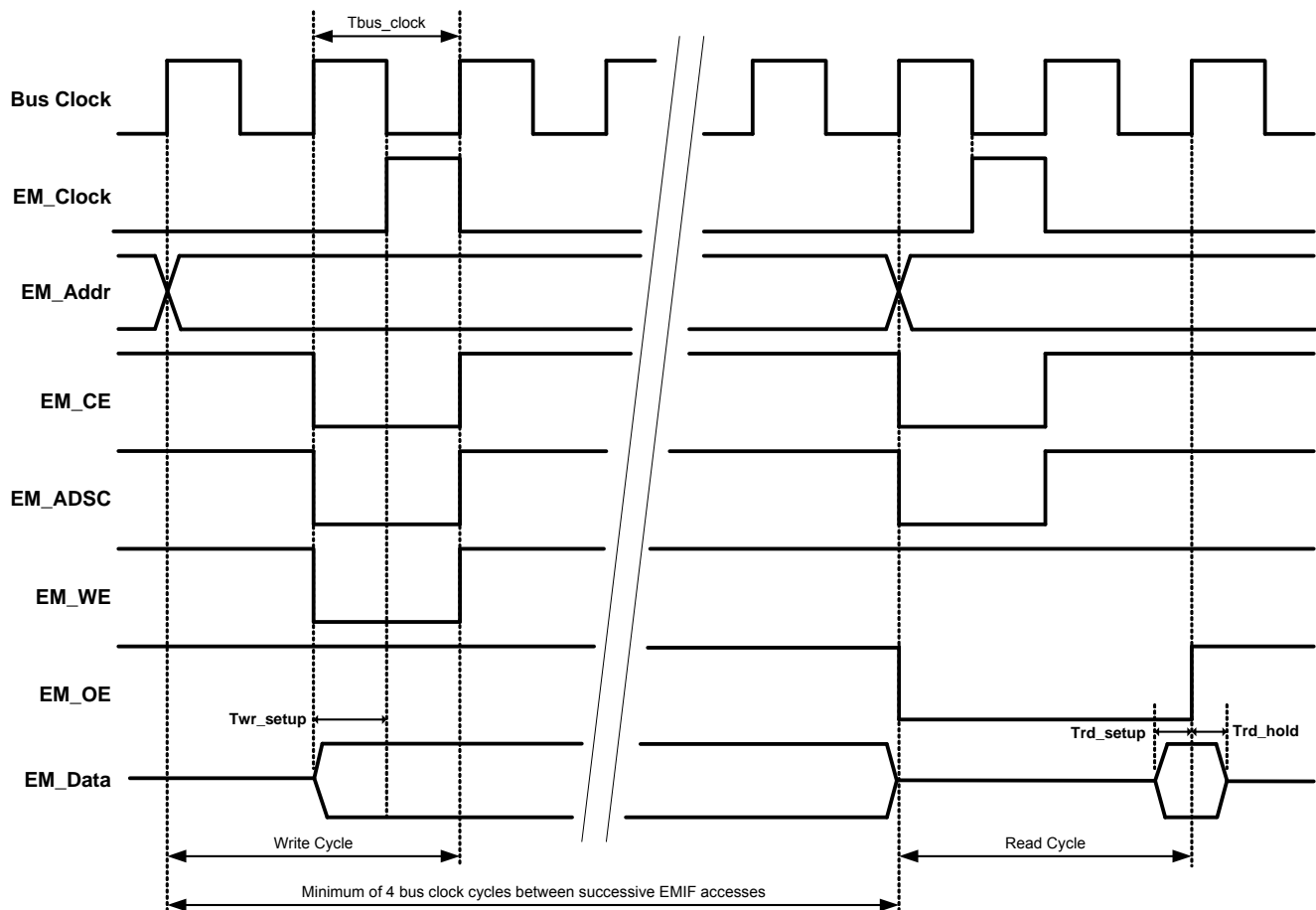


Table 11-68. Synchronous Write and Read Timing Specifications^[65]

Parameter	Description	Conditions	Min	Typ	Max	Units
Fbus_clock	Bus clock frequency ^[66]		–	–	33	MHz
Tbus_clock	Bus clock period ^[67]		30.3	–	–	ns
Twr_Setup	Time from EM_data valid to rising edge of EM_Clock		Tbus_clock – 10	–	–	ns
Trd_setup	Time that EM_data must be valid before rising edge of EM_OE		5	–	–	ns
Trd_hold	Time that EM_data must be valid after rising edge of EM_OE		5	–	–	ns

Notes

65. Based on device characterization (Not production tested).

66. EMIF signal timings are limited by GPIO frequency limitations. See “GPIO” section on page 80.

67. EMIF output signals are generally synchronized to bus clock, so EMIF signal timings are dependent on bus clock frequency.

Table 11-78. IMO AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
F _{IMO} ^[74]	IMO frequency stability (with factory trim)					
	62.6 MHz		-7	-	7	%
	48 MHz		-5	-	5	%
	24 MHz – Non USB mode		-4	-	4	%
	24 MHz – USB mode	With oscillator locking to USB bus	-0.25	-	0.25	%
	12 MHz		-3	-	3	%
	6 MHz		-2	-	2	%
	3 MHz	0 °C to 70 °C	-1	-	1	%
		-40 °C to 85 °C	-1.5	-	1.5	%
	3 MHz frequency stability after typical PCB assembly post-reflow.	Typical (non-optimized) board layout and 250 °C solder reflow. Device may be calibrated after assembly to improve performance.	-	±2	-	%
	Startup time ^[75]	From enable (during normal system operation)	-	-	13	µs
Jp-p	Jitter (peak to peak) ^[75]					
	F = 24 MHz		-	0.9	-	ns
	F = 3 MHz		-	1.6	-	ns
Jperiod	Jitter (long term) ^[75]					
	F = 24 MHz		-	0.9	-	ns
	F = 3 MHz		-	12	-	ns

Figure 11-76. IMO Frequency Variation vs. Temperature

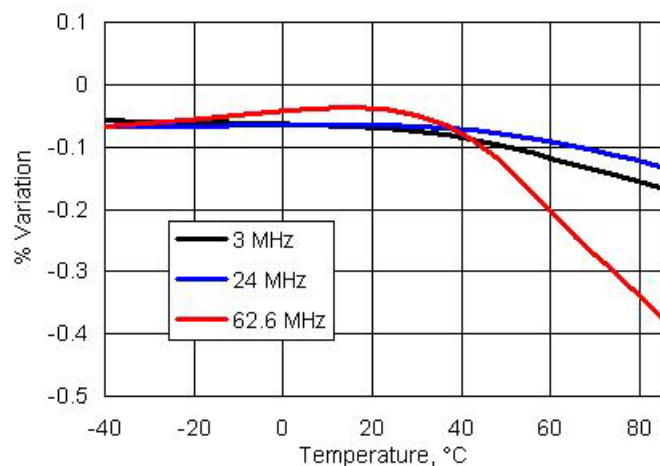
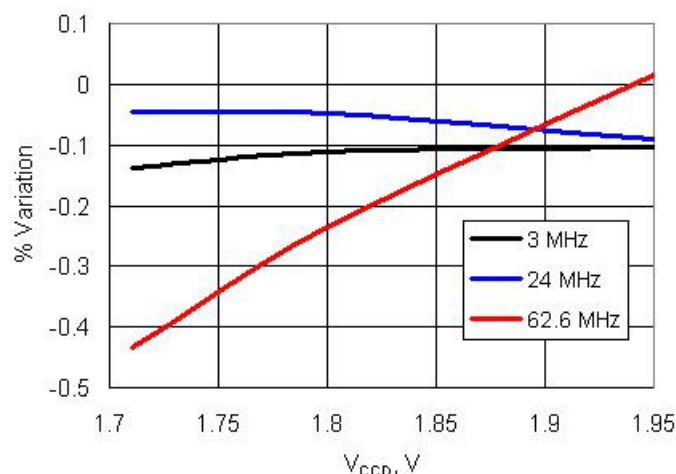


Figure 11-77. IMO Frequency Variation vs. V_{CC}



Notes

74. F_{IMO} is measured after packaging, and thus accounts for substrate and die attach stresses.

75. Based on device characterization (Not production tested).

12. Ordering Information

In addition to the features listed in [Table 12-1](#), every CY8C38 device includes: a precision on-chip voltage reference, precision oscillators, flash, ECC, DMA, a fixed function I²C, 4 KB trace RAM, JTAG/SWD programming and debug, external memory interface, and more. In addition to these features, the flexible UDBs and analog subsection support a wide range of peripherals. To assist you in selecting the ideal part, PSoC Creator makes a part recommendation after you choose the components required by your application. All CY8C38 derivatives incorporate device and flash security in user-selectable security levels; see the TRM for details.

Table 12-1. CY8C38 Family with Single Cycle 8051

Part Number	MCU Core				Analog								Digital			I/O ^[83]				Package	JTAG ID ^[84]	
	CPU Speed (MHz)	Flash (KB)	SRAM (KB)	EEPROM (KB)	LCD Segment Drive	ADC	DAC	Comparator	SC/CT Analog Blocks ^[81]	Opamps	DFB	CapSense	UDBs ^[82]	16-bit Timer/PWM	FS USB	CAN 2.0b	Total I/O	GPIO	SIO			USBIO
32 KB Flash																						
CY8C3865AXI-019	67	32	4	1	✓	20-bit Del-Sig	4	4	4	4	✓	✓	20	4	✓	–	72	62	8	2	100-pin TQFP	0x1E013069
CY8C3865LTI-014	67	32	4	1	✓	20-bit Del-Sig	4	4	4	4	✓	✓	20	4	✓	–	48	38	8	2	68-pin QFN	0x1E00E069
CY8C3865AXI-204	67	32	8	1	✓	20-bit Del-Sig	2	0	0	0	–	✓	16	4	✓	–	72	62	8	2	100-pin TQFP	0x1E0CC069
CY8C3865LTI-205	67	32	8	1	✓	20-bit Del-Sig	2	0	0	0	–	✓	16	4	✓	–	48	38	8	2	68-pin QFN	0x1E0CD069
64 KB Flash																						
CY8C3866LTI-067	67	64	8	2	✓	20-bit Del-Sig	4	4	4	2	✓	✓	24	4	✓	–	31	25	4	2	48-pin QFN	0x1E043069
CY8C3866PVI-021	67	64	8	2	✓	20-bit Del-Sig	4	4	4	2	✓	✓	24	4	✓	–	31	25	4	2	48-pin SSOP	0x1E015069
CY8C3866AXI-035	67	64	8	2	✓	20-bit Del-Sig	4	4	4	4	✓	✓	24	4	–	✓	70	62	8	0	100-pin TQFP	0x1E023069
CY8C3866AXI-039	67	64	8	2	✓	20-bit Del-Sig	4	4	4	4	✓	✓	24	4	✓	–	72	62	8	2	100-pin TQFP	0x1E027069
CY8C3866LTI-030	67	64	8	2	✓	20-bit Del-Sig	4	4	4	4	✓	✓	24	4	✓	–	48	38	8	2	68-pin QFN	0x1E01E069
CY8C3866LTI-068	67	64	8	2	✓	20-bit Del-Sig	4	4	4	2	✓	✓	24	4	✓	✓	31	25	4	2	48-pin QFN	0x1E044069
CY8C3866AXI-040	67	64	8	2	✓	20-bit Del-Sig	4	4	4	4	✓	✓	24	4	✓	✓	72	62	8	2	100-pin TQFP	0x1E028069
CY8C3866PVI-070	67	64	8	2	✓	20-bit Del-Sig	4	4	4	2	✓	✓	24	4	–	✓	29	25	4	0	48-pin SSOP	0x1E046069
CY8C3866AXI-206	67	64	8	2	✓	20-bit Del-Sig	2	2	0	2	✓	✓	20	4	✓	–	72	62	8	2	100-pin TQFP	0x1E0CE069
CY8C3866LTI-207	67	64	8	2	✓	20-bit Del-Sig	2	2	0	2	✓	✓	20	4	✓	–	48	38	8	2	68-pin QFN	0x1E0CF069
CY8C3866AXI-208	67	64	8	2	✓	20-bit Del-Sig	2	2	2	2	✓	✓	24	4	✓	✓	72	62	8	2	100-pin TQFP	0x1E0D0069
CY8C3866LTI-209	67	64	8	2	✓	20-bit Del-Sig	2	2	2	2	✓	✓	24	4	✓	✓	48	38	8	2	68-pin QFN	0x1E0D1069
CY8C3866FNI-210	67	64	8	2	✓	20-bit Del-Sig	4	4	4	4	✓	✓	24	4	✓	✓	48	38	8	2	72 WLCSP	0x1E0D2069

Notes

81. Analog blocks support a variety of functionality including TIA, PGA, and mixers. See the [Example Peripherals](#) on page 44 for more information on how analog blocks can be used.
82. UDBs support a variety of functionality including SPI, LIN, UART, timer, counter, PWM, PRS, and others. Individual functions may use a fraction of a UDB or multiple UDBs. Multiple functions can share a single UDB. See the [Example Peripherals](#) on page 44 for more information on how UDBs can be used.
83. The I/O Count includes all types of digital I/O: GPIO, SIO, and the two USB I/O. See the [I/O System and Routing](#) on page 37 for details on the functionality of each of these types of I/O.
84. The JTAG ID has three major fields. The most significant nibble (left digit) is the version, followed by a 2 byte part number and a 3 nibble manufacturer ID.

13. Packaging

Table 13-1. Package Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Units
T _A	Operating ambient temperature		–40	25.00	85	°C
T _J	Operating junction temperature		–40	–	100	°C
T _{JA}	Package θ_{JA} (48-pin SSOP)		–	49	–	°C/Watt
T _{JA}	Package θ_{JA} (48-pin QFN)		–	14	–	°C/Watt
T _{JA}	Package θ_{JA} (68-pin QFN)		–	15	–	°C/Watt
T _{JA}	Package θ_{JA} (100-pin TQFP)		–	34	–	°C/Watt
T _{JC}	Package θ_{JC} (48-pin SSOP)		–	24	–	°C/Watt
T _{JC}	Package θ_{JC} (48-pin QFN)		–	15	–	°C/Watt
T _{JC}	Package θ_{JC} (68-pin QFN)		–	13	–	°C/Watt
T _{JC}	Package θ_{JC} (100-pin TQFP)		–	10	–	°C/Watt
T _{JA}	Package θ_{JA} (72-pin CSP)		–	18	–	°C/Watt
T _{JC}	Package θ_{JC} (72-pin CSP)		–	0.13	–	°C/Watt

Table 13-2. Solder Reflow Peak Temperature

Package	Maximum Peak Temperature	Maximum Time at Peak Temperature
48-pin SSOP	260 °C	30 seconds
48-pin QFN	260 °C	30 seconds
68-pin QFN	260 °C	30 seconds
100-pin TQFP	260 °C	30 seconds
72-pin CSP	260 °C	30 seconds

Table 13-3. Package Moisture Sensitivity Level (MSL), IPC/JEDEC J-STD-2

Package	MSL
48-pin SSOP	MSL 3
48-pin QFN	MSL 3
68-pin QFN	MSL 3
100-pin TQFP	MSL 3
72-pin CSP	MSL 1

Table 14-1. Acronyms Used in this Document *(continued)*

Acronym	Description
PHUB	peripheral hub
PHY	physical layer
PICU	port interrupt control unit
PLA	programmable logic array
PLD	programmable logic device, see also PAL
PLL	phase-locked loop
PMDD	package material declaration data sheet
POR	power-on reset
PRES	precise low-voltage reset
PRS	pseudo random sequence
PS	port read data register
PSoC®	Programmable System-on-Chip™
PSRR	power supply rejection ratio
PWM	pulse-width modulator
RAM	random-access memory
RISC	reduced-instruction-set computing
RMS	root-mean-square
RTC	real-time clock
RTL	register transfer language
RTR	remote transmission request
RX	receive
SAR	successive approximation register
SC/CT	switched capacitor/continuous time
SCL	I ² C serial clock
SDA	I ² C serial data
S/H	sample and hold
SINAD	signal to noise and distortion ratio
SIO	special input/output, GPIO with advanced features. See GPIO.
SOC	start of conversion

Table 14-1. Acronyms Used in this Document *(continued)*

Acronym	Description
SOF	start of frame
SPI	Serial Peripheral Interface, a communications protocol
SR	slew rate
SRAM	static random access memory
SRES	software reset
SWD	serial wire debug, a test protocol
SWV	single-wire viewer
TD	transaction descriptor, see also DMA
THD	total harmonic distortion
TIA	transimpedance amplifier
TRM	technical reference manual
TTL	transistor-transistor logic
TX	transmit
UART	Universal Asynchronous Transmitter Receiver, a communications protocol
UDB	universal digital block
USB	Universal Serial Bus
USBIO	USB input/output, PSoC pins used to connect to a USB port
VDAC	voltage DAC, see also DAC, IDAC
WDT	watchdog timer
WOL	write once latch, see also NVL
WRES	watchdog timer reset
XRES	external reset I/O pin
XTAL	crystal

15. Reference Documents

[PSoC® 3, PSoC® 5 Architecture TRM](#)

[PSoC® 3 Registers TRM](#)

Description Title: PSoC® 3: CY8C38 Family Datasheet Programmable System-on-Chip (PSoC®) (continued)
Document Number: 001-11729

Revision	ECN	Submission Date	Orig. of Change	Description of Change
*L	2938381	05/27/10	MKEA	<p>Replaced V_{DDIO} with V_{DDD} in USBIO diagram and specification tables, added text in USBIO section of Electrical Specifications.</p> <p>Added Table 13-2 (Package MSL)</p> <p>Modified Tstorag condition and changed max spec to 100</p> <p>Added bullet (Pass) under ALU (section 7.2.2.2)</p> <p>Added figures for kHzECO and MHzECO in the External Oscillator section</p> <p>Updated Figure 6-1(Clocking Subsystem diagram)</p> <p>Removed CPUCLK_DIV in table 5-2, Deleted Clock Divider SFR subsection</p> <p>Updated PSoC Creator Framework image</p> <p>Updated SIO DC Specifications (V_{IH} and V_{IL} parameters)</p> <p>Updated bullets in Clocking System and Clocking Distribution sections</p> <p>Updated Figure 8-2</p> <p>Updated PCB Layout and Schematic, updated as per MTRB review comments</p> <p>Updated Table 6-3 (power changed to current)</p> <p>In 32kHz EC DC Specifications table, changed I_{CC} Max to 0.25</p> <p>In IMO DC Specifications table, updated Supply Current values</p> <p>Updated GPIO DC Specs table</p>
*M	2958674	06/22/10	SHEA	Minor ECN to post data sheet to external website
*N	2989685	08/04/10	MKEA	<p>INL max is changed from 16 to 32 in Table 11-20, 20-bit Delta-sigma ADC AC Specifications.</p> <p>Added to Table 6-6 a footnote and references to same.</p> <p>Added sentences to the resistive pullup and pull-down description bullets.</p> <p>Added sentence to Section 6.4.11, Adjustable Output Level.</p> <p>Updated section 5.5 External Memory Interface</p> <p>Updated Table 11-73 JTAG Interface AC Specifications</p> <p>Updated Table 11-74 SWD Interface AC Specifications</p> <p>Updated style changes as per the new template.</p>
*O	3078568	11/04/10	MKEA	<p>Added 48-SSOP pin and package details.</p> <p>Removed PLL output duty cycle spec.</p> <p>Updated "Current Digital-to-analog Converter (IDAC)" on page 97</p> <p>Updated "Voltage Digital to Analog Converter (VDAC)" on page 101</p> <p>Updated Table 11-2, "DC Specifications," on page 72</p> <p>Updated Table 11-28, "Voltage Reference Specifications," on page 95</p>