Infineon Technologies - CY8C3866AXI-208 Datasheet

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	67MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, SPI, UART/USART, USB
Peripherals	CapSense, DMA, LCD, POR, PWM, WDT
Number of I/O	62
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 5.5V
Data Converters	A/D 16x20b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c3866axi-208

Table 4-4. Boolean Instructions *(continued)*

Mnemonic	Description	Bytes	Cycles
ANL C, /bit	AND complement of direct bit to carry	2	2
ORL C, bit	OR direct bit to carry	2	2
ORL C, /bit	OR complement of direct bit to carry	2	2
MOV C, bit	Move direct bit to carry	2	2
MOV bit, C	Move carry to direct bit	2	3
JC rel	Jump if carry is set	2	3
JNC rel	Jump if no carry is set	2	3
JB bit, rel	Jump if direct bit is set	3	5
JNB bit, rel	Jump if direct bit is not set	3	5
JBC bit, rel	Jump if direct bit is set and clear bit	3	5

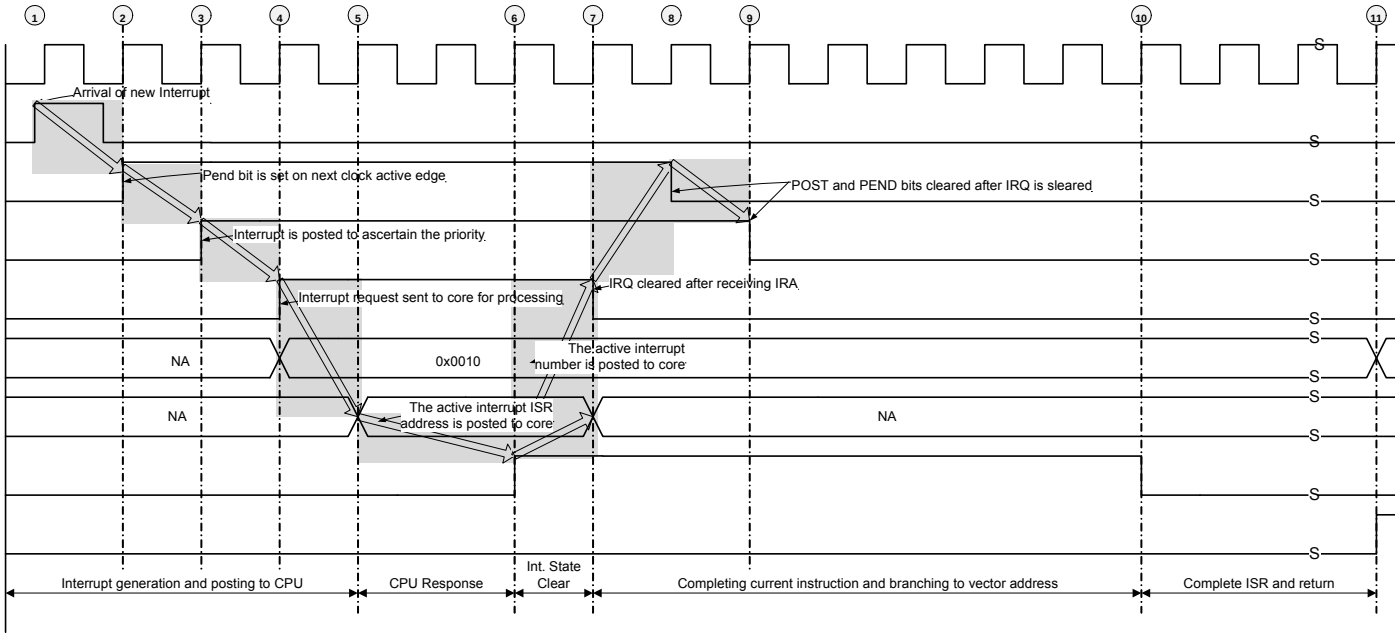
4.3.1.5 Program Branching Instructions

The 8051 supports a set of conditional and unconditional jump instructions that help to modify the program execution flow. Table 4-5 shows the list of jump instructions.

Table 4-5. Jump Instructions

Mnemonic	Description	Bytes	Cycles
ACALL addr11	Absolute subroutine call	2	4
LCALL addr16	Long subroutine call	3	4
RET	Return from subroutine	1	4
RETI	Return from interrupt	1	4
AJMP addr11	Absolute jump	2	3
LJMP addr16	Long jump	3	4
SJMP rel	Short jump (relative address)	2	3
JMP @A + DPTR	Jump indirect relative to DPTR	1	5
JZ rel	Jump if accumulator is zero	2	4
JNZ rel	Jump if accumulator is nonzero	2	4
CJNE A,Direct, rel	Compare direct byte to accumulator and jump if not equal	3	5
CJNE A, #data, rel	Compare immediate data to accumulator and jump if not equal	3	4
CJNE Rn, #data, rel	Compare immediate data to register and jump if not equal	3	4
CJNE @Ri, #data, rel	Compare immediate data to indirect RAM and jump if not equal	3	5
DJNZ Rn,rel	Decrement register and jump if not zero	2	4
DJNZ Direct, rel	Decrement direct byte and jump if not zero	3	5
NOP	No operation	1	1

Figure 4-2. Interrupt Processing Timing Diagram



Notes

- 1: Interrupt triggered asynchronous to the clock
- 2: The PEND bit is set on next active clock edge to indicate the interrupt arrival
- 3: POST bit is set following the PEND bit
- 4: Interrupt request and the interrupt number sent to CPU core after evaluation priority (Takes 3 clocks)
- 5: ISR address is posted to CPU core for branching
- 6: CPU acknowledges the interrupt request
- 7: ISR address is read by CPU for branching
- 8, 9: PEND and POST bits are cleared respectively after receiving the IRA from core
- 10: IRA bit is cleared after completing the current instruction and starting the instruction execution from ISR location (Takes 7 cycles)
- 11: IRC is set to indicate the completion of ISR, Active int. status is restored with previous status

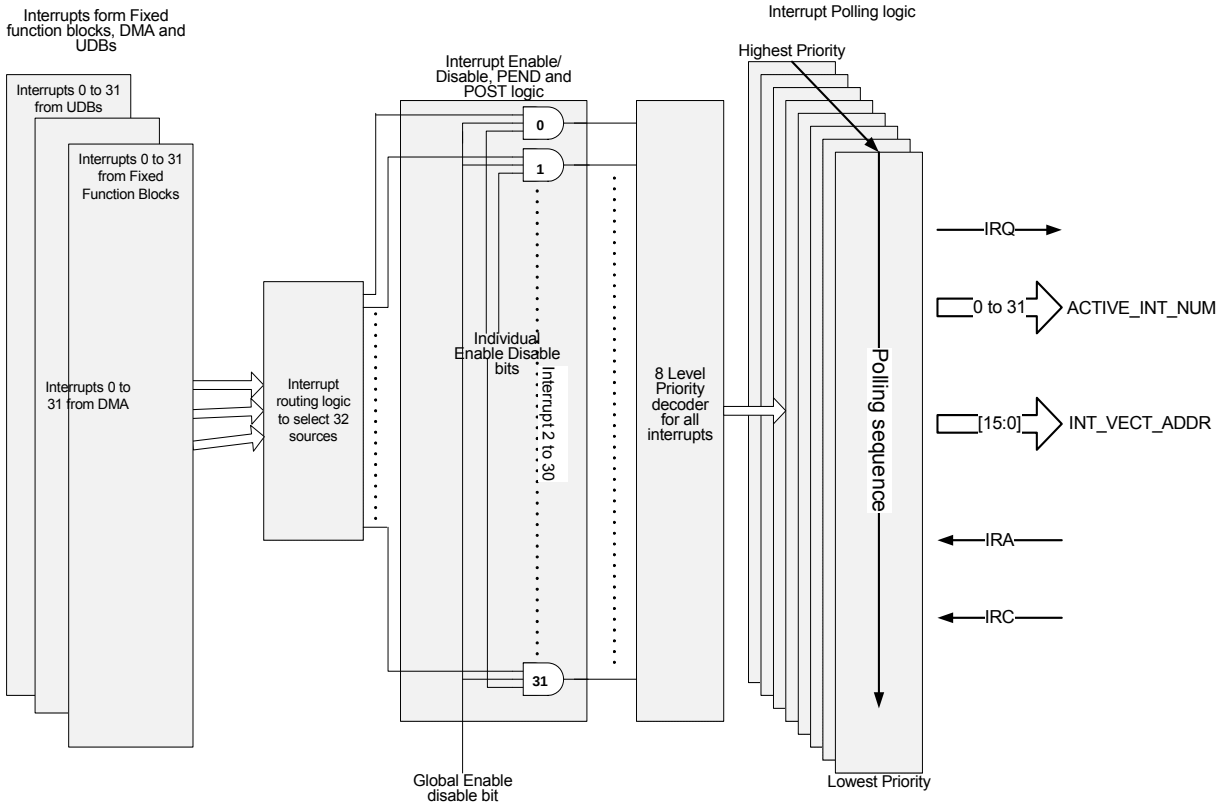
The total interrupt latency (ISR execution)

= POST + PEND + IRQ + IRA + Completing current instruction and branching

= 1+1+1+2+7 cycles

= 12 cycles

Figure 4-3. Interrupt Structure



When an interrupt is pending, the current instruction is completed and the program counter is pushed onto the stack. Code execution then jumps to the program address provided by the vector. After the ISR is completed, a RETI instruction is executed and returns execution to the instruction following the previously interrupted instruction. To do this the RETI instruction pops the program counter from the stack.

If the same priority level is assigned to two or more interrupts, the interrupt with the lower vector number is executed first. Each interrupt vector may choose from three interrupt sources: Fixed Function, DMA, and UDB. The fixed function interrupts are direct connections to the most common interrupt sources and provide the lowest resource cost connection. The DMA interrupt sources provide direct connections to the two DMA interrupt sources provided per DMA channel. The third interrupt source for vectors is from the UDB digital routing array. This allows any digital signal available to the UDB array to be used as an interrupt source. Fixed function interrupts and all interrupt sources may be routed to any interrupt vector using the UDB interrupt source connections.

5. Memory

5.1 Static RAM

CY8C38 SRAM is used for temporary data storage. Up to 8 KB of SRAM is provided and can be accessed by the 8051 or the DMA controller. See Memory Map on page 26. Simultaneous access of SRAM by the 8051 and the DMA controller is possible if different 4-KB blocks are accessed.

5.2 Flash Program Memory

Flash memory in PSoC devices provides nonvolatile storage for user firmware, user configuration data, bulk data storage, and optional ECC data. The main flash memory area contains up to 64 KB of user program space.

Up to an additional 8 KB of flash space is available for ECC. If ECC is not used this space can store device configuration data and bulk user data. User code may not be run out of the ECC flash memory section. ECC can correct one bit error and detect two bit errors per 8 bytes of firmware memory; an interrupt can be generated when an error is detected.

The CPU reads instructions located in flash through a cache controller. This improves instruction execution rate and reduces system power consumption by requiring less frequent flash access. The cache has 8 lines at 64 bytes per line for a total of 512 bytes. It is fully associative, automatically controls flash power, and can be enabled or disabled. If ECC is enabled, the cache controller also performs error checking and correction, and interrupt generation.

Flash programming is performed through a special interface and preempts code execution out of flash. The flash programming interface performs flash erasing, programming and setting code protection levels. Flash in-system serial programming (ISSP), typically used for production programming, is possible through both the SWD and JTAG interfaces. In-system programming, typically used for bootloaders, is also possible using serial interfaces such as I^2C, USB, UART, and SPI, or any communications protocol.

5.3 Flash Security

All PSoC devices include a flexible flash-protection model that prevents access and visibility to on-chip flash memory. This prevents duplication or reverse engineering of proprietary code. Flash memory is organized in blocks, where each block contains 256 bytes of program or data and 32 bytes of ECC or configuration data. A total of up to 256 blocks is provided on 64-KB flash devices.

The device offers the ability to assign one of four protection levels to each row of flash. Table 5-1 lists the protection modes available. Flash protection levels can only be changed by performing a complete flash erase. The Full Protection and Field Upgrade settings disable external access (through a debugging tool such as PSoC Creator, for example). If your application requires code update through a bootloader, then use the Field Upgrade setting. Use the Unprotected setting only when no security is needed in your application. The PSoC device also offers an advanced security feature called Device Security which permanently disables all test, programming, and debug ports, protecting your application from external access (see the "Device Security" section on page 68). For more information about how to take full advantage of the security features in PSoC, see the PSoC 3 TRM.

Table 5-1. Flash Protection

Protection Setting	Allowed	Not Allowed
Unprotected	External read and write + internal read and write	–
Factory Upgrade	External write + internal read and write	External read
Field Upgrade	Internal read and write	External read and write
Full Protection	Internal read	External read and write + internal write

Disclaimer

Note the following details of the flash code protection features on Cypress devices.

Cypress products meet the specifications contained in their particular Cypress data sheets. Cypress believes that its family of products is one of the most secure families of its kind on the market today, regardless of how they are used. There may be methods, unknown to Cypress, that can breach the code protection features. Any of these methods, to our knowledge, would be dishonest and possibly illegal. Neither Cypress nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as 'unbreakable'. Cypress is willing to work with the customer who is concerned about the integrity of their code. Code protection is constantly evolving. We at Cypress are committed to continuously improving the code protection features of our products.

5.4 EEPROM

PSoC EEPROM memory is a byte-addressable nonvolatile memory. The CY8C38 has up to 2 KB of EEPROM memory to store user data. Reads from EEPROM are random access at the byte level. Reads are done directly; writes are done by sending write commands to an EEPROM programming interface. CPU code execution can continue from flash during EEPROM writes. EEPROM is erasable and writeable at the row level. The EEPROM is divided into 128 rows of 16 bytes each. The factory default values of all EEPROM bytes are 0.

Because the EEPROM is mapped to the 8051 xdata space, the CPU can not execute out of EEPROM. There is no ECC hardware associated with EEPROM. If ECC is required it must be handled in firmware.

It can take as much as 20 milliseconds to write to EEPROM or flash. During this time the device should not be reset, or unexpected changes may be made to portions of EEPROM or flash. Reset sources (see *Section 6.3.1*) include XRES pin, software reset, and watchdog; care should be taken to make sure that these are not inadvertently activated. In addition, the low voltage detect circuits should be configured to generate an interrupt instead of a reset.

Figure 6-10. SIO Input/Output Block Diagram

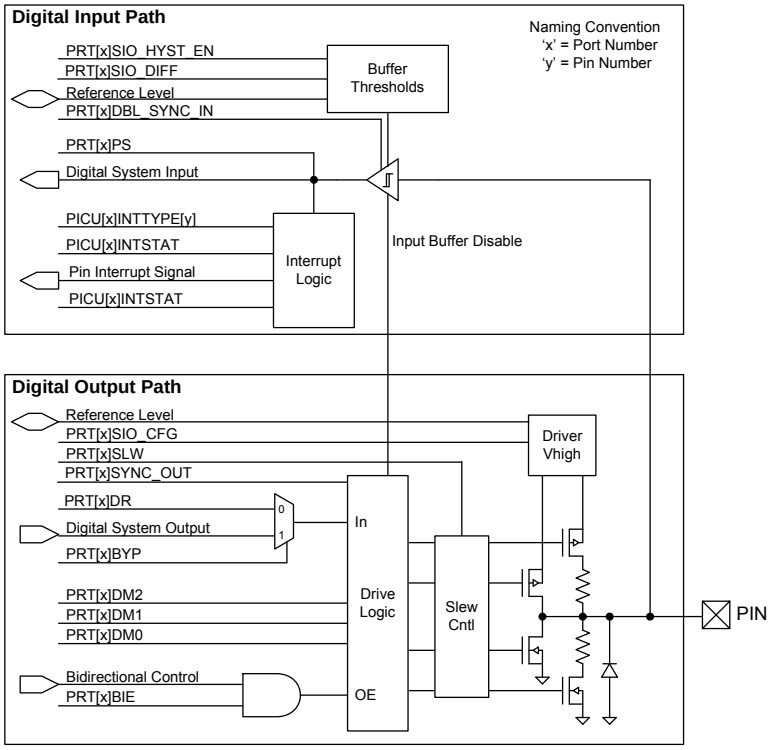


Figure 6-11. USBIO Block Diagram

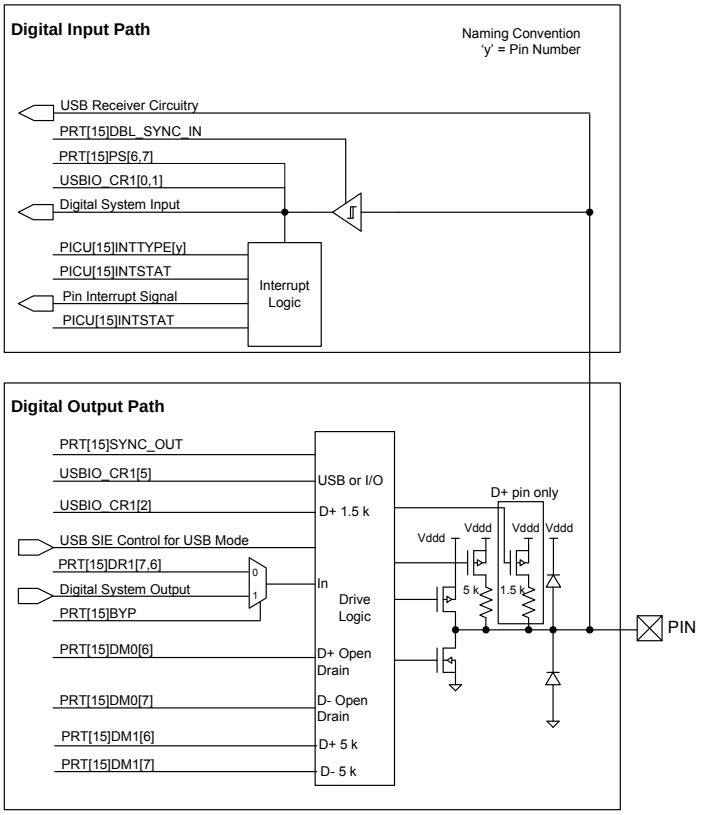
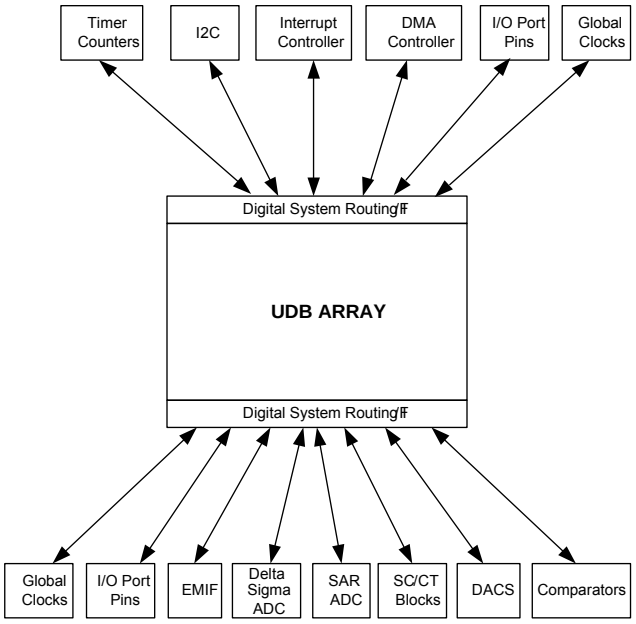
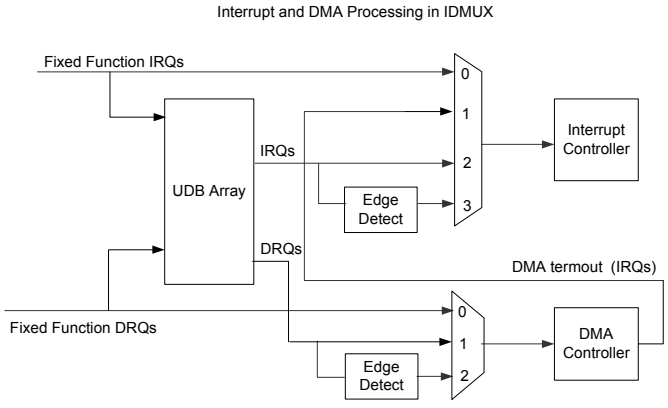


Figure 7-9. Digital System Interconnect



Interrupt and DMA routing is very flexible in the CY8C38 programmable architecture. In addition to the numerous fixed function peripherals that can generate interrupt requests, any data signal in the UDB array routing can also be used to generate a request. A single peripheral may generate multiple independent interrupt requests simplifying system and firmware design. Figure 7-10 shows the structure of the IDMUX (Interrupt/DMA Multiplexer).

Figure 7-10. Interrupt and DMA Processing in the IDMUX



7.4.1 I/O Port Routing

There are a total of 20 DSI routes to a typical 8-bit I/O port, 16 for data and four for drive strength control.

When an I/O pin is connected to the routing, there are two primary connections available, an input and an output. In conjunction with drive strength control, this can implement a bidirectional I/O pin. A data output signal has the option to be single synchronized (pipelined) and a data input signal has the option to be double synchronized. The synchronization clock is the master clock (see Figure 6-1). Normally all inputs from pins are synchronized as this is required if the CPU interacts with the signal or any signal derived from it. Asynchronous inputs have rare uses. An example of this is a feed through of combinational PLD logic from input pins to output pins.

Figure 7-11. I/O Pin Synchronization Routing

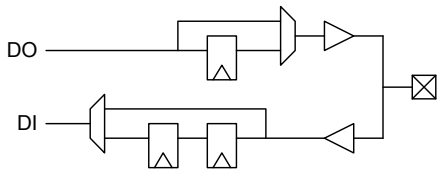
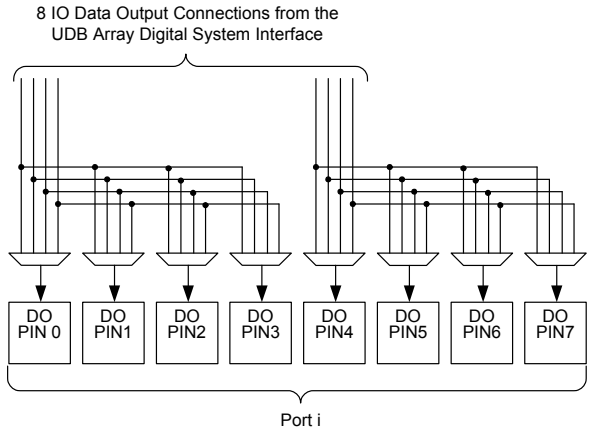


Figure 7-12. I/O Pin Output Connectivity



There are four more DSI connections to a given I/O port to implement dynamic output enable control of pins. This connectivity gives a range of options, from fully ganged 8-bits controlled by one signal, to up to four individually controlled pins. The output enable signal is useful for creating tri-state bidirectional pins and buses.

Figure 7-13. I/O Pin Output Enable Connectivity

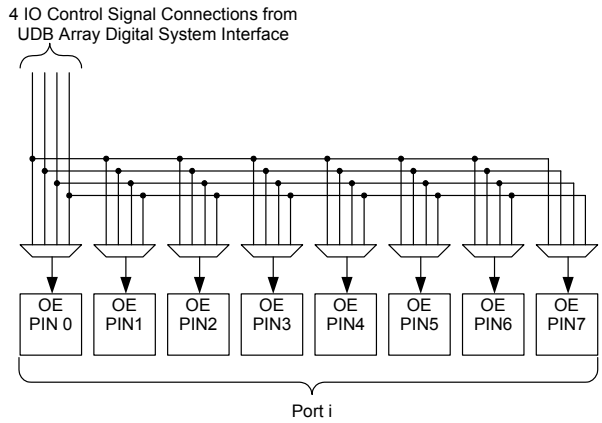
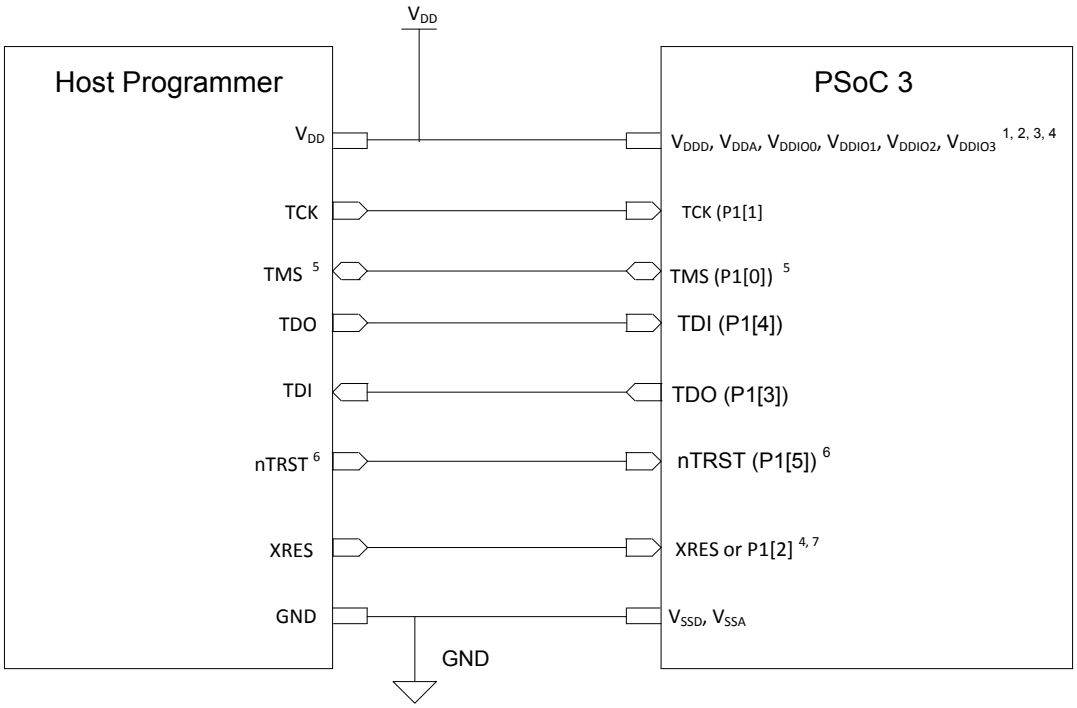


Figure 9-1. JTAG Interface Connections between PSoC 3 and Programmer



[1] The voltage levels of Host Programmer and the PSoC 3 voltage domains involved in Programming should be same. The Port 1 JTAG pins, XRES pin (XRES_N or P1[2]) are powered by V_{DDIO1}. So, V_{DDIO1} of PSoC 3 should be at same voltage level as host V_{DD}. Rest of PSoC 3 voltage domains (V_{DDD}, V_{DDA}, V_{DDIO0}, V_{DDIO2}, V_{DDIO3}) need not be at the same voltage level as host Programmer.

[2] Vdda must be greater than or equal to all other power supplies (Vddd, Vddio's) in PSoC 3.

[3] For Power cycle mode Programming, XRES pin is not required. But the Host programmer must have the capability to toggle power (Vddd, Vdda, All Vddio's) to PSoC 3. This may typically require external interface circuitry to toggle power which will depend on the programming setup. The power supplies can be brought up in any sequence, however, once stable, VDDA must be greater than or equal to all other supplies.

[4] For JTAG Programming, Device reset can also be done without connecting to the XRES pin or Power cycle mode by using the TMS,TCK,TDI, TDO pins of PSoC 3, and writing to a specific register. But this requires that the DPS setting in NVL is not equal to "Debug Ports Disabled".

[5] By default, PSoC 3 is configured for 4-wire JTAG mode unless user changes the DPS setting. So the TMS pin is unidirectional. But if the DPS setting is changed to non-JTAG mode, the TMS pin in JTAG is bi-directional as the SWD Protocol has to be used for acquiring the PSoC 3 device initially. After switching from SWD to JTAG mode, the TMS pin will be uni-directional. In such a case, unidirectional buffer should not be used on TMS line.

[6] nTRST JTAG pin (P1[5]) cannot be used to reset the JTAG TAP controlller during first time programming of PSoC 3 as the default setting is 4-wire JTAG (nTRST disabled). Use the TMS, TCK pins to do a reset of JTAG TAP controller.

[7] If XRES pin is used by host, P1[2] will be configured as XRES by default only for 48-pin devices (without dedicated XRES pin). For devices with dedicated XRES pin, P1[2] is GPIO pin by default. So use P1[2] as Reset pin only for 48-pin devices, but use dedicated XRES pin for rest of devices.

Table 11-2. DC Specifications *(continued)*

Parameter	Description	Conditions		Min	Typ[25]	Max	Units
	Sleep Mode[28]						
	CPU = OFF RTC = ON (= ECO32K ON, in low-power mode) Sleep timer = ON (= ILO ON at 1 kHz)[29] WDT = OFF I^2C Wake = OFF Comparator = OFF POR = ON Boost = OFF SIO pins in single ended input, unregulated output mode	$V_{DD} = V_{DDIO}$ = 4.5 V - 5.5 V	T = –40 °C	–	1.1	2.3	µA
			T = 25 °C	–	1.1	2.2	
			T = 85 °C	–	15	30	
		$V_{DD} = V_{DDIO}$ = 2.7 V – 3.6 V	T = –40 °C	–	1	2.2	
			T = 25 °C	–	1	2.1	
			T = 85 °C	–	12	28	
		$V_{DD} = V_{DDIO}$ = 1.71 V – 1.95 V[30]	T = 25 °C	–	2.2	4.2	
	Comparator = ON CPU = OFF RTC = OFF Sleep timer = OFF WDT = OFF I^2C Wake = OFF POR = ON Boost = OFF SIO pins in single ended input, unregulated output mode	$V_{DD} = V_{DDIO}$ = 2.7 V – 3.6 V[31]	T = 25 °C	–	2.2	2.7	
	I^2C Wake = ON CPU = OFF RTC = OFF Sleep timer = OFF WDT = OFF Comparator = OFF POR = ON Boost = OFF SIO pins in single ended input, unregulated output mode	$V_{DD} = V_{DDIO}$ = 2.7 V – 3.6 V[31]	T = 25 °C	–	2.2	2.8	
	Hibernate Mode[28]						
	Hibernate mode current All regulators and oscillators off SRAM retention GPIO interrupts are active Boost = OFF SIO pins in single ended input, unregulated output mode	$V_{DD} = V_{DDIO}$ = 4.5 V - 5.5 V	T = –40 °C	–	0.2	1.5	µA
			T = 25 °C	–	0.5	1.5	
			T = 85 °C	–	4.1	5.3	
		$V_{DD} = V_{DDIO}$ = 2.7 V – 3.6 V	T = –40 °C	–	0.2	1.5	
			T = 25 °C	–	0.2	1.5	
			T = 85 °C	–	3.2	4.2	
		$V_{DD} = V_{DDIO}$ = 1.71 V – 1.95 V[30]	T = –40 °C	–	0.2	1.5	
			T = 25 °C	–	0.3	1.5	
			T = 85 °C	–	3.3	4.3	
I_{DDAR}	Analog current consumption while device is reset[32]	$V_{DDA} \le 3.6$ V		–	0.3	0.6	mA
		$V_{DDA} > 3.6$ V		–	1.4	3.3	mA
I_{DDDR}	Digital current consumption while device is reset[32]	$V_{DDD} \le 3.6$ V		–	1.1	3.1	mA
		$V_{DDD} > 3.6$ V		–	0.7	3.1	mA

Notes
28. If V_{CCD} and V_{CCA} are externally regulated, the voltage difference between V_{CCD} and V_{CCA} must be less than 50 mV.
29. Sleep timer generates periodic interrupts to wake up the CPU. This specification applies only to those times that the CPU is off.
30. Externally regulated mode.
31. Based on device characterization (not production tested).
32. Based on device characterization (not production tested). USBIO pins tied to ground (VSSD).

11.3.3 Inductive Boost Regulator

Unless otherwise specified, operating conditions are: V_{BAT} = 0.5 V–3.6 V, V_{OUT} = 1.8 V–5.0 V, I_{OUT} = 0 mA–50 mA, L_{BOOST} = 4.7 µH–22 µH, C_{BOOST} = 22 µF || 3 × 1.0 µF || 3 × 0.1 µF, C_{BAT} = 22 µF, I_F = 1.0 A. Unless otherwise specified, all charts and graphs show typical values.

Table 11-6. Inductive Boost Regulator DC Specifications

Parameter	Description	Conditions		Min	Typ	Max	Units
V_{OUT}	Boost output voltage[34]	vsel = 1.8 V in register BOOST_CR0		1.71	1.8	1.89	V
		vsel = 1.9 V in register BOOST_CR0		1.81	1.90	2.00	V
		vsel = 2.0 V in register BOOST_CR0		1.90	2.00	2.10	V
		vsel = 2.4 V in register BOOST_CR0		2.16	2.40	2.64	V
		vsel = 2.7 V in register BOOST_CR0		2.43	2.70	2.97	V
		vsel = 3.0 V in register BOOST_CR0		2.70	3.00	3.30	V
		vsel = 3.3 V in register BOOST_CR0		2.97	3.30	3.63	V
		vsel = 3.6 V in register BOOST_CR0		3.24	3.60	3.96	V
		vsel = 5.0 V in register BOOST_CR0		4.50	5.00	5.50	V
V_{BAT}	Input voltage to boost[35]	I_{OUT} = 0 mA–5 mA	vsel = 1.8 V–2.0 V, T_A = 0 °C–70 °C	0.5	–	0.8	V
		I_{OUT} = 0 mA–15 mA	vsel = 1.8 V–5.0 V[36], T_A = –10 °C–85 °C	1.6	–	3.6	V
		I_{OUT} = 0 mA–25 mA	vsel = 1.8 V–2.7 V, T_A = –10 °C–85 °C	0.8	–	1.6	V
		I_{OUT} = 0 mA–50 mA	vsel = 1.8 V–3.3 V[36], T_A = –40 °C–85 °C	1.8	–	2.5	V
			vsel = 1.8 V–3.3 V[36], T_A = –10 °C–85 °C	1.3	–	2.5	V
			vsel = 2.5 V–5.0 V[36], T_A = –10 °C–85 °C	2.5	–	3.6	V
I_{OUT}	Output current	T_A = 0 °C–70 °C	V_{BAT} = 0.5 V–0.8 V	0	–	5	mA
		T_A = –10 °C–85 °C	V_{BAT} = 1.6 V–3.6 V	0	–	15	mA
			V_{BAT} = 0.8 V–1.6 V	0	–	25	mA
			V_{BAT} = 1.3 V–2.5 V	0	–	50	mA
			V_{BAT} = 2.5 V–3.6 V	0	–	50	mA
		T_A = –40 °C–85 °C	V_{BAT} = 1.8 V–2.5 V	0	–	50	mA
I_{LPK}	Inductor peak current			–	–	700	mA
I_Q	Quiescent current	Boost active mode		–	250	–	µA
		Boost sleep mode, I_{OUT} < 1 µA		–	25	–	µA
Reg_{LOAD}	Load regulation			–	–	10	%
Reg_{LINE}	Line regulation			–	–	10	%

Notes
34. Listed vsel options are characterized. Additional vsel options are valid and guaranteed by design.
35. The boost will start at all valid V_{BAT} conditions including down to V_{BAT} = 0.5 V.
36. If V_{BAT} is greater than or equal to V_{OUT} boost setting, then V_{OUT} will be less than V_{BAT} due to resistive losses in the boost circuit.

Figure 11-11. Efficiency vs V_{BAT}, L_{BOOST} = 4.7 µH [38]

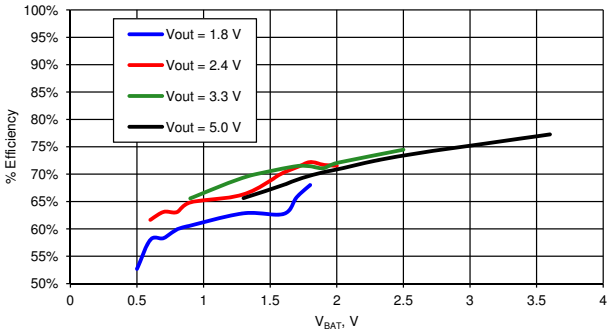


Figure 11-12. Efficiency vs V_{BAT}, L_{BOOST} = 10 µH [38]

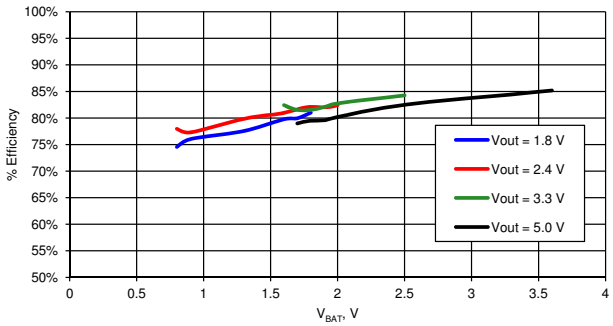


Figure 11-13. Efficiency vs V_{BAT}, L_{BOOST} = 22 µH [38]

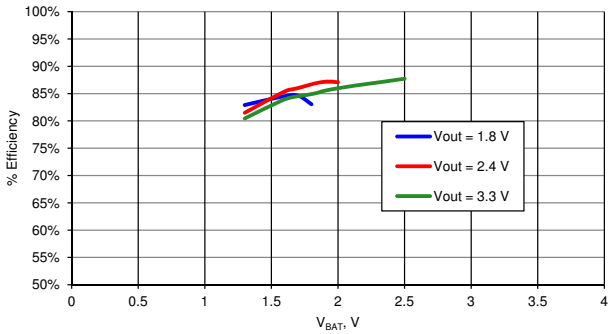
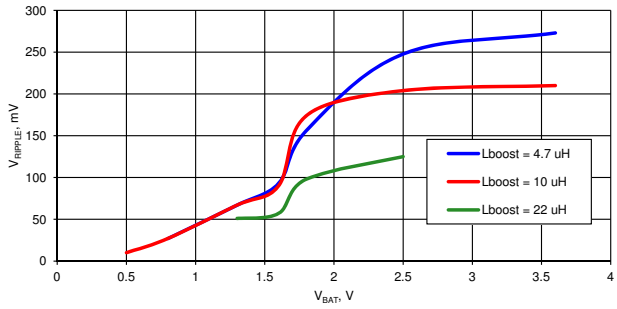


Figure 11-14. V_{RIPPLE} vs V_{BAT} [38]



Note
38. Typical example. Actual values may vary depending on external component selection, PCB layout, and other design parameters.

Table 11-12. SIO AC Specifications *(continued)*

Parameter	Description	Conditions	Min	Typ	Max	Units
Fsioout	SIO output operating frequency					
	2.7 V < V_{DDIO} < 5.5 V, Unregulated output (GPIO) mode, fast strong drive mode	90/10% V_{DDIO} into 25 pF	–	–	33	MHz
	1.71 V < V_{DDIO} < 2.7 V, Unregulated output (GPIO) mode, fast strong drive mode	90/10% V_{DDIO} into 25 pF	–	–	16	MHz
	3.3 V < V_{DDIO} < 5.5 V, Unregulated output (GPIO) mode, slow strong drive mode	90/10% V_{DDIO} into 25 pF	–	–	5	MHz
	1.71 V < V_{DDIO} < 3.3 V, Unregulated output (GPIO) mode, slow strong drive mode	90/10% V_{DDIO} into 25 pF	–	–	4	MHz
	2.7 V < V_{DDIO} < 5.5 V, Regulated output mode, fast strong drive mode	Output continuously switching into 25 pF	–	–	20	MHz
	1.71 V < V_{DDIO} < 2.7 V, Regulated output mode, fast strong drive mode	Output continuously switching into 25 pF	–	–	10	MHz
	1.71 V < V_{DDIO} < 5.5 V, Regulated output mode, slow strong drive mode	Output continuously switching into 25 pF	–	–	2.5	MHz
Fsioin	SIO input operating frequency					
	1.71 V ≤ V_{DDIO} ≤ 5.5 V	90/10% V_{DDIO}	–	–	33	MHz

Figure 11-20. SIO Output Rise and Fall Times, Fast Strong Mode, V_{DDIO} = 3.3 V, 25 pF Load

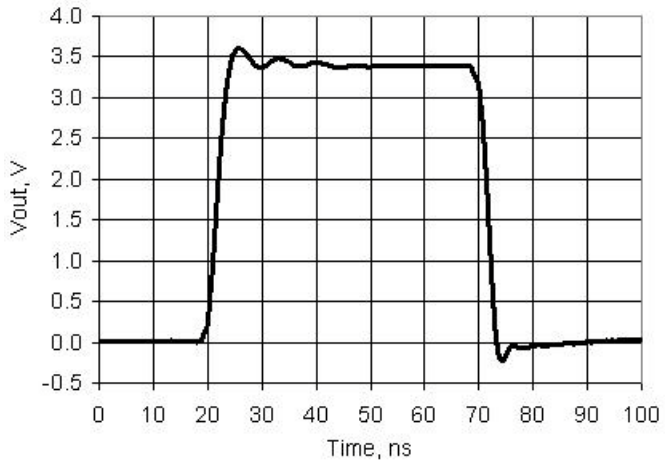


Figure 11-21. SIO Output Rise and Fall Times, Slow Strong Mode, V_{DDIO} = 3.3 V, 25 pF Load

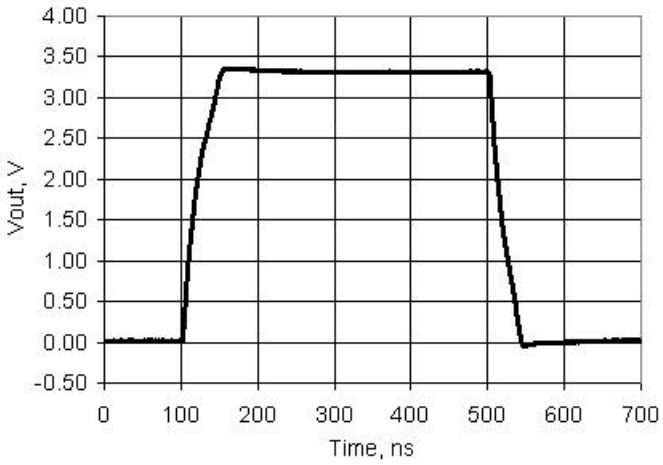


Figure 11-24. USBIO Output Rise and Fall Times, GPIO Mode, V_{DDD} = 3.3 V, 25 pF Load

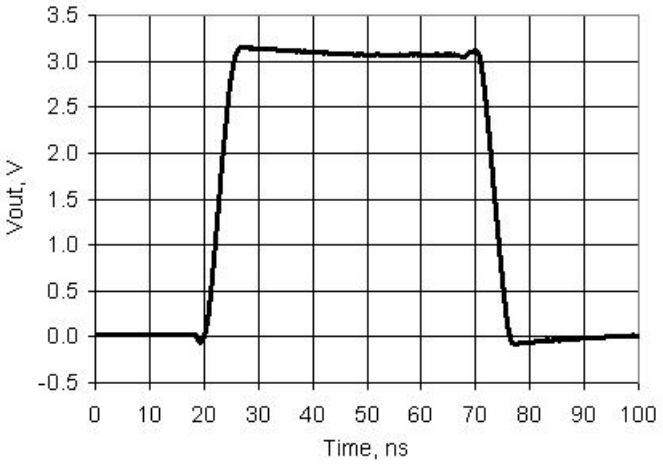


Table 11-16. USB Driver AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
Tr	Transition rise time		–	–	20	ns
Tf	Transition fall time		–	–	20	ns
TR	Rise/fall time matching	V_{USB_5}, $V_{USB\_3.3}$, see USB DC Specifications on page 111	90%	–	111%	
Vcrs	Output signal crossover voltage		1.3	–	2	V

11.5.2 Delta-sigma ADC

Unless otherwise specified, operating conditions are:

- Operation in continuous sample mode
- fclk = 3.072 MHz for resolution = 16 to 20 bits; fclk = 6.144 MHz for resolution = 8 to 15 bits
- Reference = 1.024 V internal reference bypassed on P3.2 or P0.3
- Unless otherwise specified, all charts and graphs show typical values

Table 11-21. 20-bit Delta-sigma ADC DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Resolution		8	–	20	bits
	Number of channels, single ended		–	–	No. of GPIO	–
	Number of channels, differential	Differential pair is formed using a pair of GPIOs.	–	–	No. of GPIO/2	–
	Monotonic	Yes	–	–	–	–
Ge	Gain error	Buffered, buffer gain = 1, Range = ±1.024 V, 16-bit mode, 25 °C	–	–	±0.2	%
Gd	Gain drift	Buffered, buffer gain = 1, Range = ±1.024 V, 16-bit mode	–	–	50	ppm/°C
Vos	Input offset voltage	Buffered, 16-bit mode, full voltage range	–	–	±0.2	mV
		Buffered, 16-bit mode, V_{DDA} = 1.8 V ±5%, 25 °C	–	–	±0.1	mV
TCVos	Temperature coefficient, input offset voltage	Buffer gain = 1, 16-bit, Range = ±1.024 V	–	–	1	µV/°C
	Input voltage range, single ended[47]		V_{SSA}	–	V_{DDA}	V
	Input voltage range, differential unbuffered[47]		V_{SSA}	–	V_{DDA}	V
	Input voltage range, differential, buffered[47]		V_{SSA}	–	V_{DDA} – 1	V
PSRRb	Power supply rejection ratio, buffered[47]	Buffer gain = 1, 16-bit, Range = ±1.024 V	90	–	–	dB
CMRRb	Common mode rejection ratio, buffered[47]	Buffer gain = 1, 16 bit, Range = ±1.024 V	85	–	–	dB
INL20	Integral non linearity[47]	Range = ±1.024 V, unbuffered	–	–	±32	LSB
DNL20	Differential non linearity[47]	Range = ±1.024 V, unbuffered	–	–	±1	LSB
INL16	Integral non linearity[47]	Range = ±1.024 V, unbuffered	–	–	±2	LSB
DNL16	Differential non linearity[47]	Range = ±1.024 V, unbuffered	–	–	±1	LSB
INL12	Integral non linearity[47]	Range = ±1.024 V, unbuffered	–	–	±1	LSB
DNL12	Differential non linearity[47]	Range = ±1.024 V, unbuffered	–	–	±1	LSB
INL8	Integral non linearity[47]	Range = ±1.024 V, unbuffered	–	–	±1	LSB
DNL8	Differential non linearity[47]	Range = ±1.024 V, unbuffered	–	–	±1	LSB
Rin_Buff	ADC input resistance	Input buffer used	10	–	–	MΩ
Rin_ADC16	ADC input resistance	Input buffer bypassed, 16-bit, Range = ±1.024 V	–	74[48]	–	kΩ
Rin_ADC12	ADC input resistance	Input buffer bypassed, 12 bit, Range = ±1.024 V	–	148[48]	–	kΩ
Rin_ExtRef	ADC external reference input resistance		–	70[48, 49]	–	kΩ

Notes

47. Based on device characterization (not production tested).
48. By using switched capacitors at the ADC input an effective input resistance is created. Holding the gain and number of bits constant, the resistance is proportional to the inverse of the clock frequency. This value is calculated, not measured. For more information see the Technical Reference Manual.
49. Recommend an external reference device with an output impedance <100 Ω, for example, the LM185/285/385 family. A 1-µF capacitor is recommended. For more information, see AN61290 - PSoC® 3 and PSoC 5LP Hardware Design Considerations.

Table 11-21. 20-bit Delta-sigma ADC DC Specifications *(continued)*

Parameter	Description	Conditions	Min	Typ	Max	Units
Vextref	ADC external reference input voltage, see also internal reference in Voltage Reference on page 95	Pins P0[3], P3[2]	0.9	–	1.3	V
Current Consumption						
I_{DD_20}	I_{DDA} + I_{DDD} current consumption, 20 bit[50]	187 sps, unbuffered	–	–	1.5	mA
I_{DD_16}	I_{DDA} + I_{DDD} current consumption, 16 bit[50]	48 ksps, unbuffered	–	–	1.5	mA
I_{DD_12}	I_{DDA} + I_{DDD} current consumption, 12 bit[50]	192 ksps, unbuffered	–	–	1.95	mA
I_{BUFF}	Buffer current consumption[50]		–	–	2.5	mA

Table 11-22. Delta-sigma ADC AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Startup time		–	–	4	Samples
THD	Total harmonic distortion[50]	Buffer gain = 1, 16 bit, Range = ±1.024 V	–	–	0.0032	%
20-Bit Resolution Mode						
SR20	Sample rate[50]	Range = ±1.024 V, unbuffered	7.8	–	187	sps
BW20	Input bandwidth at max sample rate[50]	Range = ±1.024 V, unbuffered	–	40	–	Hz
16-Bit Resolution Mode						
SR16	Sample rate[50]	Range = ±1.024 V, unbuffered	2	–	48	ksps
BW16	Input bandwidth at max sample rate[50]	Range = ±1.024 V, unbuffered	–	11	–	kHz
SINAD16int	Signal to noise ratio, 16-bit, internal reference[50]	Range = ±1.024V, unbuffered	81	–	–	dB
SINAD16ext	Signal to noise ratio, 16-bit, external reference[50]	Range = ±1.024 V, unbuffered	84	–	–	dB
12-Bit Resolution Mode						
SR12	Sample rate, continuous, high power[50]	Range = ±1.024 V, unbuffered	4	–	192	ksps
BW12	Input bandwidth at max sample rate[50]	Range = ±1.024 V, unbuffered	–	44	–	kHz
SINAD12int	Signal to noise ratio, 12-bit, internal reference[50]	Range = ±1.024 V, unbuffered	66	–	–	dB
8-Bit Resolution Mode						
SR8	Sample rate, continuous, high power[50]	Range = ±1.024 V, unbuffered	8	–	384	ksps
BW8	Input bandwidth at max sample rate[50]	Range = ±1.024 V, unbuffered	–	88	–	kHz
SINAD8int	Signal to noise ratio, 8-bit, internal reference[50]	Range = ±1.024 V, unbuffered	43	–	–	dB

Note
50. Based on device characterization (Not production tested).

Figure 11-37. Delta-sigma ADC DNL vs Output Code, 16-bit, 48 ksps, 25 °C V_{DDA} = 3.3 V

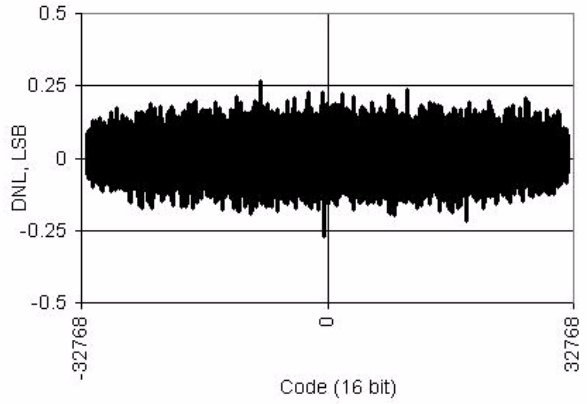
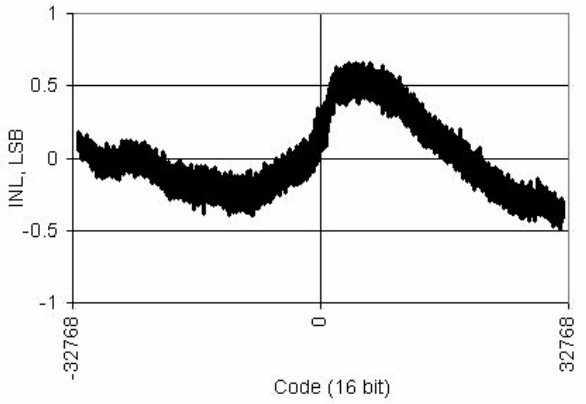


Figure 11-38. Delta-sigma ADC INL vs Output Code, 16-bit, 48 ksps, 25 °C V_{DDA} = 3.3 V



11.5.3 Voltage Reference

Table 11-28. Voltage Reference Specifications

See also ADC external reference specifications in *Section 11.5.2*.

Parameter	Description	Conditions		Min	Typ	Max	Units
V_{REF}[51]	Precision reference voltage	Initial trimming, 25 °C		1.023 (–0.1%)	1.024	1.025 (+0.1%)	V
	After typical PCB assembly, post reflow	Typical (non-optimized) board layout and 250 °C solder reflow. Device may be calibrated after assembly to improve performance	–40 °C	–	±0.5	–	%
			25 °C	–	±0.2	–	%
			85 °C	–	±0.2	–	%
	Temperature drift[52]	Box method		–	–	30	ppm/°C
	Long term drift			–	100	–	ppm/khr
	Thermal cycling drift (stability)[52, 53]			–	100	–	ppm

Figure 11-39. Voltage Reference vs. Temperature and V_{CCA}

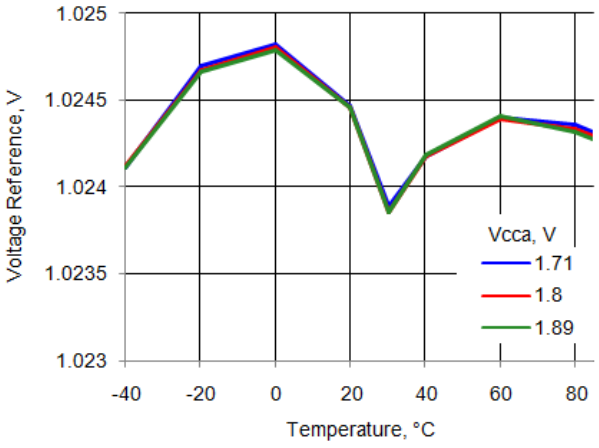
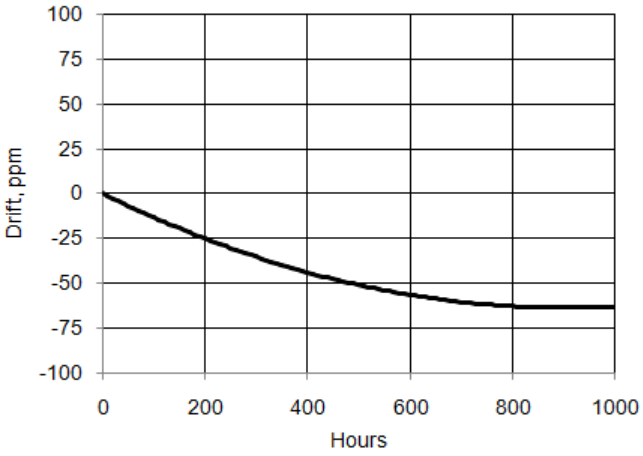


Figure 11-40. Voltage Reference Long-Term Drift



Notes
51. V_{REF} is measured after packaging, and thus accounts for substrate and die attach stresses
52. Based on device characterization (Not production tested).
53. After eight full cycles between –40 °C and 100 °C.

11.6.7 USB

Table 11-57. USB DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{USB_5}	Device supply (V_{DDD}) for USB operation	USB configured, USB regulator enabled	4.35	–	5.25	V
$V_{USB\_3.3}$		USB configured, USB regulator bypassed	3.15	–	3.6	V
V_{USB_3}		USB configured, USB regulator bypassed[60]	2.85	–	3.6	V
$I_{USB\_Configured}$	Device supply current in device active mode, bus clock and IMO = 24 MHz	V_{DDD} = 5 V, F_{CPU} = 1.5 MHz	–	10	–	mA
		V_{DDD} = 3.3 V, F_{CPU} = 1.5 MHz	–	8	–	mA
$I_{USB\_Suspended}$	Device supply current in device sleep mode	V_{DDD} = 5 V, connected to USB host, PICU configured to wake on USB resume signal	–	0.5	–	mA
		V_{DDD} = 5 V, disconnected from USB host	–	0.3	–	mA
		V_{DDD} = 3.3 V, connected to USB host, PICU configured to wake on USB resume signal	–	0.5	–	mA
		V_{DDD} = 3.3 V, disconnected from USB host	–	0.3	–	mA

11.6.8 Universal Digital Blocks (UDBs)

PSoC Creator provides a library of prebuilt and tested standard digital peripherals (UART, SPI, LIN, PRS, CRC, timer, counter, PWM, AND, OR, and so on) that are mapped to the UDB array. See the component data sheets in PSoC Creator for full AC/DC specifications, APIs, and example code.

Table 11-58. UDB AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
Datapath Performance						
F_{MAX_TIMER}	Maximum frequency of 16-bit timer in a UDB pair		–	–	67.01	MHz
F_{MAX_ADDER}	Maximum frequency of 16-bit adder in a UDB pair		–	–	67.01	MHz
F_{MAX_CRC}	Maximum frequency of 16-bit CRC/PRS in a UDB pair		–	–	67.01	MHz
PLD Performance						
F_{MAX_PLD}	Maximum frequency of a two-pass PLD function in a UDB pair		–	–	67.01	MHz
Clock to Output Performance						
t_{CLK_OUT}	Propagation delay for clock in to data out, see Figure 11-70.	25 °C, $V_{DDD} \geq 2.7$ V	–	20	25	ns
t_{CLK_OUT}	Propagation delay for clock in to data out, see Figure 11-70.	Worst-case placement, routing, and pin selection	–	–	55	ns

Note
60. Rise/fall time matching (TR) not guaranteed, see USB Driver AC Specifications on page 87.

11.9 Clocking

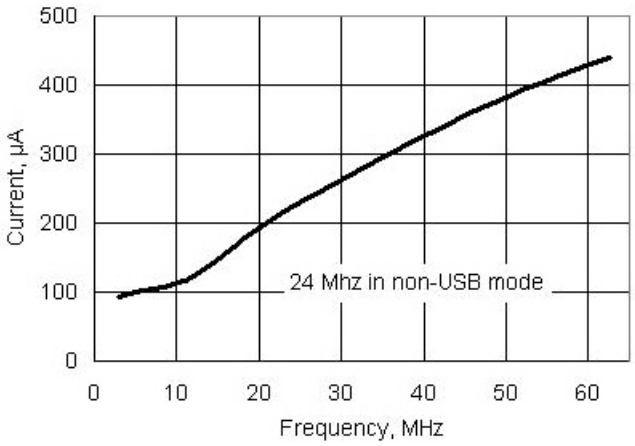
Specifications are valid for –40 °C ≤ T_A ≤ 85 °C and T_J ≤ 100 °C, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted. Unless otherwise specified, all charts and graphs show typical values.

11.9.1 Internal Main Oscillator

Table 11-77. IMO DC Specifications[73]

Parameter	Description	Conditions	Min	Typ	Max	Units
	Supply current					
	62.6 MHz		–	–	600	µA
	48 MHz		–	–	500	µA
	24 MHz – USB mode	With oscillator locking to USB bus	–	–	500	µA
	24 MHz – non USB mode		–	–	300	µA
	12 MHz		–	–	200	µA
	6 MHz		–	–	180	µA
	3 MHz		–	–	150	µA

Figure 11-75. IMO Current vs. Frequency



Note
73. Based on device characterization (Not production tested).

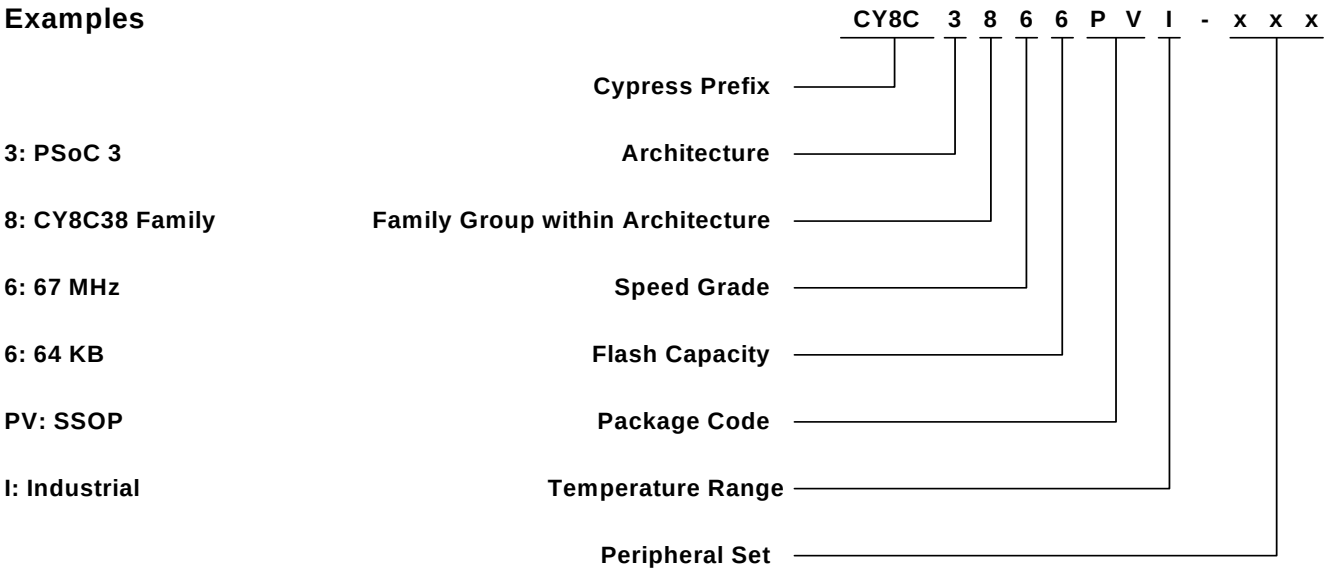
12.1 Part Numbering Conventions

PSoC 3 devices follow the part numbering convention described here. All fields are single character alphanumeric (0, 1, 2, …, 9, A, B, …, Z) unless stated otherwise.

CY8Cabcdefg-xxx

- a: Architecture
  - 3: PSoC 3
  - 5: PSoC 5
- b: Family group within architecture
  - 4: CY8C34 family
  - 6: CY8C36 family
  - 8: CY8C38 family
- c: Speed grade
  - 4: 48 MHz
  - 6: 67 MHz
- d: Flash capacity
  - 4: 16 KB
  - 5: 32 KB
  - 6: 64 KB
- ef: Package code
  - Two character alphanumeric
  - AX: TQFP
  - LT: QFN
  - PV: SSOP
  - FN: CSP
- g: Temperature range
  - C: commercial
  - I: industrial
  - A: automotive
- xxx: Peripheral set
  - Three character numeric
  - No meaning is associated with these three characters.

Examples



Tape and reel versions of these devices are available and are marked with a "T" at the end of the part number.

All devices in the PSoC 3 CY8C38 family comply to RoHS-6 specifications, demonstrating the commitment by Cypress to lead-free products. Lead (Pb) is an alloying element in solders that has resulted in environmental concerns due to potential toxicity. Cypress uses nickel-palladium-gold (NiPdAu) technology for the majority of leadframe-based packages.

A high-level review of the Cypress Pb-free position is available on our website. Specific package information is also available. Package Material Declaration data sheets (PMDDs) identify all substances contained within Cypress packages. PMDDs also confirm the absence of many banned substances. The information in the PMDDs will help Cypress customers plan for recycling or other “end of life” requirements.

Description Title: PSoC® 3: CY8C38 Family Datasheet Programmable System-on-Chip (PSoC®) *(continued)* Document Number: 001-11729				
Revision	**ECN**	**Submission Date**	**Orig. of Change**	**Description of Change**
*K	2903576	04/01/2010	MKEA	Updated Vb pin in PCB Schematic. Updated Tstartup parameter in AC Specifications table. Added Load regulation and Line regulation parameters to Inductive Boost Regulator DC Specifications table. Updated I_{CC} parameter in LCD Direct Drive DC Specs table. In page 1, updated internal oscillator range under Precision programmable clocking to start from 3 MHz. Updated I_{OUT} parameter in LCD Direct Drive DC Specs table. Updated Table 6-2 and Table 6-3. Added bullets on CapSense in page 1; added CapSense column in Section 12. Removed some references to footnote [1]. Changed INC_Rn cycles from 3 to 2 (Table 4-1). Added footnote in PLL AC Specification table. Added PLL intermediate frequency row with footnote in PLL AC Specs table. Added UDBs subsection under 11.6 Digital Peripherals. Updated Figure 2-6 (PCB Layout). Updated Pin Descriptions section and modified Figures 6-6, 6-8, 6-9. Updated LVD in Tables 6-2 and 6-3; modified Low-power modes bullet in page 1. Added note to Figures 2-5 and 6-2; Updated Figure 6-2 to add capacitors for V_{DDA} and V_{DDD} pins. Updated boost converter section (6.2.2). Updated Tstartup values in Table 11-3. Removed IPOR rows from Table 11-68. Updated 6.3.1.1, Power Voltage Level Monitors. Updated section 5.2 and Table 11-2 to correct suggestion of execution from flash. Updated V_{REF} specs in Table 11-21. Updated IDAC uncompensated gain error in Table 11-25. Updated Delay from Interrupt signal input to ISR code execution from ISR code in Table11-72. Removed other line in table. Added sentence to last paragraph of section 6.1.1.3. Updated T_{RESP}, high and low-power modes, in Table 11-24. Updated f_TCK values in Table 11-73 and f_SWDCK values in Table 11-74. Updated SNR condition in Table 11-20. Corrected unit of measurement in Table 11-21. Updated sleep wakeup time in Table 6-3 and Tsleep in Table 11-3. Added 1.71 V <= V_{DDD} < 3.3 V, SWD over USBIO pins value to Table 11-74. Removed mention of hibernate reset (HRES) from page 1 features, Table 6-3, Section 6.2.1.4, Section 6.3, and Section 6.3.1.1. Changed PPOR/PRES to TBDs in Section 6.3.1.1, Section 6.4.1.6 (changed PPOR to reset), Table 11-3 (changed PPOR to PRES), Table 11-68 (changed title, values TBD), and Table 11-69 (changed PPOR_TR to PRES_TR). Added sentence saying that LVD circuits can generate a reset to Section 6.3.1.1. Changed I_{DD} values on page 1, page 5, and Table 11-2. Changed resume time value in Section 6.2.1.3. Changed ESD HBM value in Table 11-1. Changed SNR in 16-bit resolution mode value and sample rate row in Table 11-20. Removed V_{DDA} = 1.65 V rows and changed BWag value in Table 11-22. Changed V_{IOFF} values and changed CMRR value in Table 11-23. Changed INL max value in Table 11-27. Added max value to the Quiescent current specs in Tables 11-29 and 11-31. Changed occurrences of “Block” to “Row” and deleted the “ECC not included” footnote in Table 11-57. Changed max response time value in Tables 11-69 and 11-71. Changed the Startup time in Table 11-79. Added condition to intermediate frequency row in Table 11-85. Added row to Table 11-69. Added brown out note to Section 11.8.1.

Description Title: PSoC® 3: CY8C38 Family Datasheet Programmable System-on-Chip (PSoC®) *(continued)* Document Number: 001-11729				
Revision	**ECN**	**Submission Date**	**Orig. of Change**	**Description of Change**
AA	4188568	11/14/2013	MKEA	Added SIO Comparator Specifications. Corrected typo in the V_{REF} parameter in the Voltage Reference Specifications. Added CSP information in Packaging and Ordering Information sections. Updated delta-sigma V_{OS} spec conditions.
AB	4385782	05/21/2014	MKEA	Updated General Description and Features. Added More Information and PSoC Creator sections. Updated 100-pin TQFP package diagram. Corrected number of I/O pins for CY8C3866FNI-210.
AC	4708125	03/31/2015	MKEA	Added INL4 and DNL4 specs in VDAC DC Specifications. Updated Figure 6-11. Added second note after Figure 6-4. Added a reference to Fig 6-1 in *Section 6.1.1* and *Section 6.1.2*. Updated *Section 6.2.2*. Added *Section 7.8.1*. Updated Boost specifications.
AD	4807497	06/23/2015	MKEA	Added reference to code examples in More Information. Updated typ value of TWRITE from 2 to 10 in EEPROM AC specs table. Changed “Device supply for USB operation" to "Device supply (VDDD) for USB operation" in USB DC Specifications. Clarified power supply sequencing and margin for VDDA and VDDD. Updated Serial Wire Debug Interface with limitations of debugging on Port 15. Updated Section 11.7.5. Updated Delta-sigma ADC DC Specifications
AE	4932879	09/24/2015	MKEA	Changed the Regulator Output Capacitor min and max from "-" to 0.9 and 1.1, respectively. Added reference to AN54439 in Section 11.9.3. Added MHz ECO DC specs table. Removed references to IPOR rearm issues in Section 6.3.1.1. Table 6-1: Changed DSI Fmax to 33 MHz Figure 6-1: Changed External I/O or DSI to 0-33 MHz. Table 11-10: Changed Fgpioin Max to 33 MHz Table 11-12: Changed Fsioin Max to 33 MHz.
AF	5322536	06/27/2016	MKEA	Updated More Information. Corrected typos in External Electrical Connections. Added links to CAD Libraries in Section 2.