## Details

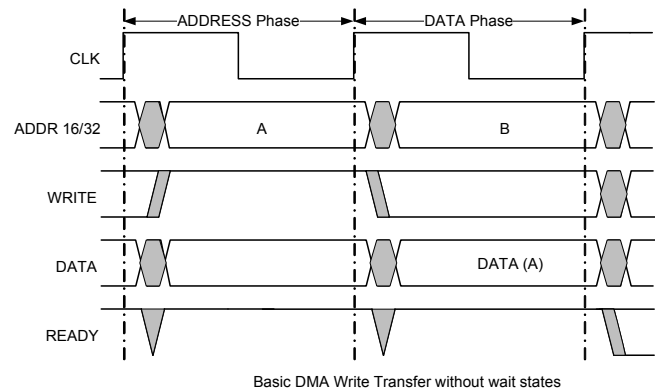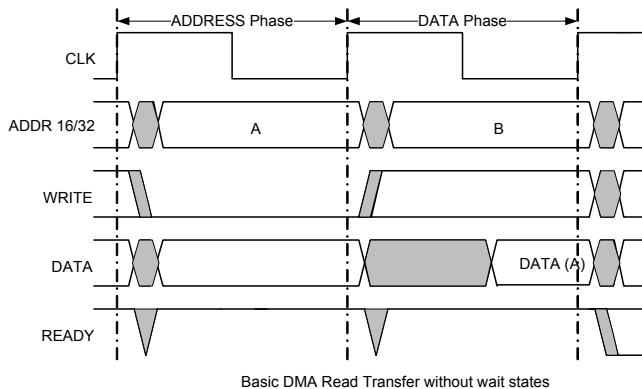| | |
|---|---|
| Product Status | Active |
| Core Processor | 8051 |
| Core Size | 8-Bit |
| Speed | 67MHz |
| Connectivity | EBI/EMI, I²C, LINbus, SPI, UART/USART, USB |
| Peripherals | CapSense, DMA, LCD, POR, PWM, WDT |
| Number of I/O | 38 |
| Program Memory Size | 64KB (64K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 2K x 8 |
| RAM Size | 8K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.71V ~ 5.5V |
| Data Converters | A/D 16x20b; D/A 4x8b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 68-VFQFN Exposed Pad |
| Supplier Device Package | 68-QFN (8x8) |
| Purchase URL | https://www.e-xfl.com/product-detail/infineon-technologies/cy8c3866lti-030 |

**Figure 2-5. 68-pin QFN Part Pinout**[7]

Top side pins (left to right, 68–52):
P2[5] (GPIO), VDDIO2, P2[4] (GPIO), P2[3] (GPIO), P2[2] (GPIO), P2[1] (GPIO), P2[0] (GPIO), P15[5] (GPOI), P15[4] (GPIO), VDDD, VSSD, VCCD, P0[7] (GPIO, IDAC2), P0[6] (GPIO, IDAC0), P0[5] (GPIO, Opamp2-), P0[4] (GPIO, Opamp2+), VDDIO0

Left side pins (1–17):
(GPIO) P2[6] — 1
(GPIO) P2[7] — 2
(I2C0: SCL, SIO) P12[4] — 3
(I2C0: SDA, SIO) P12[5] — 4
VSSB — 5
IND — 6
VBOOST — 7
VBAT — 8
VSSD — 9
XRES — 10
(TMS, SWDIO, GPIO) P1[0] — 11
(TCK, SWDCK, GPIO) P1[1] — 12
(Configurable XRES, GPIO) P1[2] — 13
(TDO, SWV, GPIO) P1[3] — 14
(TDI, GPIO) P1[4] — 15
(nTRST, GPIO) P1[5] — 16
VDDIO1 — 17

LINES SHOW VDDIO TO I/O SUPPLY ASSOCIATION

QFN
(TOP VIEW)

Right side pins (51–35):
51 — P0[3] (GPIO, Opamp0-/EXTREF0)
50 — P0[2] (GPIO, Opamp0+)
49 — P0[1] (GPIO, Opamp0OUT)
48 — P0[0] (GPIO, Opamp2OUT)
47 — P12[3] (SIO)
46 — P12[2] (SIO)
45 — VSSD
44 — VDDA
43 — VSSA
42 — VCCA
41 — P15[3] (GPIO, KHZ XTAL: XI)
40 — P15[2] (GPIO, KHZ XTAL: XO)
39 — P12[1] (SIO, I2C1: SDA)
38 — P12[0] (SIO, 12C1: SCL)
37 — P3[7] (GPIO, Opamp3OUT)
36 — P3[6] (GPIO, Opamp1OUT)
35 — VDDIO3

Bottom side pins (18–34):
18 — (GPIO) P1[6]
19 — (GPIO) P1[7]
20 — (SIO) P12[6]
21 — (SIO) P12[7]
22 — [8] (USBIO, D+, SWDIO) P15[6]
23 — [8] (USBIO, D-, SWDCK) P15[7]
24 — VDDD
25 — VSSD
26 — VCCD
27 — (MHZ XTAL: XO, GPIO) P15[0]
28 — (MHZ XTAL: XI, GPIO) P15[1]
29 — (IDAC1, GPIO) P3[0]
30 — (IDAC3, GPIO) P3[1]
31 — (OpAmp3-/Extref1, GPIO) P3[2]
32 — (Opamp3+, GPIO) P3[3]
33 — Opamp(1-, GPIO) P3[4]
34 — (Opamp1+, GPIO) P3[5]

**Notes**
7. The center pad on the QFN package should be connected to digital ground ($V_{SSD}$) for best mechanical, thermal, and electrical performance. If not connected to ground, it should be electrically floated and not connected to any other signal. For more information, see AN72845, Design Guidelines for QFN Devices
8. Pins are Do Not Use (DNU) on devices without USB. The pin must be left floating.

**Figure 4-1. DMA Timing Diagram**



Basic DMA Read Transfer without wait states



Basic DMA Write Transfer without wait states

#### 4.4.4.2 Auto Repeat DMA

Auto repeat DMA is typically used when a static pattern is repetitively read from system memory and written to a peripheral. This is done with a single TD that chains to itself.

#### 4.4.4.3 Ping Pong DMA

A ping pong DMA case uses double buffering to allow one buffer to be filled by one client while another client is consuming the data previously received in the other buffer. In its simplest form, this is done by chaining two TDs together so that each TD calls the opposite TD when complete.

#### 4.4.4.4 Circular DMA

Circular DMA is similar to ping pong DMA except it contains more than two buffers. In this case there are multiple TDs; after the last TD is complete it chains back to the first TD.

#### 4.4.4.5 Scatter Gather DMA

In the case of scatter gather DMA, there are multiple noncontiguous sources or destinations that are required to effectively carry out an overall DMA transaction. For example, a packet may need to be transmitted off of the device and the packet elements, including the header, payload, and trailer, exist in various noncontiguous locations in memory. Scatter gather DMA allows the segments to be concatenated together by using multiple TDs in a chain. The chain gathers the data from the multiple locations. A similar concept applies for the reception of data onto the device. Certain parts of the received data may need to be scattered to various locations in memory for software processing convenience. Each TD in the chain specifies the location for each discrete element in the chain.

#### 4.4.4.6 Packet Queuing DMA

Packet queuing DMA is similar to scatter gather DMA but specifically refers to packet protocols. With these protocols, there may be separate configuration, data, and status phases associated with sending or receiving a packet.

For instance, to transmit a packet, a memory mapped configuration register can be written inside a peripheral, specifying the overall length of the ensuing data phase. The CPU can set up this configuration information anywhere in system memory and copy it with a simple TD to the peripheral. After the configuration phase, a data phase TD (or a series of data phase TDs) can begin (potentially using scatter gather). When the data

phase TD(s) finish, a status phase TD can be invoked that reads some memory mapped status information from the peripheral and copies it to a location in system memory specified by the CPU for later inspection. Multiple sets of configuration, data, and status phase 'subchains' can be strung together to create larger chains that transmit multiple packets in this way. A similar concept exists in the opposite direction to receive the packets.

#### 4.4.4.7 Nested DMA

One TD may modify another TD, as the TD configuration space is memory mapped similar to any other peripheral. For example, a first TD loads a second TD's configuration and then calls the second TD. The second TD moves data as required by the application. When complete, the second TD calls the first TD, which again updates the second TD's configuration. This process repeats as often as necessary.

### 4.5 Interrupt Controller

The interrupt controller provides a mechanism for hardware resources to change program execution to a new address, independent of the current task being executed by the main code. The interrupt controller provides enhanced features not found on original 8051 interrupt controllers:

■ Thirty-two interrupt vectors

■ Jumps directly to ISR anywhere in code space with dynamic vector addresses

■ Multiple sources for each vector

■ Flexible interrupt to vector matching

■ Each interrupt vector is independently enabled or disabled

■ Each interrupt can be dynamically assigned one of eight priorities

■ Eight level nestable interrupts

■ Multiple I/O interrupt vectors

■ Software can send interrupts

■ Software can clear pending interrupts

Figure 4-2 on page 20 represents typical flow of events when an interrupt triggered. Figure 4-3 on page 21 shows the interrupt structure and priority polling.

**Figure 4-2. Interrupt Processing Timing Diagram**
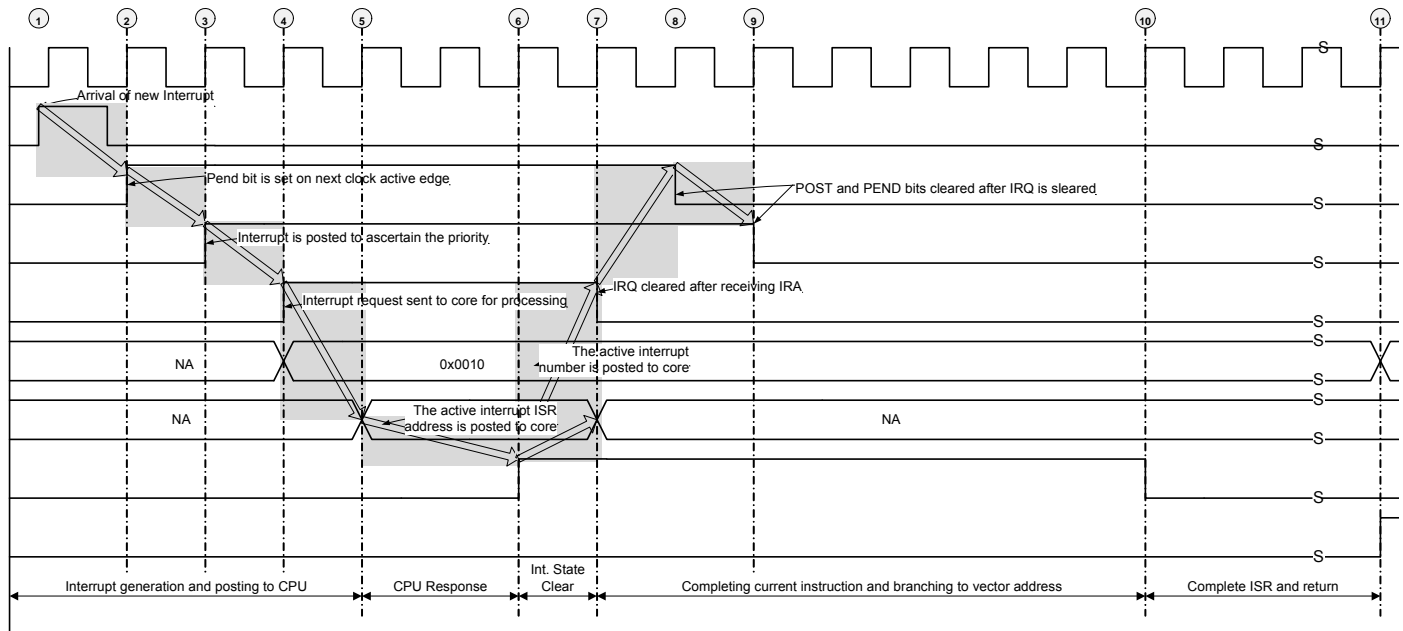


## Notes
- 1: Interrupt triggered asynchronous to the clock
- 2: The PEND bit is set on next active clock edge to indicate the interrupt arrival
- 3: POST bit is set following the PEND bit
- 4: Interrupt request and the interrupt number sent to CPU core after evaluation priority (Takes 3 clocks)
- 5: ISR address is posted to CPU core for branching
- 6: CPU acknowledges the interrupt request
- 7: ISR address is read by CPU for branching
- 8, 9: PEND and POST bits are cleared respectively after receiving the IRA from core
- 10: IRA bit is cleared after completing the current instruction and starting the instruction execution from ISR location (Takes 7 cycles)
- 11: IRC is set to indicate the completion of ISR, Active int. status is restored with previous status

The total interrupt latency (ISR execution)

= POST + PEND + IRQ + IRA + Completing current instruction and branching

= 1+1+1+2+7 cycles

= 12 cycles

**Figure 6-3. 32kHzECO Block Diagram**
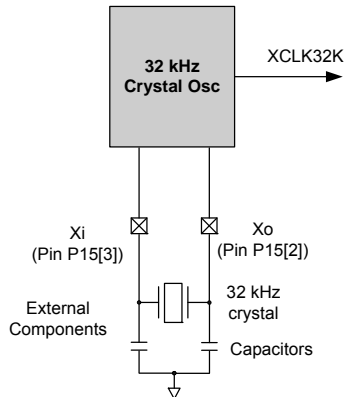


It is recommended that the external 32.768-kHz watch crystal have a load capacitance (CL) of 6 pF or 12.5 pF. Check the crystal manufacturer's datasheet. The two external capacitors, CL1 and CL2, are typically of the same value, and their total capacitance, CL1CL2 / (CL1 + CL2), including pin and trace capacitance, should equal the crystal CL value. For more information, refer to application note AN54439: PSoC 3 and PSoC 5 External Oscillators. See also pin capacitance specifications in the "GPIO" section on page 80.

*6.1.2.3 Digital System Interconnect*

The DSI provides routing for clocks taken from external clock oscillators connected to I/O. The oscillators can also be generated within the device in the digital system and UDBs.

While the primary DSI clock input provides access to all clocking resources, up to eight other DSI clocks (internally or externally generated) may be routed directly to the eight digital clock dividers. This is only possible if there are multiple precision clock sources.

*6.1.3 Clock Distribution*

All seven clock sources are inputs to the central clock distribution system. The distribution system is designed to create multiple high precision clocks. These clocks are customized for the design's requirements and eliminate the common problems found with limited resolution prescalers attached to peripherals.

The clock distribution system generates several types of clock trees.

■ The master clock is used to select and supply the fastest clock in the system for general clock requirements and clock synchronization of the PSoC device.

■ Bus clock 16-bit divider uses the master clock to generate the bus clock used for data transfers. Bus clock is the source clock for the CPU clock divider.

■ Eight fully programmable 16-bit clock dividers generate digital system clocks for general use in the digital system, as configured by the design's requirements. Digital system clocks can generate custom clocks derived from any of the seven clock sources for any purpose. Examples include baud rate generators, accurate PWM periods, and timer clocks, and many others. If more than eight digital clock dividers are required, the UDBs and fixed function timer/counter/PWMs can also generate clocks.

■ Four 16-bit clock dividers generate clocks for the analog system components that require clocking, such as ADC and mixers. The analog clock dividers include skew control to ensure that critical analog events do not occur simultaneously with digital switching events. This is done to reduce analog system noise.

Each clock divider consists of an 8-input multiplexer, a 16-bit clock divider (divide by 2 and higher) that generates ~50 percent duty cycle clocks, master clock resynchronization logic, and deglitch logic. The outputs from each digital clock tree can be routed into the digital system interconnect and then brought back into the clock system as an input, allowing clock chaining of up to 32 bits.

*6.1.4 USB Clock Domain*

The USB clock domain is unique in that it operates largely asynchronously from the main clock network. The USB logic contains a synchronous bus interface to the chip, while running on an asynchronous clock to process USB data. The USB logic requires a 48 MHz frequency. This frequency can be generated from different sources, including DSI clock at 48 MHz or doubled value of 24 MHz from internal oscillator, DSI signal, or crystal oscillator.

## 6.2 Power System

The power system consists of separate analog, digital, and I/O supply pins, labeled VDDA, VDDD, and VDDIOX, respectively. It also includes two internal 1.8-V regulators that provide the digital (VCCD) and analog (VCCA) supplies for the internal core logic. The output pins of the regulators (VCCD and VCCA) and the

VDDIO pins must have capacitors connected as shown in Figure 6-4. The two VCCD pins must be shorted together, with as short a trace as possible, and connected to a 1-µF ±10-percent X5R capacitor. The power system also contains a sleep regulator, an I$^2$C regulator, and a hibernate regulator.

**Figure 6-4. PSoC Power System**
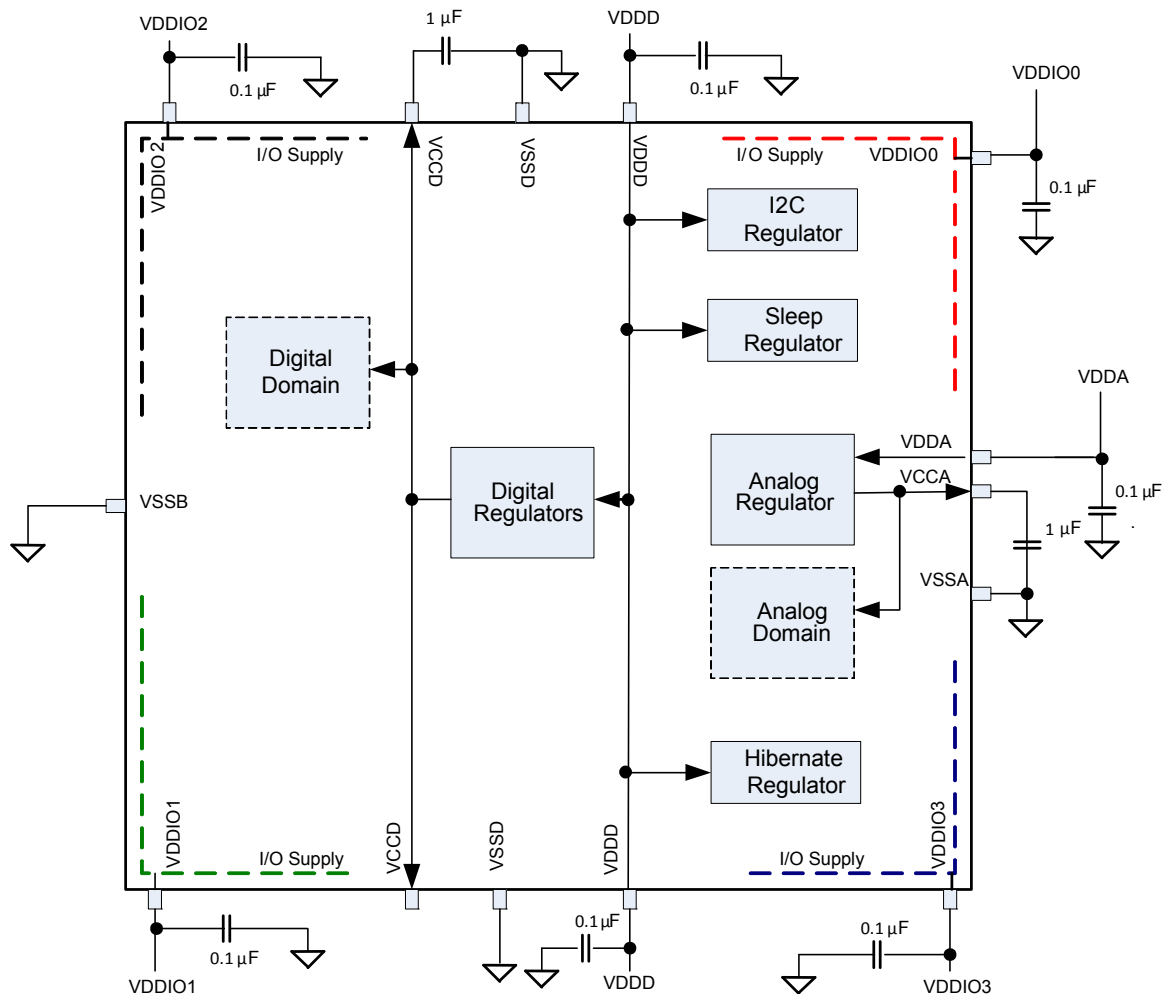


**Notes**

■ The two VCCD pins must be connected together with as short a trace as possible. A trace under the device is recommended, as shown in Figure 2-8 on page 12.

■ It is good practice to check the datasheets for your bypass capacitors, specifically the working voltage and the DC bias specifications. With some capacitors, the actual capacitance can decrease considerably when the DC bias (VDDX or VCCX in Figure 6-4) is a significant percentage of the rated working voltage.

■ You can power the device in internally regulated mode, where the voltage applied to the VDDx pins is as high as 5.5 V, and the internal regulators provide the core voltages. **In this mode, do not apply power to the VCCx pins, and do not tie the VDDx pins to the VCCx pins.**

■ You can also power the device in externally regulated mode, that is, by directly powering the VCCD and VCCA pins. In this configuration, the VDDD pins should be shorted to the VCCD pins and the VDDA pin should be shorted to the VCCA pin. The allowed supply range in this configuration is 1.71 V to 1.89 V. After power up in this configuration, the internal regulators are on by default, and should be disabled to reduce power consumption.

## 6.4 I/O System and Routing

PSoC I/Os are extremely flexible. Every GPIO has analog and digital I/O capability. All I/Os have a large number of drive modes, which are set at POR. PSoC also provides up to four individual I/O voltage domains through the VDDIO pins.

There are two types of I/O pins on every device; those with USB provide a third type. Both GPIO and SIO provide similar digital functionality. The primary differences are their analog capability and drive strength. Devices that include USB also provide two USBIO pins that support specific USB functionality as well as limited GPIO capability.

All I/O pins are available for use as digital inputs and outputs for both the CPU and digital peripherals. In addition, all I/O pins can generate an interrupt. The flexible and advanced capabilities of the PSoC I/O, combined with any signal to any pin routability, greatly simplify circuit design and board layout. All GPIO pins can be used for analog input, CapSense[13], and LCD segment drive, while SIO pins are used for voltages in excess of VDDA and for programmable output voltages.

- Features supported by both GPIO and SIO:
  - User programmable port reset state
  - Separate I/O supplies and voltages for up to four groups of I/O
  - Digital peripherals use DSI to connect the pins
  - Input or output or both for CPU and DMA
  - Eight drive modes
  - Every pin can be an interrupt source configured as rising edge, falling edge or both edges. If required, level sensitive interrupts are supported through the DSI
  - Dedicated port interrupt vector for each port

- Slew rate controlled digital output drive mode
- Access port control and configuration registers on either port basis or pin basis
- Separate port read (PS) and write (DR) data registers to avoid read modify write errors
- Special functionality on a pin by pin basis

- Additional features only provided on the GPIO pins:
  - LCD segment drive on LCD equipped devices
  - CapSense[13]
  - Analog input and output capability
  - Continuous 100 µA clamp current capability
  - Standard drive strength down to 1.7 V

- Additional features only provided on SIO pins:
  - Higher drive strength than GPIO
  - Hot swap capability (5 V tolerance at any operating $V_{DD}$)
  - Programmable and regulated high input and output drive levels down to 1.2 V
  - No analog input, CapSense, or LCD capability
  - Over voltage tolerance up to 5.5 V
  - SIO can act as a general purpose analog comparator

- USBIO features:
  - Full speed USB 2.0 compliant I/O
  - Highest drive strength for general purpose use
  - Input, output, or both for CPU and DMA
  - Input, output, or both for digital peripherals
  - Digital output (CMOS) drive mode
  - Each pin can be an interrupt source configured as rising edge, falling edge, or both edges

**Note**
13. GPIOs with opamp outputs are not recommended for use with CapSense.

### 6.4.5 Pin Interrupts

All GPIO and SIO pins are able to generate interrupts to the system. All eight pins in each port interface to their own Port Interrupt Control Unit (PICU) and associated interrupt vector. Each pin of the port is independently configurable to detect rising edge, falling edge, both edge interrupts, or to not generate an interrupt.

Depending on the configured mode for each pin, each time an interrupt event occurs on a pin, its corresponding status bit of the interrupt status register is set to '1' and an interrupt request is sent to the interrupt controller. Each PICU has its own interrupt vector in the interrupt controller and the pin status register providing easy determination of the interrupt source down to the pin level.

Port pin interrupts remain active in all sleep modes allowing the PSoC device to wake from an externally generated interrupt. While level sensitive interrupts are not directly supported; UDB provide this functionality to the system when needed.

### 6.4.6 Input Buffer Mode

GPIO and SIO input buffers can be configured at the port level for the default CMOS input thresholds or the optional LVTTL input thresholds. All input buffers incorporate Schmitt triggers for input hysteresis. Additionally, individual pin input buffers can be disabled in any drive mode.

### 6.4.7 I/O Power Supplies

Up to four I/O pin power supplies are provided depending on the device and package. Each I/O supply must be less than or equal to the voltage on the chip's analog (VDDA) pin. This feature allows users to provide different I/O voltage levels for different pins on the device. Refer to the specific device package pinout to determine VDDIO capability for a given port and pin. The SIO port pins support an additional regulated high output capability, as described in Adjustable Output Level.

### 6.4.8 Analog Connections

These connections apply only to GPIO pins. All GPIO pins may be used as analog inputs or outputs. The analog voltage present on the pin must not exceed the VDDIO supply voltage to which the GPIO belongs. Each GPIO may connect to one of the analog global busses or to one of the analog mux buses to connect any pin to any internal analog resource such as ADC or comparators. In addition, select pins provide direct connections to specific analog features such as the high current DACs or uncommitted opamps.

### 6.4.9 CapSense

This section applies only to GPIO pins. All GPIO pins may be used to create CapSense buttons and sliders[15]. See the "CapSense" section on page 63 for more information.

### 6.4.10 LCD Segment Drive

This section applies only to GPIO pins. All GPIO pins may be used to generate Segment and Common drive signals for direct glass drive of LCD glass. See the "LCD Direct Drive" section on page 62 for details.

### 6.4.11 Adjustable Output Level

This section applies only to SIO pins. SIO port pins support the ability to provide a regulated high output level for interface to external signals that are lower in voltage than the SIO's respective VDDIO. SIO pins are individually configurable to output either the standard VDDIO level or the regulated output, which is based on an internally generated reference. Typically a voltage DAC (VDAC) is used to generate the reference (see Figure 6-13). The "DAC" section on page 64 has more details on VDAC use and reference routing to the SIO pins. Resistive pullup and pull-down drive modes are not available with SIO in regulated output mode.

### 6.4.12 Adjustable Input Level

This section applies only to SIO pins. SIO pins by default support the standard CMOS and LVTTL input levels but also support a differential mode with programmable levels. SIO pins are grouped into pairs. Each pair shares a reference generator block which, is used to set the digital input buffer reference level for interface to external signals that differ in voltage from VDDIO. The reference sets the pins voltage threshold for a high logic level (see Figure 6-13). Available input thresholds are:

- $0.5 \times$ VDDIO

- $0.4 \times$ VDDIO

- $0.5 \times V_{REF}$

- $V_{REF}$

Typically a voltage DAC (VDAC) generates the $V_{REF}$ reference. "DAC" section on page 64 has more details on VDAC use and reference routing to the SIO pins.

---

**Note**
15. GPIOs with opamp outputs are not recommended for use with CapSense.

### 7.2.2 Datapath Module

The datapath contains an 8-bit single cycle ALU, with associated compare and condition generation logic. This datapath block is optimized to implement embedded functions, such as timers, counters, integrators, PWMs, PRS, CRC, shifters and dead band generators and many others.

**Figure 7-4. Datapath Top Level**
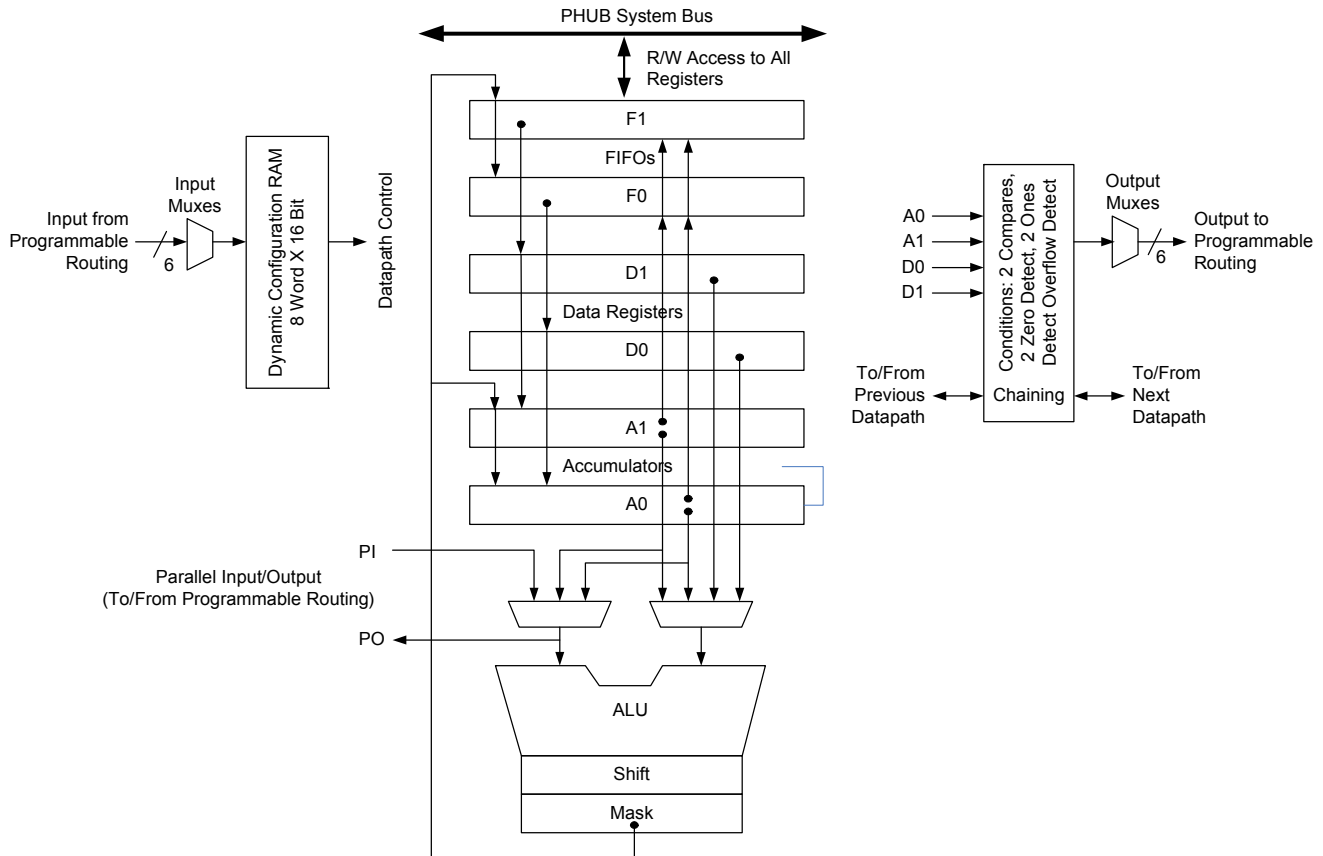
### 7.2.2.1 Working Registers

The datapath contains six primary working registers, which are accessed by CPU firmware or DMA during normal operation.

**Table 7-1. Working Datapath Registers**

| Name | Function | Description |
|------|----------|-------------|
| A0 and A1 | Accumulators | These are sources and sinks for the ALU and also sources for the compares. |
| D0 and D1 | Data Registers | These are sources for the ALU and sources for the compares. |
| F0 and F1 | FIFOs | These are the primary interface to the system bus. They can be a data source for the data registers and accumulators or they can capture data from the accumulators or ALU. Each FIFO is four bytes deep. |

### 7.2.2.2 Dynamic Configuration RAM

Dynamic configuration is the ability to change the datapath function and internal configuration on a cycle-by-cycle basis, under sequencer control. This is implemented using the 8-word × 16-bit configuration RAM, which stores eight unique 16-bit wide configurations. The address input to this RAM controls the sequence, and can be routed from any block connected to the UDB routing matrix, most typically PLD logic, I/O pins, or from the outputs of this or other datapath blocks.

**ALU**

The ALU performs eight general purpose functions. They are:

- Increment
- Decrement
- Add
- Subtract
- Logical AND
- Logical OR
- Logical XOR
- Pass, used to pass a value through the ALU to the shift register, mask, or another UDB register.

### 11.4.4 XRES

**Table 11-17. XRES DC Specifications**

| Parameter | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input voltage high threshold | | $0.7 \times V_{DDIO}$ | – | – | V |
| $V_{IL}$ | Input voltage low threshold | | – | – | $0.3 \times V_{DDIO}$ | V |
| Rpullup | Pull-up resistor | | 3.5 | 5.6 | 8.5 | kΩ |
| $C_{IN}$ | Input capacitance[46] | | – | 3 | – | pF |
| $V_H$ | Input voltage hysteresis (Schmitt-Trigger)[46] | | – | 100 | – | mV |
| Idiode | Current through protection diode to $V_{DDIO}$ and $V_{SSIO}$ | | – | – | 100 | µA |

**Table 11-18. XRES AC Specifications**

| Parameter | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $T_{RESET}$ | Reset pulse width | | 1 | – | – | µs |

## 11.5 Analog Peripherals

Specifications are valid for –40 °C ≤ $T_A$ ≤ 85 °C and $T_J$ ≤ 100 °C, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

### 11.5.1 Opamp

**Table 11-19. Opamp DC Specifications**

| Parameter | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_I$ | Input voltage range | | $V_{SSA}$ | – | $V_{DDA}$ | V |
| $V_{OS}$ | Input offset voltage | | – | – | 2.5 | mV |
| | | Operating temperature –40 °C to 70 °C | – | – | 2 | mV |
| $TCV_{OS}$ | Input offset voltage drift with temperature | Power mode = high | – | – | ±30 | µV/ °C |
| Ge1 | Gain error, unity gain buffer mode | Rload = 1 kΩ | – | – | ±0.1 | % |
| $C_{IN}$ | Input capacitance | Routing from pin | – | – | 18 | pF |
| $V_O$ | Output voltage range | 1 mA, source or sink, power mode = high | $V_{SSA}$ + 0.05 | – | $V_{DDA}$ – 0.05 | V |
| $I_{OUT}$ | Output current capability, source or sink | $V_{SSA}$ + 500 mV ≤ Vout ≤ $V_{DDA}$ –500 mV, $V_{DDA}$ > 2.7 V | 25 | – | – | mA |
| | | $V_{SSA}$ + 500 mV ≤ Vout ≤ $V_{DDA}$ –500 mV, 1.7 V = $V_{DDA}$ ≤ 2.7 V | 16 | – | – | mA |
| $I_{DD}$ | Quiescent current | Power mode = min | – | 250 | 400 | uA |
| | | Power mode = low | – | 250 | 400 | uA |
| | | Power mode = med | – | 330 | 950 | uA |
| | | Power mode = high | – | 1000 | 2500 | uA |
| CMRR | Common mode rejection ratio | | 80 | – | – | dB |
| PSRR | Power supply rejection ratio | $V_{DDA}$ ≥ 2.7 V | 85 | – | – | dB |
| | | $V_{DDA}$ < 2.7 V | 70 | – | – | dB |
| $I_{IB}$ | Input bias current[46] | 25 °C | – | 10 | – | pA |

**Note**
46. Based on device characterization (Not production tested).

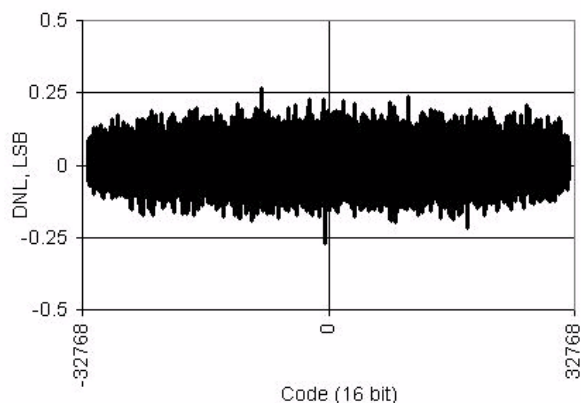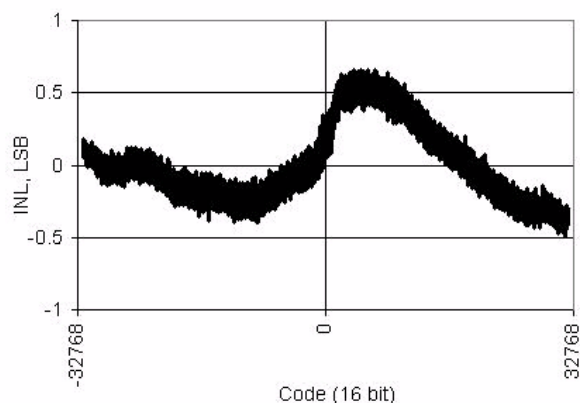**Figure 11-37. Delta-sigma ADC DNL vs Output Code, 16-bit, 48 ksps, 25 °C $V_{DDA}$ = 3.3 V**



**Figure 11-38. Delta-sigma ADC INL vs Output Code, 16-bit, 48 ksps, 25 °C $V_{DDA}$ = 3.3 V**



### 11.5.3 Voltage Reference

**Table 11-28. Voltage Reference Specifications**

See also ADC external reference specifications in *Section 11.5.2*.

| Parameter | Description | Conditions | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| $V_{REF}$[51] | Precision reference voltage | Initial trimming, 25 °C | | 1.023 (–0.1%) | 1.024 | 1.025 (+0.1%) | V |
| | After typical PCB assembly, post reflow | Typical (non-optimized) board layout and 250 °C solder reflow. Device may be calibrated after assembly to improve performance | –40 °C | – | ±0.5 | – | % |
| | | | 25 °C | – | ±0.2 | – | % |
| | | | 85 °C | – | ±0.2 | – | % |
| | Temperature drift[52] | Box method | | – | – | 30 | ppm/°C |
| | Long term drift | | | – | 100 | – | ppm/khr |
| | Thermal cycling drift (stability)[52, 53] | | | – | 100 | – | ppm |

**Figure 11-39. Voltage Reference vs. Temperature and $V_{CCA}$**
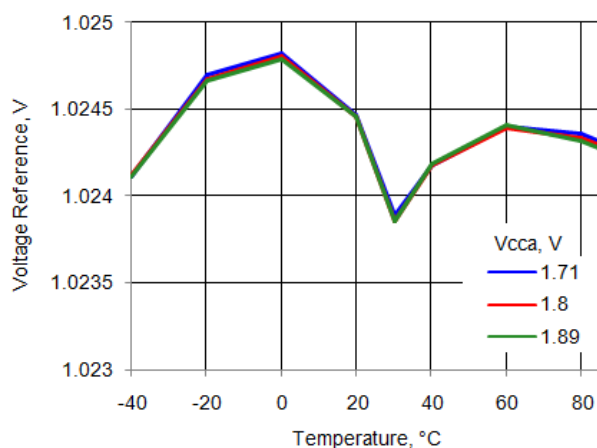


**Figure 11-40. Voltage Reference Long-Term Drift**
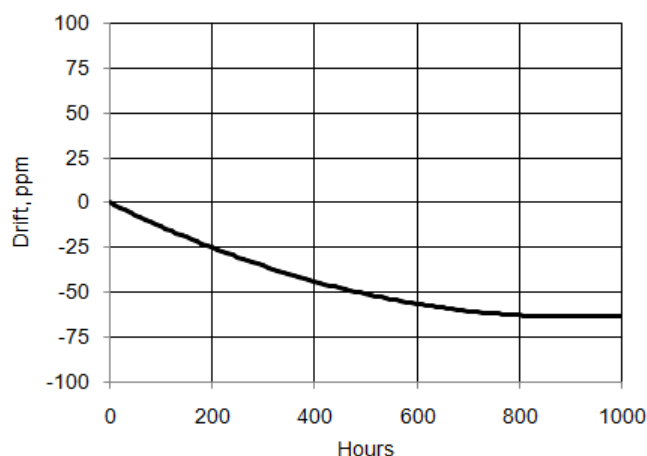


**Notes**
51. $V_{REF}$ is measured after packaging, and thus accounts for substrate and die attach stresses
52. Based on device characterization (Not production tested).
53. After eight full cycles between –40 °C and 100 °C.

### 11.5.6 Current Digital-to-analog Converter (IDAC)

All specifications are based on use of the low-resistance IDAC output pins (see Pin Descriptions on page 12 for details). See the IDAC component data sheet in PSoC Creator for full electrical specifications and APIs.

Unless otherwise specified, all charts and graphs show typical values.

**Table 11-32. IDAC DC Specifications**

| Parameter | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| | Resolution | | – | – | 8 | bits |
| $I_{OUT}$ | Output current at code = 255 | Range = 2.04 mA, code = 255, $V_{DDA} \geq 2.7$ V, Rload = 600 $\Omega$ | – | 2.04 | – | mA |
| | | Range = 2.04 mA, high speed mode, code = 255, $V_{DDA} \leq 2.7$ V, Rload = 300 $\Omega$ | – | 2.04 | – | mA |
| | | Range = 255 µA, code = 255, Rload = 600 $\Omega$ | – | 255 | – | µA |
| | | Range = 31.875 µA, code = 255, Rload = 600 $\Omega$ | – | 31.875 | – | µA |
| | Monotonicity | | – | – | Yes | |
| Ezs | Zero scale error | | – | 0 | ±1 | LSB |
| Eg | Gain error | Range = 2.04 mA, 25 °C | – | – | ±2.5 | % |
| | | Range = 255 µA, 25 ° C | – | – | ±2.5 | % |
| | | Range = 31.875 µA, 25 ° C | – | – | ±3.5 | % |
| TC_Eg | Temperature coefficient of gain error | Range = 2.04 mA | – | – | 0.04 | % / °C |
| | | Range = 255 µA | – | – | 0.04 | % / °C |
| | | Range = 31.875 µA | – | – | 0.05 | % / °C |
| INL | Integral nonlinearity | Sink mode, range = 255 µA, Codes 8 – 255, Rload = 2.4 k$\Omega$, Cload = 15 pF | – | ±0.9 | ±1 | LSB |
| | | Source mode, range = 255 µA, Codes 8 – 255, Rload = 2.4 k$\Omega$, Cload = 15 pF | – | ±1.2 | ±1.6 | LSB |
| DNL | Differential nonlinearity | Sink mode, range = 255 µA, Rload = 2.4 k$\Omega$, Cload = 15 pF | – | ±0.3 | ±1 | LSB |
| | | Source mode, range = 255 µA, Rload = 2.4 k$\Omega$, Cload = 15 pF | – | ±0.3 | ±1 | LSB |
| Vcompliance | Dropout voltage, source or sink mode | Voltage headroom at max current, Rload to $V_{DDA}$ or Rload to $V_{SSA}$, Vdiff from $V_{DDA}$ | 1 | – | – | V |

**Figure 11-49. IDAC Operating Current vs Temperature, Range = 255 µA, Code = 0, Source Mode**
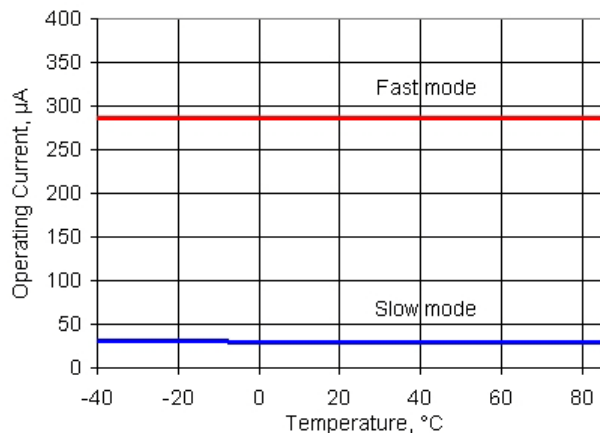


**Figure 11-50. IDAC Operating Current vs Temperature, Range = 255 µA, Code = 0, Sink Mode**
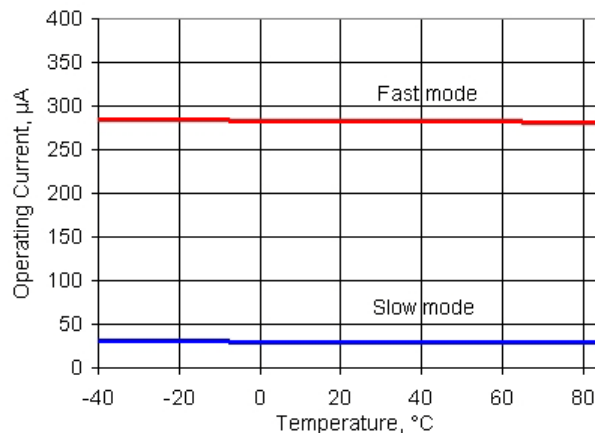


**Table 11-33. IDAC AC Specifications**

| Parameter | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $F_{DAC}$ | Update rate | | – | – | 8 | Msps |
| $T_{SETTLE}$ | Settling time to 0.5 LSB | Range = 31.875 µA or 255 µA, full scale transition, High speed mode, 600 Ω 15-pF load | – | – | 125 | ns |
| | Current noise | Range = 255 µA, source mode, High speed mode, $V_{DDA}$ = 5 V, 10 kHz | – | 340 | – | pA/sqrtHz |

**Figure 11-51. IDAC Step Response, Codes 0x40 - 0xC0, 255 µA Mode, Source Mode, High speed mode, $V_{DDA}$ = 5 V**
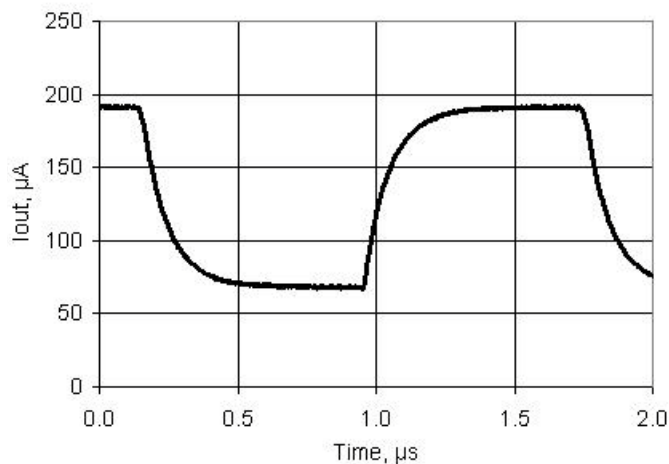


**Figure 11-52. IDAC Glitch Response, Codes 0x7F - 0x80, 255 µA Mode, Source Mode, High speed mode, $V_{DDA}$ = 5 V**
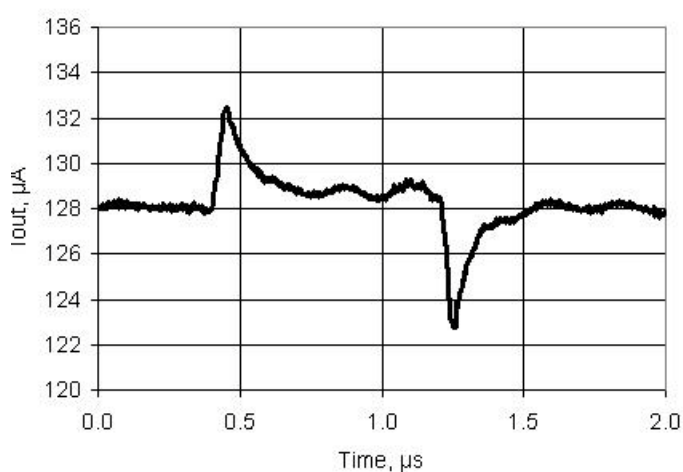
**Figure 11-55. VDAC INL vs Input Code, 1 V Mode**
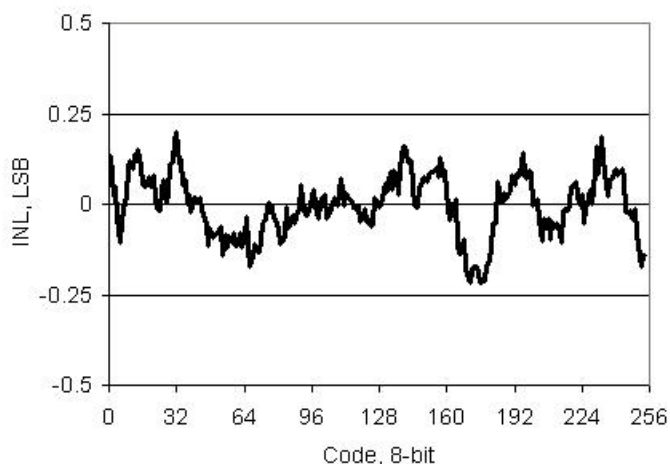


**Figure 11-56. VDAC DNL vs Input Code, 1 V Mode**
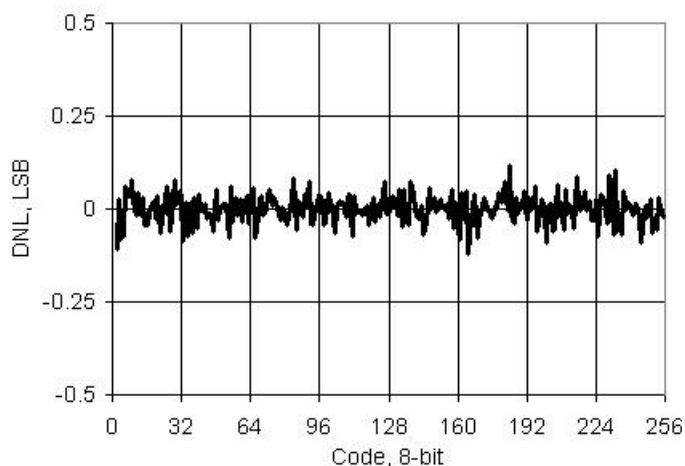


**Figure 11-57. VDAC INL vs Temperature, 1 V Mode**
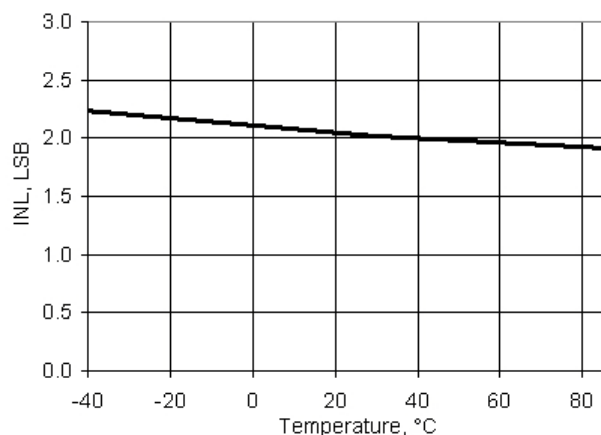


**Figure 11-58. VDAC DNL vs Temperature, 1 V Mode**
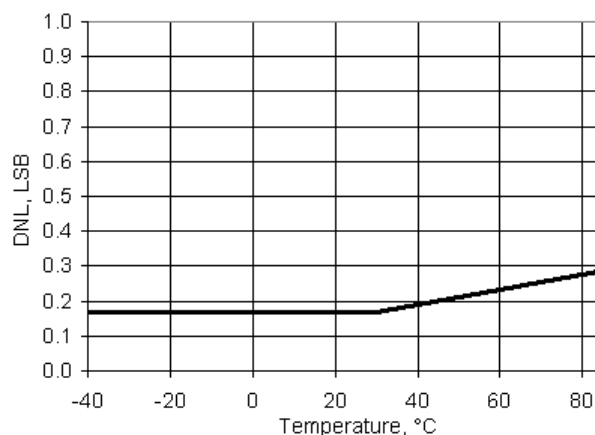


**Figure 11-59. VDAC Full Scale Error vs Temperature, 1 V Mode**
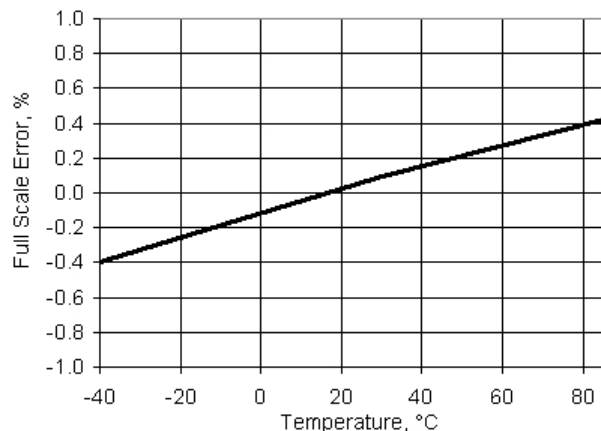


**Figure 11-60. VDAC Full Scale Error vs Temperature, 4 V Mode**
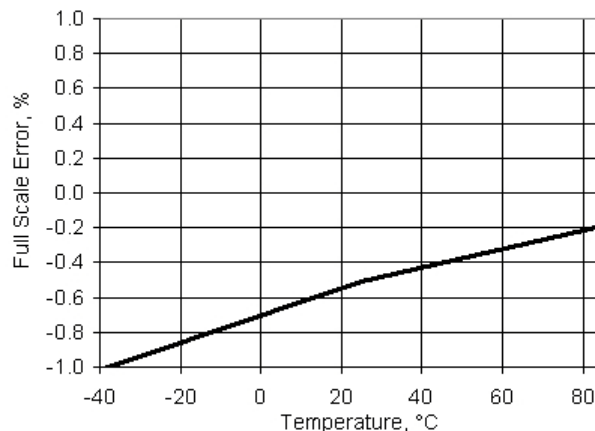
### 11.5.9 Transimpedance Amplifier

The TIA is created using a SC/CT analog block; see the TIA component data sheet in PSoC Creator for full electrical specifications and APIs.

**Table 11-38. Transimpedance Amplifier (TIA) DC Specifications**

| Parameter | Description | Conditions | Min | Typ | Max | Units |
|-----------|-------------|------------|-----|-----|-----|-------|
| V<sub>IOFF</sub> | Input offset voltage | | – | – | 10 | mV |
| Rconv | Conversion resistance[58] | R = 20K; 40 pF load | –25 | – | +35 | % |
| | | R = 30K; 40 pF load | –25 | – | +35 | % |
| | | R = 40K; 40 pF load | –25 | – | +35 | % |
| | | R = 80K; 40 pF load | –25 | – | +35 | % |
| | | R = 120K; 40 pF load | –25 | – | +35 | % |
| | | R = 250K; 40 pF load | –25 | – | +35 | % |
| | | R= 500K; 40 pF load | –25 | – | +35 | % |
| | | R = 1M; 40 pF load | –25 | – | +35 | % |
| | Quiescent current | | – | 1.1 | 2 | mA |

**Table 11-39. Transimpedance Amplifier (TIA) AC Specifications**

| Parameter | Description | Conditions | Min | Typ | Max | Units |
|-----------|-------------|------------|-----|-----|-----|-------|
| BW | Input bandwidth (–3 dB) | R = 20K; –40 pF load | 1500 | – | – | kHz |
| | | R = 120K; –40 pF load | 240 | – | – | kHz |
| | | R = 1M; –40 pF load | 25 | – | – | kHz |

**Note**
58. Conversion resistance values are not calibrated. Calibrated values and details about calibration are provided in PSoC Creator component data sheets. External precision resistors can also be used.

**Table 11-44. LCD Direct Drive AC Specifications**

| Parameter | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| f_LCD | LCD frame rate | | 10 | 50 | 150 | Hz |

## 11.6 Digital Peripherals

Specifications are valid for –40 °C ≤ $T_A$ ≤ 85 °C and $T_J$ ≤ 100 °C, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

### 11.6.1 Timer

The following specifications apply to the Timer/Counter/PWM peripheral in timer mode. Timers can also be implemented in UDBs; for more information, see the Timer component data sheet in PSoC Creator.

**Table 11-45. Timer DC Specifications**

| Parameter | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| | Block current consumption | 16-bit timer, at listed input clock frequency | – | – | – | µA |
| | 3 MHz | | – | 15 | – | µA |
| | 12 MHz | | – | 60 | – | µA |
| | 48 MHz | | – | 260 | – | µA |
| | 67 MHz | | – | 350 | – | µA |

**Table 11-46. Timer AC Specifications**

| Parameter | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| | Operating frequency | | DC | – | 67.01 | MHz |
| | Capture pulse width (Internal) | | 15 | – | – | ns |
| | Capture pulse width (external) | | 30 | – | – | ns |
| | Timer resolution | | 15 | – | – | ns |
| | Enable pulse width | | 15 | – | – | ns |
| | Enable pulse width (external) | | 30 | – | – | ns |
| | Reset pulse width | | 15 | – | – | ns |
| | Reset pulse width (external) | | 30 | – | – | ns |

*11.6.2 Counter*

The following specifications apply to the Timer/Counter/PWM peripheral, in counter mode. Counters can also be implemented in UDBs; for more information, see the Counter component data sheet in PSoC Creator.

**Table 11-47. Counter DC Specifications**

| Parameter | Description | Conditions | Min | Typ | Max | Units |
|-----------|-------------|------------|-----|-----|-----|-------|
| | Block current consumption | 16-bit counter, at listed input clock frequency | – | – | – | µA |
| | 3 MHz | | – | 15 | – | µA |
| | 12 MHz | | – | 60 | – | µA |
| | 48 MHz | | – | 260 | – | µA |
| | 67 MHz | | – | 350 | – | µA |

**Table 11-48. Counter AC Specifications**

| Parameter | Description | Conditions | Min | Typ | Max | Units |
|-----------|-------------|------------|-----|-----|-----|-------|
| | Operating frequency | | DC | – | 67.01 | MHz |
| | Capture pulse | | 15 | – | – | ns |
| | Resolution | | 15 | – | – | ns |
| | Pulse width | | 15 | – | – | ns |
| | Pulse width (external) | | 30 | | | ns |
| | Enable pulse width | | 15 | – | – | ns |
| | Enable pulse width (external) | | 30 | – | – | ns |
| | Reset pulse width | | 15 | – | – | ns |
| | Reset pulse width (external) | | 30 | – | – | ns |

*11.6.3 Pulse Width Modulation*

The following specifications apply to the Timer/Counter/PWM peripheral, in PWM mode. PWM components can also be implemented in UDBs; for more information, see the PWM component data sheet in PSoC Creator.

**Table 11-49. PWM DC Specifications**

| Parameter | Description | Conditions | Min | Typ | Max | Units |
|-----------|-------------|------------|-----|-----|-----|-------|
| | Block current consumption | 16-bit PWM, at listed input clock frequency | – | – | – | µA |
| | 3 MHz | | – | 15 | – | µA |
| | 12 MHz | | – | 60 | – | µA |
| | 48 MHz | | – | 260 | – | µA |
| | 67 MHz | | – | 350 | – | µA |

**Table 11-50. Pulse Width Modulation (PWM) AC Specifications**

| Parameter | Description | Conditions | Min | Typ | Max | Units |
|-----------|-------------|------------|-----|-----|-----|-------|
| | Operating frequency | | DC | – | 67.01 | MHz |
| | Pulse width | | 15 | – | – | ns |
| | Pulse width (external) | | 30 | – | – | ns |
| | Kill pulse width | | 15 | – | – | ns |
| | Kill pulse width (external) | | 30 | – | – | ns |
| | Enable pulse width | | 15 | – | – | ns |
| | Enable pulse width (external) | | 30 | – | – | ns |
| | Reset pulse width | | 15 | – | – | ns |
| | Reset pulse width (external) | | 30 | – | – | ns |

### 11.6.7 USB

**Table 11-57. USB DC Specifications**

| Parameter | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{USB\_5}$ | Device supply ($V_{DDD}$) for USB operation | USB configured, USB regulator enabled | 4.35 | – | 5.25 | V |
| $V_{USB\_3.3}$ | | USB configured, USB regulator bypassed | 3.15 | – | 3.6 | V |
| $V_{USB\_3}$ | | USB configured, USB regulator bypassed[60] | 2.85 | – | 3.6 | V |
| $I_{USB\_Configured}$ | Device supply current in device active mode, bus clock and IMO = 24 MHz | $V_{DDD}$ = 5 V, $F_{CPU}$ = 1.5 MHz | – | 10 | – | mA |
| | | $V_{DDD}$ = 3.3 V, $F_{CPU}$ = 1.5 MHz | – | 8 | – | mA |
| $I_{USB\_Suspended}$ | Device supply current in device sleep mode | $V_{DDD}$ = 5 V, connected to USB host, PICU configured to wake on USB resume signal | – | 0.5 | – | mA |
| | | $V_{DDD}$ = 5 V, disconnected from USB host | – | 0.3 | – | mA |
| | | $V_{DDD}$ = 3.3 V, connected to USB host, PICU configured to wake on USB resume signal | – | 0.5 | – | mA |
| | | $V_{DDD}$ = 3.3 V, disconnected from USB host | – | 0.3 | – | mA |

### 11.6.8 Universal Digital Blocks (UDBs)

PSoC Creator provides a library of prebuilt and tested standard digital peripherals (UART, SPI, LIN, PRS, CRC, timer, counter, PWM, AND, OR, and so on) that are mapped to the UDB array. See the component data sheets in PSoC Creator for full AC/DC specifications, APIs, and example code.

**Table 11-58. UDB AC Specifications**

| Parameter | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Datapath Performance | | | | | | |
| $F_{MAX\_TIMER}$ | Maximum frequency of 16-bit timer in a UDB pair | | – | – | 67.01 | MHz |
| $F_{MAX\_ADDER}$ | Maximum frequency of 16-bit adder in a UDB pair | | – | – | 67.01 | MHz |
| $F_{MAX\_CRC}$ | Maximum frequency of 16-bit CRC/PRS in a UDB pair | | – | – | 67.01 | MHz |
| PLD Performance | | | | | | |
| $F_{MAX\_PLD}$ | Maximum frequency of a two-pass PLD function in a UDB pair | | – | – | 67.01 | MHz |
| Clock to Output Performance | | | | | | |
| $t_{CLK\_OUT}$ | Propagation delay for clock in to data out, see Figure 11-70. | 25 °C, $V_{DDD} \geq 2.7$ V | – | 20 | 25 | ns |
| $t_{CLK\_OUT}$ | Propagation delay for clock in to data out, see Figure 11-70. | Worst-case placement, routing, and pin selection | – | – | 55 | ns |

**Note**
60. Rise/fall time matching (TR) not guaranteed, see USB Driver AC Specifications on page 87.

Figure 13-1. 48-pin (300 mil) SSOP Package Outline



DIMENSIONS IN INCHES $\frac{MIN.}{MAX.}$

PKG. WEIGHT: REFER TO PMDD SPEC.

SEATING PLANE

GAUGE PLANE

51-85061 *F
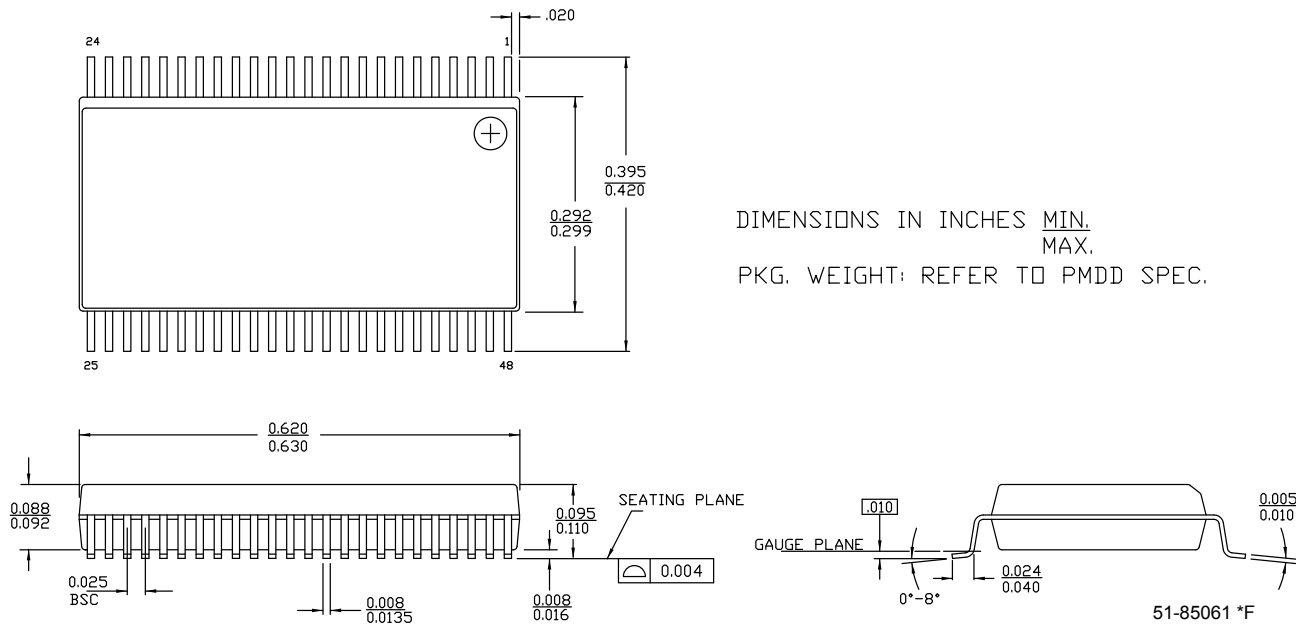
Figure 13-2. 48-pin QFN Package Outline

TOP VIEW

SIDE VIEW

BOTTOM VIEW



SOLDERABLE
EXPOSED
PAD

PIN 1 ID

PIN 1 DOT
LASER MARK
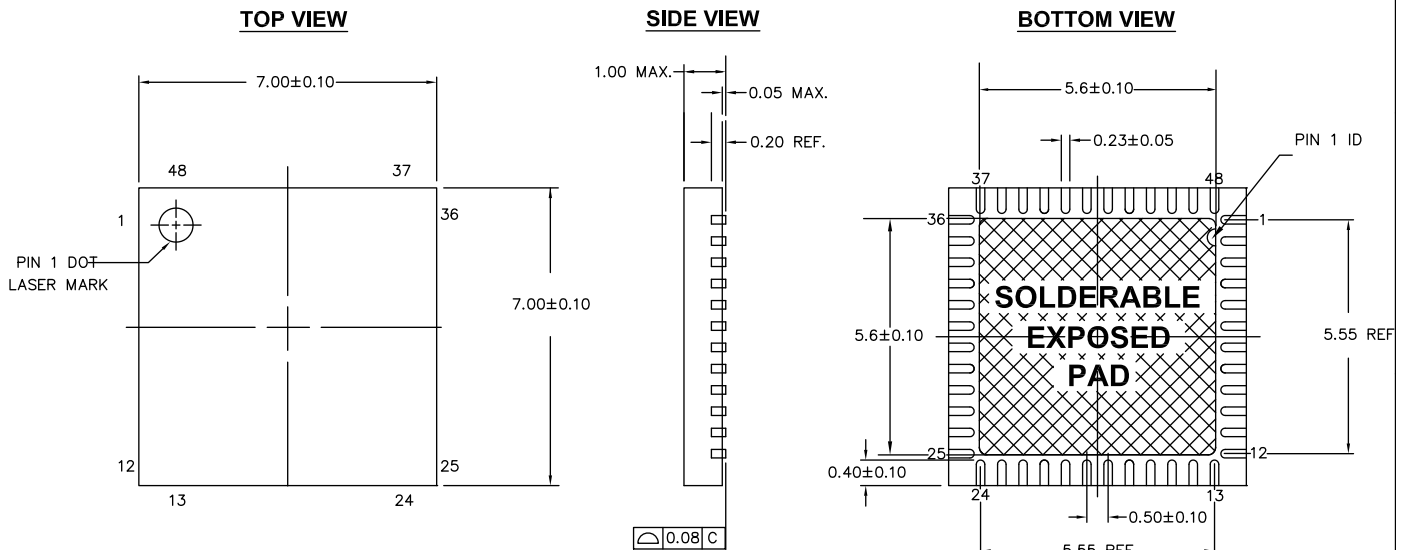
NOTES:
1. ▨ HATCH AREA IS SOLDERABLE EXPOSED METAL.
2. REFERENCE JEDEC#: MO-220
3. PACKAGE WEIGHT: REFER TO PMDD SPEC.
4. ALL DIMENSIONS ARE IN MM [MIN/MAX]
5. PACKAGE CODE

| PART # | DESCRIPTION |
|--------|-------------|
| LT48D  | LEAD FREE   |

001-45616 *E

# 16. Document Conventions

## 16.1 Units of Measure

**Table 16-1.  Units of Measure**

| Symbol | Unit of Measure |
|--------|-----------------|
| °C | degrees Celsius |
| dB | decibels |
| fF | femtofarads |
| Hz | hertz |
| KB | 1024 bytes |
| kbps | kilobits per second |
| Khr | kilohours |
| kHz | kilohertz |
| kΩ | kilohms |
| ksps | kilosamples per second |
| LSB | least significant bit |
| Mbps | megabits per second |
| MHz | megahertz |
| MΩ | megaohms |
| Msps | megasamples per second |
| µA | microamperes |
| µF | microfarads |
| µH | microhenrys |
| µs | microseconds |
| µV | microvolts |
| µW | microwatts |
| mA | milliamperes |
| ms | milliseconds |
| mV | millivolts |
| nA | nanoamperes |
| ns | nanoseconds |
| nV | nanovolts |
| Ω | ohms |
| pF | picofarads |
| ppm | parts per million |
| ps | picoseconds |
| s | seconds |
| sps | samples per second |
| sqrtHz | square root of hertz |
| V | volts |

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