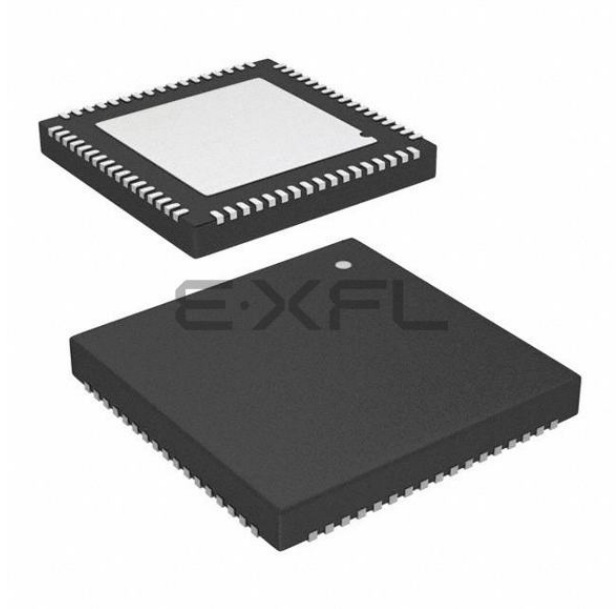

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	67MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, SPI, UART/USART, USB
Peripherals	CapSense, DMA, LCD, POR, PWM, WDT
Number of I/O	38
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 5.5V
Data Converters	A/D 16x20b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	68-VFQFN Exposed Pad
Supplier Device Package	68-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c3866lti-209t

For more details on the peripherals see the "Example Peripherals" section on page 44 of this data sheet. For information on UDBs, DSI, and other digital blocks, see the "Digital Subsystem" section on page 44 of this data sheet.

PSoC's analog subsystem is the second half of its unique configurability. All analog performance is based on a highly accurate absolute voltage reference with less than 0.1-percent error over temperature and voltage. The configurable analog subsystem includes:

- Analog muxes
- Comparators
- Voltage references
- Analog-to-digital converter (ADC)
- Digital-to-analog converters (DACs)
- Digital filter block (DFB)

All GPIO pins can route analog signals into and out of the device using the internal analog bus. This allows the device to interface up to 62 discrete analog signals. The heart of the analog subsystem is a fast, accurate, configurable delta-sigma ADC with these features:

- Less than 100 µV offset
- A gain error of 0.2 percent
- INL less than ±2 LSB
- DNL less than ±1 LSB
- SINAD better than 84 dB in 16-bit mode

This converter addresses a wide variety of precision analog applications, including some of the most demanding sensors. The output of the ADC can optionally feed the programmable DFB through the DMA without CPU intervention. You can configure the DFB to perform IIR and FIR digital filters and several user-defined custom functions. The DFB can implement filters with up to 64 taps. It can perform a 48-bit multiply-accumulate (MAC) operation in one clock cycle.

Four high-speed voltage or current DACs support 8-bit output signals at an update rate of up to 8 Msps. They can be routed out of any GPIO pin. You can create higher resolution voltage PWM DAC outputs using the UDB array. This can be used to create a pulse width modulated (PWM) DAC of up to 10 bits, at up to 48 kHz. The digital DACs in each UDB support PWM, PRS, or delta-sigma algorithms with programmable widths. In addition to the ADC, DACs, and DFB, the analog subsystem provides multiple:

- Uncommitted opamps
- Configurable switched capacitor/continuous time (SC/CT) blocks. These support:
  - Transimpedance amplifiers
  - Programmable gain amplifiers
  - Mixers
  - Other similar analog components

See the "Analog Subsystem" section on page 56 of this data sheet for more details.

PSoC's 8051 CPU subsystem is built around a single cycle pipelined 8051 8-bit processor running at up to 67 MHz. The CPU subsystem includes a programmable nested vector interrupt controller, DMA controller, and RAM. PSoC's nested vector interrupt controller provides low latency by allowing the CPU to vector directly to the first address of the interrupt service routine, bypassing the jump instruction required by other architectures. The DMA controller enables peripherals to exchange data without CPU involvement. This allows the CPU to run slower (saving power) or use those CPU cycles to improve the performance of firmware algorithms. The single cycle 8051 CPU runs ten times faster than a standard 8051 processor. The processor speed itself is configurable, allowing you to tune active power consumption for specific applications.

PSoC's nonvolatile subsystem consists of flash, byte-writeable EEPROM, and nonvolatile configuration options. It provides up to 64 KB of on-chip flash. The CPU can reprogram individual blocks of flash, enabling bootloaders. You can enable an error correcting code (ECC) for high reliability applications. A powerful and flexible protection model secures the user's sensitive information, allowing selective memory block locking for read and write protection. Up to 2 KB of byte-writeable EEPROM is available on-chip to store application data. Additionally, selected configuration options such as boot speed and pin drive mode are stored in nonvolatile memory. This allows settings to activate immediately after POR.

The three types of PSoC I/O are extremely flexible. All I/Os have many drive modes that are set at POR. PSoC also provides up to four I/O voltage domains through the VDDIO pins. Every GPIO has analog I/O, LCD drive[3], CapSense[4], flexible interrupt generation, slew rate control, and digital I/O capability. The SIOs on PSoC allow V_{OH} to be set independently of Vddio when used as outputs. When SIOs are in input mode they are high impedance. This is true even when the device is not powered or when the pin voltage goes above the supply voltage. This makes the SIO ideally suited for use on an I^2C bus where the PSoC may not be powered when other devices on the bus are. The SIO pins also have high current sink capability for applications such as LED drives. The programmable input threshold feature of the SIO can be used to make the SIO function as a general purpose analog comparator. For devices with Full-Speed USB the USB physical interface is also provided (USBIO). When not using USB these pins may also be used for limited digital functionality and device programming. All of the features of the PSoC I/Os are covered in detail in the "I/O System and Routing" section on page 37 of this data sheet.

The PSoC device incorporates flexible internal clock generators, designed for high stability and factory trimmed for high accuracy. The internal main oscillator (IMO) is the clock base for the system, and has 1-percent accuracy at 3 MHz. The IMO can be configured to run from 3 MHz up to 62 MHz. Multiple clock derivatives can be generated from the main clock frequency to meet application needs. The device provides a PLL to generate clock frequencies up to 67 MHz from the IMO, external crystal, or external reference clock.

Notes
3. This feature on select devices only. See Ordering Information on page 123 for details.
4. GPIOs with opamp outputs are not recommended for use with CapSense.

Figure 2-6. 100-pin TQFP Part Pinout

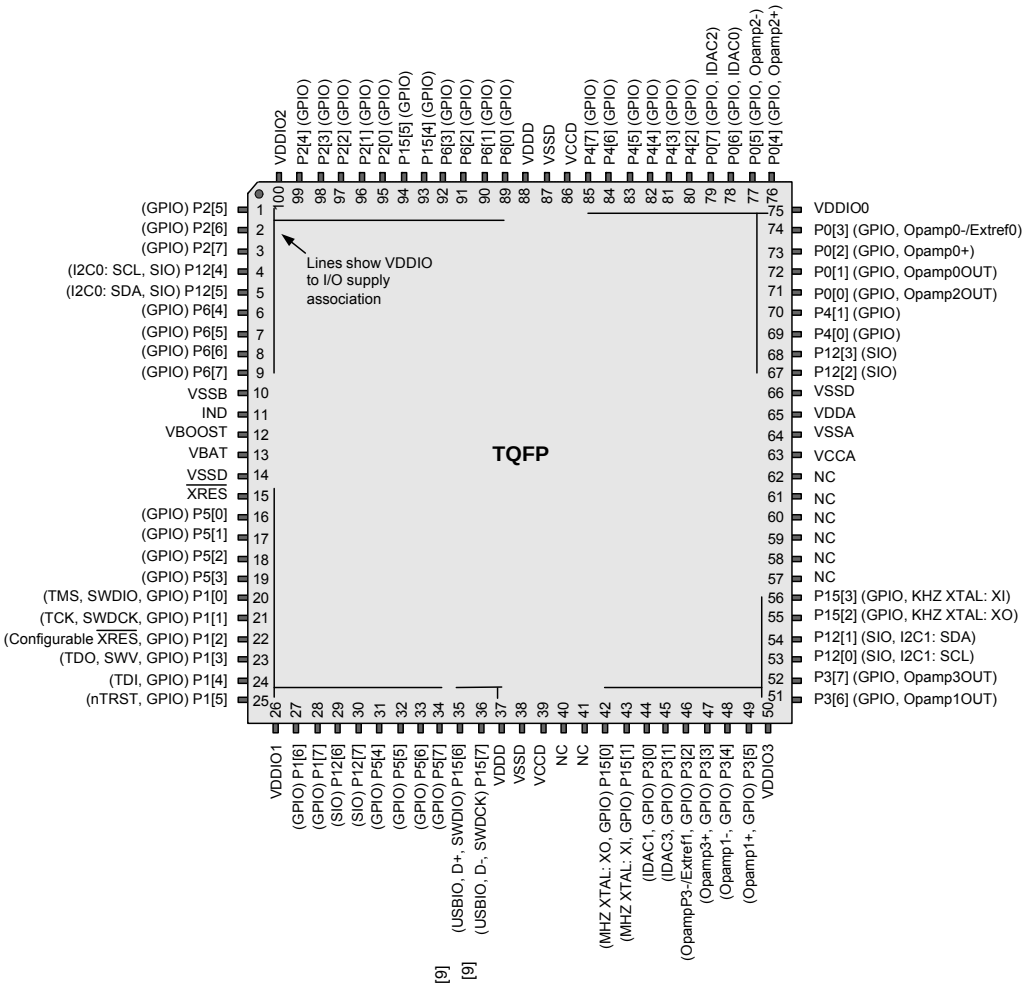
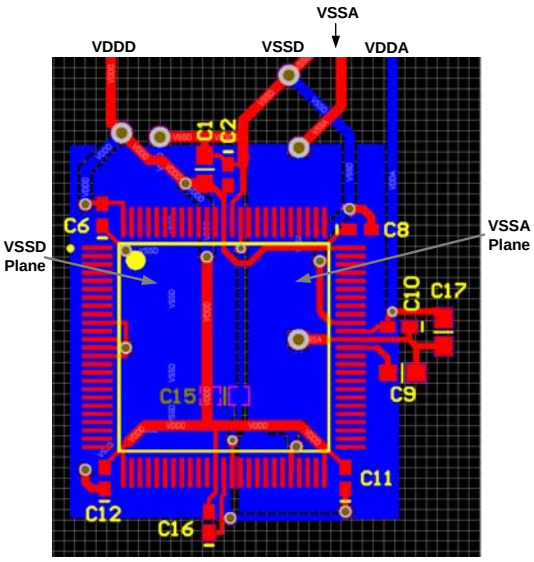


Table 2-1. V_{DDIO} and Port Pin Associations

VDDIO	Port Pins
VDDIO0	P0[7:0], P4[7:0], P12[3:2]
VDDIO1	P1[7:0], P5[7:0], P12[7:6]
VDDIO2	P2[7:0], P6[7:0], P12[5:4], P15[5:4]
VDDIO3	P3[7:0], P12[1:0], P15[3:0]
VDDD	P15[7:6] (USB D+, D-)

Note
9. Pins are Do Not Use (DNU) on devices without USB. The pin must be left floating.

Figure 2-8. Example PCB Layout for 100-pin TQFP Part for Optimal Analog Performance



3. Pin Descriptions

IDAC0, IDAC1, IDAC2, IDAC3

Low resistance output pin for high current DACs (IDAC).

Opamp0OUT, Opamp1OUT, Opamp2OUT, Opamp3OUT

High current output of uncommitted opamp[11].

Extref0, Extref1

External reference input to the analog system.

Opamp0–, Opamp1–, Opamp2–, Opamp3–

Inverting input to uncommitted opamp.

Opamp0+, Opamp1+, Opamp2+, Opamp3+

Noninverting input to uncommitted opamp.

GPIO

General purpose I/O pin provides interfaces to the CPU, digital peripherals, analog peripherals, interrupts, LCD segment drive, and CapSense[11].

I2C0: SCL, I2C1: SCL

I^2C SCL line providing wake from sleep on an address match. Any I/O pin can be used for I^2C SCL if wake from sleep is not required.

I2C0: SDA, I2C1: SDA

I^2C SDA line providing wake from sleep on an address match. Any I/O pin can be used for I^2C SDA if wake from sleep is not required.

IND

Inductor connection to boost pump.

kHz XTAL: Xo, kHz XTAL: Xi

32.768-kHz crystal oscillator pin.

MHz XTAL: Xo, MHz XTAL: Xi

4- to 25-MHz crystal oscillator pin.

nTRST

Optional JTAG test reset programming and debug port connection to reset the JTAG connection.

SIO

Special I/O provides interfaces to the CPU, digital peripherals and interrupts with a programmable high threshold voltage, analog comparator, high sink current, and high impedance state when the device is unpowered.

SWDCK

Serial wire debug clock programming and debug port connection.

SWDIO

Serial wire debug input and output programming and debug port connection.

SWV

Single wire viewer debug output.

TCK

JTAG test clock programming and debug port connection.

TDI

JTAG test data in programming and debug port connection.

TDO

JTAG test data out programming and debug port connection.

Note
11. GPIOs with opamp outputs are not recommended for use with CapSense.

5.7 Memory Map

The CY8C38 8051 memory map is very similar to the MCS-51 memory map.

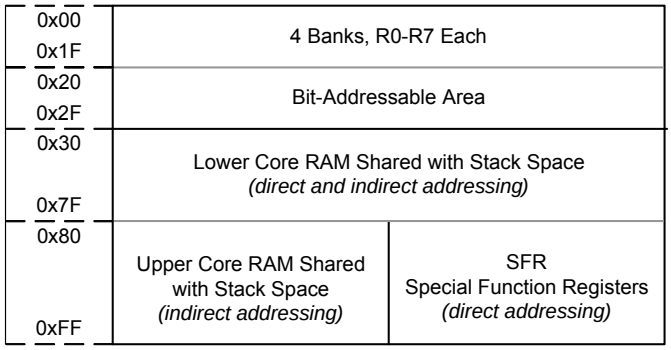
5.7.1 Code Space

The CY8C38 8051 code space is 64 KB. Only main flash exists in this space. See the Flash Program Memory on page 23.

5.7.2 Internal Data Space

The CY8C38 8051 internal data space is 384 bytes, compressed within a 256-byte space. This space consists of 256 bytes of RAM (in addition to the SRAM mentioned in Static RAM on page 23) and a 128-byte space for special function registers (SFR). See Figure 5-2. The lowest 32 bytes are used for 4 banks of registers R0-R7. The next 16 bytes are bit-addressable.

Figure 5-2. 8051 Internal Data Space



In addition to the register or bit address modes used with the lower 48 bytes, the lower 128 bytes can be accessed with direct or indirect addressing. With direct addressing mode, the upper 128 bytes map to the SFRs. With indirect addressing mode, the upper 128 bytes map to RAM. Stack operations use indirect addressing; the 8051 stack space is 256 bytes. See the "Addressing Modes" section on page 13.

5.7.3 SFRs

The SFR space provides access to frequently accessed registers. The memory map for the SFR memory space is shown in Table 5-4.

Table 5-4. SFR Map

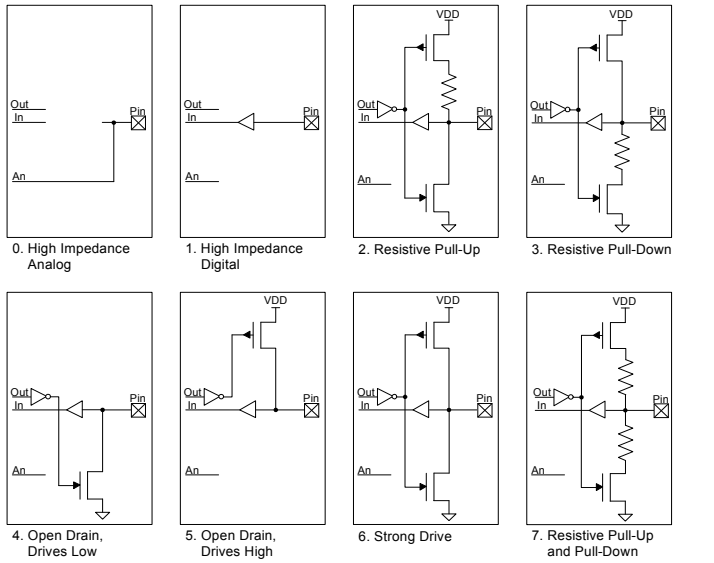
Address	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F
0×F8	SFRPRT15DR	SFRPRT15PS	SFRPRT15SEL	–	–	–	–	–
0×F0	B	–	SFRPRT12SEL	–	–	–	–	–
0×E8	SFRPRT12DR	SFRPRT12PS	MXAX	–	–	–	–	–
0×E0	ACC	–	–	–	–	–	–	–
0×D8	SFRPRT6DR	SFRPRT6PS	SFRPRT6SEL	–	–	–	–	–
0×D0	PSW	–	–	–	–	–	–	–
0×C8	SFRPRT5DR	SFRPRT5PS	SFRPRT5SEL	–	–	–	–	–
0×C0	SFRPRT4DR	SFRPRT4PS	SFRPRT4SEL	–	–	–	–	–
0×B8				–	–	–	–	–
0×B0	SFRPRT3DR	SFRPRT3PS	SFRPRT3SEL	–	–	–	–	–
0×A8	IE	–	–	–	–	–	–	–
0×A0	P2AX	–	SFRPRT1SEL	–	–	–	–	–
0×98	SFRPRT2DR	SFRPRT2PS	SFRPRT2SEL	–	–	–	–	–
0×90	SFRPRT1DR	SFRPRT1PS	–	DPX0	–	DPX1	–	–
0×88	–	SFRPRT0PS	SFRPRT0SEL	–	–	–	–	–
0×80	SFRPRT0DR	SP	DPL0	DPH0	DPL1	DPH1	DPS	–

The CY8C38 family provides the standard set of registers found on industry standard 8051 devices. In addition, the CY8C38 devices add SFRs to provide direct access to the I/O ports on the device. The following sections describe the SFRs added to the CY8C38 family.

6.4.1 Drive Modes

Each GPIO and SIO pin is individually configurable into one of the eight drive modes listed in Table 6-6. Three configuration bits are used for each pin (DM[2:0]) and set in the PRTxDM[2:0] registers. Figure 6-12 depicts a simplified pin view based on each of the eight drive modes. Table 6-6 shows the I/O pin's drive state based on the port data register value or digital array signal if bypass mode is selected. Note that the actual I/O pin voltage is determined by a combination of the selected drive mode and the load at the pin. For example, if a GPIO pin is configured for resistive pull-up mode and driven high while the pin is floating, the voltage measured at the pin is a high logic state. If the same GPIO pin is externally tied to ground then the voltage unmeasured at the pin is a low logic state.

Figure 6-12. Drive Mode



The 'Out' connection is driven from either the Digital System (when the Digital Output terminal is connected) or the Data Register (when HW connection is disabled).
The 'In' connection drives the Pin State register, and the Digital System if the Digital Input terminal is enabled and connected.
The 'An' connection connects to the Analog System.

Table 6-6. Drive Modes

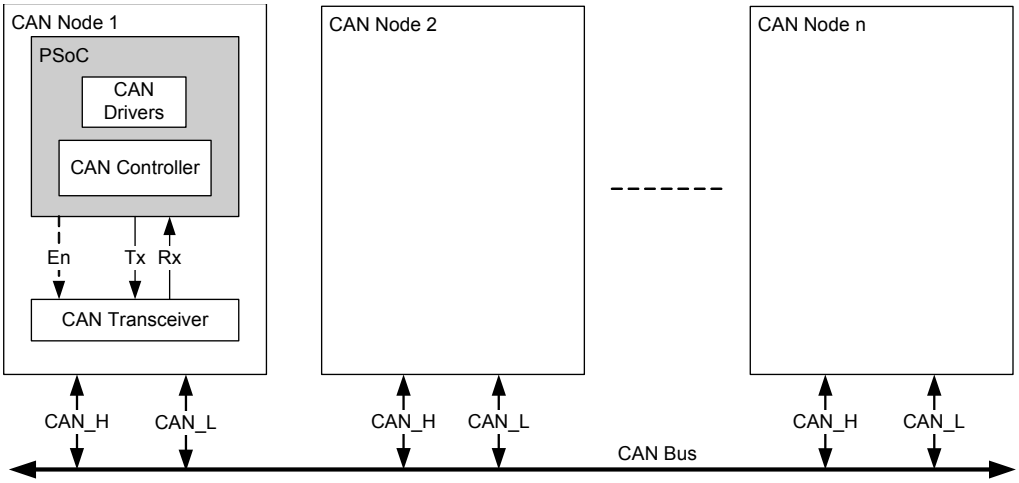
Diagram	Drive Mode	PRTxDM2	PRTxDM1	PRTxDM0	PRTxDR = 1	PRTxDR = 0
0	High impedance analog	0	0	0	High Z	High Z
1	High Impedance digital	0	0	1	High Z	High Z
2	Resistive pull-up[14]	0	1	0	Res High (5K)	Strong Low
3	Resistive pull-down[14]	0	1	1	Strong High	Res Low (5K)
4	Open drain, drives low	1	0	0	High Z	Strong Low
5	Open drain, drive high	1	0	1	Strong High	High Z
6	Strong drive	1	1	0	Strong High	Strong Low
7	Resistive pull-up and pull-down[14]	1	1	1	Res High (5K)	Res Low (5K)

Note
14. Resistive pull-up and pull-down are not available with SIO in regulated output mode.

7.5 CAN

The CAN peripheral is a fully functional controller area network (CAN) supporting communication baud rates up to 1 Mbps. The CAN controller implements the CAN2.0A and CAN2.0B specifications as defined in the Bosch specification and conforms to the ISO-11898-1 standard. The CAN protocol was originally designed for automotive applications with a focus on a high level of fault detection. This ensures high communication reliability at a low cost. Because of its success in automotive applications, CAN is used as a standard communication protocol for motion oriented machine control networks (CANOpen) and factory automation applications (DeviceNet). The CAN controller features allow the efficient implementation of higher level protocols without affecting the performance of the microcontroller CPU. Full configuration support is provided in PSoC Creator.

Figure 7-14. CAN Bus System Implementation



7.5.1 CAN Features

- CAN2.0A/B protocol implementation – ISO 11898 compliant
  - Standard and extended frames with up to 8 bytes of data per frame
  - Message filter capabilities
  - Remote Transmission Request (RTR) support
  - Programmable bit rate up to 1 Mbps
- Listen Only mode
- SW readable error counter and indicator
- Sleep mode: Wake the device from sleep with activity on the Rx pin
- Supports two or three wire interface to external transceiver (Tx, Rx, and Enable). The three-wire interface is compatible with the Philips PHY; the PHY is not included on-chip. The three wires can be routed to any I/O
- Enhanced interrupt controller
  - CAN receive and transmit buffers status
  - CAN controller error status including BusOff
- Receive path
  - 16 receive buffers each with its own message filter
  - Enhanced hardware message filter implementation that covers the ID, IDE, and RTR
  - DeviceNet addressing support
  - Multiple receive buffers linkable to build a larger receive message array
  - Automatic transmission request (RTR) response handler
  - Lost received message notification
- Transmit path
  - Eight transmit buffers
  - Programmable transmit priority
  - Round robin
  - Fixed priority
  - Message transmissions abort capability

7.5.2 Software Tools Support

CAN Controller configuration integrated into PSoC Creator:

- CAN Configuration walkthrough with bit timing analyzer
- Receive filter setup

7.9 Digital Filter Block

Some devices in the CY8C38 family of devices have a dedicated HW accelerator block used for digital filtering. The DFB has a dedicated multiplier and accumulator that calculates a 24-bit by 24-bit multiply accumulate in one bus clock cycle. This enables the mapping of a direct form FIR filter that approaches a computation rate of one FIR tap for each clock cycle. The MCU can implement any of the functions performed by this block, but at a slower rate that consumes MCU bandwidth.

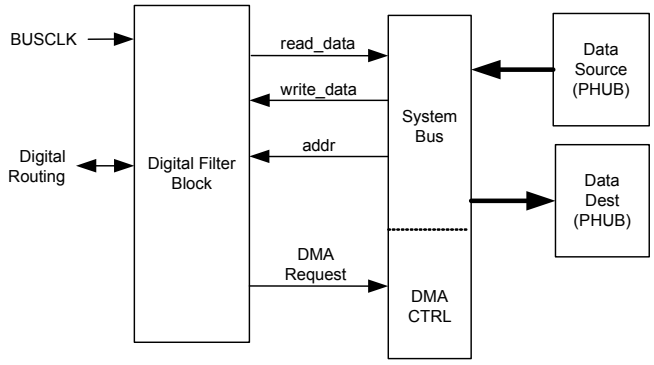
The heart of the DFB is a datapath (DP), which is the numerical calculation unit of the DFB. The DP is a 24-bit fixed-point numerical processor containing a 48-bit multiply and accumulate function (MAC), a multi-function ALU, sample and coefficient data RAMs as well as data routing, shifting, holding and rounding functions.

In the MAC, two 24-bit values can be multiplied and the result added to the 48-bit accumulator in each bus clock cycle. The MAC is the only portion of the DP that is wider than 24 bits. All results from the MAC are passed on to the ALU as 24-bit values representing the high-order 24 bits in the accumulator shifted by one (bits 46:23). The MAC assumes an implied binary point after the most significant bit.

The DP also contains an optimized ALU that supports add, subtract, comparison, threshold, absolute value, squelch, saturation, and other functions. The DP unit is controlled by seven control fields totaling 18 bits coming from the DFB Controller. For more information see the TRM.

The PSoC Creator interface provides a wizard to implement FIR and IIR digital filters with coefficients for LPF, BPF, HPF, Notch and arbitrary shape filters. 64 pairs of data and coefficients are stored. This enables a 64 tap FIR filter or up to 4 16 tap filters of either FIR or IIR formulation.

Figure 7-20. DFB Application Diagram (pwr/gnd not shown)



The typical use model is for data to be supplied to the DFB over the system bus from another on-chip system data source such as an ADC. The data typically passes through main memory or is directly transferred from another chip resource through DMA. The DFB processes this data and passes the result to another on chip resource such as a DAC or main memory through DMA on the system bus.

Data movement in or out of the DFB is typically controlled by the system DMA controller but can be moved directly by the MCU.

8. Analog Subsystem

The analog programmable system creates application specific combinations of both standard and advanced analog signal processing blocks. These blocks are then interconnected to each other and also to any pin on the device, providing a high level of design flexibility and IP security. The features of the analog subsystem are outlined here to provide an overview of capabilities and architecture.

- Flexible, configurable analog routing architecture provided by analog globals, analog mux bus, and analog local buses.
- High resolution delta-sigma ADC.
- Up to four 8-bit DACs that provide either voltage or current output.
- Four comparators with optional connection to configurable LUT outputs.
- Up to four configurable switched capacitor/continuous time (SC/CT) blocks for functions that include opamp, unity gain buffer, programmable gain amplifier, transimpedance amplifier, and mixer.
- Up to four opamps for internal use and connection to GPIO that can be used as high current output buffers.
- CapSense subsystem to enable capacitive touch sensing.
- Precision reference for generating an accurate analog voltage for internal analog blocks.

The opamp and resistor array is programmable to perform various analog functions including

- Naked operational amplifier – Continuous mode
- Unity-gain buffer – Continuous mode
- PGA – Continuous mode
- Transimpedance amplifier (TIA) – Continuous mode
- Up/down mixer – Continuous mode
- Sample and hold mixer (NRZ S/H) – Switched cap mode
- First order analog to digital modulator – Switched cap mode

8.5.1 Naked Opamp

The Naked Opamp presents both inputs and the output for connection to internal or external signals. The opamp has a unity gain bandwidth greater than 6.0 MHz and output drive current up to 650 µA. This is sufficient for buffering internal signals (such as DAC outputs) and driving external loads greater than 7.5 kohms.

8.5.2 Unity Gain

The Unity Gain buffer is a Naked Opamp with the output directly connected to the inverting input for a gain of 1.00. It has a –3 dB bandwidth greater than 6.0 MHz.

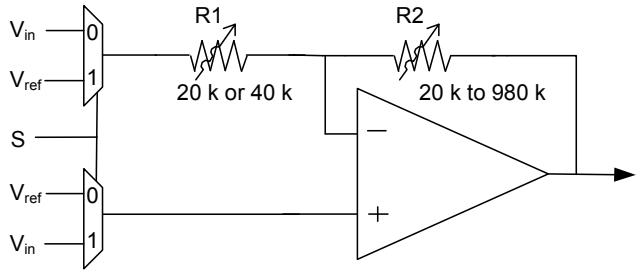
8.5.3 PGA

The PGA amplifies an external or internal signal. The PGA can be configured to operate in inverting mode or noninverting mode. The PGA function may be configured for both positive and negative gains as high as 50 and 49 respectively. The gain is adjusted by changing the values of R1 and R2 as illustrated in Figure 8-8. The schematic in Figure 8-8 shows the configuration and possible resistor settings for the PGA. The gain is switched from inverting and non inverting by changing the shared select value of the both the input muxes. The bandwidth for each gain case is listed in Table 8-3.

Table 8-3. Bandwidth

Gain	Bandwidth
1	6.0 MHz
24	340 kHz
48	220 kHz
50	215 kHz

Figure 8-8. PGA Resistor Settings



The PGA is used in applications where the input signal may not be large enough to achieve the desired resolution in the ADC, or dynamic range of another SC/CT block such as a mixer. The gain is adjustable at runtime, including changing the gain of the PGA prior to each ADC sample.

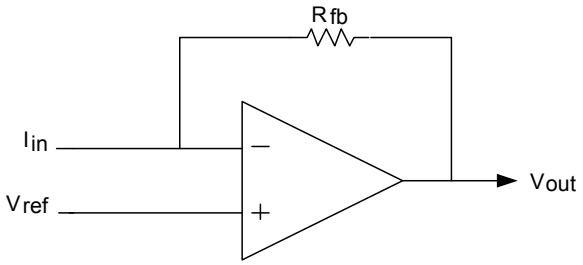
8.5.4 TIA

The Transimpedance Amplifier (TIA) converts an internal or external current to an output voltage. The TIA uses an internal feedback resistor in a continuous time configuration to convert input current to output voltage. For an input current I_{in}, the output voltage is V_{REF} - I_{in} x R_{fb}, where V_{REF} is the value placed on the non inverting input. The feedback resistor Rfb is programmable between 20 KΩ and 1 MΩ through a configuration register. Table 8-4 shows the possible values of Rfb and associated configuration settings.

Table 8-4. Feedback Resistor Settings

Configuration Word	Nominal R_{fb} (KΩ)
000b	20
001b	30
010b	40
011b	60
100b	120
101b	250
110b	500
111b	1000

Figure 8-9. Continuous Time TIA Schematic



The TIA configuration is used for applications where an external sensor's output is current as a function of some type of stimulus such as temperature, light, magnetic flux etc. In a common application, the voltage DAC output can be connected to the V_{REF} TIA input to allow calibration of the external sensor bias current by adjusting the voltage DAC output voltage.

8.6 LCD Direct Drive

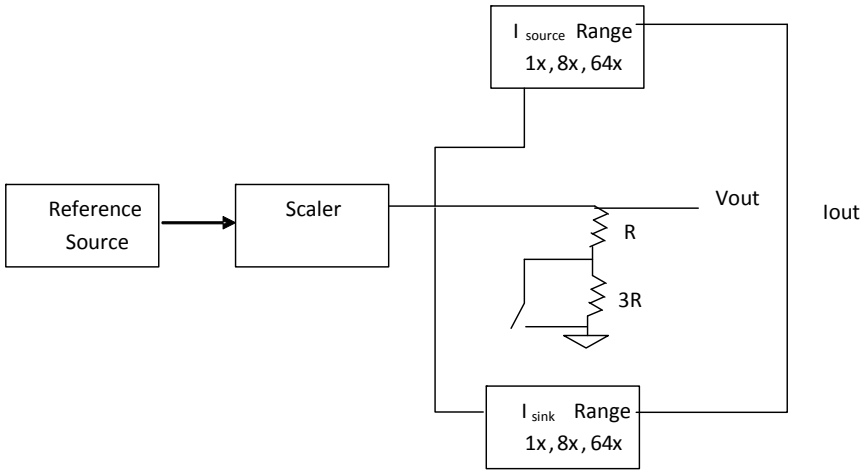
The PSoC LCD driver system is a highly configurable peripheral designed to allow PSoC to directly drive a broad range of LCD glass. All voltages are generated on chip, eliminating the need for external components. With a high multiplex ratio of up to 1/16, the CY8C38 family LCD driver system can drive a maximum of 736 segments. The PSoC LCD driver module was also designed with the conservative power budget of portable devices in mind, enabling different LCD drive modes and power down modes to conserve power.

8.9 DAC

The CY8C38 parts contain up to four Digital to Analog Convertors (DACs). Each DAC is 8-bit and can be configured for either voltage or current output. The DACs support CapSense, power supply regulation, and waveform generation. Each DAC has the following features:

- Adjustable voltage or current output in 255 steps
- Programmable step size (range selection)
- Eight bits of calibration to correct ± 25 percent of gain error
- Source and sink option for current output
- High and low speed / power modes
- 8 Msps conversion rate for current output
- 1 Msps conversion rate for voltage output
- Monotonic in nature
- Data and strobe inputs can be provided by the CPU or DMA, or routed directly from the DSI
- Dedicated low-resistance output pin for high-current mode

Figure 8-11. DAC Block Diagram



8.9.1 Current DAC

The current DAC (IDAC) can be configured for the ranges 0 to 31.875 µA, 0 to 255 µA, and 0 to 2.04 mA. The IDAC can be configured to source or sink current.

8.9.2 Voltage DAC

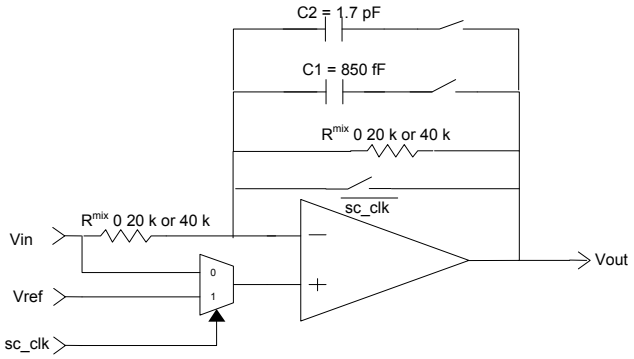
For the voltage DAC (VDAC), the current DAC output is routed through resistors. The two ranges available for the VDAC are 0 to 1.02 V and 0 to 4.08 V. In voltage mode any load connected to the output of a DAC should be purely capacitive (the output of the VDAC is not buffered).

8.10 Up/Down Mixer

In continuous time mode, the SC/CT block components are used to build an up or down mixer. Any mixing application contains an input signal frequency and a local oscillator frequency. The polarity of the clock, Fclk, switches the amplifier between inverting or noninverting gain. The output is the product of the input and the switching function from the local oscillator, with frequency components at the local oscillator plus and minus the signal frequency (Fclk + Fin and Fclk – Fin) and reduced-level frequency components at odd integer multiples of the local oscillator frequency. The local oscillator frequency is provided by the selected clock source for the mixer.

Continuous time up and down mixing works for applications with input signals and local oscillator frequencies up to 1 MHz.

Figure 8-12. Mixer Configuration



8.11 Sample and Hold

The main application for a sample and hold, is to hold a value stable while an ADC is performing a conversion. Some applications require multiple signals to be sampled simultaneously, such as for power calculations (V and I).

11. Electrical Specifications

Specifications are valid for –40 °C ≤ T_A ≤ 85 °C and T_J ≤ 100 °C, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted. The unique flexibility of the PSoC UDBs and analog blocks enable many functions to be implemented in PSoC Creator components, see the component data sheets for full AC/DC specifications of individual functions. See the "Example Peripherals" section on page 44 for further explanation of PSoC Creator components.

11.1 Absolute Maximum Ratings

Table 11-1. Absolute Maximum Ratings DC Specifications[18]

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{DDA}	Analog supply voltage relative to V_{SSA}		–0.5	–	6	V
V_{DDD}	Digital supply voltage relative to V_{SSD}		–0.5	–	6	V
V_{DDIO}	I/O supply voltage relative to V_{SSD}		–0.5	–	6	V
V_{CCA}	Direct analog core voltage input		–0.5	–	1.95	V
V_{CCD}	Direct digital core voltage input		–0.5	–	1.95	V
V_{SSA}	Analog ground voltage		V_{SSD} – 0.5	–	V_{SSD} + 0.5	V
V_{GPIO}[19]	DC input voltage on GPIO	Includes signals sourced by V_{DDA} and routed internal to the pin	V_{SSD} – 0.5	–	V_{DDIO} + 0.5	V
V_{SIO}	DC input voltage on SIO	Output disabled	V_{SSD} – 0.5	–	7	V
		Output enabled	V_{SSD} – 0.5	–	6	V
V_{IND}	Voltage at boost converter input		0.5	–	5.5	V
V_{BAT}	Boost converter supply		V_{SSD} – 0.5	–	5.5	V
I_{VDDIO}	Current per V_{DDIO} supply pin		–	–	100	mA
I_{GPIO}	GPIO current		–30	–	41	mA
I_{SIO}	SIO current		–49	–	28	mA
I_{USBIO}	USBIO current		–56	–	59	mA
V_{EXTREF}	ADC external reference inputs	Pins P0[3], P3[2]	–	–	2	V
LU	Latch up current[20]		–140	–	140	mA
ESD_{HBM}	Electrostatic discharge voltage, Human body model	V_{SSA} tied to V_{SSD}	2200	–	–	V
		V_{SSA} not tied to V_{SSD}	750	–	–	V
ESD_{CDM}	Electrostatic discharge voltage, Charge device model		500	–	–	V

Notes

18. Usage above the absolute maximum conditions listed in Table 11-1 may cause permanent damage to the device. Exposure to Absolute Maximum conditions for extended periods of time may affect device reliability. The Maximum Storage Temperature is 150 °C in compliance with JEDEC Standard JESD22-A103, High Temperature Storage Life. When used below Absolute Maximum conditions but above normal operating conditions, the device may not operate to specification.
19. The V_{DDIO} supply voltage must be greater than the maximum voltage on the associated GPIO pins. Maximum voltage on GPIO pin ≤ V_{DDIO} ≤ V_{DDA}.
20. Meets or exceeds JEDEC Spec EIA/JESD78 IC Latch-up Test.

Figure 11-49. IDAC Operating Current vs Temperature, Range = 255 µA, Code = 0, Source Mode

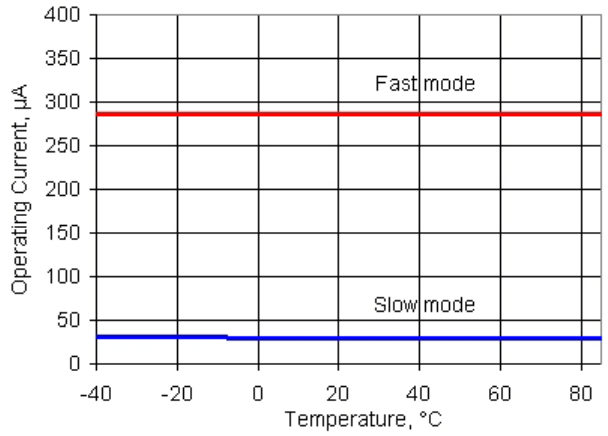


Figure 11-50. IDAC Operating Current vs Temperature, Range = 255 µA, Code = 0, Sink Mode

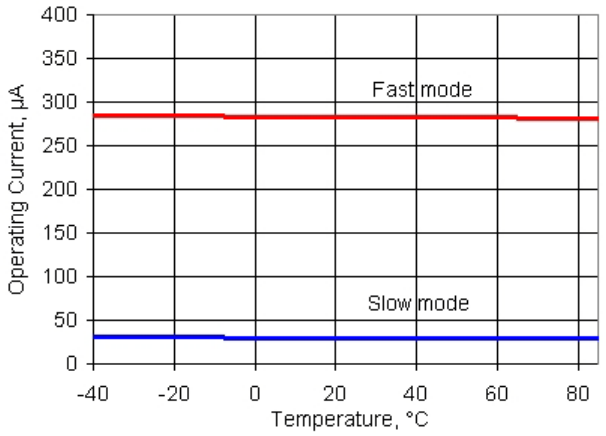


Table 11-33. IDAC AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
F_{DAC}	Update rate		–	–	8	Msps
T_{SETTLE}	Settling time to 0.5 LSB	Range = 31.875 µA or 255 µA, full scale transition, High speed mode, 600 Ω 15-pF load	–	–	125	ns
	Current noise	Range = 255 µA, source mode, High speed mode, V_{DDA} = 5 V, 10 kHz	–	340	–	pA/sqrtHz

Figure 11-51. IDAC Step Response, Codes 0x40 - 0xC0, 255 µA Mode, Source Mode, High speed mode, V_{DDA} = 5 V

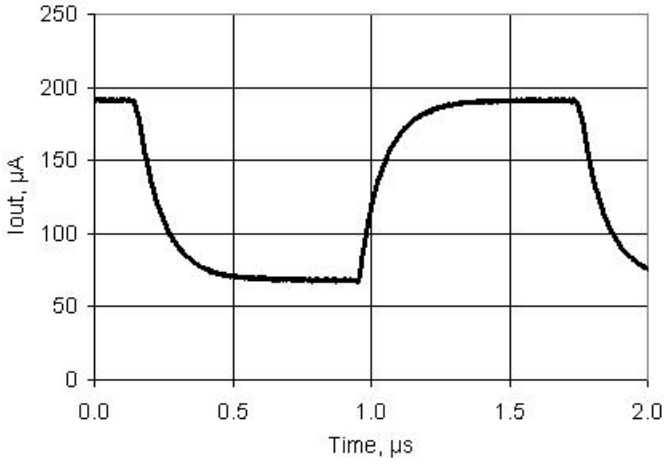


Figure 11-52. IDAC Glitch Response, Codes 0x7F - 0x80, 255 µA Mode, Source Mode, High speed mode, V_{DDA} = 5 V

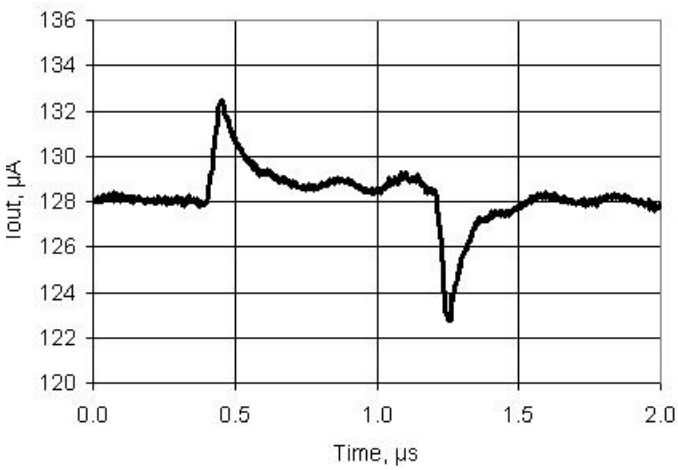


Figure 11-65. VDAC PSRR vs Frequency

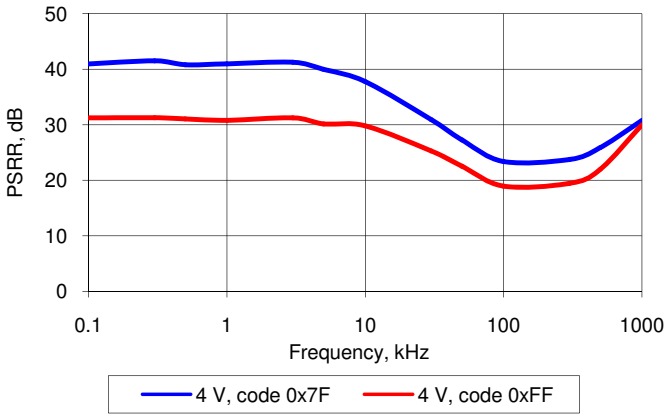
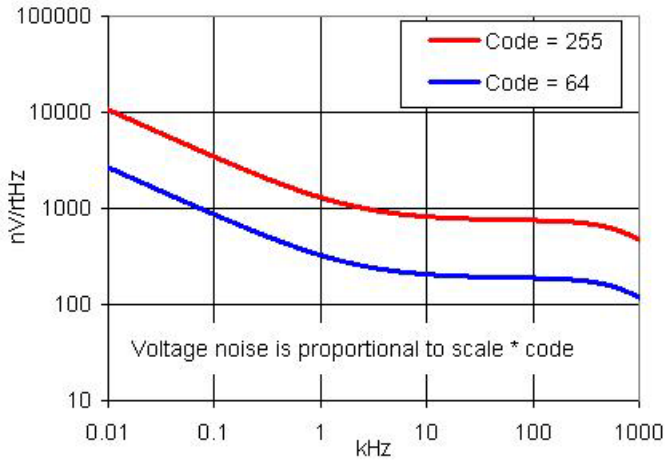


Figure 11-66. VDAC Voltage Noise, 1 V Mode, High speed mode, V_{DDA} = 5 V



11.5.8 Mixer

The mixer is created using a SC/CT analog block; see the Mixer component data sheet in PSoC Creator for full electrical specifications and APIs.

Table 11-36. Mixer DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{OS}	Input offset voltage		–	–	15	mV
	Quiescent current		–	0.9	2	mA
G	Gain		–	0	–	dB

Table 11-37. Mixer AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
f_{LO}	Local oscillator frequency	Down mixer mode	–	–	4	MHz
f_{in}	Input signal frequency	Down mixer mode	–	–	14	MHz
f_{LO}	Local oscillator frequency	Up mixer mode	–	–	1	MHz
f_{in}	Input signal frequency	Up mixer mode	–	–	1	MHz
SR	Slew rate		3	–	–	V/µs

11.5.9 Transimpedance Amplifier

The TIA is created using a SC/CT analog block; see the TIA component data sheet in PSoC Creator for full electrical specifications and APIs.

Table 11-38. Transimpedance Amplifier (TIA) DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{IOFF}	Input offset voltage		–	–	10	mV
Rconv	Conversion resistance[58]	R = 20K; 40 pF load	–25	–	+35	%
		R = 30K; 40 pF load	–25	–	+35	%
		R = 40K; 40 pF load	–25	–	+35	%
		R = 80K; 40 pF load	–25	–	+35	%
		R = 120K; 40 pF load	–25	–	+35	%
		R = 250K; 40 pF load	–25	–	+35	%
		R= 500K; 40 pF load	–25	–	+35	%
		R = 1M; 40 pF load	–25	–	+35	%
	Quiescent current		–	1.1	2	mA

Table 11-39. Transimpedance Amplifier (TIA) AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
BW	Input bandwidth (–3 dB)	R = 20K; –40 pF load	1500	–	–	kHz
		R = 120K; –40 pF load	240	–	–	kHz
		R = 1M; –40 pF load	25	–	–	kHz

Note
58. Conversion resistance values are not calibrated. Calibrated values and details about calibration are provided in PSoC Creator component data sheets. External precision resistors can also be used.

Table 11-44. LCD Direct Drive AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
f_{LCD}	LCD frame rate		10	50	150	Hz

11.6 Digital Peripherals

Specifications are valid for –40 °C ≤ T_A ≤ 85 °C and T_J ≤ 100 °C, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

11.6.1 Timer

The following specifications apply to the Timer/Counter/PWM peripheral in timer mode. Timers can also be implemented in UDBs; for more information, see the Timer component data sheet in PSoC Creator.

Table 11-45. Timer DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Block current consumption	16-bit timer, at listed input clock frequency	–	–	–	µA
	3 MHz		–	15	–	µA
	12 MHz		–	60	–	µA
	48 MHz		–	260	–	µA
	67 MHz		–	350	–	µA

Table 11-46. Timer AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Operating frequency		DC	–	67.01	MHz
	Capture pulse width (Internal)		15	–	–	ns
	Capture pulse width (external)		30	–	–	ns
	Timer resolution		15	–	–	ns
	Enable pulse width		15	–	–	ns
	Enable pulse width (external)		30	–	–	ns
	Reset pulse width		15	–	–	ns
	Reset pulse width (external)		30	–	–	ns

11.6.2 Counter

The following specifications apply to the Timer/Counter/PWM peripheral, in counter mode. Counters can also be implemented in UDBs; for more information, see the Counter component data sheet in PSoC Creator.

Table 11-47. Counter DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Block current consumption	16-bit counter, at listed input clock frequency	–	–	–	µA
	3 MHz		–	15	–	µA
	12 MHz		–	60	–	µA
	48 MHz		–	260	–	µA
	67 MHz		–	350	–	µA

Table 11-48. Counter AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Operating frequency		DC	–	67.01	MHz
	Capture pulse		15	–	–	ns
	Resolution		15	–	–	ns
	Pulse width		15	–	–	ns
	Pulse width (external)		30			ns
	Enable pulse width		15	–	–	ns
	Enable pulse width (external)		30	–	–	ns
	Reset pulse width		15	–	–	ns
	Reset pulse width (external)		30	–	–	ns

11.6.3 Pulse Width Modulation

The following specifications apply to the Timer/Counter/PWM peripheral, in PWM mode. PWM components can also be implemented in UDBs; for more information, see the PWM component data sheet in PSoC Creator.

Table 11-49. PWM DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Block current consumption	16-bit PWM, at listed input clock frequency	–	–	–	µA
	3 MHz		–	15	–	µA
	12 MHz		–	60	–	µA
	48 MHz		–	260	–	µA
	67 MHz		–	350	–	µA

Table 11-50. Pulse Width Modulation (PWM) AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Operating frequency		DC	–	67.01	MHz
	Pulse width		15	–	–	ns
	Pulse width (external)		30	–	–	ns
	Kill pulse width		15	–	–	ns
	Kill pulse width (external)		30	–	–	ns
	Enable pulse width		15	–	–	ns
	Enable pulse width (external)		30	–	–	ns
	Reset pulse width		15	–	–	ns
	Reset pulse width (external)		30	–	–	ns

11.6.7 USB

Table 11-57. USB DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{USB_5}	Device supply (V_{DDD}) for USB operation	USB configured, USB regulator enabled	4.35	–	5.25	V
$V_{USB\_3.3}$		USB configured, USB regulator bypassed	3.15	–	3.6	V
V_{USB_3}		USB configured, USB regulator bypassed[60]	2.85	–	3.6	V
$I_{USB\_Configured}$	Device supply current in device active mode, bus clock and IMO = 24 MHz	V_{DDD} = 5 V, F_{CPU} = 1.5 MHz	–	10	–	mA
		V_{DDD} = 3.3 V, F_{CPU} = 1.5 MHz	–	8	–	mA
$I_{USB\_Suspended}$	Device supply current in device sleep mode	V_{DDD} = 5 V, connected to USB host, PICU configured to wake on USB resume signal	–	0.5	–	mA
		V_{DDD} = 5 V, disconnected from USB host	–	0.3	–	mA
		V_{DDD} = 3.3 V, connected to USB host, PICU configured to wake on USB resume signal	–	0.5	–	mA
		V_{DDD} = 3.3 V, disconnected from USB host	–	0.3	–	mA

11.6.8 Universal Digital Blocks (UDBs)

PSoC Creator provides a library of prebuilt and tested standard digital peripherals (UART, SPI, LIN, PRS, CRC, timer, counter, PWM, AND, OR, and so on) that are mapped to the UDB array. See the component data sheets in PSoC Creator for full AC/DC specifications, APIs, and example code.

Table 11-58. UDB AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
Datapath Performance						
F_{MAX_TIMER}	Maximum frequency of 16-bit timer in a UDB pair		–	–	67.01	MHz
F_{MAX_ADDER}	Maximum frequency of 16-bit adder in a UDB pair		–	–	67.01	MHz
F_{MAX_CRC}	Maximum frequency of 16-bit CRC/PRS in a UDB pair		–	–	67.01	MHz
PLD Performance						
F_{MAX_PLD}	Maximum frequency of a two-pass PLD function in a UDB pair		–	–	67.01	MHz
Clock to Output Performance						
t_{CLK_OUT}	Propagation delay for clock in to data out, see Figure 11-70.	25 °C, $V_{DDD} \geq 2.7$ V	–	20	25	ns
t_{CLK_OUT}	Propagation delay for clock in to data out, see Figure 11-70.	Worst-case placement, routing, and pin selection	–	–	55	ns

Note
60. Rise/fall time matching (TR) not guaranteed, see USB Driver AC Specifications on page 87.

Table 11-78. IMO AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
F_{IMO}[74]	IMO frequency stability (with factory trim)					
	62.6 MHz		–7	–	7	%
	48 MHz		–5	–	5	%
	24 MHz – Non USB mode		–4	–	4	%
	24 MHz – USB mode	With oscillator locking to USB bus	–0.25	–	0.25	%
	12 MHz		–3	–	3	%
	6 MHz		–2	–	2	%
	3 MHz	0 °C to 70 °C	–1	–	1	%
		–40 °C to 85 °C	–1.5	–	1.5	%
	3 MHz frequency stability after typical PCB assembly post-reflow.	Typical (non-optimized) board layout and 250 °C solder reflow. Device may be calibrated after assembly to improve performance.	–	±2	–	%
	Startup time[75]	From enable (during normal system operation)	–	–	13	µs
Jp–p	Jitter (peak to peak)[75]					
	F = 24 MHz		–	0.9	–	ns
	F = 3 MHz		–	1.6	–	ns
Jperiod	Jitter (long term)[75]					
	F = 24 MHz		–	0.9	–	ns
	F = 3 MHz		–	12	–	ns

Figure 11-76. IMO Frequency Variation vs. Temperature

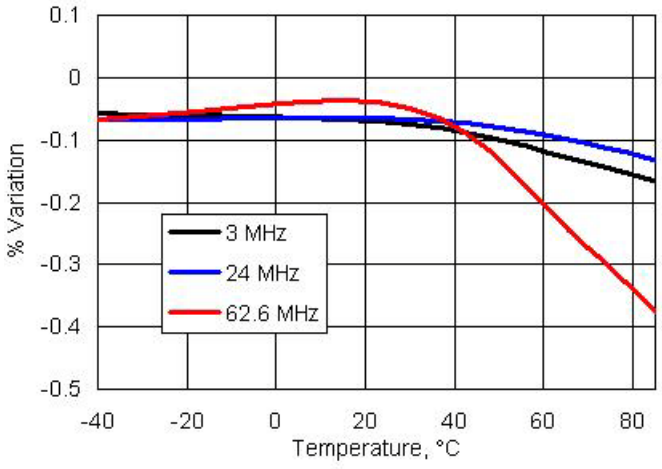
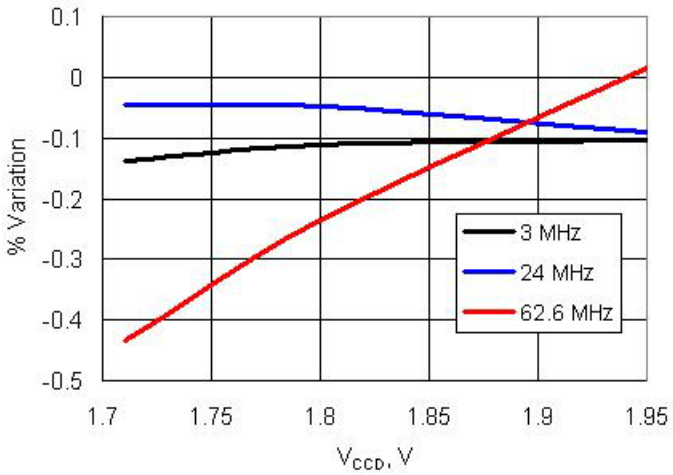


Figure 11-77. IMO Frequency Variation vs. V_{CC}



Notes
74. F_{IMO} is measured after packaging, and thus accounts for substrate and die attach stresses.
75. Based on device characterization (Not production tested).

Table 14-1. Acronyms Used in this Document *(continued)*

Acronym	Description
PHUB	peripheral hub
PHY	physical layer
PICU	port interrupt control unit
PLA	programmable logic array
PLD	programmable logic device, see also PAL
PLL	phase-locked loop
PMDD	package material declaration data sheet
POR	power-on reset
PRES	precise low-voltage reset
PRS	pseudo random sequence
PS	port read data register
PSoC®	Programmable System-on-Chip™
PSRR	power supply rejection ratio
PWM	pulse-width modulator
RAM	random-access memory
RISC	reduced-instruction-set computing
RMS	root-mean-square
RTC	real-time clock
RTL	register transfer language
RTR	remote transmission request
RX	receive
SAR	successive approximation register
SC/CT	switched capacitor/continuous time
SCL	I^2C serial clock
SDA	I^2C serial data
S/H	sample and hold
SINAD	signal to noise and distortion ratio
SIO	special input/output, GPIO with advanced features. See GPIO.
SOC	start of conversion

Table 14-1. Acronyms Used in this Document *(continued)*

Acronym	Description
SOF	start of frame
SPI	Serial Peripheral Interface, a communications protocol
SR	slew rate
SRAM	static random access memory
SRES	software reset
SWD	serial wire debug, a test protocol
SWV	single-wire viewer
TD	transaction descriptor, see also DMA
THD	total harmonic distortion
TIA	transimpedance amplifier
TRM	technical reference manual
TTL	transistor-transistor logic
TX	transmit
UART	Universal Asynchronous Transmitter Receiver, a communications protocol
UDB	universal digital block
USB	Universal Serial Bus
USBIO	USB input/output, PSoC pins used to connect to a USB port
VDAC	voltage DAC, see also DAC, IDAC
WDT	watchdog timer
WOL	write once latch, see also NVL
WRES	watchdog timer reset
XRES	external reset I/O pin
XTAL	crystal

15. Reference Documents

PSoC® 3, PSoC® 5 Architecture TRM

PSoC® 3 Registers TRM

16. Document Conventions

16.1 Units of Measure

Table 16-1. Units of Measure

Symbol	Unit of Measure
°C	degrees Celsius
dB	decibels
fF	femtofarads
Hz	hertz
KB	1024 bytes
kbps	kilobits per second
Khr	kilohours
kHz	kilohertz
kΩ	kilohms
ksps	kilosamples per second
LSB	least significant bit
Mbps	megabits per second
MHz	megahertz
MΩ	megaohms
Msps	megasamples per second
µA	microamperes
µF	microfarads
µH	microhenrys
µs	microseconds
µV	microvolts
µW	microwatts
mA	milliamperes
ms	milliseconds
mV	millivolts
nA	nanoamperes
ns	nanoseconds
nV	nanovolts
Ω	ohms
pF	picofarads
ppm	parts per million
ps	picoseconds
s	seconds
sps	samples per second
sqrtHz	square root of hertz
V	volts

Description Title: PSoC® 3: CY8C38 Family Datasheet Programmable System-on-Chip (PSoC®) *(continued)* Document Number: 001-11729				
Revision	**ECN**	**Submission Date**	**Orig. of Change**	**Description of Change**
*U	3645908	06/14/2012	MKEA	Section 2: Changed text and added figures describing Vddio source and sink. Corrected example PCB layout figure. Sections 3, 6.2: Added text about usage in externally regulated mode. Section 5.2 and elsewhere: Added text describing flash cache, and updated related text. Section 6.1, 11.91: Changed IMO startup time specification. Section 6.1.1.4: Removed text stating that FTW is a wakeup source. Section 6.2.1.4: Added paragraph clarifying limiting the frequency of IO input signals to achieve low hibernate current. Section 6.3: Changed reset status register description text. Sections 6.3.1.1, 6.3.1.2: Added text on XRES and PRES re-arm times Sections 6.3.1.1, 11.8.1: Revised description of IPOR and clarified PRES term. Added text on adjustability of buzz frequency. Section 6.4.14, 11.4: Deleted and updated text regarding SIO performance under certain power ramp conditions. Section 6.4.15: Changed text describing SIO modes for overvoltage tolerance. Section 7.8: Changed “compliant with I2C” to “compatible with I2C”. Section 7.9: Updated DFB description text. Sections 8.9, 11.5.6, 11.5.7: Changed DAC high and low speed/power mode descriptions and conditions. Section 9.1: Added a statement about support for JTAG programmers and file formats. Section 9.3: Deleted the text “debug operations are possible while the device is reset”. Section 11.1: Added specification for ESDHBM for when Vssa and Vssd are separate. Changed footnote to state that all GPIO input voltages must be less than Vddio. Changed supply ramp rate specification. Section 11.2.1: Added chip Idd specs for active and low-power modes, for multiple voltage, temperature and usage conditions. Section 11.3.3: Removed from boost mention of 22 µH inductors, and related graphs. Section 11.5.1: Changed load capacitor conditions in opamp specifications. Clarified description of opamp Iout specification. Section 11.5.3: Updated Vref temperature drift specifications. Added graphs and footnote. Section 11.5.4: Changed analog global specification descriptions and values. Section 11.5.5: Changed comparator specifications and conditions. Section 11.8.2: Voltage monitors response time specification is based on characterization. Section 13: Updated 48-QFN and 100-TQFP package drawings. Throughout document: updated terminology for “master” and “system” clock.
*V	3648803	06/18/2012	WKA/MKEA	Updated the description of changes for previous (*U) revision. No technical changes. EROS update.