# E·XFL



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#### What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

#### Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details	5
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Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	EBI/EMI, I <sup>2</sup> C, IrDA, SmartCard, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	83
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.85V ~ 3.8V
Data Converters	A/D 8x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32gg380f512-qfp100

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

# **2 System Summary**

### **2.1 System Introduction**

The EFM32 MCUs are the world's most energy friendly microcontrollers. With a unique combination of the powerful 32-bit ARM Cortex-M3, innovative low energy techniques, short wake-up time from energy saving modes, and a wide selection of peripherals, the EFM32GG microcontroller is well suited for any battery operated application as well as other systems requiring high performance and low-energy consumption. This section gives a short introduction to each of the modules in general terms and also shows a summary of the configuration for the EFM32GG380 devices. For a complete feature set and in-depth information on the modules, the reader is referred to the *EFM32GG Reference Manual*.

A block diagram of the EFM32GG380 is shown in Figure 2.1 (p. 3) .



#### Figure 2.1. Block Diagram

### 2.1.1 ARM Cortex-M3 Core

The ARM Cortex-M3 includes a 32-bit RISC processor which can achieve as much as 1.25 Dhrystone MIPS/MHz. A Memory Protection Unit with support for up to 8 memory segments is included, as well as a Wake-up Interrupt Controller handling interrupts triggered while the CPU is asleep. The EFM32 implementation of the Cortex-M3 is described in detail in *EFM32 Cortex-M3 Reference Manual*.

### 2.1.2 Debug Interface (DBG)

This device includes hardware debug support through a 2-pin serial-wire debug interface and an Embedded Trace Module (ETM) for data/instruction tracing. In addition there is also a 1-wire Serial Wire Viewer pin which can be used to output profiling information, data trace and software-generated messages.

to interface the external devices. The timing is adjustable to meet specifications of the external devices. The interface is limited to asynchronous devices.

### 2.1.11 TFT Direct Drive

The EBI contains a TFT controller which can drive a TFT via a 565 RGB interface. The TFT controller supports programmable display and port sizes and offers accurate control of frequency and setup and hold timing. Direct Drive is supported for TFT displays which do not have their own frame buffer. In that case TFT Direct Drive can transfer data from either on-chip memory or from an external memory device to the TFT at low CPU load. Automatic alpha-blending and masking is also supported for transfers through the EBI interface.

### 2.1.12 Universal Serial Bus Controller (USB)

The USB is a full-speed USB 2.0 compliant OTG host/device controller. The USB can be used in Device, On-the-go (OTG) Dual Role Device or Host-only configuration. In OTG mode the USB supports both Host Negotiation Protocol (HNP) and Session Request Protocol (SRP). The device supports both full-speed (12MBit/s) and low speed (1.5MBit/s) operation. The USB device includes an internal dedicated Descriptor-Based Scatter/Gather DMA and supports up to 6 OUT endpoints and 6 IN endpoints, in addition to endpoint 0. The on-chip PHY includes all OTG features, except for the voltage booster for supplying 5V to VBUS when operating as host.

### 2.1.13 Inter-Integrated Circuit Interface (I2C)

The  $I^2C$  module provides an interface between the MCU and a serial  $I^2C$ -bus. It is capable of acting as both a master and a slave, and supports multi-master buses. Both standard-mode, fast-mode and fast-mode plus speeds are supported, allowing transmission rates all the way from 10 kbit/s up to 1 Mbit/s. Slave arbitration and timeouts are also provided to allow implementation of an SMBus compliant system. The interface provided to software by the  $I^2C$  module, allows both fine-grained control of the transmission process and close to automatic transfers. Automatic recognition of slave addresses is provided in all energy modes.

# 2.1.14 Universal Synchronous/Asynchronous Receiver/Transmitter (US-ART)

The Universal Synchronous Asynchronous serial Receiver and Transmitter (USART) is a very flexible serial I/O module. It supports full duplex asynchronous UART communication as well as RS-485, SPI, MicroWire and 3-wire. It can also interface with ISO7816 SmartCards, IrDA and I2S devices.

### 2.1.15 Pre-Programmed USB/UART Bootloader

The bootloader presented in application note AN0042 is pre-programmed in the device at factory. The bootloader enables users to program the EFM32 through a UART or a USB CDC class virtual UART without the need for a debugger. The autobaud feature, interface and commands are described further in the application note.

### 2.1.16 Universal Asynchronous Receiver/Transmitter (UART)

The Universal Asynchronous serial Receiver and Transmitter (UART) is a very flexible serial I/O module. It supports full- and half-duplex asynchronous UART communication.

# 2.1.17 Low Energy Universal Asynchronous Receiver/Transmitter (LEUART)

The unique LEUART<sup>TM</sup>, the Low Energy UART, is a UART that allows two-way UART communication on a strict power budget. Only a 32.768 kHz clock is needed to allow UART communication up to 9600 baud/

## **3 Electrical Characteristics**

### **3.1 Test Conditions**

### **3.1.1 Typical Values**

The typical data are based on  $T_{AMB}$ =25°C and  $V_{DD}$ =3.0 V, as defined in Table 3.2 (p. 10), unless otherwise specified.

#### 3.1.2 Minimum and Maximum Values

The minimum and maximum values represent the worst conditions of ambient temperature, supply voltage and frequencies, as defined in Table 3.2 (p. 10), unless otherwise specified.

### **3.2 Absolute Maximum Ratings**

The absolute maximum ratings are stress ratings, and functional operation under such conditions are not guaranteed. Stress beyond the limits specified in Table 3.1 (p. 10) may affect the device reliability or cause permanent damage to the device. Functional operating conditions are given in Table 3.2 (p. 10).

#### Table 3.1. Absolute Maximum Ratings

Symbol	Parameter	Condition	Min	Тур	Max	Unit
T <sub>STG</sub>	Storage tempera- ture range		-40		150	°C
T <sub>S</sub>	Maximum soldering temperature	Latest IPC/JEDEC J-STD-020 Standard			260	°C
V <sub>DDMAX</sub>	External main sup- ply voltage		0		3.8	V
V <sub>IOPIN</sub>	Voltage on any I/O pin		-0.3		V <sub>DD</sub> +0.3	V
	Current per I/O pin (sink)				100	mA
IOMAX	Current per I/O pin (source)				-100	mA

### **3.3 General Operating Conditions**

### 3.3.1 General Operating Conditions

#### Table 3.2. General Operating Conditions

Symbol	Parameter	Min	Тур	Мах	Unit
T <sub>AMB</sub>	Ambient temperature range	-40		85	°C
V <sub>DDOP</sub>	Operating supply voltage	1.98		3.8	V
f <sub>APB</sub>	Internal APB clock frequency			48	MHz
f <sub>AHB</sub>	Internal AHB clock frequency			48	MHz

### 3.7 Flash

#### Table 3.6. Flash

Symbol	Parameter	Condition	Min	Тур	Max	Unit
EC <sub>FLASH</sub>	Flash erase cycles before failure		20000			cycles
		T <sub>AMB</sub> <150°C	10000			h
RET <sub>FLASH</sub>	Flash data retention	T <sub>AMB</sub> <85°C	10			years
		T <sub>AMB</sub> <70°C	20			years
t <sub>W_PROG</sub>	Word (32-bit) pro- gramming time		20			μs
4	Page erase time	LPERASE == 0	20	20.4	20.8	ms
PERASE		LPERASE == 1	40	40.4	40.8	ms
t <sub>DERASE</sub>	Device erase time				161.6	ms
	Frase current	LPERASE == 0			14 <sup>1</sup>	mA
'ERASE	Elase cullent	LPERASE == 1			7 <sup>1</sup>	mA
	Write ourrept	LPWRITE == 0			14 <sup>1</sup>	mA
WRITE	vvrite current	LPWRITE == 1			7 <sup>1</sup>	mA
V <sub>FLASH</sub>	Supply voltage dur- ing flash erase and write		1.98		3.8	V

<sup>1</sup>Measured at 25°C

### **3.8 General Purpose Input Output**

#### Table 3.7. GPIO

Symbol	Parameter	Condition	Min	Тур	Мах	Unit
V <sub>IOIL</sub>	Input low voltage				0.30V <sub>DD</sub>	V
V <sub>IOIH</sub>	Input high voltage		0.70V <sub>DD</sub>			V
		Sourcing 0.1 mA, V <sub>DD</sub> =1.98 V, GPIO_Px_CTRL DRIVEMODE = LOWEST		0.80V <sub>DD</sub>		V
	Output high volt- age (Production test condition = 3.0V, DRIVEMODE = STANDARD)	Sourcing 0.1 mA, V <sub>DD</sub> =3.0 V, GPIO_Px_CTRL DRIVEMODE = LOWEST		0.90V <sub>DD</sub>		V
		Sourcing 1 mA, V <sub>DD</sub> =1.98 V, GPIO_Px_CTRL DRIVEMODE = LOW		0.85V <sub>DD</sub>		V
VIOOH		Sourcing 1 mA, V <sub>DD</sub> =3.0 V, GPIO_Px_CTRL DRIVEMODE = LOW		0.90V <sub>DD</sub>		V
		Sourcing 6 mA, V <sub>DD</sub> =1.98 V, GPIO_Px_CTRL DRIVEMODE = STANDARD	0.75V <sub>DD</sub>			V
		Sourcing 6 mA, V <sub>DD</sub> =3.0 V, GPIO_Px_CTRL DRIVEMODE = STANDARD	0.85V <sub>DD</sub>			V



#### Figure 3.4. Typical Low-Level Output Current, 2V Supply Voltage



GPIO\_Px\_CTRL DRIVEMODE = LOWEST



GPIO\_Px\_CTRL DRIVEMODE = STANDARD



GPIO\_Px\_CTRL DRIVEMODE = LOW



GPIO\_Px\_CTRL DRIVEMODE = HIGH



#### Figure 3.5. Typical High-Level Output Current, 2V Supply Voltage



GPIO\_Px\_CTRL DRIVEMODE = STANDARD

GPIO\_Px\_CTRL DRIVEMODE = HIGH



#### Figure 3.8. Typical Low-Level Output Current, 3.8V Supply Voltage



GPIO\_Px\_CTRL DRIVEMODE = LOWEST



GPIO\_Px\_CTRL DRIVEMODE = STANDARD



GPIO\_Px\_CTRL DRIVEMODE = LOW



GPIO\_Px\_CTRL DRIVEMODE = HIGH

### 3.9 Oscillators

### 3.9.1 LFXO

#### Table 3.8. LFXO

Symbol	Parameter	Condition	Min	Тур	Max	Unit
f <sub>LFXO</sub>	Supported nominal crystal frequency			32.768		kHz
ESR <sub>LFXO</sub>	Supported crystal equivalent series re- sistance (ESR)			30	120	kOhm
C <sub>LFXOL</sub>	Supported crystal external load range		X <sup>1</sup>		25	pF
DC <sub>LFXO</sub>	Duty cycle		48	50	53.5	%
I <sub>LFXO</sub>	Current consump- tion for core and buffer after startup.	ESR=30 kOhm, C <sub>L</sub> =10 pF, LFXOBOOST in CMU_CTRL is 1		190		nA
t <sub>LFXO</sub>	Start- up time.	ESR=30 kOhm, C <sub>L</sub> =10 pF, 40% - 60% duty cycle has been reached, LFXOBOOST in CMU_CTRL is 1		400		ms

<sup>1</sup>See Minimum Load Capacitance (C<sub>LFXOL</sub>) Requirement For Safe Crystal Startup in energyAware Designer in Simplicity Studio

For safe startup of a given crystal, the Configurator tool in Simplicity Studio contains a tool to help users configure both load capacitance and software settings for using the LFXO. For details regarding the crystal configuration, the reader is referred to application note "AN0016 EFM32 Oscillator Design Consideration".

### 3.9.2 HFXO

#### Table 3.9. HFXO

Symbol	Parameter	Condition	Min	Тур	Max	Unit
f <sub>HFXO</sub>	Supported nominal crystal Frequency		4		48	MHz
	Supported crystal	Crystal frequency 48 MHz			50	Ohm
ESR <sub>HFXO</sub>	equivalent series re-	Crystal frequency 32 MHz		30	60	Ohm
	sistance (ESR)	Crystal frequency 4 MHz		400	1500	Ohm
9mHFXO	The transconduc- tance of the HFXO input transistor at crystal startup	HFXOBOOST in CMU_CTRL equals 0b11	20			mS
C <sub>HFXOL</sub>	Supported crystal external load range		5		25	pF
	Current consump- tion for HFXO after startup	4 MHz: ESR=400 Ohm, C <sub>L</sub> =20 pF, HFXOBOOST in CMU_CTRL equals 0b11		85		μA
HFX0		32 MHz: ESR=30 Ohm, C <sub>L</sub> =10 pF, HFXOBOOST in CMU_CTRL equals 0b11		165		μA
t <sub>HFXO</sub>	Startup time	32 MHz: ESR=30 Ohm, C <sub>L</sub> =10 pF, HFXOBOOST in CMU_CTRL equals 0b11		400		μs



Symbol	Parameter	Condition	Min	Тур	Max	Unit
		200 kSamples/s, 12 bit, sin- gle ended, internal 1.25V refer- ence		62		dB
		200 kSamples/s, 12 bit, single ended, internal 2.5V reference		63		dB
		200 kSamples/s, 12 bit, single ended, V <sub>DD</sub> reference		67		dB
		200 kSamples/s, 12 bit, differ- ential, internal 1.25V reference		63		dB
		200 kSamples/s, 12 bit, differ- ential, internal 2.5V reference		66		dB
		200 kSamples/s, 12 bit, differ- ential, 5V reference		66		dB
		200 kSamples/s, 12 bit, differential, $V_{DD}$ reference	63	66		dB
		200 kSamples/s, 12 bit, differ- ential, 2xV <sub>DD</sub> reference		70		dB
		1 MSamples/s, 12 bit, single ended, internal 1.25V refer- ence		58		dB
		1 MSamples/s, 12 bit, single ended, internal 2.5V reference		62		dB
		1 MSamples/s, 12 bit, single ended, V <sub>DD</sub> reference		64		dB
		1 MSamples/s, 12 bit, differen- tial, internal 1.25V reference		60		dB
		1 MSamples/s, 12 bit, differen- tial, internal 2.5V reference		64		dB
		1 MSamples/s, 12 bit, differen- tial, 5V reference		54		dB
		1 MSamples/s, 12 bit, differential, $V_{DD}$ reference		66		dB
SINAD <sub>ADC</sub>	SIgnal-to-Noise And Distortion-ratio (SINAD)	1 MSamples/s, 12 bit, differen- tial, 2xV <sub>DD</sub> reference		68		dB
		200 kSamples/s, 12 bit, sin- gle ended, internal 1.25V refer- ence		61		dB
		200 kSamples/s, 12 bit, single ended, internal 2.5V reference		65		dB
		200 kSamples/s, 12 bit, single ended, V <sub>DD</sub> reference		66		dB
		200 kSamples/s, 12 bit, differ- ential, internal 1.25V reference		63		dB
		200 kSamples/s, 12 bit, differ- ential, internal 2.5V reference		66		dB
		200 kSamples/s, 12 bit, differ- ential, 5V reference		66		dB
		200 kSamples/s, 12 bit, differential, $V_{DD}$ reference	62	65		dB

#### Figure 3.20. ADC Integral Linearity Error vs Code, Vdd = 3V, Temp = 25°C





VDD Reference



2.5V Reference



**5VDIFF Reference** 

Figure 3.22. ADC Absolute Offset, Common Mode = Vdd /2



Figure 3.23. ADC Dynamic Performance vs Temperature for all ADC References, Vdd = 3V





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Figure 3.28. OPAMP Voltage Noise Spectral Density (Unity Gain) Vout=1V



Figure 3.29. OPAMP Voltage Noise Spectral Density (Non-Unity Gain)



## **4 Pinout and Package**

#### Note

Please refer to the application note "AN0002 EFM32 Hardware Design Considerations" for guidelines on designing Printed Circuit Boards (PCB's) for the EFM32GG380.

### 4.1 Pinout

The *EFM32GG380* pinout is shown in Figure 4.1 (p. 53) and Table 4.1 (p. 53). Alternate locations are denoted by "#" followed by the location number (Multiple locations on the same pin are split with "/"). Alternate locations can be configured in the LOCATION bitfield in the \*\_ROUTE register in the module in question.

#### Figure 4.1. EFM32GG380 Pinout (top view, not to scale)



Table 4.1. Device Pinout

LQFP100 Pin# and Name						
Pin #	Pin Name	Analog	EBI	Timers	Communication	Other
1	PA0		EBI_AD09 #0/1/2	TIM0_CC0 #0/1/4	I2C0_SDA #0 LEU0_RX #4	PRS_CH0 #0 GPIO_EM4WU0
2	PA1		EBI_AD10 #0/1/2	TIM0_CC1 #0/1	I2C0_SCL #0	CMU_CLK1 #0 PRS_CH1 #0
3	PA2		EBI_AD11 #0/1/2	TIM0_CC2 #0/1		CMU_CLK0 #0



L	QFP100 Pin# and Name	Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	ЕВІ	Timers	Communication	Other
34	PA13		EBI_A01 #0/1/2	TIM2_CC1 #1		
35	PA14		EBI_A02 #0/1/2	TIM2_CC2 #1		
36	RESETn	Reset input, active low. To apply an external reset that reset is released.	source to this pin, it is re	quired to only drive this pin	low during reset, and let th	e internal pull-up ensure
37	PB9		EBI_A03 #0/1/2		U1_TX #2	
38	PB10		EBI_A04 #0/1/2		U1_RX #2	
39	PB11	DAC0_OUT0 / OPAMP_OUT0		LETIM0_OUT0 #1 TIM1_CC2 #3	I2C1_SDA #1	
40	PB12	DAC0_OUT1 / OPAMP_OUT1		LETIM0_OUT1 #1	I2C1_SCL #1	
41	AVDD_1	Analog power supply 1.				
42	PB13	HFXTAL_P			US0_CLK #4/5 LEU0_TX #1	
43	PB14	HFXTAL_N			US0_CS #4/5 LEU0_RX #1	
44	IOVDD_3	Digital IO power supply 3.		·		
45	AVDD_0	Analog power supply 0.				
46	PD0	ADC0_CH0 DAC0_OUT0ALT #4/ OPAMP_OUT0ALT OPAMP_OUT2 #1		PCNT2_S0IN #0	US1_TX #1	
47	PD1	ADC0_CH1 DAC0_OUT1ALT #4/ OPAMP_OUT1ALT		TIM0_CC0 #3 PCNT2_S1IN #0	US1_RX #1	DBG_SWO #2
48	PD2	ADC0_CH2	EBI_A27 #0/1/2	TIM0_CC1 #3	USB_DMPU #0 US1_CLK #1	DBG_SWO #3
49	PD3	ADC0_CH3 OPAMP_N2		TIM0_CC2 #3	US1_CS #1	ETM_TD1 #0/2
50	PD4	ADC0_CH4 OPAMP_P2			LEU0_TX #0	ETM_TD2 #0/2
51	PD5	ADC0_CH5 OPAMP_OUT2 #0			LEU0_RX #0	ETM_TD3 #0/2
52	PD6	ADC0_CH6 OPAMP_P1		LETIM0_OUT0 #0 TIM1_CC0 #4 PCNT0_S0IN #3	US1_RX #2 I2C0_SDA #1	LES_ALTEX0 #0 ACMP0_O #2 ETM_TD0 #0
53	PD7	ADC0_CH7 OPAMP_N1		LETIM0_OUT1 #0 TIM1_CC1 #4 PCNT0_S1IN #3	US1_TX #2 I2C0_SCL #1	CMU_CLK0 #2 LES_ALTEX1 #0 ACMP1_O #2 ETM_TCLK #0
54	PD8	BU_VIN				CMU_CLK1 #1
55	PC6	ACMP0_CH6	EBI_A05 #0/1/2		I2C0_SDA #2 LEU1_TX #0	LES_CH6 #0 ETM_TCLK #2
56	PC7	ACMP0_CH7	EBI_A06 #0/1/2		I2C0_SCL #2 LEU1_RX #0	LES_CH7 #0 ETM_TD0 #2
57	VDD_DREG	Power supply for on-chip	voltage regulator.			
58	VSS	Ground.				
59	DECOUPLE	Decouple output for on-ch	ip voltage regulator. An e	xternal capacitance of size	C <sub>DECOUPLE</sub> is required at the	nis pin.
60	PE0		EBI_A07 #0/1/2	TIM3_CC0 #1 PCNT0_S0IN #1	U0_TX #1 I2C1_SDA #2	
61	PE1		EBI_A08 #0/1/2	TIM3_CC1 #1	U0_RX #1	



L	QFP100 Pin# and Name					
Pin#	Pin Name	Analog	EBI	Timers	Communication	Other
						BOOT_RX
96	PE12		EBI_AD04 #0/1/2	TIM1_CC2 #1	US0_RX #3 US0_CLK #0 I2C0_SDA #6	CMU_CLK1 #2 LES_ALTEX6 #0
97	PE13		EBI_AD05 #0/1/2		US0_TX #3 US0_CS #0 I2C0_SCL #6	LES_ALTEX7 #0 ACMP0_O #0 GPIO_EM4WU5
98	PE14		EBI_AD06 #0/1/2	TIM3_CC0 #0	LEU0_TX #2	
99	PE15		EBI_AD07 #0/1/2	TIM3_CC1 #0	LEU0_RX #2	
100	PA15		EBI_AD08 #0/1/2	TIM3_CC2 #0		

### **4.2 Alternate Functionality Pinout**

A wide selection of alternate functionality is available for multiplexing to various pins. This is shown in Table 4.2 (p. 57). The table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

Note

Some functionality, such as analog interfaces, do not have alternate settings or a LOCA-TION bitfield. In these cases, the pinout is shown in the column corresponding to LOCA-TION 0.

Alternate			LOC	ATION				
Functionality	0	1	2	3	4	5	6	Description
ACMP0_CH0	PC0							Analog comparator ACMP0, channel 0.
ACMP0_CH1	PC1							Analog comparator ACMP0, channel 1.
ACMP0_CH2	PC2							Analog comparator ACMP0, channel 2.
ACMP0_CH3	PC3							Analog comparator ACMP0, channel 3.
ACMP0_CH4	PC4							Analog comparator ACMP0, channel 4.
ACMP0_CH5	PC5							Analog comparator ACMP0, channel 5.
ACMP0_CH6	PC6							Analog comparator ACMP0, channel 6.
ACMP0_CH7	PC7							Analog comparator ACMP0, channel 7.
ACMP0_O	PE13	PE2	PD6					Analog comparator ACMP0, digital output.
ACMP1_CH0	PC8							Analog comparator ACMP1, channel 0.
ACMP1_CH1	PC9							Analog comparator ACMP1, channel 1.
ACMP1_CH2	PC10							Analog comparator ACMP1, channel 2.
ACMP1_CH3	PC11							Analog comparator ACMP1, channel 3.
ACMP1_O	PF2	PE3	PD7					Analog comparator ACMP1, digital output.
ADC0_CH0	PD0							Analog to digital converter ADC0, input channel number 0.
ADC0_CH1	PD1							Analog to digital converter ADC0, input channel number 1.
ADC0_CH2	PD2							Analog to digital converter ADC0, input channel number 2.
ADC0_CH3	PD3							Analog to digital converter ADC0, input channel number 3.
ADC0_CH4	PD4							Analog to digital converter ADC0, input channel number 4.

#### Table 4.2. Alternate functionality overview

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Alternate			LOC	ATION				
Functionality	0	1	2	3	4	5	6	Description
EBI_A11	PE4	PE4	PE4					External Bus Interface (EBI) address output pin 11.
EBI_A12	PE5	PE5	PE5					External Bus Interface (EBI) address output pin 12.
EBI_A13	PE6	PE6	PE6					External Bus Interface (EBI) address output pin 13.
EBI_A14	PE7	PE7	PE7					External Bus Interface (EBI) address output pin 14.
EBI_A15	PC8	PC8	PC8					External Bus Interface (EBI) address output pin 15.
EBI_A16	PB0	PB0	PB0					External Bus Interface (EBI) address output pin 16.
EBI_A17	PB1	PB1	PB1					External Bus Interface (EBI) address output pin 17.
EBI_A18	PB2	PB2	PB2					External Bus Interface (EBI) address output pin 18.
EBI_A19	PB3	PB3	PB3					External Bus Interface (EBI) address output pin 19.
EBI_A20	PB4	PB4	PB4					External Bus Interface (EBI) address output pin 20.
EBI_A21	PB5	PB5	PB5					External Bus Interface (EBI) address output pin 21.
EBI_A22	PB6	PB6	PB6					External Bus Interface (EBI) address output pin 22.
EBI_A23	PC0	PC0	PC0					External Bus Interface (EBI) address output pin 23.
EBI_A24	PC1	PC1	PC1					External Bus Interface (EBI) address output pin 24.
EBI_A25	PC2	PC2	PC2					External Bus Interface (EBI) address output pin 25.
EBI_A26	PC4	PC4	PC4					External Bus Interface (EBI) address output pin 26.
EBI_A27	PD2	PD2	PD2					External Bus Interface (EBI) address output pin 27.
EBI_AD00	PE8	PE8	PE8					External Bus Interface (EBI) address and data input / out- put pin 00.
EBI_AD01	PE9	PE9	PE9					External Bus Interface (EBI) address and data input / out- put pin 01.
EBI_AD02	PE10	PE10	PE10					External Bus Interface (EBI) address and data input / out- put pin 02.
EBI_AD03	PE11	PE11	PE11					External Bus Interface (EBI) address and data input / out- put pin 03.
EBI_AD04	PE12	PE12	PE12					External Bus Interface (EBI) address and data input / out- put pin 04.
EBI_AD05	PE13	PE13	PE13					External Bus Interface (EBI) address and data input / out- put pin 05.
EBI_AD06	PE14	PE14	PE14					External Bus Interface (EBI) address and data input / out- put pin 06.
EBI_AD07	PE15	PE15	PE15					External Bus Interface (EBI) address and data input / out- put pin 07.
EBI_AD08	PA15	PA15	PA15					External Bus Interface (EBI) address and data input / out- put pin 08.
EBI_AD09	PA0	PA0	PA0					External Bus Interface (EBI) address and data input / out- put pin 09.
EBI_AD10	PA1	PA1	PA1					External Bus Interface (EBI) address and data input / out- put pin 10.
EBI_AD11	PA2	PA2	PA2					External Bus Interface (EBI) address and data input / out- put pin 11.
EBI_AD12	PA3	PA3	PA3					External Bus Interface (EBI) address and data input / out- put pin 12.
EBI_AD13	PA4	PA4	PA4					External Bus Interface (EBI) address and data input / out- put pin 13.
EBI_AD14	PA5	PA5	PA5					External Bus Interface (EBI) address and data input / out- put pin 14.
EBI_AD15	PA6	PA6	PA6					External Bus Interface (EBI) address and data input / out-put pin 15.

### 4.5 LQFP100 Package

#### Figure 4.3. LQFP100



#### Note:

- 1. Datum 'T', 'U' and 'Z' to be determined at datum plane 'H'.
- 2. Datum 'D' and 'E' to be determined at seating plane datum 'Y'.
- 3. Dimension 'D1' and 'E1' do not include mold protrusions. Allowable protrusion is 0.25 per side. Dimensions 'D1' and 'E1' do include mold mismatch and are determined at datum plane datum 'H'.
- 4. Dimension 'b' does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum 'b' dimension by more than 0.08 mm. Dambar can not be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm
- 5. Exact shape of each corner is optional.

# 6 Chip Marking, Revision and Errata

### 6.1 Chip Marking

In the illustration below package fields and position are shown.

Figure 6.1. Example Chip Marking (top view)



### 6.2 Revision

The revision of a chip can be determined from the "Revision" field in Figure 6.1 (p. 69).

### 6.3 Errata

Please see the errata document for EFM32GG380 for description and resolution of device erratas. This document is available in Simplicity Studio and online at: http://www.silabs.com/support/pages/document-library.aspx?p=MCUs--32-bit

# **7 Revision History**

### 7.1 Revision 1.40

March 21st, 2016

Added clarification on conditions for INL<sub>ADC</sub> and DNL<sub>ADC</sub> parameters.

Reduced maximum and typical current consumption for all EM0 entries except 48 MHz in the Current Consumption table in the Electrical Characteristics section.

Increased maximum specifications for EM2 current, EM3 current, and EM4 current in the Current Consumption table in the Electrical Characteristics section.

Increased typical specification for EM2 and EM3 current at 85 C in the Current Consumption table in the Electrical Characteristics section.

Added EM2, EM3, and EM4 current consumption vs. temperature graphs.

Added a new EM2 entry and specified the existing specification is for EM0 for the BOD threshold on falling external supply voltage in the Power Management table in the Electrical Characteristics section.

Reduced maximum input leakage current in the GPIO table in the Electrical Characteristics section.

Added a maximum current consumption specification to the LFRCO table in the Electrical Characteristics section.

Added maximum specifications for the active current including references for two channels to the DAC table in the Electrical Characteristics section.

Increased the maximum specification for DAC offset voltage in the DAC table in the Electrical Characteristics section.

Increased the typical specifications for active current with FULLBIAS=1 and capacitive sense internal resistance in the ACMP table in the Electrical Characteristics section.

Added minimum and maximum specifications and updated the typical value for the VCMP offset voltage in the VCMP table in the Electrical Characteristics section.

Removed the maximum specification and reduced the typical value for hysteresis in the VCMP table in the Electrical Characteristics section.

Updated all graphs in the Electrical Characteristics section to display data for 2.0 V as the minimum voltage.

### 7.2 Revision 1.30

May 23rd, 2014

Removed "preliminary" markings

Updated HFRCO figures.

Corrected single power supply voltage minimum value from 1.85V to 1.98V.

Updated Current Consumption information.

Updated Power Management information.



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