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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	EBI/EMI, I ² C, IrDA, SmartCard, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	83
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.85V ~ 3.8V
Data Converters	A/D 8x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32gg380f512-qfp100t

2.1.3 Memory System Controller (MSC)

The Memory System Controller (MSC) is the program memory unit of the EFM32GG microcontroller. The flash memory is readable and writable from both the Cortex-M3 and DMA. The flash memory is divided into two blocks; the main block and the information block. Program code is normally written to the main block. Additionally, the information block is available for special user data and flash lock bits. There is also a read-only page in the information block containing system and device calibration data. Read and write operations are supported in the energy modes EM0 and EM1.

2.1.4 Direct Memory Access Controller (DMA)

The Direct Memory Access (DMA) controller performs memory operations independently of the CPU. This has the benefit of reducing the energy consumption and the workload of the CPU, and enables the system to stay in low energy modes when moving for instance data from the USART to RAM or from the External Bus Interface to a PWM-generating timer. The DMA controller uses the PL230 μ DMA controller licensed from ARM.

2.1.5 Reset Management Unit (RMU)

The RMU is responsible for handling the reset functionality of the EFM32GG.

2.1.6 Energy Management Unit (EMU)

The Energy Management Unit (EMU) manage all the low energy modes (EM) in EFM32GG microcontrollers. Each energy mode manages if the CPU and the various peripherals are available. The EMU can also be used to turn off the power to unused SRAM blocks.

2.1.7 Clock Management Unit (CMU)

The Clock Management Unit (CMU) is responsible for controlling the oscillators and clocks on-board the EFM32GG. The CMU provides the capability to turn on and off the clock on an individual basis to all peripheral modules in addition to enable/disable and configure the available oscillators. The high degree of flexibility enables software to minimize energy consumption in any specific application by not wasting power on peripherals and oscillators that are inactive.

2.1.8 Watchdog (WDOG)

The purpose of the watchdog timer is to generate a reset in case of a system failure, to increase application reliability. The failure may e.g. be caused by an external event, such as an ESD pulse, or by a software failure.

2.1.9 Peripheral Reflex System (PRS)

The Peripheral Reflex System (PRS) system is a network which lets the different peripheral module communicate directly with each other without involving the CPU. Peripheral modules which send out Reflex signals are called producers. The PRS routes these reflex signals to consumer peripherals which apply actions depending on the data received. The format for the Reflex signals is not given, but edge triggers and other functionality can be applied by the PRS.

2.1.10 External Bus Interface (EBI)

The External Bus Interface provides access to external parallel interface devices such as SRAM, FLASH, ADCs and LCDs. The interface is memory mapped into the address bus of the Cortex-M3. This enables seamless access from software without manually manipulating the IO settings each time a read or write is performed. The data and address lines are multiplexed in order to reduce the number of pins required

to interface the external devices. The timing is adjustable to meet specifications of the external devices. The interface is limited to asynchronous devices.

2.1.11 TFT Direct Drive

The EBI contains a TFT controller which can drive a TFT via a 565 RGB interface. The TFT controller supports programmable display and port sizes and offers accurate control of frequency and setup and hold timing. Direct Drive is supported for TFT displays which do not have their own frame buffer. In that case TFT Direct Drive can transfer data from either on-chip memory or from an external memory device to the TFT at low CPU load. Automatic alpha-blending and masking is also supported for transfers through the EBI interface.

2.1.12 Universal Serial Bus Controller (USB)

The USB is a full-speed USB 2.0 compliant OTG host/device controller. The USB can be used in Device, On-the-go (OTG) Dual Role Device or Host-only configuration. In OTG mode the USB supports both Host Negotiation Protocol (HNP) and Session Request Protocol (SRP). The device supports both full-speed (12MBit/s) and low speed (1.5MBit/s) operation. The USB device includes an internal dedicated Descriptor-Based Scatter/Gather DMA and supports up to 6 OUT endpoints and 6 IN endpoints, in addition to endpoint 0. The on-chip PHY includes all OTG features, except for the voltage booster for supplying 5V to VBUS when operating as host.

2.1.13 Inter-Integrated Circuit Interface (I²C)

The I²C module provides an interface between the MCU and a serial I²C-bus. It is capable of acting as both a master and a slave, and supports multi-master buses. Both standard-mode, fast-mode and fast-mode plus speeds are supported, allowing transmission rates all the way from 10 kbit/s up to 1 Mbit/s. Slave arbitration and timeouts are also provided to allow implementation of an SMBus compliant system. The interface provided to software by the I²C module, allows both fine-grained control of the transmission process and close to automatic transfers. Automatic recognition of slave addresses is provided in all energy modes.

2.1.14 Universal Synchronous/Asynchronous Receiver/Transmitter (USART)

The Universal Synchronous Asynchronous serial Receiver and Transmitter (USART) is a very flexible serial I/O module. It supports full duplex asynchronous UART communication as well as RS-485, SPI, MicroWire and 3-wire. It can also interface with ISO7816 SmartCards, IrDA and I2S devices.

2.1.15 Pre-Programmed USB/UART Bootloader

The bootloader presented in application note AN0042 is pre-programmed in the device at factory. The bootloader enables users to program the EFM32 through a UART or a USB CDC class virtual UART without the need for a debugger. The autobaud feature, interface and commands are described further in the application note.

2.1.16 Universal Asynchronous Receiver/Transmitter (UART)

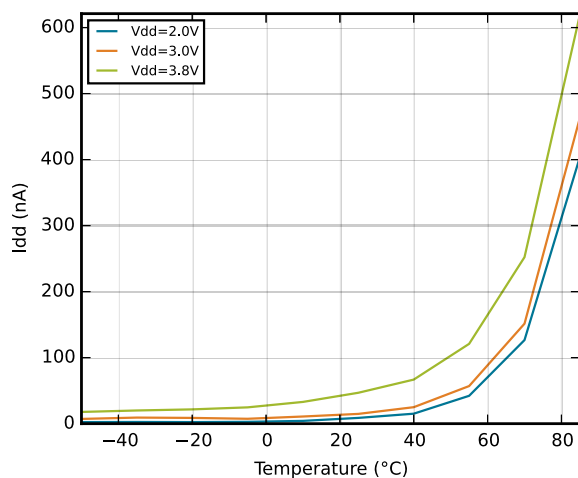
The Universal Asynchronous serial Receiver and Transmitter (UART) is a very flexible serial I/O module. It supports full- and half-duplex asynchronous UART communication.

2.1.17 Low Energy Universal Asynchronous Receiver/Transmitter (LEUART)

The unique LEUART[™], the Low Energy UART, is a UART that allows two-way UART communication on a strict power budget. Only a 32.768 kHz clock is needed to allow UART communication up to 9600 baud/

3.4.3 EM4 Current Consumption

Figure 3.3. EM4 current consumption.



3.5 Transition between Energy Modes

The transition times are measured from the trigger to the first clock edge in the CPU.

Table 3.4. Energy Modes Transitions

Symbol	Parameter	Min	Typ	Max	Unit
t_{EM10}	Transition time from EM1 to EM0		0		HF-CORE-CLK cycles
t_{EM20}	Transition time from EM2 to EM0		2		μ s
t_{EM30}	Transition time from EM3 to EM0		2		μ s
t_{EM40}	Transition time from EM4 to EM0		163		μ s

3.6 Power Management

The EFM32GG requires the AVDD_x, VDD_DREG and IOVDD_x pins to be connected together (with optional filter) at the PCB level. For practical schematic recommendations, please see the application note, "AN0002 EFM32 Hardware Design Considerations".

3.7 Flash

Table 3.6. Flash

Symbol	Parameter	Condition	Min	Typ	Max	Unit
EC _{FLASH}	Flash erase cycles before failure		20000			cycles
RET _{FLASH}	Flash data retention	T _{AMB} <150°C	10000			h
		T _{AMB} <85°C	10			years
		T _{AMB} <70°C	20			years
t _{W_PROG}	Word (32-bit) programming time		20			µs
t _{PERASE}	Page erase time	LPERASE == 0	20	20.4	20.8	ms
		LPERASE == 1	40	40.4	40.8	ms
t _{DERASE}	Device erase time				161.6	ms
I _{ERASE}	Erase current	LPERASE == 0			14 ¹	mA
		LPERASE == 1			7 ¹	mA
I _{WRITE}	Write current	LPWRITE == 0			14 ¹	mA
		LPWRITE == 1			7 ¹	mA
V _{FLASH}	Supply voltage during flash erase and write		1.98		3.8	V

¹ Measured at 25°C

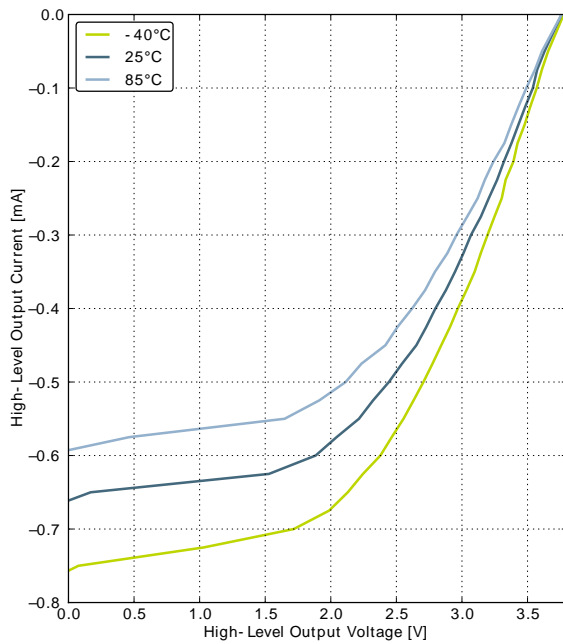
3.8 General Purpose Input Output

Table 3.7. GPIO

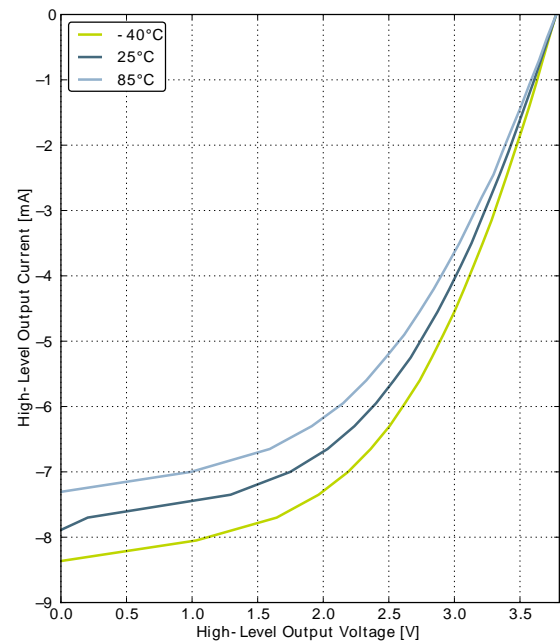
Symbol	Parameter	Condition	Min	Typ	Max	Unit
V _{IOIL}	Input low voltage				0.30V _{DD}	V
V _{IOIH}	Input high voltage		0.70V _{DD}			V
V _{IOOH}	Output high voltage (Production test condition = 3.0V, DRIVEMODE = STANDARD)	Sourcing 0.1 mA, V _{DD} =1.98 V, GPIO_Px_CTRL DRIVEMODE = LOWEST		0.80V _{DD}		V
		Sourcing 0.1 mA, V _{DD} =3.0 V, GPIO_Px_CTRL DRIVEMODE = LOWEST		0.90V _{DD}		V
		Sourcing 1 mA, V _{DD} =1.98 V, GPIO_Px_CTRL DRIVEMODE = LOW		0.85V _{DD}		V
		Sourcing 1 mA, V _{DD} =3.0 V, GPIO_Px_CTRL DRIVEMODE = LOW		0.90V _{DD}		V
		Sourcing 6 mA, V _{DD} =1.98 V, GPIO_Px_CTRL DRIVEMODE = STANDARD	0.75V _{DD}			V
		Sourcing 6 mA, V _{DD} =3.0 V, GPIO_Px_CTRL DRIVEMODE = STANDARD	0.85V _{DD}			V

Symbol	Parameter	Condition	Min	Typ	Max	Unit
		Sourcing 20 mA, $V_{DD}=1.98$ V, GPIO_Px_CTRL DRIVEMODE = HIGH	$0.60V_{DD}$			V
		Sourcing 20 mA, $V_{DD}=3.0$ V, GPIO_Px_CTRL DRIVEMODE = HIGH	$0.80V_{DD}$			V
V_{IOOL}	Output low voltage (Production test condition = 3.0V, DRIVEMODE = STANDARD)	Sinking 0.1 mA, $V_{DD}=1.98$ V, GPIO_Px_CTRL DRIVEMODE = LOWEST		$0.20V_{DD}$		V
		Sinking 0.1 mA, $V_{DD}=3.0$ V, GPIO_Px_CTRL DRIVEMODE = LOWEST		$0.10V_{DD}$		V
		Sinking 1 mA, $V_{DD}=1.98$ V, GPIO_Px_CTRL DRIVEMODE = LOW		$0.10V_{DD}$		V
		Sinking 1 mA, $V_{DD}=3.0$ V, GPIO_Px_CTRL DRIVEMODE = LOW		$0.05V_{DD}$		V
		Sinking 6 mA, $V_{DD}=1.98$ V, GPIO_Px_CTRL DRIVEMODE = STANDARD			$0.30V_{DD}$	V
		Sinking 6 mA, $V_{DD}=3.0$ V, GPIO_Px_CTRL DRIVEMODE = STANDARD			$0.20V_{DD}$	V
		Sinking 20 mA, $V_{DD}=1.98$ V, GPIO_Px_CTRL DRIVEMODE = HIGH			$0.35V_{DD}$	V
		Sinking 20 mA, $V_{DD}=3.0$ V, GPIO_Px_CTRL DRIVEMODE = HIGH			$0.20V_{DD}$	V
I_{IOLEAK}	Input leakage current	High Impedance IO connected to GROUND or V_{DD}		± 0.1	± 40	nA
R_{PU}	I/O pin pull-up resistor			40		kOhm
R_{PD}	I/O pin pull-down resistor			40		kOhm
R_{IOESD}	Internal ESD series resistor			200		Ohm
$t_{IOGLITCH}$	Pulse width of pulses to be removed by the glitch suppression filter		10		50	ns
t_{IOOF}	Output fall time	GPIO_Px_CTRL DRIVEMODE = LOWEST and load capacitance $C_L=12.5-25$ pF.	$20+0.1C_L$		250	ns
		GPIO_Px_CTRL DRIVEMODE = LOW and load capacitance $C_L=350-600$ pF	$20+0.1C_L$		250	ns
V_{IOHYST}	I/O pin hysteresis ($V_{IOTHR+} - V_{IOTHR-}$)	$V_{DD} = 1.98 - 3.8$ V	$0.10V_{DD}$			V

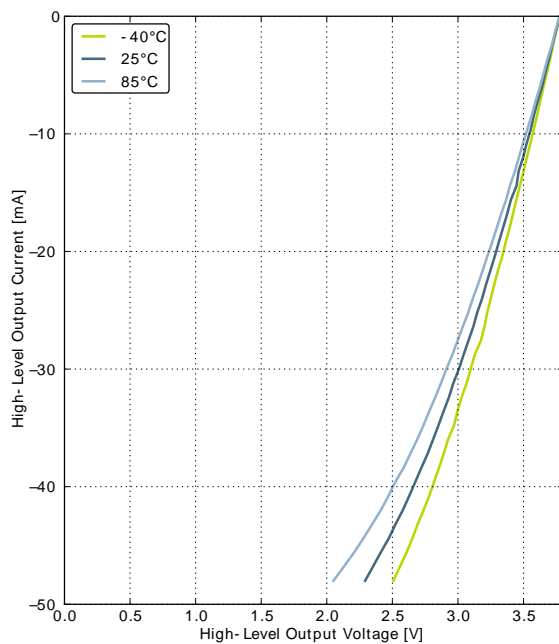
Figure 3.9. Typical High-Level Output Current, 3.8V Supply Voltage



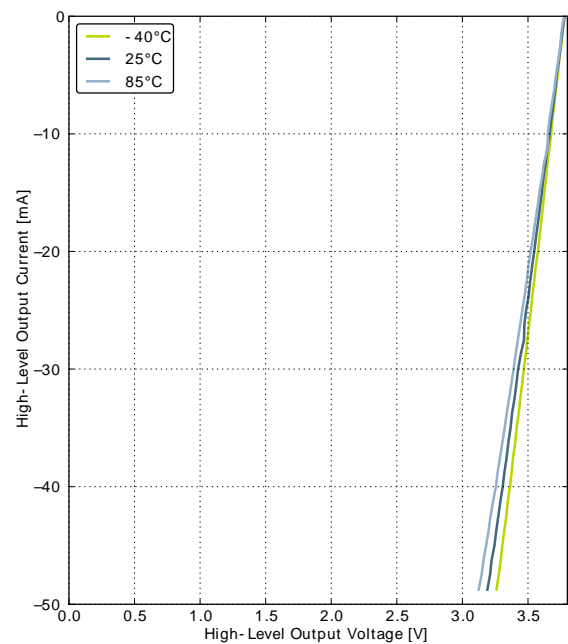
GPIO_Px_CTRL DRIVEMODE = LOWEST



GPIO_Px_CTRL DRIVEMODE = LOW



GPIO_Px_CTRL DRIVEMODE = STANDARD



GPIO_Px_CTRL DRIVEMODE = HIGH

Symbol	Parameter	Condition	Min	Typ	Max	Unit
GAIN _{ED}	Gain error drift	1.25V reference		0.01 ²	0.033 ³	%/°C
		2.5V reference		0.01 ²	0.03 ³	%/°C
OFFSET _{ED}	Offset error drift	1.25V reference		0.2 ²	0.7 ³	LSB/°C
		2.5V reference		0.2 ²	0.62 ³	LSB/°C

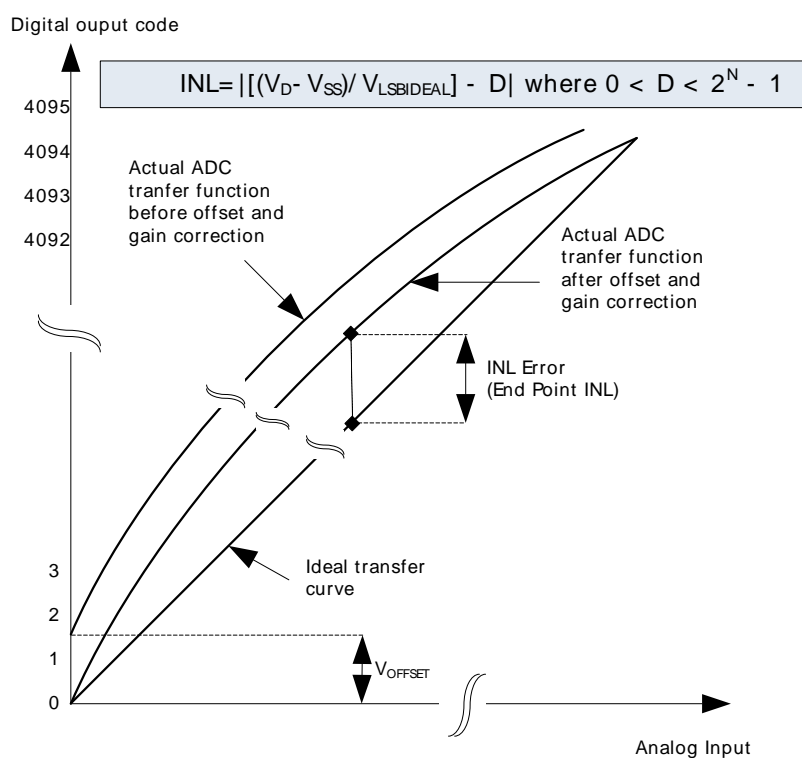
¹On the average every ADC will have one missing code, most likely to appear around 2048 +/- n*512 where n can be a value in the set {-3, -2, -1, 1, 2, 3}. There will be no missing code around 2048, and in spite of the missing code the ADC will be monotonic at all times so that a response to a slowly increasing input will always be a slowly increasing output. Around the one code that is missing, the neighbour codes will look wider in the DNL plot. The spectra will show spurs on the level of -78dBc for a full scale input for chips that have the missing code issue.

²Typical numbers given by $\text{abs}(\text{Mean}) / (85 - 25)$.

³Max number given by $(\text{abs}(\text{Mean}) + 3 \times \text{stddev}) / (85 - 25)$.

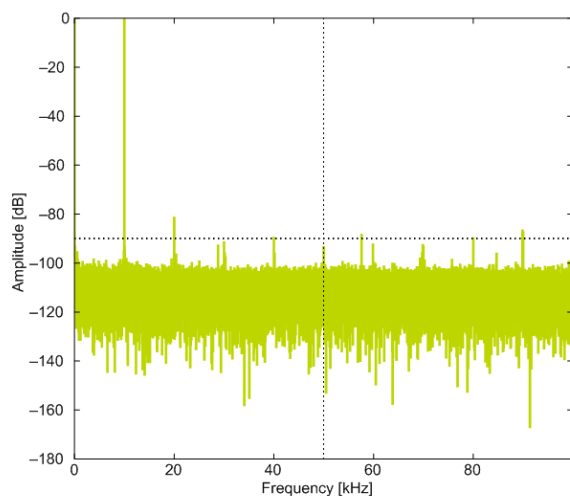
The integral non-linearity (INL) and differential non-linearity parameters are explained in Figure 3.17 (p. 32) and Figure 3.18 (p. 33) , respectively.

Figure 3.17. Integral Non-Linearity (INL)

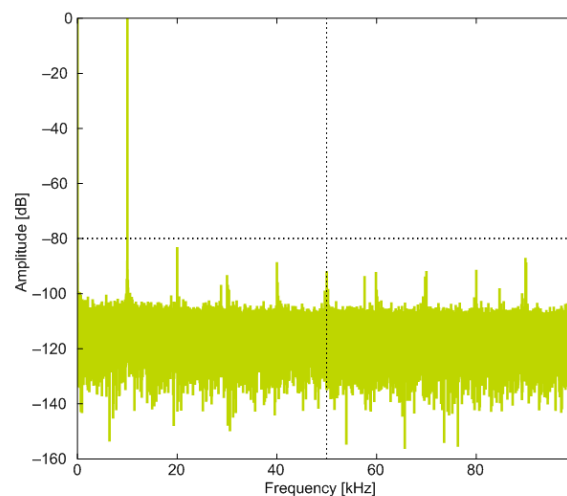


3.10.1 Typical performance

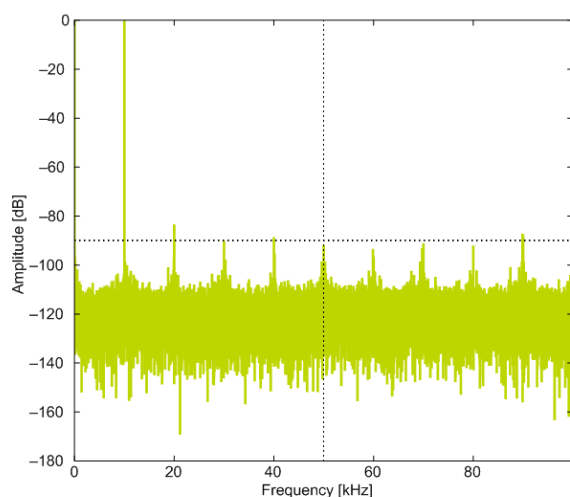
Figure 3.19. ADC Frequency Spectrum, $V_{dd} = 3V$, $Temp = 25^{\circ}C$



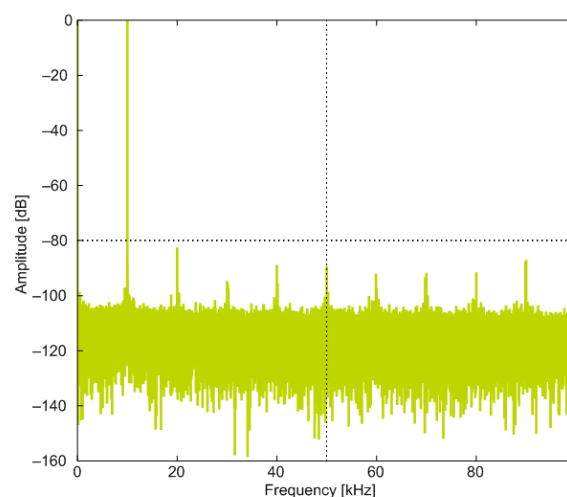
1.25V Reference



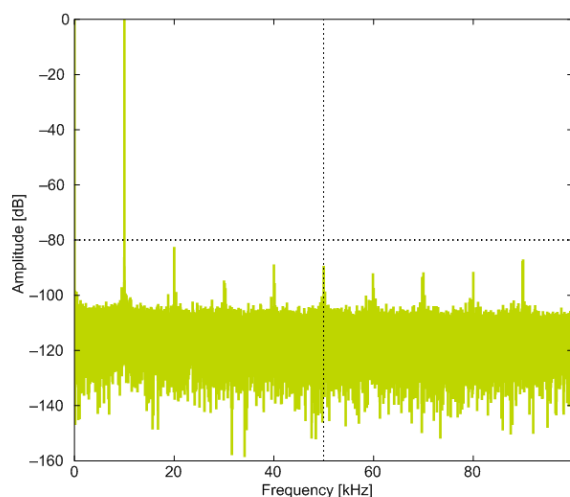
2.5V Reference



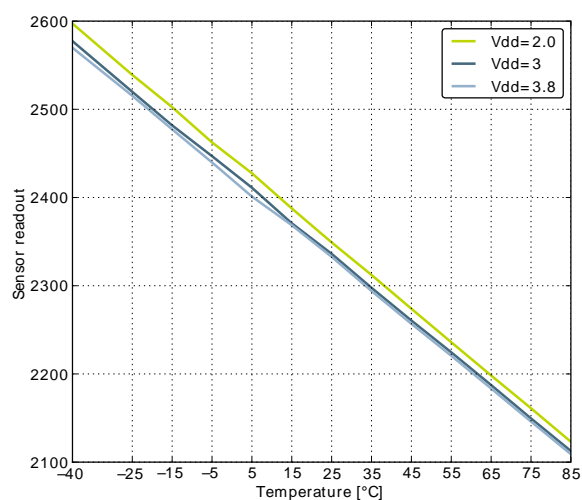
2XVDDVSS Reference



5VDIFF Reference



VDD Reference

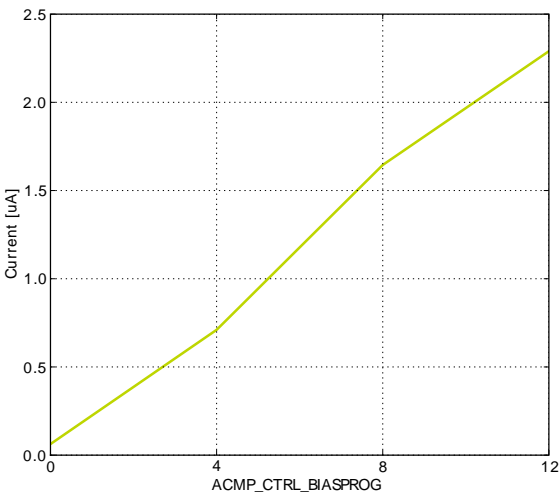
Figure 3.24. ADC Temperature sensor readout

3.11 Digital Analog Converter (DAC)

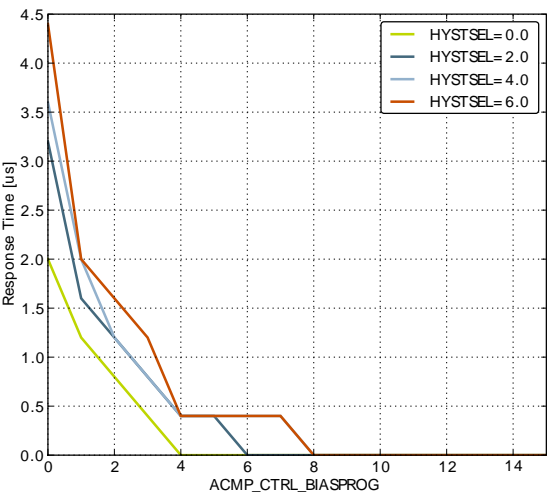
Table 3.15. DAC

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DACOUT}	Output voltage range	VDD voltage reference, single ended	0		V_{DD}	V
		VDD voltage reference, differential	$-V_{DD}$		V_{DD}	V
V_{DACCM}	Output common mode voltage range		0		V_{DD}	V
I_{DAC}	Active current including references for 2 channels	500 kSamples/s, 12 bit		400 ¹	600 ¹	μA
		100 kSamples/s, 12 bit		200 ¹	260 ¹	μA
		1 kSamples/s 12 bit NORMAL		17 ¹	25 ¹	μA
SR_{DAC}	Sample rate				500	ksamples/s
f_{DAC}	DAC clock frequency	Continuous Mode			1000	kHz
		Sample/Hold Mode			250	kHz
		Sample/Off Mode			250	kHz
$CYC_{DACCONV}$	Clock cycles per conversion			2		
$t_{DACCONV}$	Conversion time		2			μs
$t_{DACSETTLE}$	Settling time			5		μs
SNR_{DAC}	Signal to Noise Ratio (SNR)	500 kSamples/s, 12 bit, single ended, internal 1.25V reference		58		dB
		500 kSamples/s, 12 bit, single ended, internal 2.5V reference		59		dB
		500 kSamples/s, 12 bit, differential, internal 1.25V reference		58		dB

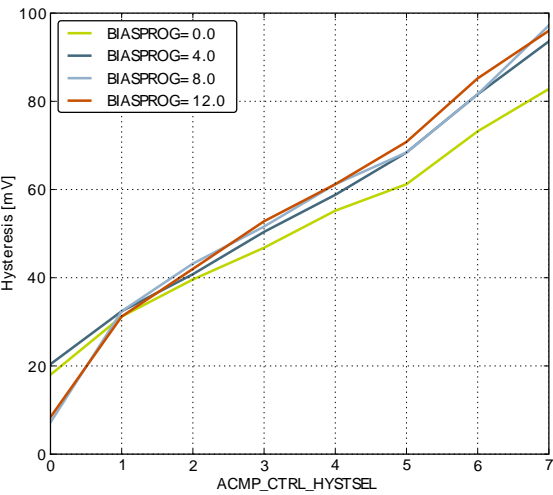
Figure 3.30. ACMP Characteristics, Vdd = 3V, Temp = 25°C, FULLBIAS = 0, HALFBIAS = 1



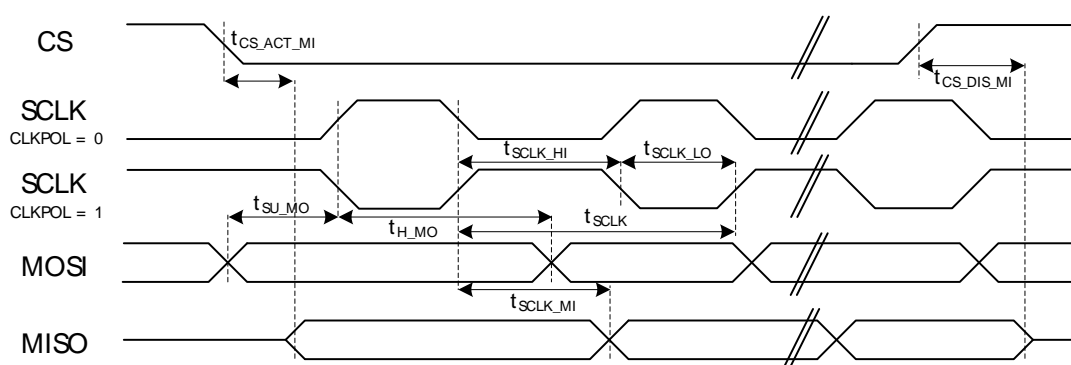
Current consumption, HYSTSEL = 4



Response time



Hysteresis

Figure 3.37. SPI Slave Timing**Table 3.28. SPI Slave Timing**

Symbol	Parameter	Min	Typ	Max	Unit
$t_{SCLK_sl}^{1,2}$	SCKL period	$2 * t_{HFPER-CLK}$			ns
$t_{SCLK_hi}^{1,2}$	SCLK high period	$3 * t_{HFPER-CLK}$			ns
$t_{SCLK_lo}^{1,2}$	SCLK low period	$3 * t_{HFPER-CLK}$			ns
$t_{CS_ACT_MI}^{1,2}$	CS active to MISO	4.00		30.00	ns
$t_{CS_DIS_MI}^{1,2}$	CS disable to MISO	4.00		30.00	ns
$t_{SU_MO}^{1,2}$	MOSI setup time	4.00			ns
$t_{H_MO}^{1,2}$	MOSI hold time	$2 + 2 * t_{HF-CLK}$			ns
$t_{SCLK_MI}^{1,2}$	SCLK to MISO	$9 + t_{HFPER-CLK}$		$36 + 2 * t_{HF-CLK}$	ns

¹ Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0)

² Measurement done at 10% and 90% of V_{DD} (figure shows 50% of V_{DD})

3.18 USB

The USB hardware in the EFM32GG380 passes all tests for USB 2.0 Full Speed certification. See the test-report distributed with application note "AN0046 - USB Hardware Design Guide".

3.19 Digital Peripherals

Table 3.29. Digital Peripherals

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{USART}	USART current	USART idle current, clock enabled		4.9		$\mu A / MHz$
I_{UART}	UART current	UART idle current, clock enabled		3.4		$\mu A / MHz$
I_{LEUART}	LEUART current	LEUART idle current, clock enabled		140		nA
I_{I2C}	I2C current	I2C idle current, clock enabled		6.1		$\mu A / MHz$

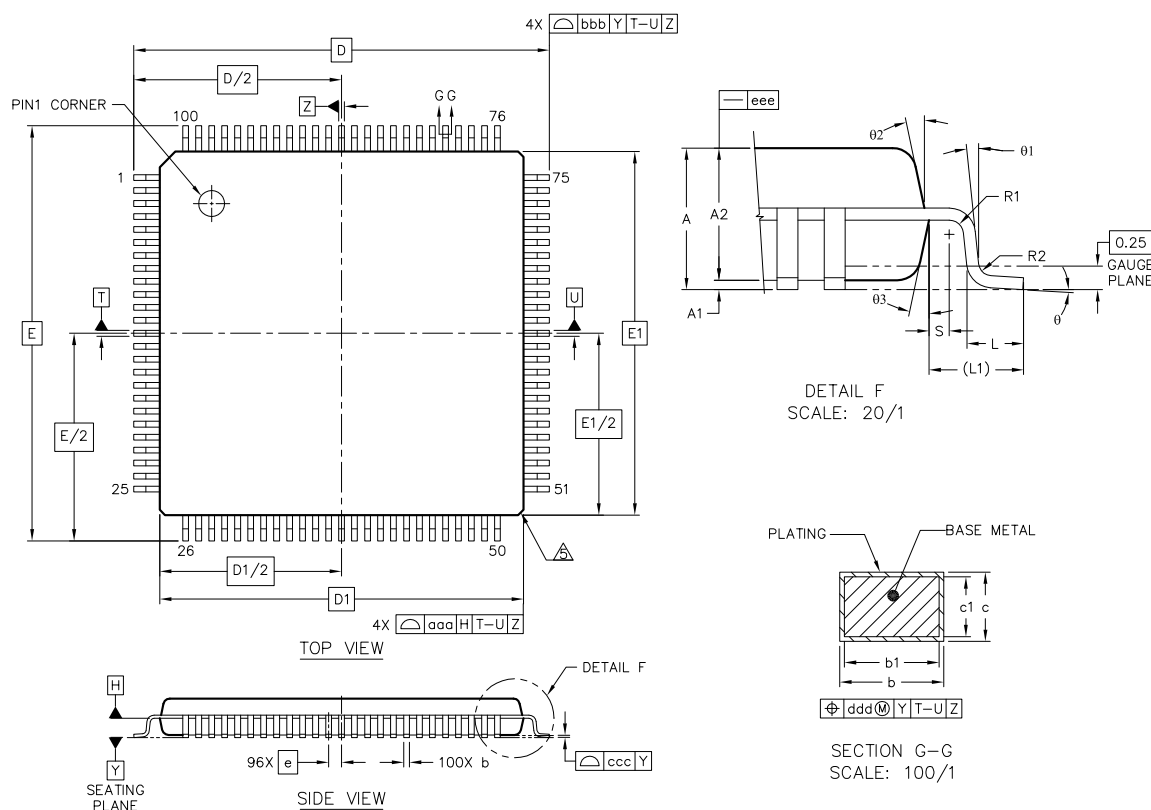
Symbol	Parameter	Condition	Min	Typ	Max	Unit
I _{TIMER}	TIMER current	TIMER_0 idle current, clock enabled		6.9		μA/ MHz
I _{LETIMER}	LETIMER current	LETIMER idle current, clock enabled		119		nA
I _{PCNT}	PCNT current	PCNT idle current, clock enabled		54		nA
I _{RTC}	RTC current	RTC idle current, clock enabled		54		nA
I _{AES}	AES current	AES idle current, clock enabled		3.2		μA/ MHz
I _{GPIO}	GPIO current	GPIO idle current, clock enabled		3.7		μA/ MHz
I _{EBI}	EBI current	EBI idle current, clock enabled		11.8		μA/ MHz
I _{PRS}	PRS current	PRS idle current		3.5		μA/ MHz
I _{DMA}	DMA current	Clock enable		11.0		μA/ MHz

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
EBI_ALE		PC11	PC11					External Bus Interface (EBI) Address Latch Enable output.
EBI_ARDY	PF2	PF2	PF2					External Bus Interface (EBI) Hardware Ready Control input.
EBI_BL0	PF6	PF6	PF6					External Bus Interface (EBI) Byte Lane/Enable pin 0.
EBI_BL1	PF7	PF7	PF7					External Bus Interface (EBI) Byte Lane/Enable pin 1.
EBI_CS0	PD9	PD9	PD9					External Bus Interface (EBI) Chip Select output 0.
EBI_CS1	PD10	PD10	PD10					External Bus Interface (EBI) Chip Select output 1.
EBI_CS2	PD11	PD11	PD11					External Bus Interface (EBI) Chip Select output 2.
EBI_CS3	PD12	PD12	PD12					External Bus Interface (EBI) Chip Select output 3.
EBI_CSTFT	PA7	PA7	PA7					External Bus Interface (EBI) Chip Select output TFT.
EBI_DCLK	PA8	PA8	PA8					External Bus Interface (EBI) TFT Dot Clock pin.
EBI_DTEN	PA9	PA9	PA9					External Bus Interface (EBI) TFT Data Enable pin.
EBI_HSNC	PA11	PA11	PA11					External Bus Interface (EBI) TFT Horizontal Synchronization pin.
EBI_NANDREn	PC3	PC3	PC3					External Bus Interface (EBI) NAND Read Enable output.
EBI_NANDWEEn	PC5	PC5	PC5					External Bus Interface (EBI) NAND Write Enable output.
EBI_REn	PF5	PF9	PF5					External Bus Interface (EBI) Read Enable output.
EBI_VSNC	PA10	PA10	PA10					External Bus Interface (EBI) TFT Vertical Synchronization pin.
EBI_WEn		PF8						External Bus Interface (EBI) Write Enable output.
ETM_TCLK	PD7	PF8	PC6	PA6				Embedded Trace Module ETM clock .
ETM_TD0	PD6	PF9	PC7	PA2				Embedded Trace Module ETM data 0.
ETM_TD1	PD3		PD3	PA3				Embedded Trace Module ETM data 1.
ETM_TD2	PD4		PD4	PA4				Embedded Trace Module ETM data 2.
ETM_TD3	PD5		PD5	PA5				Embedded Trace Module ETM data 3.
GPIO_EM4WU0	PA0							Pin can be used to wake the system up from EM4
GPIO_EM4WU1	PA6							Pin can be used to wake the system up from EM4
GPIO_EM4WU2	PC9							Pin can be used to wake the system up from EM4
GPIO_EM4WU3	PF1							Pin can be used to wake the system up from EM4
GPIO_EM4WU4	PF2							Pin can be used to wake the system up from EM4
GPIO_EM4WU5	PE13							Pin can be used to wake the system up from EM4
HFX TAL_N	PB14							High Frequency Crystal negative pin. Also used as external optional clock input pin.
HFX TAL_P	PB13							High Frequency Crystal positive pin.
I2C0_SCL	PA1	PD7	PC7		PC1	PF1	PE13	I2C0 Serial Clock Line input / output.
I2C0_SDA	PA0	PD6	PC6		PC0	PF0	PE12	I2C0 Serial Data input / output.
I2C1_SCL	PC5	PB12	PE1					I2C1 Serial Clock Line input / output.
I2C1_SDA	PC4	PB11	PE0					I2C1 Serial Data input / output.
LES_ALTEX0	PD6							LESENSE alternate exit output 0.
LES_ALTEX1	PD7							LESENSE alternate exit output 1.
LES_ALTEX2	PA3							LESENSE alternate exit output 2.
LES_ALTEX3	PA4							LESENSE alternate exit output 3.
LES_ALTEX4	PA5							LESENSE alternate exit output 4.

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
TIM1_CC1		PE11	PB1	PB8	PD7			Timer 1 Capture Compare input / output channel 1.
TIM1_CC2		PE12	PB2	PB11				Timer 1 Capture Compare input / output channel 2.
TIM2_CC0	PA8	PA12	PC8					Timer 2 Capture Compare input / output channel 0.
TIM2_CC1	PA9	PA13	PC9					Timer 2 Capture Compare input / output channel 1.
TIM2_CC2	PA10	PA14	PC10					Timer 2 Capture Compare input / output channel 2.
TIM3_CC0	PE14	PE0						Timer 3 Capture Compare input / output channel 0.
TIM3_CC1	PE15	PE1						Timer 3 Capture Compare input / output channel 1.
TIM3_CC2	PA15	PE2						Timer 3 Capture Compare input / output channel 2.
U0_RX	PF7	PE1	PA4					UART0 Receive input.
U0_TX	PF6	PE0	PA3					UART0 Transmit output. Also used as receive input in half duplex communication.
U1_RX		PF11	PB10	PE3				UART1 Receive input.
U1_TX		PF10	PB9	PE2				UART1 Transmit output. Also used as receive input in half duplex communication.
US0_CLK	PE12	PE5	PC9		PB13	PB13		USART0 clock input / output.
US0_CS	PE13	PE4	PC8		PB14	PB14		USART0 chip select input / output.
US0_RX	PE11	PE6	PC10	PE12	PB8	PC1		USART0 Asynchronous Receive. USART0 Synchronous mode Master Input / Slave Output (MISO).
US0_TX	PE10	PE7	PC11	PE13	PB7	PC0		USART0 Asynchronous Transmit. Also used as receive input in half duplex communication. USART0 Synchronous mode Master Output / Slave Input (MOSI).
US1_CLK	PB7	PD2	PF0					USART1 clock input / output.
US1_CS	PB8	PD3	PF1					USART1 chip select input / output.
US1_RX	PC1	PD1	PD6					USART1 Asynchronous Receive. USART1 Synchronous mode Master Input / Slave Output (MISO).
US1_TX	PC0	PD0	PD7					USART1 Asynchronous Transmit. Also used as receive input in half duplex communication. USART1 Synchronous mode Master Output / Slave Input (MOSI).
US2_CLK	PC4	PB5						USART2 clock input / output.
US2_CS	PC5	PB6						USART2 chip select input / output.
US2_RX	PC3	PB4						USART2 Asynchronous Receive. USART2 Synchronous mode Master Input / Slave Output (MISO).
US2_TX	PC2	PB3						USART2 Asynchronous Transmit. Also used as receive input in half duplex communication. USART2 Synchronous mode Master Output / Slave Input (MOSI).
USB_DM	PF10							USB D- pin.
USB_DMPU	PD2							USB D- Pullup control.
USB_DP	PF11							USB D+ pin.
USB_ID	PF12							USB ID pin. Used in OTG mode.
USB_VBUS	USB_VBUS							USB 5 V VBUS input.
USB_VBUSEN	PF5							USB 5 V VBUS enable.

4.5 LQFP100 Package

Figure 4.3. LQFP100



Note:

1. Datum 'T', 'U' and 'Z' to be determined at datum plane 'H'.
2. Datum 'D' and 'E' to be determined at seating plane datum 'Y'.
3. Dimension 'D1' and 'E1' do not include mold protrusions. Allowable protrusion is 0.25 per side. Dimensions 'D1' and 'E1' do include mold mismatch and are determined at datum plane datum 'H'.
4. Dimension 'b' does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum 'b' dimension by more than 0.08 mm. Dambar can not be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm
5. Exact shape of each corner is optional.

5 PCB Layout and Soldering

5.1 Recommended PCB Layout

Figure 5.1. LQFP100 PCB Land Pattern

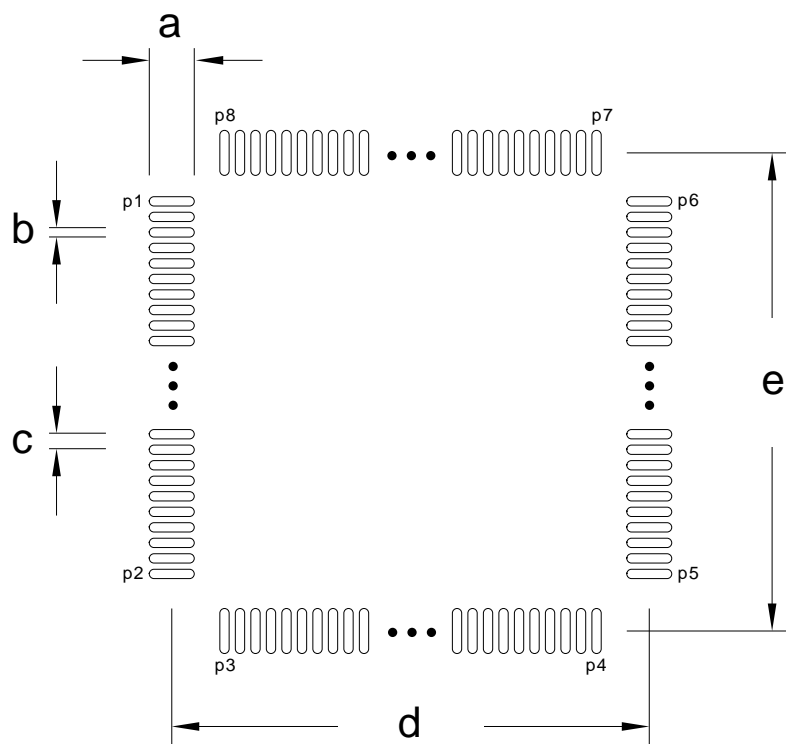


Table 5.1. QFP100 PCB Land Pattern Dimensions (Dimensions in mm)

Symbol	Dim. (mm)	Symbol	Pin number	Symbol	Pin number
a	1.45	P1	1	P6	75
b	0.30	P2	25	P7	76
c	0.50	P3	26	P8	100
d	15.40	P4	50	-	-
e	15.40	P5	51	-	-

Figure 5.2. LQFP100 PCB Solder Mask

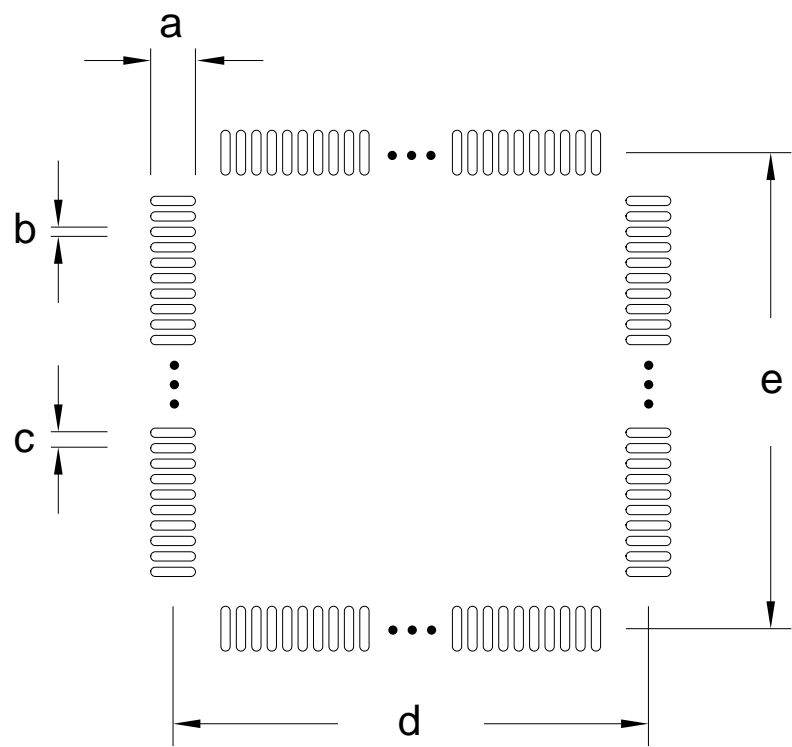
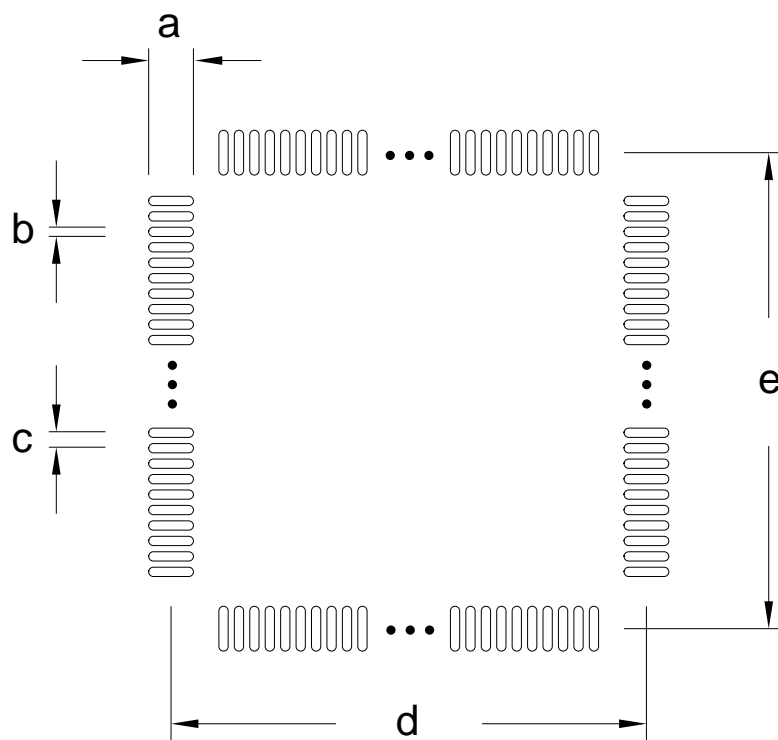


Table 5.2. QFP100 PCB Solder Mask Dimensions (Dimensions in mm)

Symbol	Dim. (mm)
a	1.57
b	0.42
c	0.50
d	15.40
e	15.40

Figure 5.3. LQFP100 PCB Stencil Design**Table 5.3. QFP100 PCB Stencil Design Dimensions (Dimensions in mm)**

Symbol	Dim. (mm)
a	1.35
b	0.20
c	0.50
d	15.40
e	15.40

1. The drawings are not to scale.
2. All dimensions are in millimeters.
3. All drawings are subject to change without notice.
4. The PCB Land Pattern drawing is in compliance with IPC-7351B.
5. Stencil thickness 0.125 mm.
6. For detailed pin-positioning, see Figure 4.3 (p. 64) .

5.2 Soldering Information

The latest IPC/JEDEC J-STD-020 recommendations for Pb-Free reflow soldering should be followed.

B Contact Information

Silicon Laboratories Inc.

400 West Cesar Chavez

Austin, TX 78701

Please visit the Silicon Labs Technical Support web page:

<http://www.silabs.com/support/pages/contacttechnicalsupport.aspx>

and register to submit a technical support request.

List of Equations

3.1. Total ACMP Active Current 43

3.2. VCMP Trigger Level as a Function of Level Setting 45