



Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

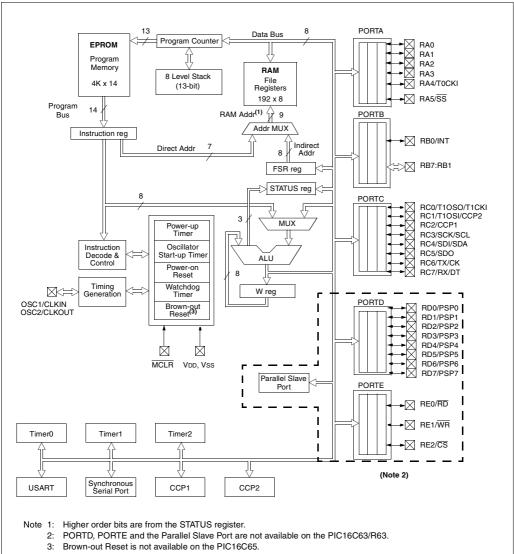
Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	I ² C, SPI
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	22
Program Memory Size	3.5KB (2K x 14)
Program Memory Type	ОТР
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 6V
Data Converters	-
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16c62a-04-so

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong





Pin Name	DIP Pin#	PLCC Pin#	TQFP MQFP Pin#	Pin Type	Buffer Type	Description
						PORTD can be a bi-directional I/O port or parallel slave port for interfacing to a microprocessor bus.
RD0/PSP0	19	21	38	I/O	ST/TTL ⁽⁶⁾	
RD1/PSP1	20	22	39	I/O	ST/TTL ⁽⁶⁾	
RD2/PSP2	21	23	40	I/O	ST/TTL ⁽⁶⁾	
RD3/PSP3	22	24	41	I/O	ST/TTL ⁽⁶⁾	
RD4/PSP4	27	30	2	I/O	ST/TTL ⁽⁶⁾	
RD5/PSP5	28	31	3	I/O	ST/TTL ⁽⁶⁾	
RD6/PSP6	29	32	4	I/O	ST/TTL ⁽⁶⁾	
RD7/PSP7	30	33	5	I/O	ST/TTL ⁽⁶⁾	
						PORTE is a bi-directional I/O port.
RE0/RD	8	9	25	I/O	ST/TTL ⁽⁶⁾	RE0 can also be read control for the parallel slave port.
RE1/WR	9	10	26	I/O	ST/TTL ⁽⁶⁾	RE1 can also be write control for the parallel slave port.
RE2/CS	10	11	27	I/O	ST/TTL ⁽⁶⁾	RE2 can also be select control for the parallel slave port.
Vss	12,31	13,34	6,29	Р		Ground reference for logic and I/O pins.
Vdd	11,32	12,35	7,28	Р		Positive supply for logic and I/O pins.
NC	-	1,17,	12,13,	—	_	These pins are not internally connected. These pins should
		28,40	33,34			be left unconnected.
Legend: I = input	O = outp) = input/		P = power
	— = Not	used	T	TL = TTL	input	ST = Schmitt Trigger input

TABLE 3-3: PIC16C64/64A/R64/65/65A/R65/67 PINOUT DESCRIPTION (Cont.'d)

Note 1: Pin functions T1OSO and T1OSI are reversed on the PIC16C64.

2: CCP2 and the USART are not available on the PIC16C64/64A/R64.

3: This buffer is a Schmitt Trigger input when configured in RC oscillator mode and a CMOS input otherwise.

4: This buffer is a Schmitt Trigger input when configured as the external interrupt.

5: This buffer is a Schmitt Trigger input when used in serial programming mode.

6: This buffer is a Schmitt Trigger input when configured as general purpose I/O and a TTL input when used in the Parallel Slave Port mode (for interfacing to a microprocessor bus).

Example 4-1 shows the calling of a subroutine in page 1 of the program memory. This example assumes that the PCLATH is saved and restored by the interrupt service routine (if interrupts are used).

EXAMPLE 4-1: CALL OF A SUBROUTINE IN PAGE 1 FROM PAGE 0

ORG 0x	500	
BSF	PCLATH, 3	;Select page 1 (800h-FFFh)
BCF	PCLATH,4	;Only on >4K devices
CALL	SUB1_P1	;Call subroutine in
	:	;page 1 (800h-FFFh)
	:	
	:	
ORG 0x	900	
SUB1_P	1:	;called subroutine
	:	;page 1 (800h-FFFh)
	:	
RETURN		;return to Call subroutine ;in page 0 (000h-7FFh)

4.5 Indirect Addressing, INDF and FSR Registers

Applicable	Devices	

The INDF register is not a physical register. Addressing the INDF register will cause indirect addressing.

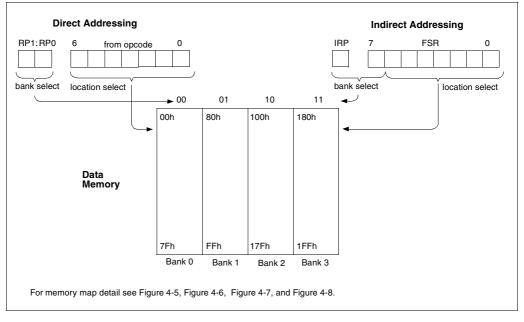
Indirect addressing is possible by using the INDF register. Any instruction using the INDF register actually accesses the register pointed to by the File Select Register, FSR. Reading the INDF register itself indirectly (FSR = '0') will produce 00h. Writing to the INDF register indirectly results in a no-operation (although status bits may be affected). An effective 9-bit address is obtained by concatenating the 8-bit FSR register and the IRP bit (STATUS<7>), as shown in Figure 4-25.

A simple program to clear RAM location 20h-2Fh using indirect addressing is shown in Example 4-2.

EXAMPLE 4-2: INDIRECT ADDRESSING

NEXT	movlw movwf clrf incf btfss	0x20 FSR INDF FSR,F FSR,4	<pre>;initialize pointer ; to RAM ;clear INDF register ;inc pointer ;all done?</pre>
CONTINUE	goto	NEXT	;NO, clear next
	:		;YES, continue

FIGURE 4-25: DIRECT/INDIRECT ADDRESSING



8.0 TIMER1 MODULE

Applicable Devices

61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

Timer1 is a 16-bit timer/counter consisting of two 8-bit registers (TMR1H and TMR1L) which are readable and writable. Register TMR1 (TMR1H:TMR1L) increments from 0000h to FFFFh and rolls over to 0000h. The TMR1 Interrupt, if enabled, is generated on overflow which is latched in interrupt flag bit TMR1IF (PIR1<0>). This interrupt can be enabled/disabled by setting/clearing the TMR1 interrupt enable bit TMR1IE (PIE1<0>).

Timer1 can operate in one of two modes:

- · As a timer
- · As a counter

The operating mode is determined by clock select bit, TMR1CS (T1CON<1>) (Figure 8-2).

In timer mode, Timer1 increments every instruction cycle. In counter mode, it increments on every rising edge of the external clock input.

Timer1 can be enabled/disabled by setting/clearing control bit TMR1ON (T1CON<0>).

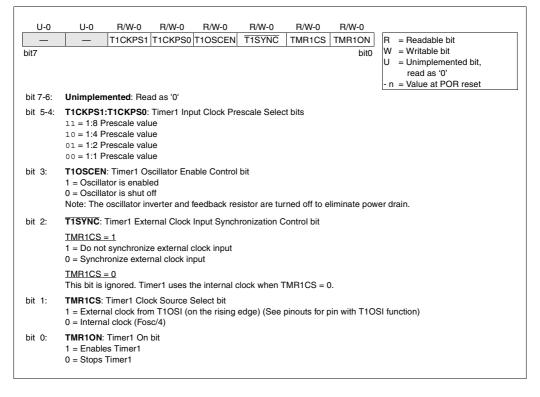
Timer1 also has an internal "reset input". This reset can be generated by CCP1 or CCP2 (Capture/Compare/ PWM) module. See Section 10.0 for details. Figure 8-1 shows the Timer1 control register.

For the PIC16C62A/R62/63/R63/64A/R64/65A/R65/ R66/67, when the Timer1 oscillator is enabled (T1OSCEN is set), the RC1 and RC0 pins become inputs. That is, the TRISC<1:0> value is ignored.

For the PIC16C62/64/65, when the Timer1 oscillator is enabled (T1OSCEN is set), RC1 pin becomes an input, however the RC0 pin will have to be configured as an input by setting the TRISC<0> bit.

The Timer1 module also has a software programmable prescaler.

FIGURE 8-1: T1CON: TIMER1 CONTROL REGISTER (ADDRESS 10h)



10.0 CAPTURE/COMPARE/PWM (CCP) MODULE(s)

Applicable Devices

61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67	CCP1
61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67	CCP2

Each CCP (Capture/Compare/PWM) module contains a 16-bit register which can operate as a 16-bit capture register, as a 16-bit compare register, or as a PWM master/slave duty cycle register. Both the CCP1 and CCP2 modules are identical in operation, with the exception of the operation of the special event trigger. Table 10-1 and Table 10-2 show the resources and interactions of the CCP modules(s). In the following sections, the operation of a CCP module is described with respect to CCP1. CCP2 operates the same as CCP1, except where noted.

CCP1 module:

Capture/Compare/PWM Register1 (CCPR1) is comprised of two 8-bit registers: CCPR1L (low byte) and CCPR1H (high byte). The CCP1CON register controls the operation of CCP1. All are readable and writable.

CCP2 module:

Capture/Compare/PWM Register2 (CCPR2) is comprised of two 8-bit registers: CCPR2L (low byte) and CCPR2H (high byte). The CCP2CON register controls the operation of CCP2. All are readable and writable.

For use of the CCP modules, refer to the *Embedded Control Handbook*, "Using the CCP Modules" (AN594).

TABLE 10-1: CCP MODE - TIMER RESOURCE

CCP Mode	Timer Resource
Capture	Timer1
Compare	Timer1
PWM	Timer2

TABLE 10-2: INTERACTION OF TWO CCP MODULES

CCPx Mode	CCPy Mode	Interaction
Capture	Capture	Same TMR1 time-base.
Capture	Compare	The compare should be configured for the special event trigger, which clears TMR1.
Compare	Compare	The compare(s) should be configured for the special event trigger, which clears TMR1.
PWM	PWM	The PWMs will have the same frequency, and update rate (TMR2 interrupt).
PWM	Capture	None
PWM	Compare	None

11.0 SYNCHRONOUS SERIAL PORT (SSP) MODULE

11.1 SSP Module Overview

The Synchronous Serial Port (SSP) module is a serial interface useful for communicating with other peripheral or microcontroller devices. These peripheral devices may be Serial EEPROMs, shift registers, display drivers, A/D converters, etc. The SSP module can operate in one of two modes:

- Serial Peripheral Interface (SPI)
- Inter-Integrated Circuit (I²C)

The SSP module in l^2 C mode works the same in all PIC16C6X devices that have an SSP module. However the SSP Module in SPI mode has differences between the PIC16C66/67 and the other PIC16C6X devices.

The register definitions and operational description of SPI mode has been split into two sections because of the differences between the PIC16C66/67 and the other PIC16C6X devices. The default reset values of both the SPI modules is the same regardless of the device:

11.2 SPI Mode for PIC16C62/62A/R62/63/R63/64/	
64A/R64/65/65A/R6584	
11.3 SPI Mode for PIC16C66/67 89	
11.4 I ² C [™] Overview95	
11.5 SSP I ² C Operation	

Refer to Application Note AN578, "Use of the SSP Module in the I^2C Multi-Master Environment."

13.2.3 EXTERNAL CRYSTAL OSCILLATOR CIRCUIT

Either a prepackaged oscillator can be used or a simple oscillator circuit with TTL gates can be built. Prepackaged oscillators provide a wide operating range and better stability. A well-designed crystal oscillator will provide good performance with TTL gates. Two types of crystal oscillator circuits can be used; one with series resonance, or one with parallel resonance.

Figure 13-6 shows implementation of a parallel resonant oscillator circuit. The circuit is designed to use the fundamental frequency of the crystal. The 74AS04 inverter performs the 180-degree phase shift that a parallel oscillator requires. The 4.7 k Ω resistor provides the negative feedback for stability. The 10 k Ω potentiometer biases the 74AS04 in the linear region. This could be used for external oscillator designs.

FIGURE 13-6: EXTERNAL PARALLEL RESONANT CRYSTAL OSCILLATOR CIRCUIT

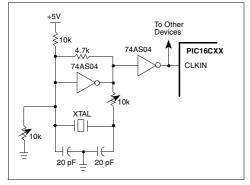
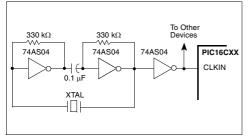


Figure 13-7 shows a series resonant oscillator circuit. This circuit is also designed to use the fundamental frequency of the crystal. The inverter performs a 180-degree phase shift in a series resonant oscillator circuit. The 330 k Ω resistors provide the negative feedback to bias the inverters in their linear region.

FIGURE 13-7: EXTERNAL SERIES RESONANT CRYSTAL OSCILLATOR CIRCUIT



13.2.4 RC OSCILLATOR

For timing insensitive applications the RC device option offers additional cost savings. The RC oscillator frequency is a function of the supply voltage, the resistor (Rext) and capacitor (Cext) values, and the operating temperature. In addition to this, the oscillator frequency will vary from unit to unit due to normal process parameter variation. Furthermore, the difference in lead frame capacitance between package types will also affect the oscillation frequency, especially for low Cext values. The user also needs to take into account variation due to tolerance of external R and C components used. Figure 13-8 shows how the RC combination is connected to the PIC16CXX. For Rext values below 2.2 k Ω , the oscillator operation may become unstable or stop completely. For very high Rext values (e.g. 1 M Ω), the oscillator becomes sensitive to noise, humidity and leakage. Thus, we recommend keeping Rext between 3 k Ω and 100 k Ω .

Although the oscillator will operate with no external capacitor (Cext = 0 pF), we recommend using values above 20 pF for noise and stability reasons. With no or small external capacitance, the oscillation frequency can vary dramatically due to changes in external capacitances, such as PCB trace capacitance or package lead frame capacitance.

See characterization data for desired device for RC frequency variation from part to part due to normal process variation. The variation is larger for larger R (since leakage current variation will affect RC frequency more for large R) and for smaller C (since variation of input capacitance will affect RC frequency more).

See characterization data for desired device for variation of oscillator frequency due to VDD for given Rext/ Cext values as well as frequency variation due to operating temperature for given R, C, and VDD values.

The oscillator frequency, divided by 4, is available on the OSC2/CLKOUT pin, and can be used for test purposes or to synchronize other logic (see Figure 3-5 for waveform).

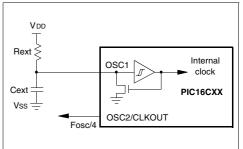


FIGURE 13-8: RC OSCILLATOR MODE

COMF	Complement f	DECFSZ	Decrement f, Skip if 0
Syntax:	[<i>label</i>] COMF f,d	Syntax:	[label] DECFSZ f,d
Operands:	$\begin{array}{l} 0\leq f\leq 127\\ d\in [0,1] \end{array}$	Operands:	$\begin{array}{l} 0 \leq f \leq 127 \\ d \in [0,1] \end{array}$
Operation:	$(\bar{f}) \rightarrow (destination)$	Operation:	(f) - 1 \rightarrow (destination);
Status Affected:	Z		skip if result = 0
Encoding:	00 1001 dfff ffff	Status Affected:	None
Description:	The contents of register 'f' are comple- mented. If 'd' is 0 the result is stored in	Encoding:	00 1011 dfff ffff
Words: Cycles:	W. If 'd' is 1 the result is stored back in register 'f'. 1	Description:	The contents of register 'f' are decre- mented. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'. If the result is 1, the next instruction, is executed. If the result is 0, then a NOP is
Q Cycle Activity:	Q1 Q2 Q3 Q4		executed instead making it a 2TCY instruc- tion.
, ,	Decode Read Process Write to	Words:	1
	register data destination	Cycles:	1(2)
		Q Cycle Activity:	Q1 Q2 Q3 Q4
Example	COMF REG1, 0 Before Instruction	, ,	Decode Read Process Write to register 'f' data destination
	$\begin{array}{rcl} REG1 &=& 0x13\\ After Instruction & \\ REG1 &=& 0x13\\ W &=& 0xEC \end{array}$	lf Skip:	Q1 Q2 Q3 Q4 No- Operation Operation Operation Operation
DECF	Decrement f		
Syntax:	[<i>label</i>] DECF f,d	Example	HERE DECFSZ CNT, 1 GOTO LOOP
Operands:	$0 \le f \le 127$		CONTINUE •
	d ∈ [0,1]		•
Operation:	$d \in [0,1]$ (f) - 1 \rightarrow (destination)		• Before Instruction
Operation: Status Affected:			• Before Instruction PC = address HERE
•	(f) - 1 \rightarrow (destination)		PC = address HERE After Instruction
Status Affected:	(f) - 1 → (destination) Z 00 0011 dfff ffff Decrement register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is		PC = address HERE After Instruction CNT = CNT - 1 if CNT = 0, PC = address CONTINUE
Status Affected: Encoding:	(f) - 1 → (destination) Z 00 0011 dfff ffff		$\begin{array}{rcl} PC &=& address {}_{HERE}\\ \textbf{After Instruction}\\ & CNT &=& CNT-1\\ & & & & \\ & & & & \\ & & & & \\ & & & &$
Status Affected: Encoding: Description: Words:	(f) - 1 \rightarrow (destination) Z Decrement register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'.		PC = address HERE After Instruction CNT = CNT - 1 if CNT = 0, PC = address CONTINUE
Status Affected: Encoding: Description: Words: Cycles:	(f) - 1 \rightarrow (destination) Z Decrement register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'.		$\begin{array}{rcl} PC &=& address \ HERE \\ \textbf{After Instruction} \\ & \textbf{CNT} &=& \textbf{CNT} \cdot 1 \\ & \text{if } \textbf{CNT} &=& 0, \\ & \textbf{PC} &=& address \ \textbf{CONTINUE} \\ & \text{if } \textbf{CNT} \neq& 0, \end{array}$
Status Affected: Encoding: Description: Words:	(f) - 1 \rightarrow (destination) Z 00 0011 dfff ffff Decrement register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'. 1 1		$\begin{array}{rcl} PC &=& address \mbox{ HERE} \\ \mbox{After Instruction} \\ CNT &=& CNT - 1 \\ \mbox{if CNT} &=& 0, \\ PC &=& address \mbox{ continue} \\ \mbox{if CNT} &\neq& 0, \\ \end{array}$
Status Affected: Encoding: Description: Words: Cycles:	(f) - 1 \rightarrow (destination) Z 00 0011 dfff ffff Decrement register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'. 1 1 Q1 Q2 Q3 Q4 Decode Read Process Write to data destination		$\begin{array}{rcl} PC &=& address \ HERE \\ \textbf{After Instruction} \\ & \textbf{CNT} &=& \textbf{CNT} \cdot 1 \\ & \text{if } \textbf{CNT} &=& 0, \\ & \textbf{PC} &=& address \ \textbf{CONTINUE} \\ & \text{if } \textbf{CNT} \neq& 0, \end{array}$
Status Affected: Encoding: Description: Words: Cycles: Q Cycle Activity:	$ \begin{array}{c c} (f) - 1 \rightarrow (destination) \\ \hline Z \\ \hline 00 & 0011 & dfff & ffff \\ \hline Decrement register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'. \\ 1 & & \\ 1 & & \\ Q1 & Q2 & Q3 & Q4 \\ \hline \hline Decode & Read & Process & Write to destination \\ \hline & & \\ f'' & & \\ \end{array} $		$\begin{array}{rcl} PC &=& address {}_{HERE}\\ \textbf{After Instruction}\\ & CNT &=& CNT-1\\ & & & & \\ & & & & \\ & & & & \\ & & & &$
Status Affected: Encoding: Description: Words: Cycles: Q Cycle Activity:	(f) - 1 \rightarrow (destination) Z 00 0011 dfff ffff Decrement register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'. 1 2 Q1 Q2 Q3 Q4 Decode Read Process Write to data destination DECF CNT, 1 Before Instruction CNT = 0x01		PC = address HERE After Instruction CNT = CNT - 1 if CNT = 0, PC = address CONTINUE if CNT ≠ 0,
Status Affected: Encoding: Description: Words: Cycles: Q Cycle Activity:	(f) - 1 → (destination) Z 00 0011 dfff fff Decrement register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'. 1 1 Q1 Q2 Q3 Q4 Decode Read Process Write to register data destination DECF CNT, 1 Before Instruction CNT = 0x01 Z = 0		$\begin{array}{rcl} PC &=& address \ HERE \\ \textbf{After Instruction} \\ & \textbf{CNT} &=& \textbf{CNT} \cdot 1 \\ & \text{if } \textbf{CNT} &=& 0, \\ & \textbf{PC} &=& address \ \textbf{CONTINUE} \\ & \text{if } \textbf{CNT} \neq& 0, \end{array}$
Status Affected: Encoding: Description: Words: Cycles: Q Cycle Activity:	(f) - 1 \rightarrow (destination) Z 00 0011 dfff ffff Decrement register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'. 1 2 Q1 Q2 Q3 Q4 Decode Read Process Write to data destination DECF CNT, 1 Before Instruction CNT = 0x01		$\begin{array}{rcl} PC &=& address \mbox{ HERE} \\ \mbox{After Instruction} \\ CNT &=& CNT - 1 \\ \mbox{if CNT} &=& 0, \\ PC &=& address \mbox{ continue} \\ \mbox{if CNT} &\neq& 0, \\ \end{array}$

Applicable Devices	61	60	601	Deo	62	Dec	61	611	DGA	65	65A	Dee	66	67
Applicable Devices	01	02	02A	n02	03	n03	04	04A	n04	05	05A	H00	00	07

		Standard Operating Conditions (unless otherwise stated)						
		Operating temperature -				S ≤ TA	$\Delta \leq +125^{\circ}C$ for extended,	
	RACTERISTICS				-40°C	≤ T/	$\Lambda \leq +85^{\circ}$ C for industrial and	
	ARACIERISTICS				0°C	≤ T⁄	$A \le +70^{\circ}C$ for commercial	
		Operatir	ng voltage	VDD r	ange as c	describe	ed in DC spec Section 15.1 and	
		Section	15.2.					
Param	Characteristic	Sym	Min	Typ†	Max	Units	Conditions	
No.								
	Output High Voltage							
D090	I/O ports (Note 3)	Voh	VDD-0.7	-	-	v	IOH = -3.0 mA,	
						-	$VDD = 4.5V, -40^{\circ}C \text{ to } +85^{\circ}C$	
D090A			VDD-0.7	-	-	v	IOH = -2.5 mA,	
							VDD = 4.5V, -40°C to +125°C	
D092	OSC2/CLKOUT (RC osc config)		VDD-0.7	-	-	V	IOH = -1.3 mA,	
							VDD = 4.5V, -40°C to +85°C	
D092A			VDD-0.7	-	-	V	IOH = -1.0 mA,	
							VDD = 4.5V, -40°C to +125°C	
D150*	Open-Drain High Voltage	Vod	-	-	14	V	RA4 pin	
	Capacitive Loading Specs on							
	Output Pins							
D100	OSC2 pin	Cosc2			15	pF	In XT, HS and LP modes when	
							external clock is used to drive	
							OSC1.	
D101	All I/O pins and OSC2 (in RC mode)	Cio			50	pF		

The parameters are characterized but not tested.

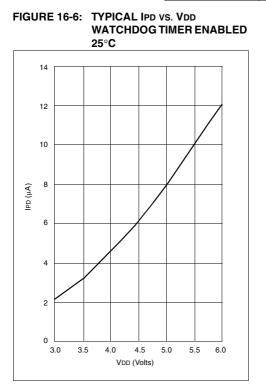
*

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

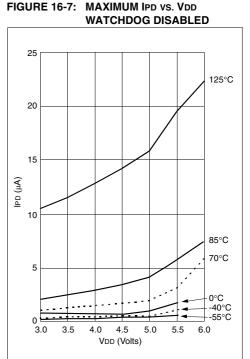
Note 1: In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C6X be driven with external clock in RC mode.

 The leakage current on the MCLR/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as current sourced by the pin.



Applicable Devices 61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67



Data based on matrix samples. See first page of this section for details.

Applicable Devices 61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

FIGURE 16-12: TYPICAL IDD VS. FREQUENCY (EXTERNAL CLOCK, 25°C)

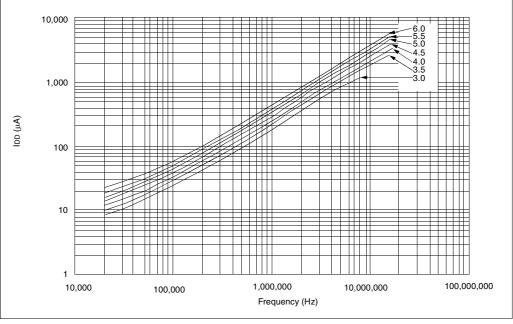
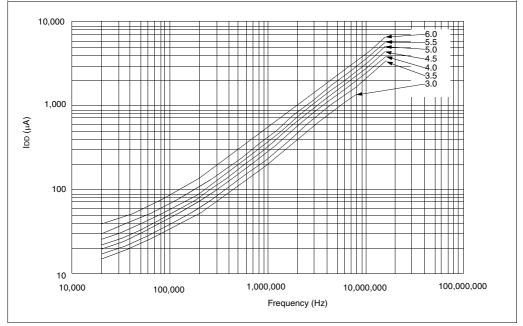


FIGURE 16-13: MAXIMUM IDD vs. FREQUENCY (EXTERNAL CLOCK, -40° TO +85°C)



Applicable Devices 61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

FIGURE 17-9: I²C BUS START/STOP BITS TIMING

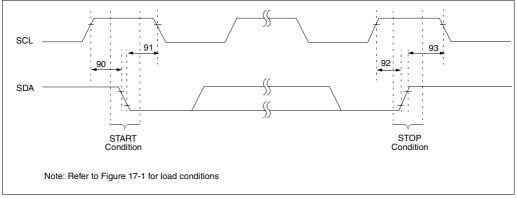


TABLE 17-9: I²C BUS START/STOP BITS REQUIREMENTS

Parameter No.	Sym	Characteristic		Min	Тур	Max	Units	Conditions	
90	TSU:STA	START condition	100 kHz mode	4700	—	—	-	Only relevant for repeated START	
		Setup time	400 kHz mode	600	_	—	ns	condition	
91	THD:STA	START condition	100 kHz mode	4000	_	_		After this period the first clock	
		Hold time	400 kHz mode	600	_	—	ns	pulse is generated	
92	TSU:STO	STOP condition	100 kHz mode	4700	_	_			
		Setup time	400 kHz mode	600		_	ns		
93	THD:STO	STOP condition	100 kHz mode	4000	_	_			
		Hold time	400 kHz mode	600	—	—	ns		

Applicable Devices 61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67



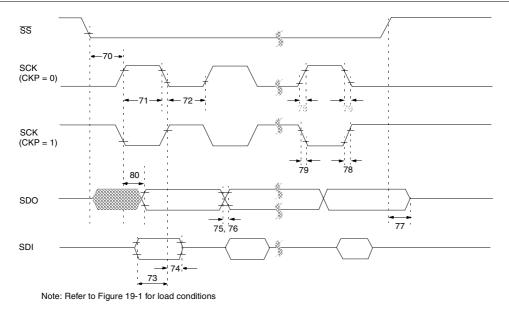


TABLE 19-8: SPI MODE REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Тур†	Max	Units	Conditions
70	TssL2scH, TssL2scL	\overline{SS} ↓ to SCK↓ or SCK↑ input	Тсү	—	—	ns	
71	TscH	SCK input high time (slave mode)	Tcy + 20	_	_	ns	
72	TscL	SCK input low time (slave mode)	Tcy + 20	_	_	ns	
73	TdiV2scH, TdiV2scL	Setup time of SDI data input to SCK edge	50	—	—	ns	
74	TscH2diL, TscL2diL	Hold time of SDI data input to SCK edge	50	_	—	ns	
75	TdoR	SDO data output rise time		10	25	ns	
76	TdoF	SDO data output fall time		10	25	ns	
77	TssH2doZ	SS↑ to SDO output hi-impedance	10	_	50	ns	
78	TscR	SCK output rise time (master mode)		10	25	ns	
79	TscF	SCK output fall time (master mode)	_	10	25	ns	
80	TscH2doV, TscL2doV	SDO data output valid after SCK edge	_	_	50	ns	

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Applicable Devices 61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

FIGURE 21-3: CLKOUT AND I/O TIMING

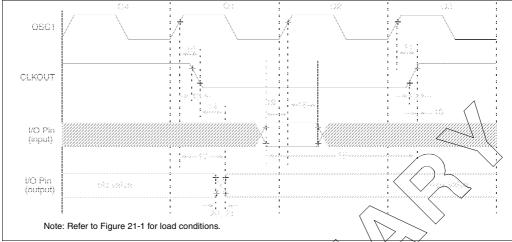


TABLE 21-3: CLKOUT AND I/O TIMING F	REQUIREMENTS
-------------------------------------	--------------

		1		$\sim \rightarrow$	/ /			
Param	Sym	Characteristic	<	Min	Typt	∨ Max	Units	Conditions
No.					\checkmark			
10*	TosH2ckL	OSC1↑ to CLKOUT↓) /	75	200	ns	Note 1
11*	TosH2ckH	OSC1↑ to CLKOUT↑		$\backslash - \checkmark$	75	200	ns	Note 1
12*	TckR	CLKOUT rise time	$\sim 1 M /$	\searrow	35	100	ns	Note 1
13*	TckF	CLKOUT fall time	\sum	> -	35	100	ns	Note 1
14*	TckL2ioV	CLKOUT \downarrow to Port out valid \land	/ /	—	—	0.5TCY + 20	ns	Note 1
15*	TioV2ckH	Port in valid before CLKOUT	$///\sim$	Tosc + 200	—		ns	Note 1
16*	TckH2iol	Port in hold after CLKOUT ↑	$\overline{\langle \langle \rangle}$	0	—		ns	Note 1
17*	TosH2ioV	OSC1 [↑] (Q1 cycle) to Port out val	id 🔪	_	50	150	ns	
18*	TosH2ioI	OSC1↑ (Q2 cycle) to Port input	PIC16CR63/R65	100	—		ns	
		invalid (I/O in hold time)	PIC16LCR63/R65	200	—		ns	
19*	TioV2osH	Port input valid to OSC11 (I/Q in	setup time)	0	—		ns	
20*	TioR	Port output rise time	PIC16CR63/R65	_	10	40	ns	
		\frown	PIC16LCR63/R65	—	—	80	ns	
21*	TioF	Port output fall time	PIC16CR63/R65	_	10	40	ns	
	\langle	$\langle \checkmark \land \rangle$	PIC16LCR63/R65	_	—	80	ns	
22††*	Tinp	INT pin high or low time	•	Тсү	—	-	ns	
23††*	Trbp	RB7:RB4 change INT high or low	time	Тсү	—	_	ns	
* 1	hose narang	eters are characterized but not test	her					

These parameters are characterized but not tested.

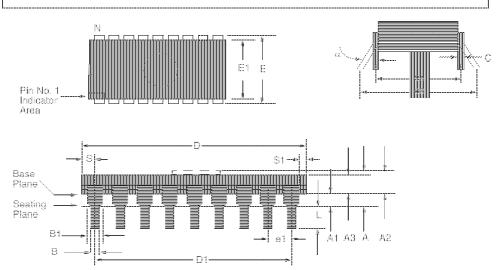
† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

t† These parameters are asynchronous events not related to any internal clock edge.

Note 1: Measurements are taken in RC Mode where CLKOUT output is 4 x Tosc.

24.6 18-Lead Ceramic CERDIP Dual In-line with Window (300 mil) (JW)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Package Group: Ceramic CERDIP Dual In-Line (CDP)							
	Millimeters						
Symbol	Min	Max	Notes	Min	Max	Notes	
α	0°	10°		0°	10°		
А	_	5.080		_	0.200		
A1	0.381	1.778		0.015	0.070		
A2	3.810	4.699		0.150	0.185		
A3	3.810	4.445		0.150	0.175		
В	0.355	0.585		0.014	0.023		
B1	1.270	1.651	Typical	0.050	0.065	Typical	
С	0.203	0.381	Typical	0.008	0.015	Typical	
D	22.352	23.622		0.880	0.930		
D1	20.320	20.320	Reference	0.800	0.800	Reference	
E	7.620	8.382		0.300	0.330		
E1	5.588	7.874		0.220	0.310		
e1	2.540	2.540	Reference	0.100	0.100	Reference	
eA	7.366	8.128	Typical	0.290	0.320	Typical	
eB	7.620	10.160		0.300	0.400		
L	3.175	3.810		0.125	0.150		
Ν	18	18		18	18		
S	0.508	1.397		0.020	0.055		
S1	0.381	1.270		0.015	0.050		

F.7 PIC16C7XX Family of Devces

		PIC16C710	PIC16C71	PIC16C711	PIC16C715	PIC16C72	PIC16CR72 ⁽¹⁾
Clock	Maximum Frequency of Operation (MHz)	20	20	20	20	20	20
	EPROM Program Memory (x14 words)	512	1K	1K	2К	2К	—
Memory	ROM Program Memory (14K words)	_	_	—	_	_	2К
	Data Memory (bytes)	36	36	68	128	128	128
	Timer Module(s)	TMR0	TMR0	TMR0	TMR0	TMR0, TMR1, TMR2	TMR0, TMR1, TMR2
Peripherals	Capture/Compare/ PWM Module(s)	—	_	—	—	1	1
	Serial Port(s) (SPI/I ² C, USART)	—	_	—	_	SPI/I ² C	SPI/I ² C
	Parallel Slave Port	—	—	—	—	—	—
	A/D Converter (8-bit) Channels	4	4	4	4	5	5
	Interrupt Sources	4	4	4	4	8	8
	I/O Pins	13	13	13	13	22	22
	Voltage Range (Volts)	3.0-6.0	3.0-6.0	3.0-6.0	3.0-5.5	2.5-6.0	3.0-5.5
Features	In-Circuit Serial Programming	Yes	Yes	Yes	Yes	Yes	Yes
	Brown-out Reset	Yes	—	Yes	Yes	Yes	Yes
	Packages	18-pin DIP, SOIC; 20-pin SSOP	18-pin DIP, SOIC	18-pin DIP, SOIC; 20-pin SSOP	18-pin DIP, SOIC; 20-pin SSOP	28-pin SDIP, SOIC, SSOP	28-pin SDIP, SOIC, SSOP

		PIC16C73A	PIC16C74A	PIC16C76	PIC16C77
Clock	Maximum Frequency of Oper- ation (MHz)	20	20	20	20
Memory	EPROM Program Memory (x14 words)	4K	4K	8K	8K
	Data Memory (bytes)	192	192	368	368
	Timer Module(s)	TMR0, TMR1, TMR2	TMR0, TMR1, TMR2	TMR0, TMR1, TMR2	TMR0, TMR1, TMR2
Peripherals	Capture/Compare/PWM Mod- ule(s)	2	2	2	2
	Serial Port(s) (SPI/I ² C, USART)	SPI/I ² C, USART	SPI/I ² C, USART	SPI/I ² C, USART	SPI/I ² C, USART
	Parallel Slave Port	_	Yes	—	Yes
	A/D Converter (8-bit) Channels	5	8	5	8
	Interrupt Sources	11	12	11	12
	I/O Pins	22	33	22	33
	Voltage Range (Volts)	2.5-6.0	2.5-6.0	2.5-6.0	2.5-6.0
Features	In-Circuit Serial Programming	Yes	Yes	Yes	Yes
T cuturoo	Brown-out Reset	Yes	Yes	Yes	Yes
	Packages	28-pin SDIP, SOIC	40-pin DIP; 44-pin PLCC, MQFP, TQFP	28-pin SDIP, SOIC	40-pin DIP; 44-pin PLCC, MQFP, TQFP

All PIC16/17 Family devices have Power-on Reset, selectable Watchdog Timer, selectable code protect and high I/O current capability. All PIC16C7XX Family devices use serial programming with clock pin RB6 and data pin RB7.

Note 1: Please contact your local Microchip sales office for availability of these devices.

LIST OF EQUATION AND EXAMPLES

Example 3-1:	Instruction Pipeline Flow 18
Example 4-1:	Call of a Subroutine in Page 1
	from Page 0 49
Example 4-2:	Indirect Addressing 49
Example 5-1:	Initializing PORTA51
Example 5-2:	Initializing PORTB53
Example 5-3:	Initializing PORTC55
Example 5-4:	Read-Modify-Write Instructions on an
	I/O Port 60
Example 7-1:	Changing Prescaler (Timer0→WDT)69
Example 7-2:	Changing Prescaler (WDT→Timer0)69
Example 8-1:	Reading a 16-bit
	Free-running Timer73
Example 10-1:	Changing Between
	Capture Prescalers79
Example 10-2:	PWM Period and Duty
	Cycle Calculation81
Example 11-1:	Loading the SSPBUF
	(SSPSR) Register
Example 11-2:	Loading the SSPBUF
	(SSPSR) Register (PIC16C66/67)91
Example 12-1:	Calculating Baud Rate Error 107
Example 13-1:	Saving Status and W
	Registers in RAM139
Example 13-2:	Saving Status, W, and
	PCLATH Registers in RAM
	(All other PIC16C6X devices)

LIST OF FIGURES

Figure 3-1:	PIC16C61 Block Diagram10
Figure 3-2:	PIC16C62/62A/R62/64/64A/R64
	Block Diagram11
Figure 3-3:	PIC16C63/R63/65/65A/R65
	Block Diagram12
Figure 3-4:	PIC16C66/67 Block Diagram 13
Figure 3-5:	Clock/Instruction Cycle18
Figure 4-1:	PIC16C61 Program Memory Map
	and Stack19
Figure 4-2:	PIC16C62/62A/R62/64/64A/
	R64 Program Memory Map and Stack 19
Figure 4-3:	PIC16C63/R63/65/65A/R65 Program
	Memory Map and Stack19
Figure 4-4:	PIC16C66/67 Program Memory
	Map and Stack
Figure 4-5:	PIC16C61 Register File Map20
Figure 4-6:	PIC16C62/62A/R62/64/64A/
	R64 Register File Map21
Figure 4-7:	PIC16C63/R63/65/65A/R65
	Register File Map21
Figure 4-8:	PIC16C66/67 Data Memory Map22
Figure 4-9:	STATUS Register
	(Address 03h, 83h, 103h, 183h)35
Figure 4-10:	OPTION Register
	(Address 81h, 181h)36
Figure 4-11:	INTCON Register
	(Address 0Bh, 8Bh, 10Bh 18Bh)37
Figure 4-12:	PIE1 Register for PIC16C62/62A/R62
	(Address 8Ch)
Figure 4-13:	PIE1 Register for PIC16C63/R63/66
	(Address 8Ch)39
Figure 4-14:	PIE1 Register for PIC16C64/64A/R64
	(Address 8Ch)

Figure 4-15:	PIE1 Register for PIC16C65/65A/R65/67
	(Address 8Ch) 40
Figure 4-16:	PIR1 Register for PIC16C62/62A/R62
	(Address 0Ch) 41
Figure 4-17:	PIR1 Register for PIC16C63/R63/66
Eiseren 4 10	Address 0Ch)
Figure 4-18:	PIR1 Register for PIC16C64/64A/R64
Eiguro 4 10:	(Address 0Ch)
Figure 4-19:	PIR1 Register for PIC16C65/65A/R65/67 (Address 0Ch)
Figure 4-20:	PIE2 Register (Address 8Dh)
Figure 4-21:	PIR2 Register (Address 0Dh)
Figure 4-22:	PCON Register for PIC16C62/64/65
5.	(Address 8Eh) 47
Figure 4-23:	PCON Register for PIC16C62A/R62/63/
-	R63/64A/R64/65A/R65/66/67
	(Address 8Eh) 47
Figure 4-24:	Loading of PC in Different Situations 48
Figure 4-25:	Direct/Indirect Addressing 49
Figure 5-1:	Block Diagram of the
	RA3:RA0 Pins and the RA5 Pin 51
Figure 5-2:	Block Diagram of the RA4/T0CKI Pin 51
Figure 5-3:	Block Diagram of the
	RB7:RB4 Pins for PIC16C61/62/64/65 53
Figure 5-4:	Block Diagram of the
	RB7:RB4 Pins for PIC16C62A/63/R63/
	64A/65A/R65/66/67
Figure 5-5:	Block Diagram of the
Figure F C	RB3:RB0 Pins
Figure 5-6: Figure 5-7:	PORTC Block Diagram
Figure 5-7.	PORTD Block Diagram (In I/O Port Mode)57
Figure 5-8:	PORTE Block Diagram
rigure 5 0.	(In I/O Port Mode)
Figure 5-9:	TRISE Register (Address 89h)
Figure 5-10:	Successive I/O Operation
Figure 5-11:	PORTD and PORTE as a Parallel
5	Slave Port61
Figure 5-12:	Parallel Slave Port Write Waveforms 62
Figure 5-13:	Parallel Slave Port Read Waveforms 62
Figure 7-1:	Timer0 Block Diagram 65
Figure 7-2:	Timer0 Timing: Internal Clock/No
	Prescaler 65
Figure 7-3:	Timer0 Timing: Internal
	Clock/Prescale 1:2
Figure 7-4:	TMR0 Interrupt Timing
Figure 7-5:	Timer0 Timing With External Clock
Figure 7-6:	Block Diagram of the Timer0/WDT
	Prescaler
Figure 8-1:	T1CON: Timer1 Control Register
	(Address 10h)
Figure 8-2:	Timer1 Block Diagram
Figure 9-1:	T2CON: Timer2 Control Register
Figure 9-2:	(Address 12h)
Figure 10-1:	CCP1CON Register (Address 17h) /
riguio ro r.	CCP2CON Register (Address 1Dh)
Figure 10-2:	Capture Mode Operation
	Block Diagram
Figure 10-3:	Compare Mode Operation
0	Block Diagram
Figure 10-4:	Simplified PWM Block Diagram
Figure 10-5:	PWM Output 80
Figure 11-1:	SSPSTAT: Sync Serial Port Status
	Register (Address 94h) 84

Figure 23-12:	SPI Slave Mode Timing (CKE = 1)
Figure 23-13:	I ² C Bus Start/Stop Bits Timing278
Figure 23-14: Figure 23-15:	I ² C Bus Data Timing
Figure 23-15.	USART Synchronous Transmission (Master/Slave) Timing
Figure 23-16:	USART Synchronous Receive
1 iguro 20 101	(Master/Slave) Timing
Figure 24-1:	Typical IPD vs. VDD
	(WDT Disabled, RC Mode)
Figure 24-2:	Maximum IPD vs. VDD
	(WDT Disabled, RC Mode) 281
Figure 24-3:	Typical IPD vs. VDD @ 25°C
	(WDT Enabled, RC Mode)282
Figure 24-4:	Maximum IPD vs. VDD
Figure 04 Fr	(WDT Enabled, RC Mode)
Figure 24-5:	Typical RC Oscillator Frequency vs. VDD
Figure 24-6:	Typical RC Oscillator
riguie 24 0.	Frequency vs. VDD
Figure 24-7:	Typical RC Oscillator
	Frequency vs. VDD
Figure 24-8:	Typical IPD vs. VDD Brown-out
	Detect Enabled (RC Mode)283
Figure 24-9:	Maximum IPD vs. VDD Brown-out
	Detect Enabled
	(85°C to -40°C, RC Mode)
Figure 24-10:	Typical IPD vs. Timer1 Enabled
	(32 kHz, RC0/RC1 = 33 pF/33 pF,
Figure 24-11:	RC Mode)
1 igule 24-11.	(32 kHz, RC0/RC1 = 33 pF/33 pF,
	85°C to -40°C, RC Mode)
Figure 24-12:	Typical IDD vs. Frequency
0	(RC Mode @ 22 pF, 25°C)
Figure 24-13:	Maximum IDD vs. Frequency
	(RC Mode @ 22 pF, -40°C to 85°C)
Figure 24-14:	Typical IDD vs. Frequency
	(RC Mode @ 100 pF, 25°C)
Figure 24-15:	Maximum IDD vs. Frequency
Figure 24-16:	(RC Mode @ 100 pF, -40°C to 85°C) 285 Typical IDD vs. Frequency
Figure 24-10.	(RC Mode @ 300 pF, 25°C)
Figure 24-17:	Maximum IDD vs. Frequency
guio 2 i i i i	(RC Mode @ 300 pF, -40°C to 85°C) 286
Figure 24-18:	Typical IDD vs. Capacitance @ 500 kHz
	(RC Mode)
Figure 24-19:	Transconductance(gm) of HS
	Oscillator vs. VDD287
Figure 24-20:	Transconductance(gm) of LP
	Oscillator vs. VDD
Figure 24-21:	Transconductance(gm) of XT
	Oscillator vs. VDD
Figure 24-22:	(LP Mode, 25°C)
Figure 24-23:	
. iguio 2 i 20i	(HS Mode, 25°C)
Figure 24-24:	Typical XTAL Startup Time vs. VDD
0	(XT Mode, 25°C)
Figure 24-25:	Typical Idd vs. Frequency
	(LP Mode, 25°C)
Figure 24-26:	Maximum IDD vs. Frequency
F i 0 4	(LP Mode, 85°C to -40°C)289
Figure 24-27:	Typical IDD vs. Frequency
Figure 24-28:	(XT Mode, 25°C)
i iyure 24-28:	Maximum IDD vs. Frequency (XT Mode, -40°C to 85°C)289

Figure 24-29:	Typical IDD vs. Frequency
	(HS Mode, 25°C) 290
Figure 24-30:	Maximum IDD vs. Frequency
	(HS Mode, -40°C to 85°C) 290

Table 18-1:	Cross Reference of Device Specs		
	for Oscillator Configurations and		
	Frequencies of Operation		
	(Commercial Devices)		
Table 18-2:	External Clock Timing		
Table 19.0	Requirements		
Table 18-3:	CLKOUT and I/O Timing Requirements190		
Table 18-4:	Reset, Watchdog Timer,		
1000 10 4.	Oscillator Start-up Timer and		
	Power-up Timer Requirements		
Table 18-5:	Timer0 and Timer1 External		
	Clock Requirements 192		
Table 18-6:	Capture/Compare/PWM		
	Requirements (CCP1) 193		
Table 18-7:	Parallel Slave Port Requirements (PIC16C64)		
	194		
Table 18-8:	SPI Mode Requirements 195		
Table 18-9:	I ² C Bus Start/Stop Bits		
Table 10 10.	Requirements		
Table 18-10:	I ² C Bus Data Requirements		
Table 19-1:	Cross Reference of Device Specs for Oscillator Configurations and		
	Frequencies of Operation		
	(Commercial Devices)		
Table 19-2:	External Clock Timing		
10010 10 21	Requirements		
Table 19-3:	CLKOUT and I/O Timing		
	Requirements		
Table 19-4:	Reset, Watchdog Timer,		
	Oscillator Start-up Timer,		
	Power-up Timer, and Brown-out		
	Reset Requirements		
Table 19-5:	Timer0 and Timer1 External		
	Clock Requirements		
Table 19-6:	Capture/Compare/PWM Requirements (CCP1)		
Table 19-7:	Parallel Slave Port Requirements		
	(PIC16C64A/R64)210		
Table 19-8:	SPI Mode Requirements		
Table 19-9:	I ² C Bus Start/Stop Bits		
	Requirements		
Table 19-10:	I ² C Bus Data Requirements		
Table 20-1:	Cross Reference of Device Specs		
	for Oscillator Configurations and		
	Frequencies of Operation		
	(Commercial Devices)		
Table 20-2:	External Clock Timing		
Table 00.2	Requirements		
Table 20-3:	CLKOUT and I/O Timing Requirements222		
Table 20-4:	Reset, Watchdog Timer,		
10010 20 1.	Oscillator Start-up Timer and		
	Power-up Timer Requirements		
Table 20-5:	Timer0 and Timer1 External		
	Clock Requirements		
Table 20-6:	Capture/Compare/PWM		
	Requirements (CCP1 and CCP2)225		
Table 20-7:	Parallel Slave Port Requirements		
Table 20-8:	SPI Mode Requirements		
Table 20-9:	I ² C Bus Start/Stop Bits		
	Requirements		
Table 20-10: Table 20-11:	i ² C Bus Data Requirements		
1 abie 20-11.	Requirements		
	104410110110		

Table 20-12:	USART Synchronous Receive
Table 21-1:	Requirements
	Specs for Oscillator Configurations
	and Frequencies of Operation
T 11 01 0	(Commercial Devices)
Table 21-2:	External Clock Timing
Table 21-3:	Requirements
	Requirements
Table 21-4:	Reset, Watchdog Timer, Oscillator
	Start-up Timer, Power-up Timer, and
	Brown-out Reset Requirements 239
Table 21-5:	Timer0 and Timer1 External
T 11 01 0	Clock Requirements
Table 21-6:	Capture/Compare/PWM
Table 21-7:	Requirements (CCP1 and CCP2)
	(PIC16C65A)
Table 21-8:	SPI Mode Requirements
Table 21-9:	I ² C Bus Start/Stop Bits
	Requirements
Table 21-10:	I ² C Bus Data Requirements 245
Table 21-11:	USART Synchronous
Table of to	Transmission Requirements
Table 21-12:	USART Synchronous Receive Requirements
Table 22-1:	Cross Reference of Device Specs
	for Oscillator Configurations and
	Frequencies of Operation
	(Commercial Devices)
Table 22-2:	External Clock Timing
	Requirements
Table 22-3:	CLKOUT and I/O Timing
Table 22-4:	Requirements
Table 22-4.	Reset, Watchdog Timer, Oscillator Start-up Timer,
	Power-up Timer, and Brown-out
	Reset Requirements
Table 22-5:	Timer0 and Timer1 External
	Clock Requirements 256
Table 22-6:	Capture/Compare/PWM
T-1-1-00 7	Requirements (CCP1 and CCP2) 257
Table 22-7:	Parallel Slave Port Requirements
Table 22-8:	(PIC16CR65)258 SPI Mode Requirements
Table 22-9:	I ² C Bus Start/Stop Bits
	Requirements
Table 22-10:	I ² C Bus Data Requirements 261
Table 22-11:	USART Synchronous Transmission
T 11 00 10	Requirements
Table 22-12:	USART Synchronous Receive
Table 23-1:	Requirements
14510 20 11	for Oscillator Configurations and
	Frequencies of Operation
	(Commercial Devices) 263
Table 23-2:	External Clock Timing
Table CO. C	Requirements
Table 23-3:	CLKOUT and I/O Timing Requirements 270
Table 23-4:	Reset, Watchdog Timer,
. 4510 20 7.	Oscillator Start-up Timer,
	Power-up Timer, and Brown-out
	Reset Requirements 271

READER RESPONSE

It is our intention to provide you with the best documentation possible to ensure successful use of your Microchip product. If you wish to provide your comments on organization, clarity, subject matter, and ways in which our documentation can better serve you, please FAX your comments to the Technical Publications Manager at (602) 786-7578.

Please list the following information, and use this outline to provide us with your comments about this Data Sheet.

To:	Technical Publications Manager	Total Pages Sent				
RE:	Reader Response					
Fror	om: Name					
	Company					
	Address					
	City / State / ZIP / Country					
	Telephone: ()	FAX: ()				
	plication (optional):					
Woι	ould you like a reply?YN					
Device: PIC16C6X Literature Number: DS30234E						
Que	lestions:					
4	What are the best features of this document?					
1.	what are the best leatures of this document?					
2.	. How does this document meet your hardware and software development needs?					
3.	Do you find the organization of this data sheet easy to follow? If not, why?					
4.	4. What additions to the data sheet do you think would enhance the structure and subject?					
_						
5.	What deletions from the data sheet could be made wit	hout affecting the overall usefulness?				
6	Is there any incorrect or misleading information (what a	and whore \2				
0.						
7.	How would you improve this document?					
	<i>y</i>					
8.	How would you improve our software, systems, and sil	icon products?				