

Welcome to E-XFL.COM

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	I ² C, SPI
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	22
Program Memory Size	3.5KB (2K x 14)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 6V
Data Converters	-
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.300", 7.62mm)
Supplier Device Package	28-SPDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16c62a-04-sp

1.0 GENERAL DESCRIPTION

The PIC16CXX is a family of low-cost, high-performance, CMOS, fully-static, 8-bit microcontrollers.

All PIC16/17 microcontrollers employ an advanced RISC architecture. The PIC16CXX microcontroller family has enhanced core features, eight-level deep stack, and multiple internal and external interrupt sources. The separate instruction and data buses of the Harvard architecture allow a 14-bit wide instruction word with separate 8-bit wide data. The two stage instruction pipeline allows all instructions to execute in a single cycle, except for program branches (which require two cycles). A total of 35 instructions (reduced instruction set) are available. Additionally, a large register set gives some of the architectural innovations used to achieve a very high performance.

PIC16CXX microcontrollers typically achieve a 2:1 code compression and a 4:1 speed improvement over other 8-bit microcontrollers in their class.

The **PIC16C61** device has 36 bytes of RAM and 13 I/O pins. In addition a timer/counter is available.

The **PIC16C62/62A/R62** devices have 128 bytes of RAM and 22 I/O pins. In addition, several peripheral features are available, including: three timer/counters, one Capture/Compare/PWM module and one serial port. The Synchronous Serial Port can be configured as either a 3-wire Serial Peripheral Interface (SPI™) or the two-wire Inter-Integrated Circuit (I²C) bus.

The **PIC16C63/R63** devices have 192 bytes of RAM, while the **PIC16C66** has 368 bytes. All three devices have 22 I/O pins. In addition, several peripheral features are available, including: three timer/counters, two Capture/Compare/PWM modules and two serial ports. The Synchronous Serial Port can be configured as either a 3-wire Serial Peripheral Interface (SPI) or the two-wire Inter-Integrated Circuit (I²C) bus. The Universal Synchronous Asynchronous Receiver Transmitter (USART) is also known as a Serial Communications Interface or SCI.

The **PIC16C64/64A/R64** devices have 128 bytes of RAM and 33 I/O pins. In addition, several peripheral features are available, including: three timer/counters, one Capture/Compare/PWM module and one serial port. The Synchronous Serial Port can be configured as either a 3-wire Serial Peripheral Interface (SPI) or the two-wire Inter-Integrated Circuit (I²C) bus. An 8-bit Parallel Slave Port is also provided.

The **PIC16C65/65A/R65** devices have 192 bytes of RAM, while the **PIC16C67** has 368 bytes. All four devices have 33 I/O pins. In addition, several peripheral features are available, including: three timer/counters, two Capture/Compare/PWM modules and two serial ports. The Synchronous Serial Port can be configured as either a 3-wire Serial Peripheral Interface (SPI) or the two-wire Inter-Integrated Circuit (I²C) bus. The Universal Synchronous Asynchronous Receiver Transmitter

(USART) is also known as a Serial Communications Interface or SCI. An 8-bit Parallel Slave Port is also provided.

The PIC16C6X device family has special features to reduce external components, thus reducing cost, enhancing system reliability and reducing power consumption. There are four oscillator options, of which the single pin RC oscillator provides a low-cost solution, the LP oscillator minimizes power consumption, XT is a standard crystal, and the HS is for High Speed crystals. The SLEEP (power-down) mode offers a power saving mode. The user can wake the chip from SLEEP through several external and internal interrupts, and resets.

A highly reliable Watchdog Timer with its own on-chip RC oscillator provides protection against software lock-up.

A UV erasable CERDIP packaged version is ideal for code development, while the cost-effective One-Time-Programmable (OTP) version is suitable for production in any volume.

The PIC16C6X family fits perfectly in applications ranging from high-speed automotive and appliance control to low-power remote sensors, keyboards and telecom processors. The EPROM technology makes customization of application programs (transmitter codes, motor speeds, receiver frequencies, etc.) extremely fast and convenient. The small footprint packages make this microcontroller series perfect for all applications with space limitations. Low-cost, low-power, high performance, ease-of-use, and I/O flexibility make the PIC16C6X very versatile even in areas where no microcontroller use has been considered before (e.g. timer functions, serial communication, capture and compare, PWM functions, and co-processor applications).

1.1 Family and Upward Compatibility

Those users familiar with the PIC16C5X family of microcontrollers will realize that this is an enhanced version of the PIC16C5X architecture. Please refer to Appendix A for a detailed list of enhancements. Code written for PIC16C5X can be easily ported to PIC16CXX family of devices (Appendix B).

1.2 Development Support

PIC16C6X devices are supported by the complete line of Microchip Development tools.

Please refer to Section 15.0 for more details about Microchip's development tools.

2.0 PIC16C6X DEVICE VARIETIES

A variety of frequency ranges and packaging options are available. Depending on application and production requirements, the proper device option can be selected using the information in the PIC16C6X Product Identification System section at the end of this data sheet. When placing orders, please use that page of the data sheet to specify the correct part number.

For the PIC16C6X family of devices, there are four device "types" as indicated in the device number:

1. **C**, as in PIC16C64. These devices have EPROM type memory and operate over the standard voltage range.
2. **LC**, as in PIC16LC64. These devices have EPROM type memory and operate over an extended voltage range.
3. **CR**, as in PIC16CR64. These devices have ROM program memory and operate over the standard voltage range.
4. **LCR**, as in PIC16LCR64. These devices have ROM program memory and operate over an extended voltage range.

2.1 UV Erasable Devices

The UV erasable version, offered in CERDIP package is optimal for prototype development and pilot programs. This version can be erased and reprogrammed to any of the oscillator modes.

Microchip's PICSTART® Plus and PRO MATE® II programmers both support programming of the PIC16C6X.

2.2 One-Time-Programmable (OTP) Devices

The availability of OTP devices is especially useful for customers who need the flexibility for frequent code updates and small volume applications.

The OTP devices, packaged in plastic packages, permit the user to program them once. In addition to the program memory, the configuration bits must also be programmed.

2.3 Quick-Turnaround-Production (QTP) Devices

Microchip offers a QTP Programming Service for factory production orders. This service is made available for users who choose not to program a medium to high quantity of units and whose code patterns have stabilized. The devices are identical to the OTP devices but with all EPROM locations and configuration options already programmed by the factory. Certain code and prototype verification procedures apply before production shipments are available. Please contact your local Microchip Technology sales office for more details.

2.4 Serialized Quick-Turnaround Production (SQTPSM) Devices

Microchip offers a unique programming service where a few user-defined locations in each device are programmed with different serial numbers. The serial numbers may be random, pseudo-random, or sequential.

Serial programming allows each device to have a unique number which can serve as an entry-code, password, or ID number.

ROM devices do not allow serialization information in the program memory space. The user may have this information programmed in the data memory space.

For information on submitting ROM code, please contact your regional sales office.

2.5 Read Only Memory (ROM) Devices

Microchip offers masked ROM versions of several of the highest volume parts, thus giving customers a low cost option for high volume, mature products.

For information on submitting ROM code, please contact your regional sales office.

7.3.1 SWITCHING PRESCALER ASSIGNMENT

The prescaler assignment is fully under software control, i.e., it can be changed “on the fly” during program execution.

Note: To avoid an unintended device RESET, the following instruction sequence (shown in Example 7-1) must be executed when changing the prescaler assignment from Timer0 to the WDT. This precaution must be followed even if the WDT is disabled.

EXAMPLE 7-1: CHANGING PRESCALER (TIMER0→WDT)

```

1) BSF    STATUS, RP0    ;Bank 1
Lines 2 and 3 do NOT have to 2) MOVLW  b'xx0x0xxx'    ;Select clock source and prescale value of
be included if the final desired 3) MOVWF  OPTION_REG    ;other than 1:1
prescale value is other than 1:1. 4) BCF    STATUS, RP0    ;Bank 0
If 1:1 is final desired value, then 5) CLRWF  TMR0          ;Clear TMR0 and prescaler
a temporary prescale value is      6) BSF    STATUS, RP1    ;Bank 1
set in lines 2 and 3 and the final 7) MOVLW  b'xxxx1xxx'    ;Select WDT, do not change prescale value
prescale value will be set in lines 8) MOVWF  OPTION_REG    ;
10 and 11.                       9) CLRWDT                ;Clears WDT and prescaler
                                   10) MOVLW  b'xxxx1xxx'    ;Select new prescale value and WDT
                                   11) MOVWF  OPTION_REG    ;
                                   12) BCF    STATUS, RP0    ;Bank 0

```

To change prescaler from the WDT to the Timer0 module, use the sequence shown in Example 7-2.

EXAMPLE 7-2: CHANGING PRESCALER (WDT→TIMER0)

```

CLRWDT                ;Clear WDT and prescaler
BSF    STATUS, RP0    ;Bank 1
MOVLW  b'xxx0xxx'    ;Select TMR0, new prescale value and clock source
MOVWF  OPTION_REG    ;
BCF    STATUS, RP0    ;Bank 0

```

TABLE 7-1: REGISTERS ASSOCIATED WITH TIMER0

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other resets
01h, 101h	TMR0	Timer0 module's register								xxxx xxxx	uuuu uuuu
0Bh,8Bh, 10Bh,18Bh	INTCON	GIE	PEIE ⁽¹⁾	TOIE	INTE	RBIE	TOIF	INTF	RBIF	0000 000x	0000 000u
81h, 181h	OPTION	RBPU	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
85h	TRISA	—	—	PORTA Data Direction Register ⁽¹⁾						--11 1111	--11 1111

Legend: x = unknown, u = unchanged, - = unimplemented locations read as '0'. Shaded cells are not used by Timer0.

Note 1: TRISA<5> and bit PEIE are not implemented on the PIC16C61, read as '0'.

PIC16C6X

8.1 Timer1 Operation in Timer Mode

Applicable Devices													
61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67

Timer mode is selected by clearing bit TMR1CS (T1CON<1>). In this mode, the input clock to the timer is $F_{osc}/4$. The synchronize control bit T1SYNC (T1CON<2>) has no effect since the internal clock is always in sync.

8.2 Timer1 Operation in Synchronized Counter Mode

Applicable Devices													
61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67

Counter mode is selected by setting bit TMR1CS. In this mode the timer increments on every rising edge of clock input on T1OSI when enable bit T1OSCEN is set or pin with T1CKI when bit T1OSCEN is cleared.

Note: The T1OSI function is multiplexed to different pins, depending on the device. See the pinout descriptions to see which pin has the T1OSI function.

If T1SYNC is cleared, then the external clock input is synchronized with internal phase clocks. The synchronization is done after the prescaler stage. The prescaler stage is an asynchronous ripple counter.

In this configuration, during SLEEP mode, Timer1 will not increment even if an external clock is present, since the synchronization circuit is shut off. The prescaler, however, will continue to increment.

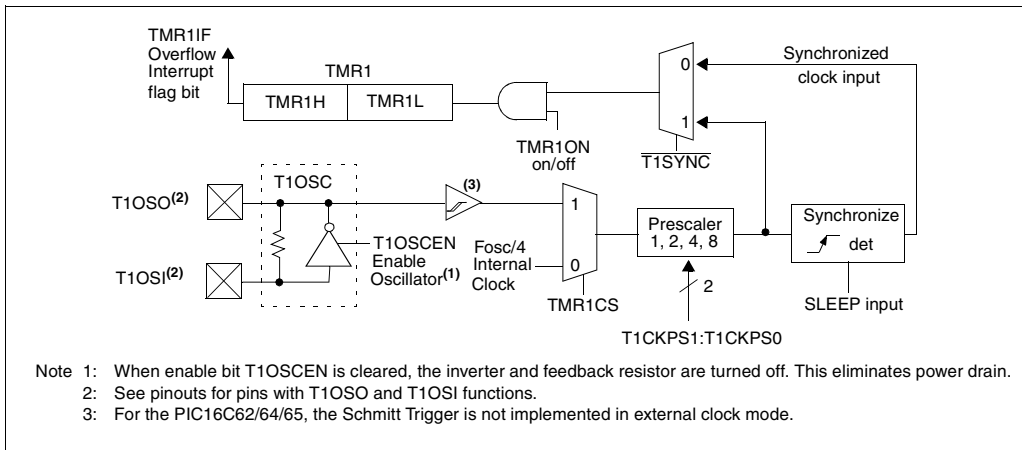
8.2.1 EXTERNAL CLOCK INPUT TIMING FOR SYNCHRONIZED COUNTER MODE

When an external clock input is used for Timer1 in synchronized counter mode, it must meet certain requirements. The external clock requirement is due to internal phase clock (T_{osc}) synchronization. Also, there is a delay in the actual incrementing of TMR1 after synchronization.

When the prescaler is 1:1, the external clock input is the same as the prescaler output. The synchronization of T1CKI with the internal phase clocks is accomplished by sampling the prescaler output on the Q2 and Q4 cycles of the internal phase clocks. Therefore, it is necessary for T1CKI to be high for at least $2T_{osc}$ (and a small RC delay of 20 ns) and low for at least $2T_{osc}$ (and a small RC delay of 20 ns). Refer to appropriate electrical specification section, parameters 45, 46, and 47.

When a prescaler other than 1:1 is used, the external clock input is divided by the asynchronous ripple-counter type prescaler so that the prescaler output is symmetrical. In order for the external clock to meet the sampling requirement, the ripple counter must be taken into account. Therefore, it is necessary for T1CKI to have a period of at least $4T_{osc}$ (and a small RC delay of 40 ns) divided by the prescaler value. The only requirement on T1CKI high and low time is that they do not violate the minimum pulse width requirements of 10 ns). Refer to applicable electrical specification section, parameters 40, 42, 45, 46, and 47.

FIGURE 8-2: TIMER1 BLOCK DIAGRAM



Steps to follow when setting up an Asynchronous Transmission:

1. Initialize the SPBRG register for the appropriate baud rate. If a high speed baud rate is desired, then set bit BRGH. (Section 12.1).
2. Enable the asynchronous serial port by clearing bit SYNC and setting bit SPEN.
3. If interrupts are desired, then set enable bit TXIE.
4. If 9-bit transmission is desired, then set transmit bit TX9.
5. Enable the transmission by setting bit TXEN, which will also set bit TXIF.
6. If 9-bit transmission is selected, the ninth bit should be loaded in bit TX9D.
7. Load data to the TXREG register (starts transmission).

FIGURE 12-8: ASYNCHRONOUS MASTER TRANSMISSION

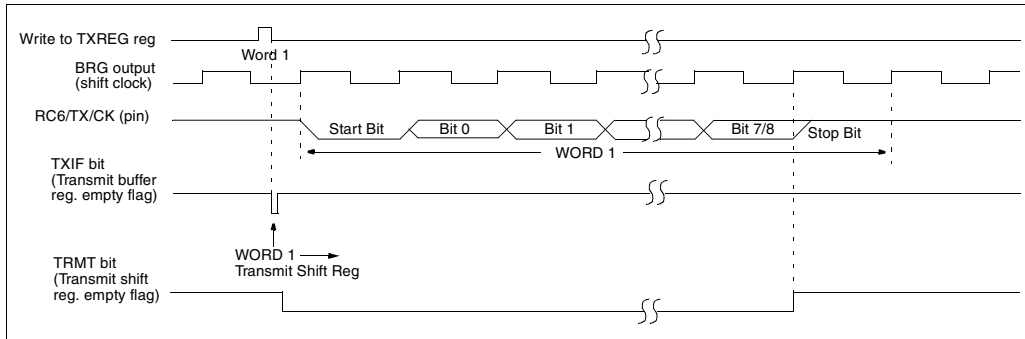


FIGURE 12-9: ASYNCHRONOUS MASTER TRANSMISSION (BACK TO BACK)

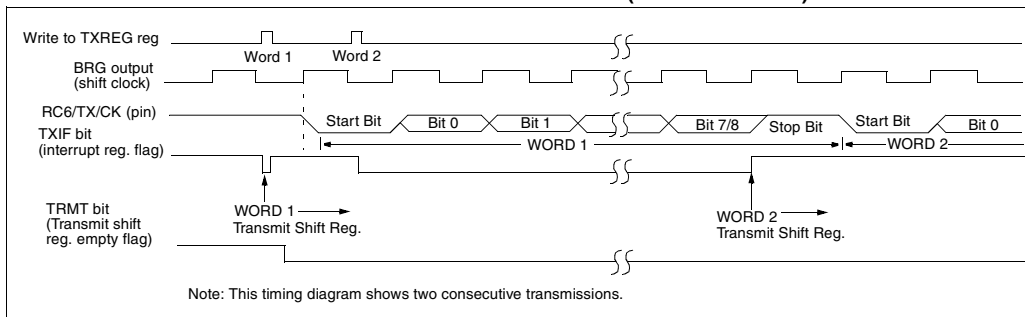


TABLE 12-6: REGISTERS ASSOCIATED WITH ASYNCHRONOUS TRANSMISSION

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
0Ch	PIR1	PSPIF ⁽¹⁾	(2)	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
18h	RCSTA	SPEN	RX9	SREN	CREN	—	FERR	OERR	RX9D	0000 -00x	0000 -00x
19h	TXREG	USART Transmit Register								0000 0000	0000 0000
8Ch	PIE1	PSPIE ⁽¹⁾	(2)	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
98h	TXSTA	CSRC	TX9	TXEN	SYNC	—	BRGH	TRMT	TX9D	0000 -010	0000 -010
99h	SPBRG	Baud Rate Generator Register								0000 0000	0000 0000

Legend: x = unknown, - = unimplemented locations read as '0'. Shaded cells are not used for Asynchronous Transmission.

Note 1: PSPIF and PSPIE are reserved on the PIC16C63/R63/66, always maintain these bits clear.

Note 2: PIR1<6> and PIE1<6> are reserved, always maintain these bits clear.

TABLE 13-12: INITIALIZATION CONDITIONS FOR ALL REGISTERS (Cont.'d)

Register	Applicable Devices															Power-on Reset Brown-out Reset	MCLR Reset during: – normal operation – SLEEP WDT Reset	Wake-up via interrupt or WDT Wake-up
	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67				
TRISD	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67	1111 1111	1111 1111	uuuu uuuu	
TRISE	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67	0000 -111	0000 -111	uuuu -uuu	
PIE1	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67	00-- 0000	00-- 0000	uu-- uuuu	
	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67	0000 0000	0000 0000	uuuu uuuu	
PIE2	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67	---- --0	---- --0	---- --u	
PCON	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67	---- --0u	---- --uu	---- --uu	
	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67	---- --0-	---- --u-	---- --u-	
PR2	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67	1111 1111	1111 1111	1111 1111	
SSPADD	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67	0000 0000	0000 0000	uuuu uuuu	
SSPSTAT	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67	--00 0000	--00 0000	--uu uuuu	
TXSTA	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67	0000 -010	0000 -010	uuuu -uuu	
SPBRG	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67	0000 0000	0000 0000	uuuu uuuu	

Legend: u = unchanged, x = unknown, - = unimplemented bit read as '0', q = value depends on condition.

Note 1: One or more bits in INTCON, PIR1 and/or PIR2 will be affected (to cause wake-up).

2: When the wake-up is due to an interrupt and the global enable bit, GIE is set, the PC is loaded with the interrupt vector (0004h) after execution of PC + 1.

3: See Table 13-10 and Table 13-11 for reset value for specific conditions.

PIC16C6X

SLEEP

Syntax: [*label*] SLEEP

Operands: None

Operation: 00h → WDT,
0 → WDT prescaler,
1 → \overline{TO} ,
0 → \overline{PD}

Status Affected: \overline{TO} , \overline{PD}

Encoding:

00	0000	0110	0011
----	------	------	------

Description: The power-down status bit, \overline{PD} is cleared. Time-out status bit, \overline{TO} is set. Watchdog Timer and its prescaler are cleared. The processor is put into SLEEP mode with the oscillator stopped. See Section 13.8 for more details.

Words: 1

Cycles: 1

Q Cycle Activity:

	Q1	Q2	Q3	Q4
Decode	No-Operation	No-Operation	Go to Sleep	

Example: SLEEP

SUBLW

Subtract W from Literal

Syntax: [*label*] SUBLW k

Operands: $0 \leq k \leq 255$

Operation: $k - (W) \rightarrow (W)$

Status Affected: C, DC, Z

Encoding:

11	110x	kkkk	kkkk
----	------	------	------

Description: The W register is subtracted (2's complement method) from the eight bit literal 'k'. The result is placed in the W register.

Words: 1

Cycles: 1

Q Cycle Activity:

	Q1	Q2	Q3	Q4
Decode	Read literal 'k'	Process data	Write to W	

Example 1: SUBLW 0x02

Before Instruction

W = 1
C = ?
Z = ?

After Instruction

W = 1
C = 1; result is positive
Z = 0

Example 2: Before Instruction

W = 2
C = ?
Z = ?

After Instruction

W = 0
C = 1; result is zero
Z = 1

Example 3: Before Instruction

W = 3
C = ?
Z = ?

After Instruction

W = 0xFF
C = 0; result is negative
Z = 0

15.0 ELECTRICAL CHARACTERISTICS FOR PIC16C61

Absolute Maximum Ratings †

Ambient temperature under bias.....	-55°C to +125°C
Storage temperature.....	-65°C to +150°C
Voltage on any pin with respect to V _{SS} (except V _{DD} , $\overline{\text{MCLR}}$, and RA4).....	-0.3V to (V _{DD} + 0.3V)
Voltage on V _{DD} with respect to V _{SS}	-0.3V to +7.5V
Voltage on $\overline{\text{MCLR}}$ with respect to V _{SS} (Note 2).....	0V to +14V
Voltage on RA4 pin with respect to V _{SS}	0V to +14V
Total power dissipation (Note 1).....	800 mW
Maximum current out of V _{SS} pin.....	150 mA
Maximum current into V _{DD} pin.....	100 mA
Input clamp current, I _{IK} (V _I < 0 or V _I > V _{DD}).....	± 20 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{DD}).....	± 20 mA
Maximum output current sunk by any I/O pin.....	25 mA
Maximum output current sourced by any I/O pin.....	20 mA
Maximum current sunk by PORTA.....	80 mA
Maximum current sourced by PORTA.....	50 mA
Maximum current sunk by PORTB.....	150 mA
Maximum current sourced by PORTB.....	100 mA

Note 1: Power dissipation is calculated as follows: $P_{dis} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD} - V_{OH}) \times I_{OH}\} + \sum (V_{OL} \times I_{OL})$

Note 2: Voltage spikes below V_{SS} at the $\overline{\text{MCLR}}$ pin, inducing currents greater than 80 mA, may cause latch-up. Thus, a series resistor of 50-100Ω should be used when applying a “low” level to the $\overline{\text{MCLR}}$ pin rather than pulling this pin directly to V_{SS}.

† NOTICE: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 15-1: CROSS REFERENCE OF DEVICE SPECS FOR OSCILLATOR CONFIGURATIONS AND FREQUENCIES OF OPERATION (COMMERCIAL DEVICES)

OSC	PIC16C61-04	PIC16C61-20	PIC16LC61-04	JW Devices
RC	V _{DD} : 4.0V to 6.0V I _{DD} : 3.3 mA max. at 5.5V I _{PD} : 14 μA max. at 4V Freq: 4 MHz max.	V _{DD} : 4.5V to 5.5V I _{DD} : 1.8 mA typ. at 5.5V I _{PD} : 1.0 μA typ. at 4V Freq: 4 MHz max.	V _{DD} : 3.0V to 6.0V I _{DD} : 1.4 mA typ. at 3.0V I _{PD} : 0.6 μA typ. at 3V Freq: 4 MHz max.	V _{DD} : 4.0V to 6.0V I _{DD} : 3.3 mA max. at 5.5V I _{PD} : 14 μA max. at 4V Freq: 4 MHz max.
XT	V _{DD} : 4.0V to 6.0V I _{DD} : 3.3 mA max. at 5.5V I _{PD} : 14 μA max. at 4V Freq: 4 MHz max.	V _{DD} : 4.5V to 5.5V I _{DD} : 1.8 mA typ. at 5.5V I _{PD} : 1.0 μA typ. at 4V Freq: 4 MHz max.	V _{DD} : 3.0V to 6.0V I _{DD} : 1.4 mA typ. at 3.0V I _{PD} : 0.6 μA typ. at 3V Freq: 4 MHz max.	V _{DD} : 4.0V to 6.0V I _{DD} : 3.3 mA max. at 5.5V I _{PD} : 14 μA max. at 4V Freq: 4 MHz max.
HS	V _{DD} : 4.5V to 5.5V I _{DD} : 13.5 mA typ. at 5.5V I _{PD} : 1.0 μA typ. at 4.5V Freq: 4 MHz max.	V _{DD} : 4.5V to 5.5V I _{DD} : 30 mA max. at 5.5V I _{PD} : 1.0 μA typ. at 4.5V Freq: 20 MHz max.	Not recommended for use in HS mode	V _{DD} : 4.5V to 5.5V I _{DD} : 30 mA max. at 5.5V I _{PD} : 1.0 μA typ. at 4.5V Freq: 20 MHz max.
LP	V _{DD} : 4.0V to 6.0V I _{DD} : 15 μA typ. at 32 kHz, 4.0V I _{PD} : 0.6 μA typ. at 4.0V Freq: 200 kHz max.	Not recommended for use in LP mode	V _{DD} : 3.0V to 6.0V I _{DD} : 32 μA max. at 32 kHz, 3.0V I _{PD} : 9 μA max. at 3.0V Freq: 200 kHz max.	V _{DD} : 3.0V to 6.0V I _{DD} : 32 μA max. at 32 kHz, 3.0V I _{PD} : 9 μA max. at 3.0V Freq: 200 kHz max.

The shaded sections indicate oscillator selections which are tested for functionality, but not for MIN/MAX specifications. It is recommended that the user select the device type that ensures the specifications required.

16.0 DC AND AC CHARACTERISTICS GRAPHS AND TABLES FOR PIC16C61

The graphs and tables provided in this section are for design guidance and are not tested or guaranteed.

In some graphs or tables the data presented are outside specified operating range (i.e., outside specified V_{DD} range). This is for information only and devices are guaranteed to operate properly only within the specified range.

Note: The data presented in this section is a statistical summary of data collected on units from different lots over a period of time and matrix samples. 'Typical' represents the mean of the distribution while 'max' or 'min' represents (mean $+3\sigma$) and (mean -3σ) respectively where σ is standard deviation.

FIGURE 16-1: TYPICAL RC OSCILLATOR FREQUENCY vs. TEMPERATURE

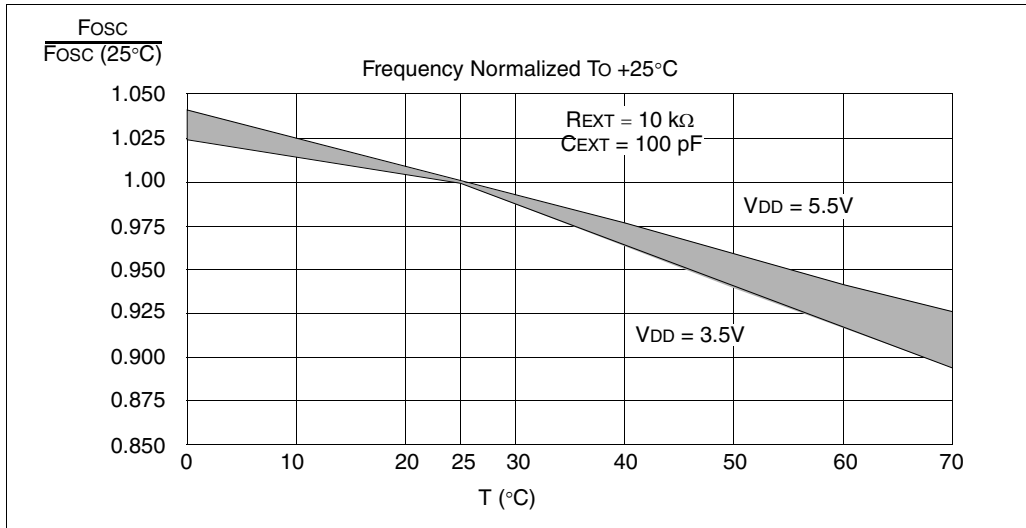


TABLE 16-1: RC OSCILLATOR FREQUENCIES

Cext	Rext	Average Fosc @ 5V, 25°C	
		Fosc	% Variation
20 pF	4.7k	4.52 MHz	± 17.35%
	10k	2.47 MHz	± 10.10%
	100k	290.86 kHz	± 11.90%
100 pF	3.3k	1.92 MHz	± 9.43%
	4.7k	1.48 MHz	± 9.83%
	10k	788.77 kHz	± 10.92%
	100k	88.11 kHz	± 16.03%
300 pF	3.3k	726.89 kHz	± 10.97%
	4.7k	573.95 kHz	± 10.14%
	10k	307.31 kHz	± 10.43%
	100k	33.82 kHz	± 11.24%

The percentage variation indicated here is part to part variation due to normal process distribution. The variation indicated is ± 3 standard deviation from average value for $V_{DD} = 5V$.

PIC16C6X

Applicable Devices 61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

FIGURE 16-12: TYPICAL I_{DD} vs. FREQUENCY (EXTERNAL CLOCK, 25°C)

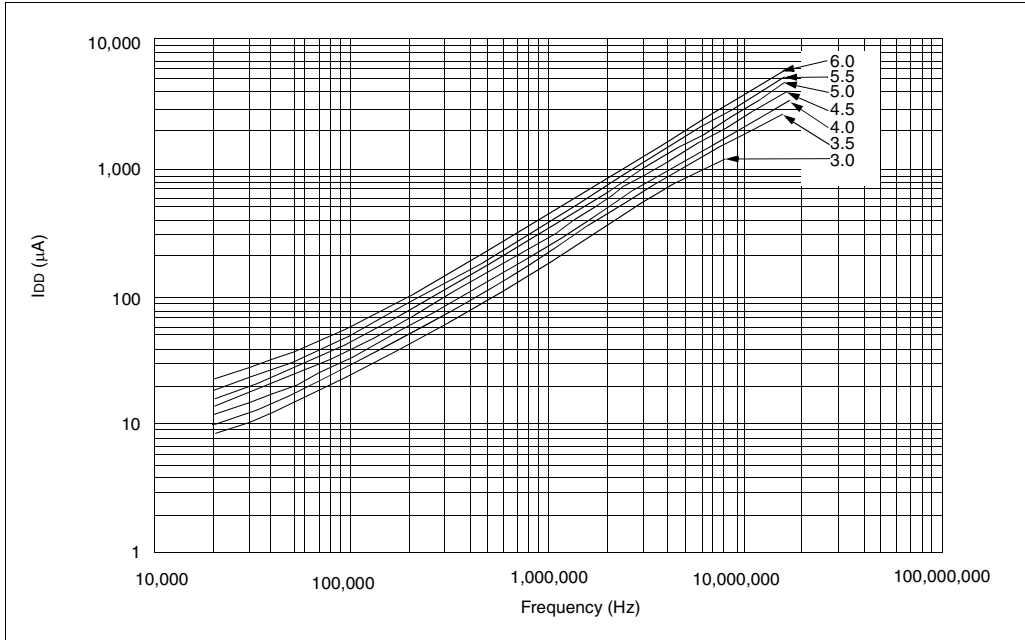
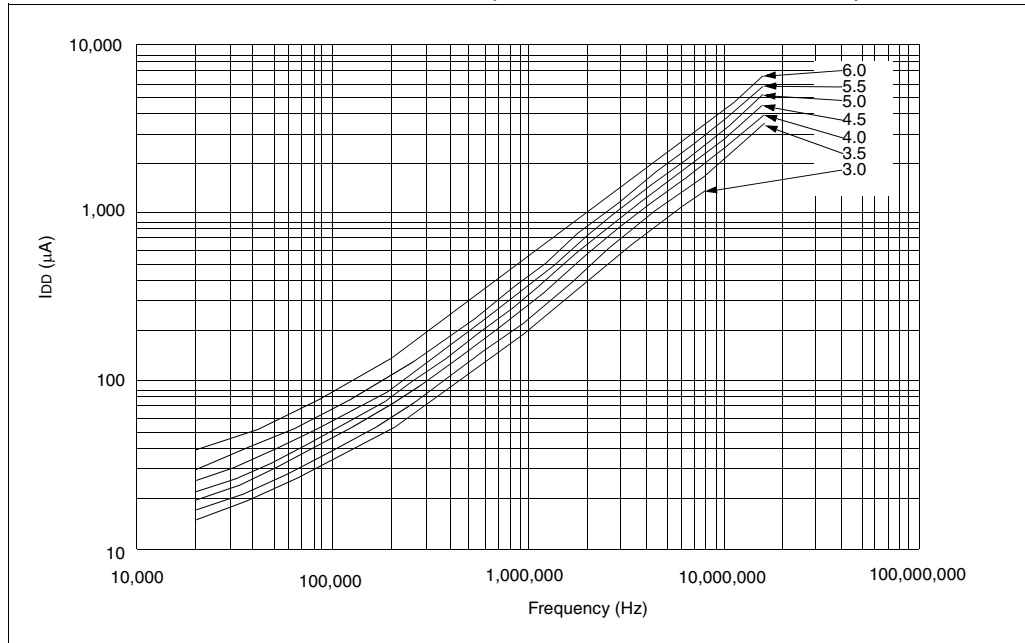
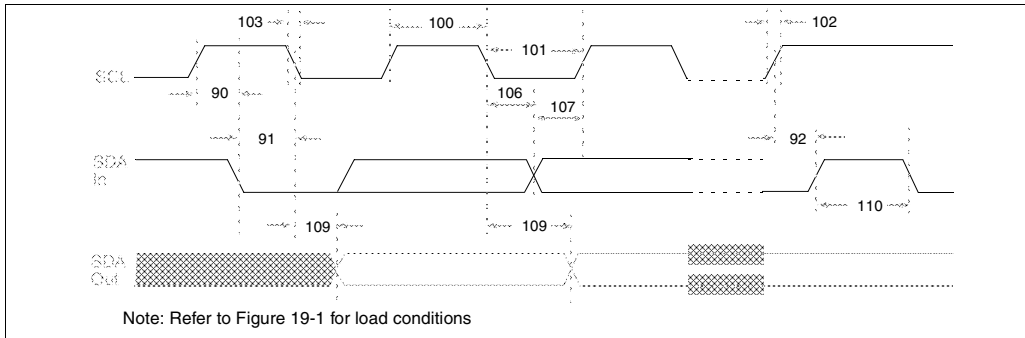


FIGURE 16-13: MAXIMUM I_{DD} vs. FREQUENCY (EXTERNAL CLOCK, -40° TO +85°C)



Data based on matrix samples. See first page of this section for details.

FIGURE 19-10: I²C BUS DATA TIMING



Note: Refer to Figure 19-1 for load conditions

TABLE 19-10: I²C BUS DATA REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Max	Units	Conditions	
100	THIGH	Clock high time	100 kHz mode	4.0	—	μs	Device must operate at a minimum of 1.5 MHz
			400 kHz mode	0.6	—	μs	Device must operate at a minimum of 10 MHz
			SSP Module	1.5TCY	—		
101	TLOW	Clock low time	100 kHz mode	4.7	—	μs	Device must operate at a minimum of 1.5 MHz
			400 kHz mode	1.3	—	μs	Device must operate at a minimum of 10 MHz
			SSP Module	1.5TCY	—		
102	TR	SDA and SCL rise time	100 kHz mode	—	1000	ns	
			400 kHz mode	20 + 0.1Cb	300	ns	Cb is specified to be from 10-400 pF
103	TF	SDA and SCL fall time	100 kHz mode	—	300	ns	
			400 kHz mode	20 + 0.1Cb	300	ns	Cb is specified to be from 10-400 pF
90	TSU:STA	START condition setup time	100 kHz mode	4.7	—	μs	Only relevant for repeated START condition
			400 kHz mode	0.6	—	μs	
91	THD:STA	START condition hold time	100 kHz mode	4.0	—	μs	After this period the first clock pulse is generated
			400 kHz mode	0.6	—	μs	
106	THD:DAT	Data input hold time	100 kHz mode	0	—	ns	
			400 kHz mode	0	0.9	μs	
107	TSU:DAT	Data input setup time	100 kHz mode	250	—	ns	Note 2
			400 kHz mode	100	—	ns	
92	TSU:STO	STOP condition setup time	100 kHz mode	4.7	—	μs	
			400 kHz mode	0.6	—	μs	
109	TAA	Output valid from clock	100 kHz mode	—	3500	ns	Note 1
			400 kHz mode	—	—	ns	
110	TBUF	Bus free time	100 kHz mode	4.7	—	μs	Time the bus must be free before a new transmission can start
			400 kHz mode	1.3	—	μs	
	Cb	Bus capacitive loading	—	400	pF		

Note 1: As a transmitter, the device must provide this internal minimum delay time to bridge the undefined region (min. 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

2: A fast-mode (400 kHz) I²C-bus device can be used in a standard-mode (100 kHz) I²C-bus system, but the requirement tsu:DAT ≥ 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line TR max.+tsu:DAT = 1000 + 250 = 1250 ns (according to the standard-mode I²C bus specification) before the SCL line is released.

PIC16C6X

Applicable Devices 61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

20.1 DC Characteristics: PIC16C63/65A-04 (Commercial, Industrial, Extended) PIC16C63/65A-10 (Commercial, Industrial, Extended) PIC16C63/65A-20 (Commercial, Industrial, Extended)

DC CHARACTERISTICS		Standard Operating Conditions (unless otherwise stated)						
		Operating temperature -40°C ≤ TA ≤ +125°C for extended, -40°C ≤ TA ≤ +85°C for industrial and 0°C ≤ TA ≤ +70°C for commercial						
Param No.	Characteristic	Sym	Min	Typ†	Max	Units	Conditions	
D001 D001A	Supply Voltage	VDD	4.0 4.5	- -	6.0 5.5	V V	XT, RC and LP osc configuration HS osc configuration	
D002*	RAM Data Retention Voltage (Note 1)	VDR	-	1.5	-	V		
D003	VDD start voltage to ensure internal Power-on Reset signal	VPOR	-	VSS	-	V	See section on Power-on Reset for details	
D004*	VDD rise rate to ensure internal Power-on Reset signal	SVDD	0.05	-	-	V/ms	See section on Power-on Reset for details	
D005	Brown-out Reset Voltage	BVDD	3.7 3.7	4.0 4.0	4.3 4.4	V V	BODEN configuration bit is enabled Extended Range Only	
D010	Supply Current (Note 2, 5)	IDD	-	2.7	5	mA	XT, RC, osc config FOSC = 4 MHz, VDD = 5.5V (Note 4)	
D013			-	10	20	mA	HS osc config FOSC = 20 MHz, VDD = 5.5V	
D015*	Brown-out Reset Current (Note 6)	ΔIBOR	-	350	425	μA	BOR enabled, VDD = 5.0V	
D020 D021 D021A D021B	Power-down Current (Note 3, 5)	IPD	- - - -	10.5 1.5 1.5 2.5	42 16 19 19	μA μA μA μA	VDD = 4.0V, WDT enabled, -40°C to +85°C VDD = 4.0V, WDT disabled, -0°C to +70°C VDD = 4.0V, WDT disabled, -40°C to +85°C VDD = 4.0V, WDT disabled, -40°C to +125°C	
D023*	Brown-out Reset Current (Note 6)	ΔIBOR	-	350	425	μA	BOR enabled, VDD = 5.0V	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.

The test conditions for all IDD measurements in active operation mode are:
OSC1 = external square wave, from rail to rail; all I/O pins tristated, pulled to VDD,
MCLR = VDD; WDT enabled/disabled as specified.

3: The power down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

4: For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula $I_r = V_{DD}/2R_{ext}$ (mA) with Rext in kOhm.

5: Timer1 oscillator (when enabled) adds approximately 20 μA to the specification. This value is from characterization and is for design guidance only. This is not tested.

6: The Δ current is the additional current consumed when this peripheral is enabled. This current should be added to the base IDD or IPD measurement.

FIGURE 20-7: CAPTURE/COMPARE/PWM TIMINGS (CCP1 AND CCP2)

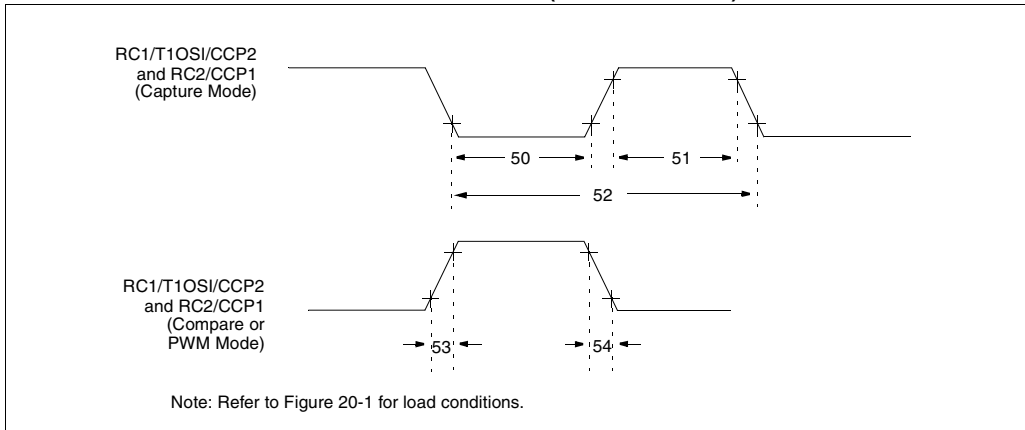


TABLE 20-6: CAPTURE/COMPARE/PWM REQUIREMENTS (CCP1 AND CCP2)

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions	
50*	TccL	CCP1 and CCP2 input low time	No Prescaler	$0.5T_{CY} + 20$	—	—	ns	
			With Prescaler	PIC16C63/65A	10	—	—	ns
				PIC16LC63/65A	20	—	—	ns
51*	TccH	CCP1 and CCP2 input high time	No Prescaler	$0.5T_{CY} + 20$	—	—	ns	
			With Prescaler	PIC16C63/65A	10	—	—	ns
				PIC16LC63/65A	20	—	—	ns
52*	TccP	CCP1 and CCP2 input period	$\frac{3T_{CY} + 40}{N}$	—	—	ns	N = prescale value (1, 4, or 16)	
53*	TccR	CCP1 and CCP2 output rise time	PIC16C63/65A	—	10	25	ns	
			PIC16LC63/65A	—	25	45	ns	
54*	TccF	CCP1 and CCP2 output fall time	PIC16C63/65A	—	10	25	ns	
			PIC16LC63/65A	—	25	45	ns	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

PIC16C6X

Applicable Devices **61** **62** **62A** **R62** **63** **R63** **64** **64A** **R64** **65** **65A** **R65** **66** **67**

FIGURE 23-12: TYPICAL I_{DD} vs. FREQUENCY (RC MODE @ 22 pF, 25°C)

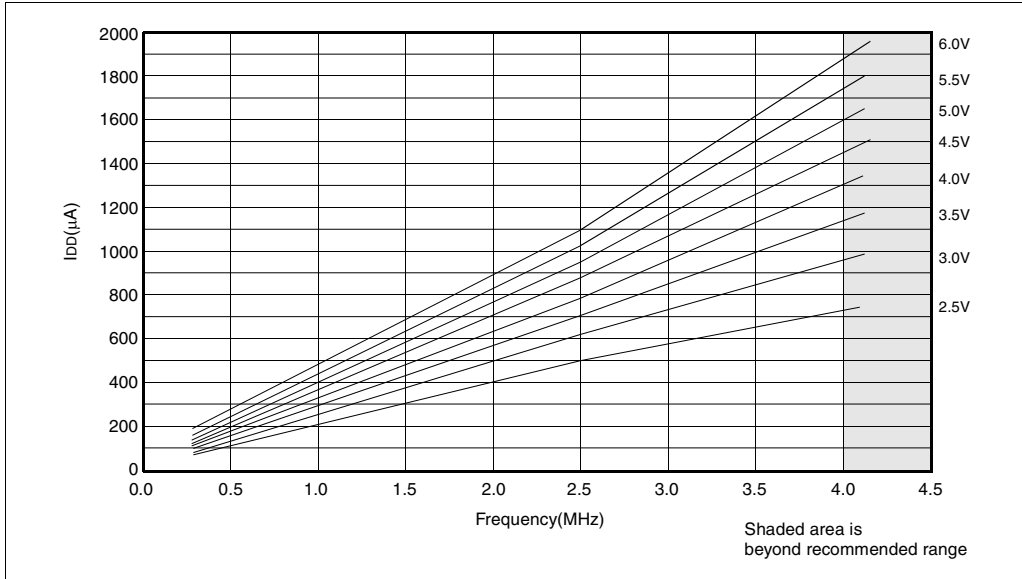
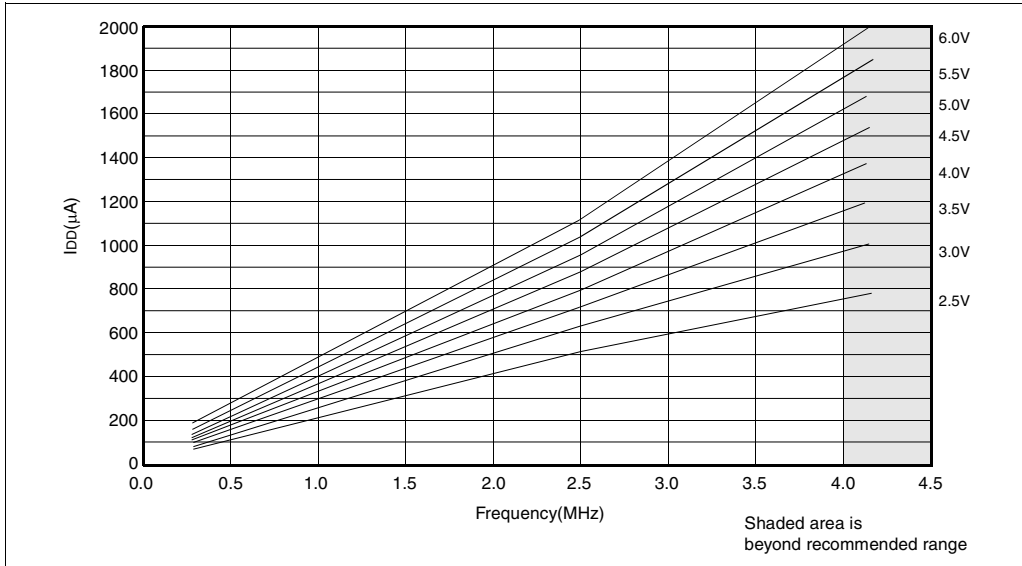


FIGURE 23-13: MAXIMUM I_{DD} vs. FREQUENCY (RC MODE @ 22 pF, -40°C TO 85°C)



Data based on matrix samples. See first page of this section for details.

PIC16C6X

Applicable Devices 61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

FIGURE 23-22: TYPICAL XTAL STARTUP TIME vs. VDD (LP MODE, 25°C)

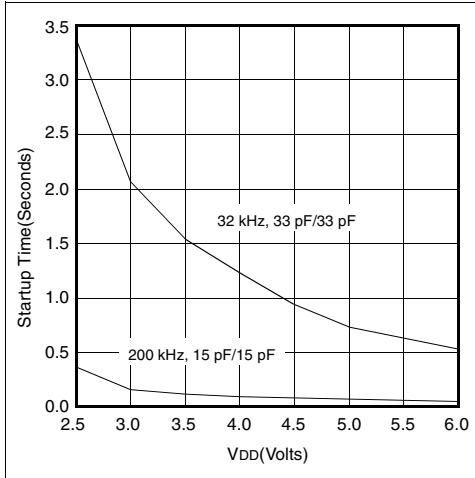


FIGURE 23-24: TYPICAL XTAL STARTUP TIME vs. VDD (XT MODE, 25°C)

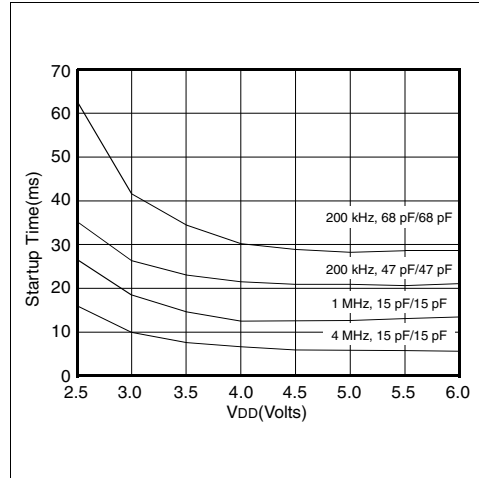


FIGURE 23-23: TYPICAL XTAL STARTUP TIME vs. VDD (HS MODE, 25°C)

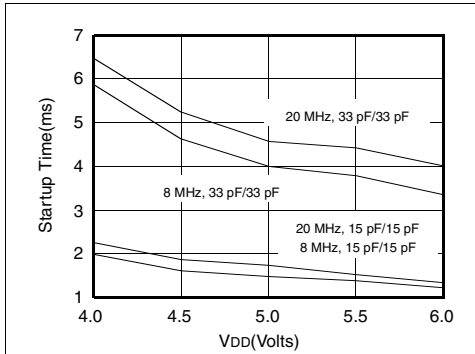


TABLE 23-2: CAPACITOR SELECTION FOR CRYSTAL OSCILLATORS

Osc Type	Crystal Freq	Cap. Range C1	Cap. Range C2
LP	32 kHz	33 pF	33 pF
	200 kHz	15 pF	15 pF
XT	200 kHz	47-68 pF	47-68 pF
	1 MHz	15 pF	15 pF
	4 MHz	15 pF	15 pF
HS	4 MHz	15 pF	15 pF
	8 MHz	15-33 pF	15-33 pF
	20 MHz	15-33 pF	15-33 pF
Crystals Used			
32 kHz	Epson C-001R32.768K-A	± 20 PPM	
200 kHz	STD XTL 200.000KHz	± 20 PPM	
1 MHz	ECS ECS-10-13-1	± 50 PPM	
4 MHz	ECS ECS-40-20-1	± 50 PPM	
8 MHz	EPSON CA-301 8.000M-C	± 30 PPM	
20 MHz	EPSON CA-301 20.000M-C	± 30 PPM	

Data based on matrix samples. See first page of this section for details.

Registers

CCP1CON	
Diagram	78
Section	78
Summary	24, 26, 28, 30, 32
CCP2CON	
Diagram	78
Section	78
Summary	26, 30, 32
CCPR1H	
Summary	24, 26, 28, 30, 32
CCPR1L	
Summary	24, 26, 28, 30, 32
CCPR2H	
Summary	26, 30, 32
CCPR2L	
Summary	26, 30, 32
FSR	
Indirect Addressing	49
Summary	24, 26, 28, 30, 32, 34
INDF	
Indirect Addressing	49
Summary	24, 26, 28, 30, 32, 34
INTCON	
Diagram	37
Section	37
Summary	24, 26, 28, 30, 32, 34
OPTION	
Diagram	36
Section	36
Summary	25, 27, 29, 31, 33, 34
PCL	
Section	48
Summary	24, 26, 28, 30, 32, 34
PCLATH	
Section	48
Summary	24, 26, 28, 30, 32, 34
PCON	
Diagram	47
Section	47
Summary	25, 27, 29, 31, 33
PIE1	
Diagram	40
Section	38
Summary	25, 27, 29, 31, 33
PIE2	
Diagram	45
Section	45
Summary	27, 31, 33
PIR1	
Diagram	44
Section	41
Summary	24, 26, 28, 30, 32
PIR2	
Diagram	46
Section	46
Summary	26, 30, 32
PORTA	
Section	51
Summary	24, 26, 28, 30, 32
PORTB	
Section	53
Summary	24, 26, 28, 30, 32, 34
PORTC	
Section	55
Summary	24, 26, 28, 30, 32

PORTD	
Section	57
Summary	28, 30, 32
PORTE	
Section	58
Summary	28, 30, 32
PR2	
Summary	25, 27, 29, 31, 33
RCREG	
Summary	26, 30, 32
RCSTA	
Diagram	106
Summary	26, 30, 32
SPBRG	
Summary	27, 31, 33
SSPBUF	
Section	86
Summary	24, 26, 28, 30, 32
SSPCON	
Diagram	85
Summary	24, 26, 28, 30, 32
SSPSR	
Section	86
SSPSTAT	
Diagram	84
Section	84
Summary	25, 27, 29, 31, 33
STATUS	
Diagram	35
Section	35
Summary	24, 26, 28, 30, 32, 34
T1CON	
Diagram	71
Section	71
Summary	24, 26, 28, 30, 32
T2CON	
Diagram	75
Section	75
Summary	24, 26, 28, 30, 32
TMR0	
Summary	24, 26, 28, 30, 32, 34
TMR1H	
Summary	24, 26, 28, 30, 32
TMR1L	
Summary	24, 26, 28, 30, 32
TMR2	
Summary	24, 26, 28, 30, 32
TRISA	
Section	51
Summary	25, 27, 29, 31, 33
TRISB	
Section	53
Summary	25, 27, 29, 31, 33, 34
TRISC	
Section	55
Summary	25, 27, 29, 31, 33
TRISD	
Section	57
Summary	29, 31, 33
TRISE	
Diagram	58
Section	58
Summary	29, 31, 33
TXREG	
Summary	26, 30, 32

PIC16C6X

TXSTA	
Diagram	105
Section	105
Summary	31, 33
W	9
Special Function Registers, Initialization	
Conditions	132
Special Function Registers, Reset Conditions	131
Special Function Register Summary ...	24, 26, 28, 30, 32
File Maps	21
Resets	128
ROM	7
RP0 bit	20, 35
RP1	35
RX9	106
RX9D	106
S	
S	84, 89
SCI - See Universal Synchronous Asynchronous Receiver Transmitter (USART)	
SCK	86
SCL	100
SDI	86
SDO	86
Serial Port Enable bit, SPEN	106
Serial Programming	142
Serial Programming, Block Diagram	142
Serialized Quick-Turnaround-Production	7
Single Receive Enable bit, SREN	106
Slave Mode	
SCL	100
SDA	100
SLEEP Mode	123, 141
SMP	89
Software Simulator (MPSIM)	161
SPBRG	25, 27, 29, 31, 33, 34
Special Features, Section	123
SPEN	106
SPI	
Block Diagram	86, 91
Master Mode	92
Master Mode Timing	93
Mode	86
Serial Clock	91
Serial Data In	91
Serial Data Out	91
Slave Mode Timing	94
Slave Mode Timing Diagram	93
Slave Select	91
SPI clock	92
SPI Mode	91
SSPCON	90
SSPSTAT	89
SPI Clock Edge Select bit, CKE	89
SPI Data Input Sample Phase Select bit, SMP	89
SPI Mode	86
SREN	106
SS	86
SSP	
Module Overview	83
Section	83
SSPBUF	92
SSPCON	90
SSPSR	92
SSPSTAT	89
SSP in I ² C Mode - See I ² C	
SSPADD	25, 27, 29, 31, 33, 34, 99
SSPBUF	24, 26, 28, 30, 32, 34, 99
SSPCON	24, 26, 28, 30, 32, 34, 85, 90
SSPEN	85, 90
SSPIE	38
SSPIF	41
SSPM3:SSPM0	85, 90
SSPOV	85, 90, 100
SSPSTAT	25, 27, 29, 31, 33, 34, 84, 99
SSPSTAT Register	89
Stack	48
Start bit, S	84, 89
STATUS	24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34
Status bits	130, 131
Status Bits During Various Resets	131
Stop bit, P	84, 89
Switching Prescalers	69
SYNC, USART Mode Select bit, SYNC	105
Synchronizing Clocks, TMR0	67
Synchronous Serial Port (SSP)	
Block Diagram, SPI Mode	86
SPI Master/Slave Diagram	87
SPI Mode	86
Synchronous Serial Port Enable bit, SSPEN	85, 90
Synchronous Serial Port Interrupt Enable bit, SSPIE	38
Synchronous Serial Port Interrupt Flag bit, SSPIF	41
Synchronous Serial Port Mode Select bits,	
SSPM3:SSPM0	85, 90
Synchronous Serial Port Module	83
Synchronous Serial Port Status Register	89
T	
T0CS	36
TOIE	37
TOIF	37
T0SE	36
T1CKPS1:T1CKPS0	71
T1CON	24, 26, 28, 30, 32, 34
T1OSCEN	71
T1SYNC	71
T2CKPS1:T2CKPS0	75
T2CON	24, 26, 28, 30, 32, 34, 75
Time-out	130
Time-out bit	35
Time-out Sequence	130
Timer Modules	
Overview, all	63
Timer0	
Block Diagram	65
Counter Mode	65
External Clock	67
Interrupt	65
Overview	63
Prescaler	68
Section	65
Timer Mode	65
Timing Diagram/Timing Diagrams	
Timer0	65
TMR0 register	65
Timer1	
Block Diagram	72
Capacitor Selection	73
Counter Mode, Asynchronous	73
Counter Mode, Synchronous	72
External Clock	73
Oscillator	73

Overview	63	Watchdog Timer	207
Prescaler.....	72	PIC16C63	
Read/Write in Asynchronous Counter Mode	73	Brown-out Reset.....	239
Section.....	71	Capture/Compare/PWM	241
Synchronizing with External Clock.....	72	CLKOUT and I/O	238
Timer Mode	72	External Clock	237
TMR1 Register Pair	71	I ² C Bus Data.....	245
Timer2		I ² C Bus Start/Stop Bits	244
Block Diagram	75	Oscillator Start-up Timer.....	239
Overview	63	Power-up Timer.....	239
Postscaler	75	Reset.....	239
Prescaler.....	75	SPI Mode.....	243
Timer0 Clock Synchronization, Delay	67	Timer0	240
Timer0 Interrupt	138	Timer1	240
Timer1 Clock Source Select bit, TMR1CS.....	71	USART Synchronous Receive	
Timer1 External Clock Input Synchronization		(Master/Slave)	246
Control bit, T1SYNC	71	Watchdog Timer	239
Timer1 Input Clock Prescale Select bits	71	PIC16C64	
Timer1 Mode Selection	78	Capture/Compare/PWM	193
Timer1 On bit, TMR1ON	71	CLKOUT and I/O	190
Timer1 Oscillator Enable Control bit, T1OSCEM	71	External Clock	189
Timer2 Clock Prescale Select bits,		I ² C Bus Data.....	197
T2CKPS1:T2CKPS0	75	I ² C Bus Start/Stop Bits	196
Timer2 Module	75	Oscillator Start-up Timer.....	191
Timer2 On bit, TMR2ON	75	Parallel Slave Port.....	194
Timer2 Output Postscale Select bits,		Power-up Timer.....	191
TOUTPS3:TOUTPS0	75	Reset.....	191
Timing Diagrams		SPI Mode.....	195
Brown-out Reset	129	Timer0	192
I ² C Clock Synchronization	98	Timer1	192
I ² C Data Transfer Wait State	96	Watchdog Timer	191
I ² C Multi-Master Arbitration.....	98	PIC16C64A	
I ² C Reception (7-bit Address)	101	Brown-out Reset.....	207
PIC16C61		Capture/Compare/PWM	209
CLKOUT and I/O	170	CLKOUT and I/O	206
External Clock	169	External Clock	205
Oscillator Start-up Timer.....	171	I ² C Bus Data.....	213
Power-up Timer	171	I ² C Bus Start/Stop Bits	212
Reset	171	Oscillator Start-up Timer.....	207
Timer0.....	172	Parallel Slave Port.....	210
Watchdog Timer	171	Power-up Timer.....	207
PIC16C62		Reset.....	207
Capture/Compare/PWM	193	SPI Mode.....	211
CLKOUT and I/O	190	Timer0	208
External Clock	189	Timer1	208
I ² C Bus Data	197	Watchdog Timer	207
I ² C Bus Start/Stop Bits	196	PIC16C65	
Oscillator Start-up Timer.....	191	Capture/Compare/PWM	225
Power-up Timer	191	CLKOUT and I/O	222
Reset	191	External Clock	221
SPI Mode	195	I ² C Bus Data.....	229
Timer0.....	192	I ² C Bus Start/Stop Bits	228
Timer1.....	192	Oscillator Start-up Timer.....	223
Watchdog Timer	191	Parallel Slave Port.....	226
PIC16C62A		Reset	223
Brown-out Reset	207	SPI Mode.....	227
Capture/Compare/PWM	209	Timer0	224
CLKOUT and I/O	206	Timer1	224
External Clock	205	USART Synchronous Receive	
I ² C Bus Data.....	213	(Master/Slave)	230
I ² C Bus Start/Stop Bits	212	Watchdog Timer	223
Oscillator Start-up Timer.....	207	PIC16C65A	
Power-up Timer	207	Brown-out Reset.....	239
Reset	207	Capture/Compare/PWM	241
SPI Mode	211	CLKOUT and I/O	238
Timer0.....	208	External Clock	237
Timer1.....	208	I ² C Bus Data.....	245

PIC16C6X

Table 23-5:	Timer0 and Timer1 External Clock Requirements	272
Table 23-6:	Capture/Compare/PWM Requirements (CCP1 and CCP2)	273
Table 23-7:	Parallel Slave Port Requirements (PIC16C67) 274	
Table 23-8:	SPI Mode Requirements.....	277
Table 23-9:	I ² C Bus Start/Stop Bits Requirements	278
Table 23-10:	I ² C Bus Data Requirements	279
Table 23-11:	USART Synchronous Transmission Requirements	280
Table 23-12:	USART Synchronous Receive Requirements	280
Table 24-1:	RC Oscillator Frequencies	287
Table 24-2:	Capacitor Selection for Crystal Oscillators	288
Table E-1:	Pin Compatible Devices.....	315

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Information contained in this publication regarding device applications and the like is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION, INCLUDING BUT NOT LIMITED TO ITS CONDITION, QUALITY, PERFORMANCE, MERCHANTABILITY OR FITNESS FOR PURPOSE. Microchip disclaims all liability arising from this information and its use. Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights.

Trademarks

The Microchip name and logo, the Microchip logo, dsPIC, FlashFlex, KEELoQ, KEELoQ logo, MPLAB, PIC, PICmicro, PICSTART, PIC³² logo, rPIC, SST, SST Logo, SuperFlash and UNI/O are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

FilterLab, Hampshire, HI-TECH C, Linear Active Thermistor, MTP, SEEVAL and The Embedded Control Solutions Company are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Silicon Storage Technology is a registered trademark of Microchip Technology Inc. in other countries.

Analog-for-the-Digital Age, Application Maestro, BodyCom, chipKIT, chipKIT logo, CodeGuard, dsPICDEM, dsPICDEM.net, dsPICworks, dsSPEAK, ECAN, ECONOMONITOR, FanSense, HI-TIDE, In-Circuit Serial Programming, ICSP, MINDI, MiWi, MPASM, MPF, MPLAB Certified logo, MPLIB, MPLINK, mTouch, Omniclient Code Generation, PICC, PICC-18, PICDEM, PICDEM.net, PICkit, PICtail, REAL ICE, rLAB, Select Mode, SQI, Serial Quad I/O, Total Endurance, TSHARC, UniWinDriver, WiperLock, ZENA and Z-Scale are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

GestIC and ULPP are registered trademarks of Microchip Technology Germany II GmbH & Co. & KG, a subsidiary of Microchip Technology Inc., in other countries.

All other trademarks mentioned herein are property of their respective companies.

© 1997-2013, Microchip Technology Incorporated, Printed in the U.S.A., All Rights Reserved.

Printed on recycled paper.

ISBN: 9781620769652

Microchip received ISO/TS-16949:2009 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELoQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.

**QUALITY MANAGEMENT SYSTEM
CERTIFIED BY DNV
= ISO/TS 16949 =**