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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	22
Program Memory Size	7KB (4K x 14)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	192 x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 6V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16c63-20i-so

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

NOTES:

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4.2.2.3 INTCON REGISTER

Applicable Devices

61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

The INTCON Register is a readable and writable register which contains the various enable and flag bits for the TMR0 register overflow, RB port change and external RB0/INT pin interrupts.

Note: Interrupt flag bits get set when an interrupt condition occurs regardless of the state of its corresponding enable bit or the global enable bit, GIE (INTCON<7>).

FIGURE 4-11: INTCON REGISTER (ADDRESS 0Bh, 8Bh, 10Bh 18Bh)

B/W-0	B/W-0	B/W-0	B/W-0	B/W-0	B/W-0	B/W-0	B/W-x			
GIE	PEIE	TOIE	INTE	RBIE	TOIF	INTE	RBIF	R = Readable bit		
bit7	<u> </u>	<u> </u>	l			1	bitO	W = Writable bit U = Unimplemented bit, read as '0' - n = Value at POR reset x = unknown		
bit 7:	GIE: ⁽¹⁾ Global Interrupt Enable bit 1 = Enables all un-masked interrupts 0 = Disables all interrupts									
bit 6:	 bit 6: PEIE:⁽²⁾ Peripheral Interrupt Enable bit 1 = Enables all un-masked peripheral interrupts 0 = Disables all peripheral interrupts 									
bit 5:	T0IE: TMR0 Overflow Interrupt Enable bit 1 = Enables the TMR0 overflow interrupt 0 = Disables the TMR0 overflow interrupt									
bit 4:	INTE: RB0/INT External Interrupt Enable bit 1 = Enables the RB0/INT external interrupt 0 = Disables the RB0/INT external interrupt									
bit 3:	RBIE: RB I 1 = Enable 0 = Disable	Port Chang s the RB po s the RB p	e Interrupt ort change ort change	Enable bit interrupt interrupt						
bit 2:	TOIF: TMR 1 = TMR0 0 = TMR0	0 Overflow register ove register did	Interrupt Flerflowed (m not overflo	ag bit ust be cleai w	red in softwa	re)				
bit 1:	INTF: RB0 1 = The RE 0 = The RE	/INT Exterr 30/INT exte 30/INT exte	nal Interrupt rnal interru rnal interru	Flag bit ot occurred ot did not o	(must be cle ccur	ared in soft	ware)			
bit 0:	RBIF: RB I 1 = At leas 0 = None o	Port Chang t one of the of the RB7:I	e Interrupt RB7:RB4 RB4 pins ha	Flag bit bins change we change	ed state (see d state	Section 5.2	2 to clear the	interrupt)		
Note 1:	1: For the PIC16C61/62/64/65, if an interrupt occurs while the GIE bit is being cleared, the GIE bit may unintentionally be re-enabled by the RETFIE instruction in the user's Interrupt Service Routine. Refer to Section 13.5 for a detailed description.									
2:	I NE PEIE I	Dit (bit6) is i	unimplemer	nted on the	PIC16C61, r	ead as '0'.				
Interri globa enabli	Interrupt flag bits get set when an interrupt condition occurs regardless of the state of its corresponding enable bit or the global enable bit, GIE (INTCON<7>). User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.									

4.2.2.8 PCON REGISTER

Applicable Devices

61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

The Power Control register (PCON) contains a flag bit to allow differentiation between a Power-on Reset to an external MCLR reset or WDT reset. Those devices with brown-out detection circuitry contain an additional bit to differentiate a Brown-out Reset condition from a Poweron Reset condition.

Note: BOR is unknown on Power-on Reset. It must then be set by the user and checked on subsequent resets to see if BOR is clear, indicating a brown-out has occurred. The BOR status bit is a "don't care" and is not necessarily predictable if the brown-out circuit is disabled (by clearing the BODEN bit in the Configuration word).

FIGURE 4-22: PCON REGISTER FOR PIC16C62/64/65 (ADDRESS 8Eh)



FIGURE 4-23: PCON REGISTER FOR PIC16C62A/R62/63/R63/64A/R64/65A/R65/66/67 (ADDRESS 8Eh)



FIGURE 5-4: BLOCK DIAGRAM OF THE RB7:RB4 PINS FOR PIC16C62A/63/R63/64A/65A/ R65/66/67



TABLE 5-3: PORTB FUNCTIONS

FIGURE 5-5: BLOCK DIAGRAM OF THE RB3:RB0 PINS



Name	Bit#	Buffer Type	Function
RB0/INT	bit0	TTL/ST ⁽¹⁾	Input/output pin or external interrupt input. Internal software programmable weak pull-up.
RB1	bit1	TTL	Input/output pin. Internal software programmable weak pull-up.
RB2	bit2	TTL	Input/output pin. Internal software programmable weak pull-up.
RB3	bit3	TTL	Input/output pin. Internal software programmable weak pull-up.
RB4	bit4	TTL	Input/output pin (with interrupt on change). Internal software programmable weak pull-up.
RB5	bit5	TTL	Input/output pin (with interrupt on change). Internal software programmable weak pull-up.
RB6	bit6	TTL/ST ⁽²⁾	Input/output pin (with interrupt on change). Internal software programmable weak pull-up. Serial programming clock.
RB7	bit7	TTL/ST ⁽²⁾	Input/output pin (with interrupt on change). Internal software programmable weak pull-up. Serial programming data.

Legend: TTL = TTL input, ST = Schmitt Trigger input

Note 1: This buffer is a Schmitt Trigger input when configured as the external interrupt.

2: This buffer is a Schmitt Trigger input when used in serial programming mode.

TABLE 5-4: SUMMARY OF REGISTERS ASSOCIATED WITH PORTB

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other resets
06h, 106h	PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx xxxx	uuuu uuuuu
86h, 186h	TRISB	PORTB D	ata Directior	n Register						1111 1111	1111 1111
81h, 181h	OPTION	RBPU	INTEDG	TOCS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111

Legend: x = unknown, u = unchanged. Shaded cells are not used by PORTB.

10.3 PWM Mode

Applicable Devices 61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

In Pulse Width Modulation (PWM) mode, the CCP1 pin produces up to a 10-bit resolution PWM output. Since the CCP1 pin is multiplexed with the PORTC data latch, the TRISC<2> bit must be cleared to make the CCP1 pin an output.

Note: Clearing the CCP1CON register will force the CCP1 PWM output latch to the default low level. This is not the PORTC I/O data latch.

Figure 10-4 shows a simplified block diagram of the CCP module in PWM mode.

For a step by step procedure on how to set up the CCP module for PWM operation, see Section 10.3.3.

FIGURE 10-4: SIMPLIFIED PWM BLOCK DIAGRAM



A PWM output (Figure 10-5) has a time base (period) and a time that the output stays high (duty cycle). The frequency of the PWM is the inverse of the period (1/period).

FIGURE 10-5: PWM OUTPUT



10.3.1 PWM PERIOD

The PWM period is specified by writing to the PR2 register. The PWM period can be calculated using the following formula:

PWM period = [(PR2) + 1] • 4 • TOSC • (TMR2 prescale value)

PWM frequency is defined as 1 / [PWM period].

When TMR2 is equal to PR2, the following three events occur on the next increment cycle:

- TMR2 is cleared
- The PWM duty cycle is latched from CCPR1L into CCPR1H
- The CCP1 pin is set (exception: if PWM duty cycle = 0%, the CCP1 pin will not be set)

Note:	The Timer2 postscaler (see Section 9.1) is
	not used in the determination of the PWM
	frequency. The postscaler could be used to
	have a servo update rate at a different fre-
	quency than the PWM output.

10.3.2 PWM DUTY CYCLE

The PWM duty cycle is specified by writing to the CCPR1L register and to the CCP1CON<5:4> bits. Up to 10-bit resolution is available: the CCPR1L contains the eight MSbs and the CCP1CON<5:4> contains the two LSbs. This 10-bit value is represented by CCPR1L:CCP1CON<5:4>. The following equation is used to calculate the PWM duty cycle in time:

PWM duty cycle = (CCPR1L:CCP1CON<5:4>) • Tosc • (TMR2 prescale value)

CCPR1L and CCP1CON<5:4> can be written to at any time, but the duty cycle value is not latched into CCPR1H until after a match between PR2 and TMR2 occurs (i.e., the period is complete). In PWM mode, CCPR1H is a read-only register.

The CCPR1H register and a 2-bit internal latch are used to double buffer the PWM duty cycle. This double buffering is essential for glitchless PWM operation.

When the CCPR1H and 2-bit latch match TMR2 concatenated with an internal 2-bit Q clock or 2 bits of the TMR2 prescaler, the CCP1 pin is cleared.

Maximum PWM resolution (bits) for a given PWM frequency:

$$= \frac{\log\left(\frac{FOSC}{FPWM}\right)}{\log(2)} \quad \text{bits}$$

Note: If the PWM duty cycle value is longer than the PWM period the CCP1 pin will not be forced to the low level.

11.0 SYNCHRONOUS SERIAL PORT (SSP) MODULE

11.1 SSP Module Overview

The Synchronous Serial Port (SSP) module is a serial interface useful for communicating with other peripheral or microcontroller devices. These peripheral devices may be Serial EEPROMs, shift registers, display drivers, A/D converters, etc. The SSP module can operate in one of two modes:

- Serial Peripheral Interface (SPI)
- Inter-Integrated Circuit (I²C)

The SSP module in l^2 C mode works the same in all PIC16C6X devices that have an SSP module. However the SSP Module in SPI mode has differences between the PIC16C66/67 and the other PIC16C6X devices.

The register definitions and operational description of SPI mode has been split into two sections because of the differences between the PIC16C66/67 and the other PIC16C6X devices. The default reset values of both the SPI modules is the same regardless of the device:

11.2	SPI Mode for PIC16C62/62A/R62/63/R63/64	1/
	64A/R64/65/65A/R65 8	4
11.3	SPI Mode for PIC16C66/67 8	9
11.4	I ² C [™] Overview9	5
11.5	SSP I ² C Operation	9

Refer to Application Note AN578, "Use of the SSP Module in the I^2C Multi-Master Environment."

11.5 <u>SSP I²C Operation</u>

The SSP module in I^2C mode fully implements all slave functions, except general call support, and provides interrupts on start and stop bits in hardware to facilitate firmware implementations of the master functions. The SSP module implements the standard mode specifications as well as 7-bit and 10-bit addressing. Two pins are used for data transfer. These are the RC3/SCK/SCL pin, which is the clock (SCL), and the RC4/SDI/SDA pin, which is the data (SDA). The user must configure these pins as inputs or outputs through the TRISC<4:3> bits. The SSP module functions are enabled by setting SSP Enable bit SSPEN (SSP-CON<5>).

FIGURE 11-24: SSP BLOCK DIAGRAM (I²C MODE)



The SSP module has five registers for I^2C operation. These are the:

- SSP Control Register (SSPCON)
- SSP Status Register (SSPSTAT)
- Serial Receive/Transmit Buffer (SSPBUF)
- SSP Shift Register (SSPSR) Not directly accessible
- SSP Address Register (SSPADD)

The SSPCON register allows control of the I^2C operation. Four mode selection bits (SSPCON<3:0>) allow one of the following I^2C modes to be selected:

- I²C Slave mode (7-bit address)
- I²C Slave mode (10-bit address)
- I²C Slave mode (7-bit address), with start and stop bit interrupts enabled
- I²C Slave mode (10-bit address), with start and stop bit interrupts enabled
- I²C Firmware controlled Master Mode, slave is idle

Selection of any I^2C mode, with the SSPEN bit set, forces the SCL and SDA pins to be open drain, provided these pins are programmed to inputs by setting the appropriate TRISC bits.

The SSPSTAT register gives the status of the data transfer. This information includes detection of a START or STOP bit, specifies if the received byte was data or address if the next byte is the completion of 10-bit address, and if this will be a read or write data transfer. The SSPSTAT register is read only.

The SSPBUF is the register to which transfer data is written to or read from. The SSPSR register shifts the data in or out of the device. In receive operations, the SSPBUF and SSPSR create a doubled buffered receiver. This allows reception of the next byte to begin before reading the last byte of received data. When the complete byte is received, it is transferred to the SSPBUF register and flag bit SSPIF is set. If another complete byte is received before the SSPBUF register is read, a receiver overflow has occurred and bit SSPOV (SSPCON<6>) is set and the byte in the SSPSR is lost.

The SSPADD register holds the slave address. In 10-bit mode, the user first needs to write the high byte of the address (1111 0 A9 A8 0). Following the high byte address match, the low byte of the address needs to be loaded (A7:A0).

11.5.1.2 RECEPTION

When the R/ \overline{W} bit of the address byte is clear and an address match occurs, the R/ \overline{W} bit of the SSPSTAT register is cleared. The received address is loaded into the SSPBUF register.

When the address byte overflow condition exists, then no acknowledge (\overline{ACK}) pulse is given. An overflow condition is defined as either bit BF (SSPSTAT<0>) is set or bit SSPOV (SSPCON<6>) is set. An SSP interrupt is generated for each data transfer byte. Flag bit SSPIF (PIR1<3>) must be cleared in software. The SSPSTAT register is used to determine the status of the byte.

FIGURE 11-25: I²C WAVEFORMS FOR RECEPTION (7-BIT ADDRESS)

Receiving Address R/W=0 Receiving Data ACK Receiving Data ACK SDA /A7_ A6 A5 A4 A3 A2 A1 ACK D7 D6 D5 D4 D3 D2 D1 D0 D7 D6 D5 D4 D3 D2 D1 D0 D3 D2 D1 D0 S0 A7 A6 A5 A4 A3 A2 A1 D5 D6 D5 D4 D3 D2 D1 D0 D3 D2 D1 D0 C ACK ACK ACK ACK ACK D3 D2 D1 D0 D3 D2 D1 D0 C ACK ACK	
SSPIF (PIR1<3>) Cleared in software BF (SSPSTAT<0>) SSPBUF register is read	Bus Master terminates transfer
SSPOV (SSPCON<6>) Bit SSPOV is set because the SSPBUF register is still full.	
ACK is not sent.	

12.1.1 SAMPLING

The data on the RC7/RX/DT pin is sampled three times by a majority detect circuit to determine if a high or a low level is present at the RX pin. If bit BRGH (TXSTA<2>) is clear (i.e., at the low baud rates), the sampling is done on the seventh, eighth and ninth falling edges of a x16 clock (Figure 12-3). If bit BRGH is set (i.e., at the high baud rates), the sampling is done on the 3 clock edges preceding the second rising edge after the first falling edge of a x4 clock (Figure 12-4 and Figure 12-5).

FIGURE 12-3: RX PIN SAMPLING SCHEME (BRGH = 0) PIC16C63/R63/65/65A/R65)



FIGURE 12-4: RX PIN SAMPLING SCHEME (BRGH = 1) (PIC16C63/R63/65/65A/R65)







12.4 USART Synchronous Slave Mode

Applicable Devices

61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

Synchronous Slave Mode differs from Master Mode in the fact that the shift clock is supplied externally at the CK pin (instead of being supplied internally in master mode). This allows the device to transfer or receive data while in SLEEP mode. Slave mode is entered by clearing bit CSRC (TXSTA<7>).

12.4.1 USART SYNCHRONOUS SLAVE TRANSMIT

The operation of the synchronous master and slave modes are identical except in the case of the SLEEP mode.

If two words are written to the TXREG and then the SLEEP instruction is executed, the following will occur:

- a) The first word will immediately transfer to the TSR register and transmit.
- b) The second word will remain in TXREG register.
- c) Flag bit TXIF will not be set.
- d) When the first word has been shifted out of TSR, the TXREG register will transfer the second word to the TSR and flag bit TXIF will now be set.
- e) If enable bit TXIE is set, the interrupt will wake the chip from SLEEP and if the global interrupt is enabled, the program will branch to the interrupt vector (0004h).

Steps to follow when setting up Synchronous Slave Transmission:

- 1. Enable the synchronous slave serial port by setting bits SYNC and SPEN, and clearing bit CSRC.
- 2. Clear bits CREN and SREN.
- 3. If interrupts are desired, then set enable bit $\mathsf{TXIE}.$
- 4. If 9-bit transmission is desired, then set bit TX9.
- 5. Enable the transmission by setting bit TXEN.
- 6. If 9-bit transmission is selected, the ninth bit should be loaded in bit TX9D.
- 7. Start transmission by loading data to the TXREG register.

12.4.2 USART SYNCHRONOUS SLAVE RECEPTION

The operation of the synchronous master and slave modes is identical except in the case of the SLEEP mode. Also, enable bit SREN is a don't care in slave mode.

If receive is enabled by setting bit CREN prior to the SLEEP instruction, then a word may be received during SLEEP. On completely receiving the word, the RSR register will transfer the data to the RCREG register and if enable bit RCIE is set, the interrupt generated will wake the chip from SLEEP. If the global interrupt is enabled, the program will branch to the interrupt vector (0004h).

Steps to follow when setting up a Synchronous Slave Reception:

- Enable the synchronous master serial port by setting bits SYNC and SPEN, and clearing bit CSRC.
- 2. If interrupts are desired, then set enable bit RCIE.
- 3. If 9-bit reception is desired, then set bit RX9.
- 4. To enable reception, set enable bit CREN.
- Flag bit RCIF will be set when reception is complete, and an interrupt will be generated if enable bit RCIE was set.
- Read the RCSTA register to get the ninth bit (if enabled) and determine if any error occurred during reception.
- 7. Read the 8-bit received data by reading the RCREG register.
- 8. If any error occurred, clear the error by clearing enable bit CREN.

Applicable Devices 61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

NOTES:

Applicable Devices 61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67





TABLE 18-8: SPI MODE REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Тур†	Max	Units	Conditions
70*	TssL2scH, TssL2scL	$\overline{SS}\downarrow$ to SCK \downarrow or SCK \uparrow input	Тсү	_	—	ns	
71*	TscH	SCK input high time (slave mode)	Tcy + 20	_	_	ns	
72*	TscL	SCK input low time (slave mode)	Tcy + 20	_	_	ns	
73*	TdiV2scH, TdiV2scL	Setup time of SDI data input to SCK edge	50	_	—	ns	
74*	TscH2diL, TscL2diL	Hold time of SDI data input to SCK edge	50	_	_	ns	
75*	TdoR	SDO data output rise time		10	25	ns	
76*	TdoF	SDO data output fall time		10	25	ns	
77*	TssH2doZ	$\overline{\text{SS}}\uparrow$ to SDO output hi-impedance	10	_	50	ns	
78*	TscR	SCK output rise time (master mode)		10	25	ns	
79*	TscF	SCK output fall time (master mode)	_	10	25	ns	
80*	TscH2doV, TscL2doV	SDO data output valid after SCK edge	_	_	50	ns	

These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Applicable Devices 61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67





TABLE 19-8: SPI MODE REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Typ†	Мах	Units	Conditions
70	TssL2scH, TssL2scL	$\overline{SS}\downarrow$ to SCK \downarrow or SCK \uparrow input	Тсү	_	l	ns	
71	TscH	SCK input high time (slave mode)	TCY + 20	_	_	ns	
72	TscL	SCK input low time (slave mode)	Tcy + 20	—		ns	
73	TdiV2scH, TdiV2scL	Setup time of SDI data input to SCK edge	50	_		ns	
74	TscH2diL, TscL2diL	Hold time of SDI data input to SCK edge	50	_		ns	
75	TdoR	SDO data output rise time	_	10	25	ns	
76	TdoF	SDO data output fall time		10	25	ns	
77	TssH2doZ	SS↑ to SDO output hi-impedance	10	—	50	ns	
78	TscR	SCK output rise time (master mode)		10	25	ns	
79	TscF	SCK output fall time (master mode)	_	10	25	ns	
80	TscH2doV, TscL2doV	SDO data output valid after SCK edge	_	_	50	ns	

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Applicable Devices 61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

20.3 DC Characteristics: PIC16C63/65A-04 (Commercial, Industrial, Extended) PIC16C63/65A-10 (Commercial, Industrial, Extended) PIC16C63/65A-20 (Commercial, Industrial, Extended) PIC16LC63/65A-04 (Commercial, Industrial)

		Standard Operating Conditions (unless otherwise stated)									
		$\label{eq:constraint} Operating \ temperature \qquad -40^{\circ}C \qquad \leq TA \leq +125^{\circ}C \ for \ extended,$									
	RACTERISTICS				-40°0	C ≤T	$A \le +85^{\circ}C$ for industrial and				
20 0114					0°C	≤T	$A \le +70^{\circ}C$ for commercial				
		Operatir	ng voltage	Vdd	range as o	describ	ed in DC spec Section 20.1 and				
		Section	20.2								
Param	Characteristic	Sym	Min	Тур	Max	Units	Conditions				
NO.				T							
	Input Low Voltage										
	I/O ports	VIL									
D030	with TTL buffer		Vss	-	0.15Vdd	V	For entire VDD range				
D030A			Vss	-	0.8V	V	$4.5V \le VDD \le 5.5V$				
D031	with Schmitt Trigger buffer		Vss	-	0.2Vdd	V					
D032	MCLR, OSC1 (in RC mode)		Vss	-	0.2Vdd	V					
D033	OSC1 (in XT, HS and LP)		Vss	-	0.3Vdd	V	Note1				
	Input High Voltage										
	I/O ports	VIH		-							
D040	with TTL buffer		2.0	-	VDD	V	$4.5V \le VDD \le 5.5V$				
D040A			0.25VDD	-	Vdd	V	For entire VDD range				
			+ 0.8V				-				
D041	with Schmitt Trigger buffer		0.8VDD	-	Vdd	V	For entire VDD range				
D042	MCLR		0.8VDD	-	Vdd	V					
D042A	OSC1 (XT, HS and LP)		0.7Vdd	-	Vdd	V	Note1				
D043	OSC1 (in RC mode)		0.9Vdd	-	Vdd	V					
D070	PORTB weak pull-up current	IPURB	50	250	400	μΑ	VDD = 5V, VPIN = VSS				
	Input Leakage Current (Notes 2, 3)										
D060	I/O ports	lı∟	-	-	±1	μA	Vss \leq VPIN \leq VDD, Pin at hi-				
						•	impedance				
D061	MCLR, RA4/T0CKI		-	-	±5	μA	$Vss \le VPIN \le VDD$				
D063	OSC1		-	-	±5	μA	Vss \leq VPIN \leq VDD, XT, HS and				
						•	LP osc configuration				
	Output Low Voltage						-				
D080	I/O ports	VOL	-	-	0.6	v	IOL = 8.5 mA, VDD = 4.5V,				
							-40°C to +85°C				
D080A			-	-	0.6	v	IOL = 7.0 mA, VDD = 4.5V,				
							-40°C to +125°C				
D083	OSC2/CLKOUT (RC osc config)		-	-	0.6	V	IOL = 1.6 mA, VDD = 4.5V,				
							-40°C to +85°C				
D083A			-	-	0.6	V	IOL = 1.2 mA, VDD = 4.5V,				
							-40°C to +125°C				

These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C6X be driven with external clock in RC mode.

 The leakage current on the MCLR/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as current sourced by the pin.

*

Applicable Devices	61	62	62A	B62	63	B63	64	64A	B64	65	65A	B65	66	67
Applicable Berliebe	•••	02	00,0	1102	00	1100	•••	0.0.1	1101	00	0071	1100	00	0.

		Standard Operating Conditions (unless otherwise stated)								
		Operating temperature $-40^{\circ}C \leq TA \leq +125^{\circ}C$ for extended,								
		$-40^{\circ}C \leq TA \leq +85^{\circ}C$ for industrial and								
DC CHA	RACTERISTICS				0°C	≤T	$A \le +70^{\circ}C$ for commercial			
		Operatir	ng voltage	VDD	range as o	describ	ed in DC spec Section 20.1 and			
		Section 20.2								
Param	Characteristic	Sym	Min	Тур	Max	Units	Conditions			
No.		-		†						
	Output High Voltage									
D090	I/O ports (Note 3)	Vон	VDD-0.7	-	-	V	IOH = -3.0 mA, VDD = 4.5V, -40°С to +85°С			
D090A			Vdd-0.7	-	-	V	IOH = -2.5 mA, VDD = 4.5V, -40°С to +125°С			
D092	OSC2/CLKOUT (RC osc config)		VDD-0.7	-	-	V	IOH = -1.3 mA, VDD = 4.5V, -40°С to +85°С			
D092A			VDD-0.7	-	-	V	IOH = -1.0 mA, VDD = 4.5V, -40°С to +125°С			
D150*	Open-Drain High Voltage	Vod	-	-	14	V	RA4 pin			
	Capacitive Loading Specs on Out- put Pins									
D100	OSC2 pin	Cosc2	-	-	15	pF	In XT, HS and LP modes when external clock is used to drive OSC1.			
D101	All I/O pins and OSC2 (in RC mode)	CIO	-	-	50	pF				
D102	SCL, SDA in I ² C mode	Cb	-	-	400	pF				

These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C6X be driven with external clock in RC mode.

 The leakage current on the MCLR/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as current sourced by the pin.

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21.0 ELECTRICAL CHARACTERISTICS FOR PIC16CR63/R65

Absolute Maximum Ratings (†)

Ambient temperature under bias	55°C to +125°C
Storage temperature	-65°C to +150°C
Voltage on any pin with respect to Vss (except VDD, MCLR, and RA4)	-0.3V to (VDD + 0.3V)
Voltage on VDD with respect to Vss	-0.3V to +7.5V
Voltage on MCLR with respect to Vss (Note 2)	
Voltage on RA4 with respect to Vss	
Total power dissipation (Note 1)	
Maximum current out of Vss pin	
Maximum current into VDD pin	
Input clamp current, Iк (VI < 0 or VI > VDD)	±20 mA
Output clamp current, loк (Vo < 0 or Vo > VDD)	±20 mA
Maximum output current sunk by any I/O pin	
Maximum output current sourced by any I/O pin	
Maximum current sunk by PORTA, PORTB, and PORTE (Note 3) (combined)	
Maximum current sourced by PORTA, PORTB, and PORTE (Note 3) (combined)	.p200 mA
Maximum current sunk by PORTC and PORTD (Note 3) (combined)	
Maximum current sourced by PORTC and PORTD (Note 3) (combined)	
	\mathbf{t} (\mathbf{A} (\mathbf{a}) \mathbf{A} (\mathbf{a}

- **Note 1:** Power dissipation is calculated as follows: Pdis = $VDx \{IDD \SigmaIOH\} + \Sigma (VDD VOH) \times IOH\} + \Sigma (VOI \times IOL)$
- Note 2: Voltage spikes below Vss at the MCLR/VPP pin, inducing currents greater than 80 mA, may cause latch-up. Thus, a series resistor of 50-100Ω should be used when applying a "fow" level to the MCLR/VPP pin rather than pulling this pin directly to Vss.
- Note 3: PORTD and PORTE not available on the P(C16CR63.

† NOTICE: Stresses above those listed under "Absolute Maximum Patings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 21-1: CROSS REFERENCE OF DEVICE SPECS FOR OSCILLATOR CONFIGURATIONS AND FREQUENCES OF OPERATION (COMMERCIAL DEVICES)

osc	PIC16CR63-04 PIC16CR65-04	PIC16CR63-10 PIC16CR65-10	PIC16CR63-20 PIC16CR65-20	PIC16LCR63-04 PIC16LCR65-04	JW Devices
RC	VDD: 4.0V to 5.5V IDD: 5 mA max. at 5.5V IPD: 16 μA max. at 4V Freq: 4 MHz max	VDD: 4.5V to 5.5V IDD: 2.7 mA typ. at 5.5V IRD: 1.5 µA typ. at 4V Freq: 4 MHz max.	VDD: 4.5V to 5.5V IDD: 2.7 mA typ. at 5.5V IPD: 1.5 μA typ. at 4V Freq: 4 MHz max.	VDD: 3.0V to 5.5V IDD: 3.8 mA max. at 3V IPD: 5 μA max. at 3V Freq: 4 MHz max.	VDD: 4.0V to 5.5V IDD: 5 mA max. at 5.5V IPD: 16 μA max. at 4V Freq: 4 MHz max.
ХТ	VDD: 4.0V to 5:5V IDD: 5 mA max. at 5.5V IPD: 16 hA max. at 4V Freq: 4 MHz max.	Vod: 4.5V to 5.5V IDD: 2.7 mA typ. at 5.5V IPD: 1.5 μA typ. at 4V Freq: 4 MHz max.	VDD: 4.5V to 5.5V IDD: 2.7 mA typ. at 5.5V IPD: 1.5 μA typ. at 4V Freq: 4 MHz max.	VDD: 3.0V to 5.5V IDD: 3.8 mA max. at 3V IPD: 5 μA max. at 3V Freq: 4 MHz max.	VDD: 4.0V to 5.5V IDD: 5 mA max. at 5.5V IPD: 16 μA max. at 4V Freq: 4 MHz max.
HS	VDD: 4.5V to 5.5V IDD: 13:5 mA typ. at 5.5V	VDD: 4.5V to 5.5V IDD: 10 mA max. at 5.5V	VDD: 4.5V to 5.5V IDD: 20 mA max. at 5.5V	Not recommended for use in HS mode	VDD: 4.5V to 5.5V IDD: 20 mA max. at 5.5V
	IPD: 1.5 μA typ. at 4.5V	IPD 1.5 μA typ. at 4.5V	IPD: 1.5 μA typ. at 4.5V		IPD: 1.5 μA typ. at 4.5V
LP	Preq. 4 Min2 IIIax. VDD: 4.0V to 5.5V IDD: 52.5 μA typ. at 32 kHz, 4.0V IPD: 0.9 μA typ. at 4.0V Freq: 200 kHz max.	Not recommended for use in LP mode	Not recommended for use in LP mode	VDD: 3.0V to 5.5V IDD: 48 μA max. at 32 kHz, 3.0V IPD: 5 μA max. at 3.0V Freq: 200 kHz max.	Preq. 20 Min2 fildx. VDD: 3.0V to 5.5V IDD: 48 μA max. at 32 kHz, 3.0V IPD: 5 μA max. at 3.0V Freq: 200 kHz max.

The shaded sections indicate oscillator selections which are tested for functionality, but not for MIN/MAX specifications. It is recommended that the user select the device type that ensures the specifications required.

Applicable Devices 61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

FIGURE 21-12: USART SYNCHRONOUS TRANSMISSION (MASTER/SLAVE) TIMING



TABLE 21-11: USART SYNCHRONOUS TRANSMISSION REQUIREMENTS

Param	Sym	Characteristic		Min	Тур†	Max	Units	Conditions
110.								
120*	TckH2dtV	SYNC XMIT (MASTER & SLAVE)	PIC16CR63/R65	_		80	ns	
		Clock high to data out valid	PIC16LCR63/R65	_	Ι	100	ns	
121*	Tckrf	Clock out rise time and fall time	PIC16CR63/R65	_	_	45	ns	
		(Master Mode)	PIC16LCR63/R65	_	Ι	50	ns	
122*	Tdtrf	Data out rise time and fall time	PIC16CR63/R65	_	Ι	45	ns	
			PIC16LCR63/R65	_	_	50	ns	

* These parameters are characterized but not tested.

†: Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 21-13: USART SYNCHRONOUS RECEIVE (MASTER/SLAVE) TIMING



TABLE 21-12: USART SYNCHRONOUS RECEIVE REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Тур†	Мах	Units	Conditions
125*	TdtV2ckL	SYNC RCV (MASTER & SLAVE) Data setup before CK \downarrow (DT setup time)	15		_	ns	
126*	TckL2dtl	Data hold after CK \downarrow (DT hold time)	15			ns	

These parameters are characterized but not tested.

†: Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

APPENDIX A: MODIFICATIONS

The following are the list of modifications over the PIC16C5X microcontroller family:

- Instruction word length is increased to 14-bits. This allows larger page sizes both in program memory (2K now as opposed to 512 before) and register file (128 bytes now versus 32 bytes before).
- 2. A PC high latch register (PCLATH) is added to handle program memory paging. PA2, PA1, PA0 bits are removed from STATUS register.
- 3. Data memory paging is redefined slightly. STA-TUS register is modified.
- Four new instructions have been added: RETURN, RETFIE, ADDLW, and SUBLW. Two instructions TRIS and OPTION are being phased out although they are kept for compatibility with PIC16C5X.
- 5. OPTION and TRIS registers are made addressable.
- 6. Interrupt capability is added. Interrupt vector is at 0004h.
- 7. Stack size is increased to 8 deep.
- 8. Reset vector is changed to 0000h.
- Reset of all registers is revisited. Five different reset (and wake-up) types are recognized. Registers are reset differently.
- 10. Wake-up from SLEEP through interrupt is added.
- 11. Two separate timers, Oscillator Start-up Timer (OST) and Power-up Timer (PWRT), are included for more reliable power-up. These timers are invoked selectively to avoid unnecessary delays on power-up and wake-up.
- 12. PORTB has weak pull-ups and interrupt on change feature.
- 13. Timer0 pin is also a port pin (RA4/T0CKI) now.
- 14. FSR is made a full 8-bit register.
- "In-circuit programming" is made possible. The user can program PIC16CXX devices using only five pins: VDD, VSS, VPP, RB6 (clock) and RB7 (data in/out).
- Power Control register (PCON) is added with a Power-on Reset status bit (POR).(Not on the PIC16C61).
- Brown-out Reset has been added to the following devices: PIC16C62A/R62/63/R63/64A/R64/65A/R65/66/ 67.

APPENDIX B: COMPATIBILITY

To convert code written for PIC16C5X to PIC16CXX, the user should take the following steps:

- Remove any program memory page select operations (PA2, PA1, PA0 bits) for CALL, GOTO.
- Revisit any computed jump operations (write to PC or add to PC, etc.) to make sure page bits are set properly under the new scheme.
- 3. Eliminate any data memory page switching. Redefine data variables to reallocate them.
- 4. Verify all writes to STATUS, OPTION, and FSR registers since these have changed.
- 5. Change reset vector to 0000h.

TXSTA

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