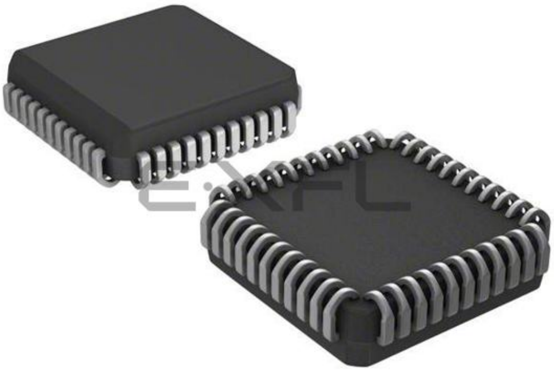
Microchip Technology - PIC16C64A-04E/L Datasheet



What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	I²C, SPI
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	33
Program Memory Size	3.5KB (2K x 14)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 6V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	44-PLCC (16.59x16.59)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16c64a-04e-l

TABLE 3-1: PIC16C61 PINOUT DESCRIPTION

Pin Name	DIP Pin#	SOIC Pin#	Pin Type	Buffer Type	Description
OSC1/CLKIN	16	16	I	ST/CMOS(1)	Oscillator crystal input/external clock source input.
OSC2/CLKOUT	15	15	O	—	Oscillator crystal output. Connects to crystal or resonator in crystal oscillator mode. In RC mode, the pin outputs CLKOUT which has 1/4 the frequency of OSC1, and denotes the instruction cycle rate.
$\overline{\text{MCLR}}$/VPP	4	4	I/P	ST	Master clear reset input or programming voltage input. This pin is an active low reset to the device.
					PORTA is a bi-directional I/O port.
RA0	17	17	I/O	TTL	
RA1	18	18	I/O	TTL	
RA2	1	1	I/O	TTL	
RA3	2	2	I/O	TTL	
RA4/T0CKI	3	3	I/O	ST	RA4 can also be the clock input to the Timer0 timer/counter. Output is open drain type.
					PORTB is a bi-directional I/O port. PORTB can be software programmed for internal weak pull-up on all inputs.
RB0/INT	6	6	I/O	TTL/ST(2)	RB0 can also be the external interrupt pin.
RB1	7	7	I/O	TTL	
RB2	8	8	I/O	TTL	
RB3	9	9	I/O	TTL	
RB4	10	10	I/O	TTL	Interrupt on change pin.
RB5	11	11	I/O	TTL	Interrupt on change pin.
RB6	12	12	I/O	TTL/ST(3)	Interrupt on change pin. Serial programming clock.
RB7	13	13	I/O	TTL/ST(3)	Interrupt on change pin. Serial programming data.
VSS	5	5	P	—	Ground reference for logic and I/O pins.
VDD	14	14	P	—	Positive supply for logic and I/O pins.

Legend: I = input O = output I/O = input/output P = power
— = Not used TTL = TTL input ST = Schmitt Trigger input

Note 1: This buffer is a Schmitt Trigger input when configured in RC oscillator mode and a CMOS input otherwise.
2: This buffer is a Schmitt Trigger input when configured as the external interrupt.
3: This buffer is a Schmitt Trigger input when used in serial programming mode.

FIGURE 7-3: TIMER0 TIMING: INTERNAL CLOCK/PRESCALE 1:2

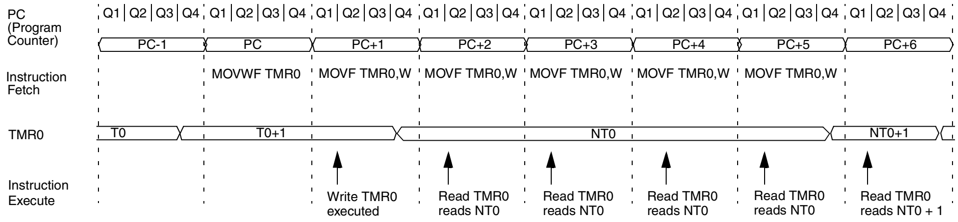
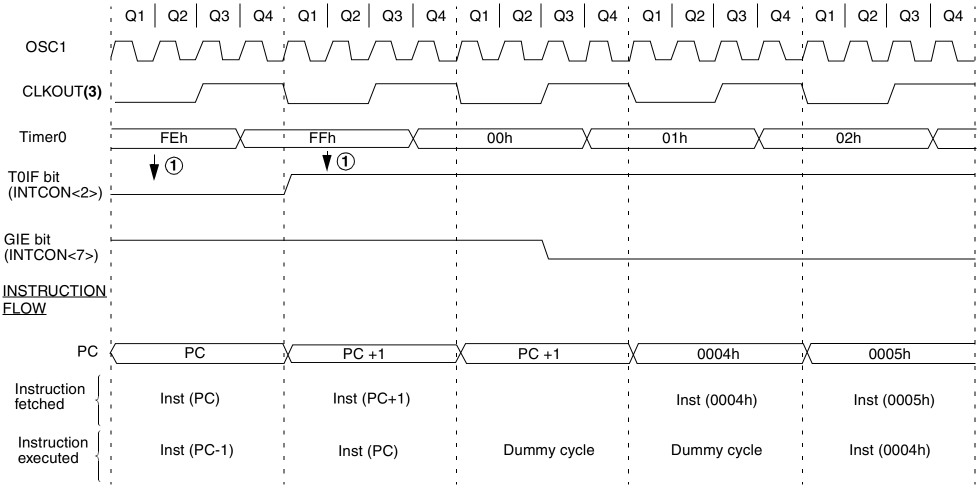


FIGURE 7-4: TMR0 INTERRUPT TIMING



Note 1: Interrupt flag bit T0IF is sampled here (every Q1).
2: Interrupt latency = 4Tcy where Tcy = instruction cycle time.
3: CLKOUT is available only in RC oscillator mode.

FIGURE 12-2: RCSTA: RECEIVE STATUS AND CONTROL REGISTER (ADDRESS 18h)

R/W-0	R/W-0	R/W-0	R/W-0	U-0	R-0	R-0	R-x
SPEN	RX9	SREN	CREN	—	FERR	OERR	RX9D
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as ‘0’
\- n = Value at POR reset
x = unknown

bit 7: **SPEN**: Serial Port Enable bit
(Configures RC7/RX/DT and RC6/TX/CK pins as serial port pins when bits TRISC<7:6> are set)
1 = Serial port enabled
0 = Serial port disabled

bit 6: **RX9**: 9-bit Receive Enable bit
1 = Selects 9-bit reception
0 = Selects 8-bit reception

bit 5: **SREN**: Single Receive Enable bit

<u>Asynchronous mode</u>
Don’t care

<u>Synchronous mode - master</u>
1 = Enables single receive
0 = Disables single receive
This bit is cleared after reception is complete.

<u>Synchronous mode - slave</u>
Unused in this mode

bit 4: **CREN**: Continuous Receive Enable bit

<u>Asynchronous mode</u>
1 = Enables continuous receive
0 = Disables continuous receive

<u>Synchronous mode</u>
1 = Enables continuous receive until enable bit CREN is cleared (CREN overrides SREN)
0 = Disables continuous receive

bit 3: **Unimplemented:** Read as '0'

bit 2: **FERR**: Framing Error bit
1 = Framing error (Can be updated by reading RCREG register and receive next valid byte)
0 = No framing error

bit 1: **OERR**: Overrun Error bit
1 = Overrun error (Can be cleared by clearing bit CREN)
0 = No overrun error

bit 0: **RX9D**: 9th bit of received data (Can be parity bit)

13.2 Oscillator Configurations

Applicable Devices													
61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67

13.2.1 OSCILLATOR TYPES

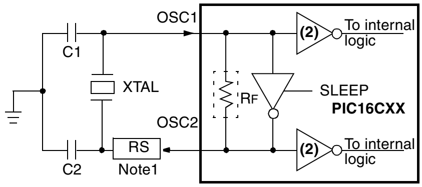
The PIC16CXX can be operated in four different oscillator modes. The user can program two configuration bits (FOSC1 and FOSC0) to select one of these four modes:

- LP Low Power Crystal
- XT Crystal/Resonator
- HS High Speed Crystal/Resonator
- RC Resistor/Capacitor

13.2.2 CRYSTAL OSCILLATOR/CERAMIC RESONATORS

In LP, XT, or HS modes a crystal or ceramic resonator is connected to the OSC1/CLKIN and OSC2/CLKOUT pins to establish oscillation (Figure 13-4). The PIC16CXX oscillator design requires the use of a parallel cut crystal. Use of a series cut crystal may give a frequency out of the crystal manufacturers specifications. When in LP, XT, or HS modes, the device can have an external clock source to drive the OSC1/CLKIN pin (Figure 13-5).

FIGURE 13-4: CRYSTAL/CERAMIC RESONATOR OPERATION (HS, XT OR LP OSC CONFIGURATION)

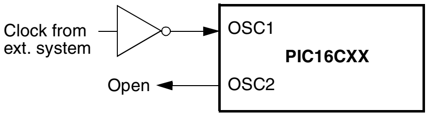


See Table 13-1, Table 13-3, Table 13-2 and Table 13-4 for recommended values of C1 and C2.

Note 1: A series resistor may be required for AT strip cut crystals.

2: For the PIC16C61 the buffer is on the OSC2 pin, all other devices have the buffer on the OSC1 pin.

FIGURE 13-5: EXTERNAL CLOCK INPUT OPERATION (HS, XT OR LP OSC CONFIGURATION)



13.3 Reset

Applicable Devices															
61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67		

The PIC16CXX differentiates between various kinds of reset:

- Power-on Reset (POR)
- $\overline{\text{MCLR}}$ reset during normal operation
- $\overline{\text{MCLR}}$ reset during SLEEP
- WDT Reset (normal operation)
- Brown-out Reset (BOR) - Not on PIC16C61/62/64/65

Some registers are not affected in any reset condition, their status is unknown on POR and unchanged in any other reset. Most other registers are reset to a “reset state” on Power-on Reset (POR), on $\overline{\text{MCLR}}$ or WDT Reset, on $\overline{\text{MCLR}}$ reset during SLEEP, and on Brown-out Reset (BOR). They are not affected by a WDT Wake-up, which is viewed as the resumption of normal operation.

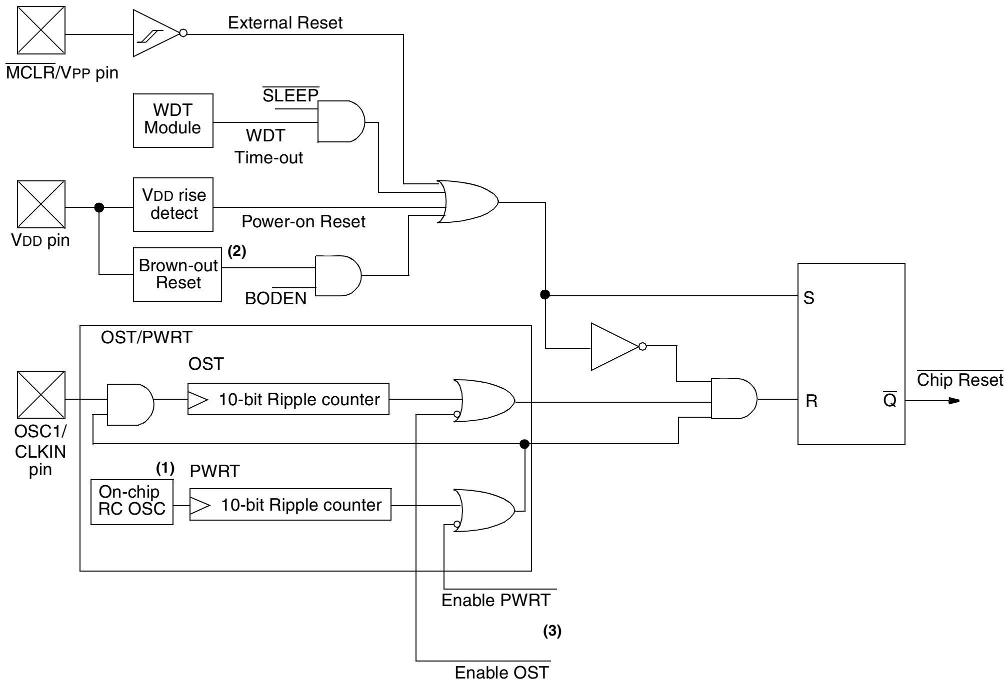
The $\overline{\text{TO}}$ and $\overline{\text{PD}}$ bits are set or cleared differently in different reset situations as indicated in Table 13-7, Table 13-8, and Table 13-9. These bits are used in software to determine the nature of the reset. See Table 13-12 for a full description of reset states of all registers.

A simplified block diagram of the on-chip reset circuit is shown in Figure 13-9.

On the PIC16C62A/R62/63/R63/64A/R64/65A/R65/66/67, the $\overline{\text{MCLR}}$ reset path has a noise filter to detect and ignore small pulses. See parameter #34 for pulse width specifications.

It should be noted that a WDT Reset does not drive the $\overline{\text{MCLR}}$ pin low.

FIGURE 13-9: SIMPLIFIED BLOCK DIAGRAM OF ON-CHIP RESET CIRCUIT



Note 1: This is a separate oscillator from the RC oscillator of the CLKIN pin.
2: Brown-out Reset is NOT implemented on the PIC16C61/62/64/65.
3: See Table 13-5 and Table 13-6 for time-out situations.

TABLE 13-12: INITIALIZATION CONDITIONS FOR ALL REGISTERS

Register	Applicable Devices														Power-on Reset Brown-out Reset	$\overline{\text{MCLR}}$ Reset during: – normal operation – SLEEP WDT Reset	Wake-up via interrupt or WDT Wake-up
W	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67	`xxxx xxxx`	`uuuu uuuu`	`uuuu uuuu`
INDF	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67	N/A	N/A	N/A
TMR0	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67	`xxxx xxxx`	`uuuu uuuu`	`uuuu uuuu`
PCL	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67	`0000h`	`0000h`	`PC + 1`(2)
STATUS	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67	`0001 1xxx`	`000q quuu`(3)	`uuuq quuu`(3)
FSR	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67	`xxxx xxxx`	`uuuu uuuu`	`uuuu uuuu`
PORTA	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67	`---x xxxx`	`---u uuuu`	`---u uuuu`
	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67	`--xx xxxx`	`--uu uuuu`	`--uu uuuu`
PORTB	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67	`xxxx xxxx`	`uuuu uuuu`	`uuuu uuuu`
PORTC	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67	`xxxx xxxx`	`uuuu uuuu`	`uuuu uuuu`
PORTD	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67	`xxxx xxxx`	`uuuu uuuu`	`uuuu uuuu`
PORTE	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67	`---- -xxx`	`---- -uuu`	`---- -uuu`
PCLATH	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67	`---0 0000`	`---0 0000`	`---u uuuu`
INTCON	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67	`0000 000x`	`0000 000u`	`uuuu uuuu`(1)
PIR1	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67	`00-- 0000`	`00-- 0000`	`uu-- uuuu`(1)
	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67	`0000 0000`	`0000 0000`	`uuuu uuuu`(1)
PIR2	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67	`---- ---0`	`---- ---0`	`---- ---u`(2)
TMR1L	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67	`xxxx xxxx`	`uuuu uuuu`	`uuuu uuuu`
TMR1H	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67	`xxxx xxxx`	`uuuu uuuu`	`uuuu uuuu`
T1CON	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67	`--00 0000`	`--uu uuuu`	`--uu uuuu`
TMR2	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67	`0000 0000`	`0000 0000`	`uuuu uuuu`
T2CON	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67	`-000 0000`	`-000 0000`	`-uuu uuuu`
SSPBUF	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67	`xxxx xxxx`	`uuuu uuuu`	`uuuu uuuu`
SSPCON	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67	`0000 0000`	`0000 0000`	`uuuu uuuu`
CCPR1L	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67	`xxxx xxxx`	`uuuu uuuu`	`uuuu uuuu`
CCPR1H	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67	`xxxx xxxx`	`uuuu uuuu`	`uuuu uuuu`
CCP1CON	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67	`--00 0000`	`--00 0000`	`--uu uuuu`
RCSTA	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67	`0000 -00x`	`0000 -00x`	`uuuu -uuu`
TXREG	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67	`0000 0000`	`0000 0000`	`uuuu uuuu`
RCREG	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67	`0000 0000`	`0000 0000`	`uuuu uuuu`
CCPR2L	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67	`xxxx xxxx`	`uuuu uuuu`	`uuuu uuuu`
CCPR2H	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67	`xxxx xxxx`	`uuuu uuuu`	`uuuu uuuu`
CCP2CON	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67	`0000 0000`	`0000 0000`	`uuuu uuuu`
OPTION	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67	`1111 1111`	`1111 1111`	`uuuu uuuu`
TRISA	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67	`---1 1111`	`---1 1111`	`---u uuuu`
	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67	`--11 1111`	`--11 1111`	`--uu uuuu`
TRISB	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67	`1111 1111`	`1111 1111`	`uuuu uuuu`
TRISC	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67	`1111 1111`	`1111 1111`	`uuuu uuuu`

Legend: `u` = unchanged, `x` = unknown, `-` = unimplemented bit read as '0', q = value depends on condition.

Note 1: One or more bits in INTCON, PIR1 and/or PIR2 will be affected (to cause wake-up).

2: When the wake-up is due to an interrupt and the global enable bit, GIE is set, the PC is loaded with the interrupt vector (0004h) after execution of PC + 1.

3: See Table 13-10 and Table 13-11 for reset value for specific conditions.

FIGURE 13-11: TIME-OUT SEQUENCE ON POWER-UP ($\overline{\text{MCLR}}$ NOT TIED TO VDD): CASE 1

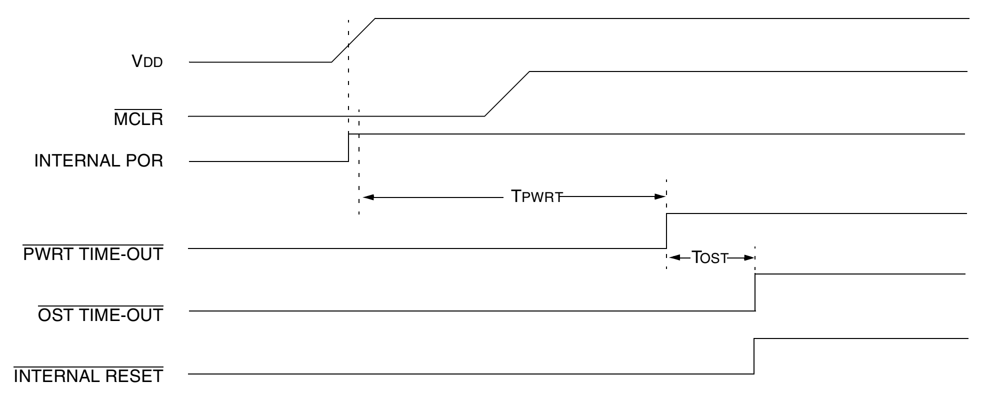


FIGURE 13-12: TIME-OUT SEQUENCE ON POWER-UP ($\overline{\text{MCLR}}$ NOT TIED TO VDD): CASE 2

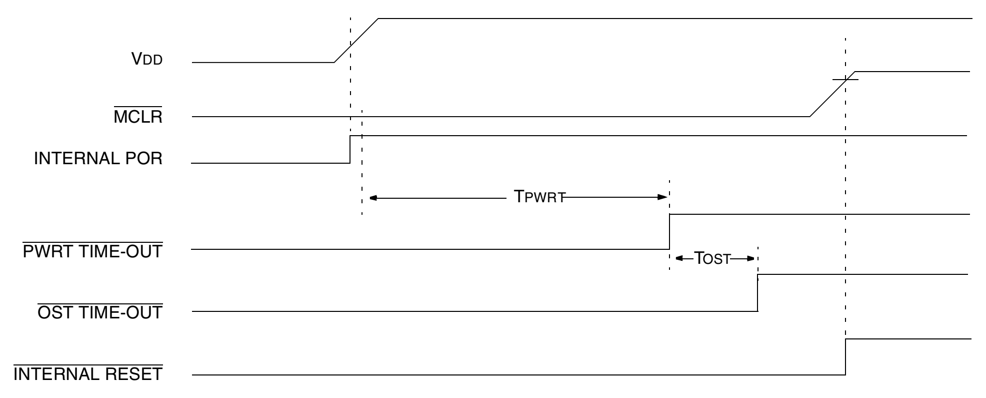
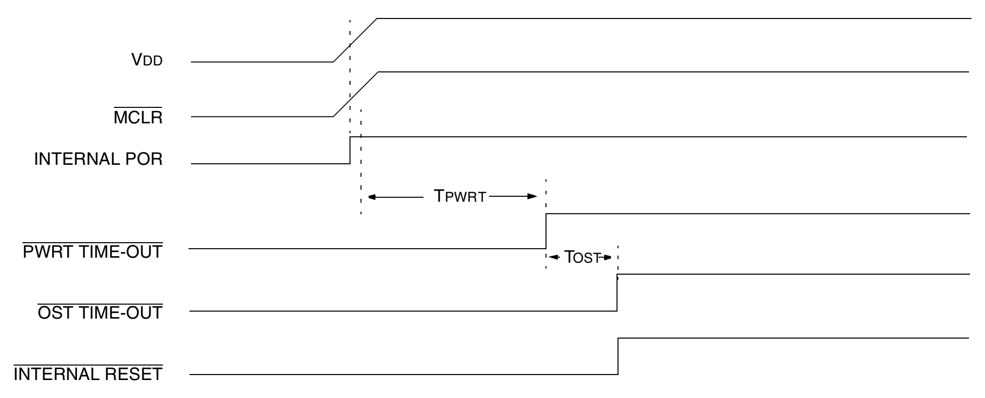


FIGURE 13-13: TIME-OUT SEQUENCE ON POWER-UP ($\overline{\text{MCLR}}$ TIED TO VDD)



Applicable Devices	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67

NOTES:

Applicable Devices	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67

17.4 Timing Parameter Symbology

The timing parameter symbols have been created following one of the following formats:

1. TppS2ppS	3. TCC:ST	(I^2C specifications only)
2. TppS	4. Ts	(I^2C specifications only)

T			
F	Frequency	T	Time

Lowercase letters (pp) and their meanings:

pp			
cc	CCP1	osc	OSC1
ck	CLKOUT	rd	$\overline{\text{RD}}$
cs	$\overline{\text{CS}}$	rw	$\overline{\text{RD}}$ or $\overline{\text{WR}}$
di	SDI	sc	SCK
do	SDO	ss	$\overline{\text{SS}}$
dt	Data in	t0	T0CKI
io	I/O port	t1	T1CKI
mc	$\overline{\text{MCLR}}$	wr	$\overline{\text{WR}}$

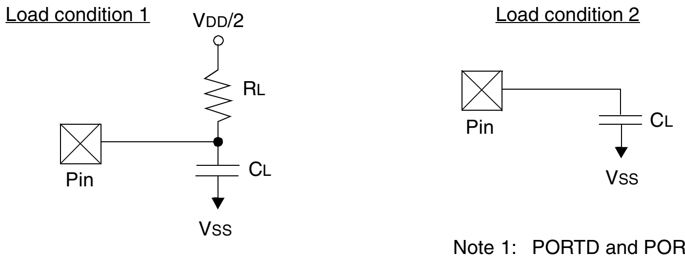
Uppercase letters and their meanings:

S			
F	Fall	P	Period
H	High	R	Rise
I	Invalid (Hi-impedance)	V	Valid
L	Low	Z	Hi-impedance
I^2C only			
AA	output access	High	High
BUF	Bus free	Low	Low

TCC:ST (I^2C specifications only)

CC			
HD	Hold	SU	Setup
ST			
DAT	DATA input hold	STO	STOP condition
STA	START condition		

FIGURE 17-1: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS



RL = 464Ω

CL = 50 pF for all pins except OSC2/CLKOUT but including D and E outputs as ports

15 pF for OSC2 output

Note 1: PORTD and PORTE are not implemented on the PIC16C62.

Applicable Devices	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67

17.5 Timing Diagrams and Specifications

FIGURE 17-2: EXTERNAL CLOCK TIMING

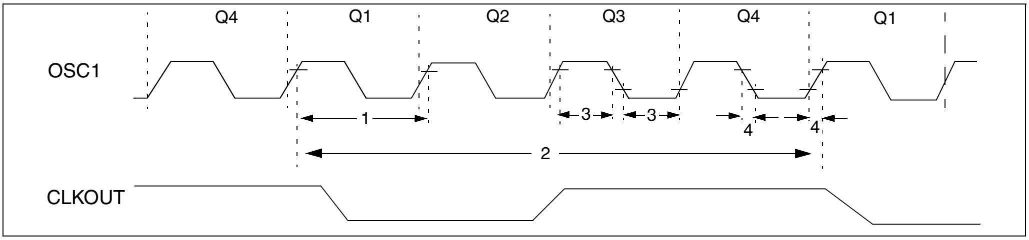


TABLE 17-2: EXTERNAL CLOCK TIMING REQUIREMENTS

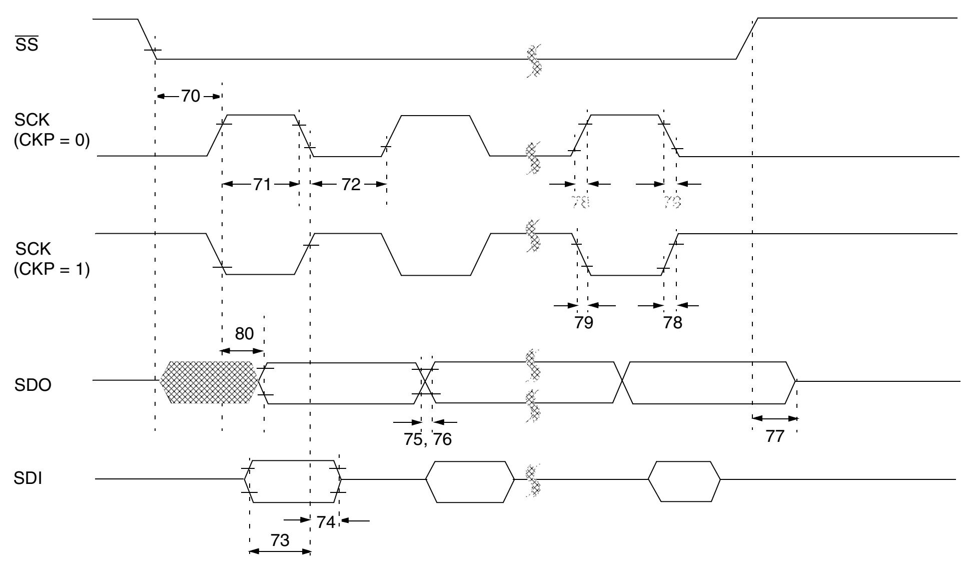
Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
	Fosc	**External CLKIN Frequency (Note 1)**	DC	—	4	MHz	XT and RC osc mode
			DC	—	4	MHz	HS osc mode (-04)
			DC	—	10	MHz	HS osc mode (-10)
			DC	—	20	MHz	HS osc mode (-20)
			DC	—	200	kHz	LP osc mode
		Oscillator Frequency (Note 1)	DC	—	4	MHz	RC osc mode
			0.1	—	4	MHz	XT osc mode
			4	—	20	MHz	HS osc mode
			5	—	200	kHz	LP osc mode
1	Tosc	**External CLKIN Period (Note 1)**	250	—	—	ns	XT and RC osc mode
			250	—	—	ns	HS osc mode (-04)
			100	—	—	ns	HS osc mode (-10)
			50	—	—	ns	HS osc mode (-20)
			5	—	—	µs	LP osc mode
		Oscillator Period (Note 1)	250	—	—	ns	RC osc mode
			250	—	10,000	ns	XT osc mode
			250	—	250	ns	HS osc mode (-04)
			100	—	250	ns	HS osc mode (-10)
			50	—	1,000	ns	HS osc mode (-20)
			5	—	—	µs	LP osc mode
2	TCY	**Instruction Cycle Time (Note 1)**	200	TCY	DC	ns	TCY = 4/FOSC
3	TosL, TosH	**External Clock in (OSC1) High or Low Time**	100	—	—	ns	XT oscillator
			2.5	—	—	µs	LP oscillator
			15	—	—	ns	HS oscillator
4	TosR, TosF	**External Clock in (OSC1) Rise or Fall Time**	—	—	25	ns	XT oscillator
			—	—	50	ns	LP oscillator
			—	—	15	ns	HS oscillator

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Instruction cycle period (TCY) equals four times the input oscillator time-base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min." values with an external clock applied to the OSC1/CLKIN pin. When an external clock input is used, the "Max." cycle time limit is "DC" (no clock) for all devices.

Applicable Devices	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67

FIGURE 18-9: SPI MODE TIMING



Note: Refer to Figure 18-1 for load conditions

TABLE 18-8: SPI MODE REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
70*	TssL2scH, TssL2scL	$\overline{\text{SS}}$↓ to SCK↓ or SCK↑ input	TCY	—	—	ns	
71*	TscH	SCK input high time (slave mode)	TCY + 20	—	—	ns	
72*	TscL	SCK input low time (slave mode)	TCY + 20	—	—	ns	
73*	TdiV2scH, TdiV2scL	Setup time of SDI data input to SCK edge	50	—	—	ns	
74*	TscH2diL, TscL2diL	Hold time of SDI data input to SCK edge	50	—	—	ns	
75*	TdoR	SDO data output rise time	—	10	25	ns	
76*	TdoF	SDO data output fall time	—	10	25	ns	
77*	TssH2doZ	$\overline{\text{SS}}$↑ to SDO output hi-impedance	10	—	50	ns	
78*	TscR	SCK output rise time (master mode)	—	10	25	ns	
79*	TscF	SCK output fall time (master mode)	—	10	25	ns	
80*	TscH2doV, TscL2doV	SDO data output valid after SCK edge	—	—	50	ns	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Applicable Devices	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67

FIGURE 19-11: USART SYNCHRONOUS TRANSMISSION (MASTER/SLAVE) TIMING

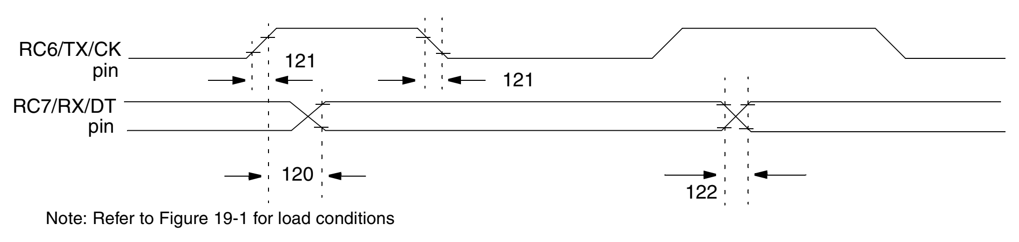


TABLE 19-11: USART SYNCHRONOUS TRANSMISSION REQUIREMENTS

Parameter No.	Sym	Characteristic		Min	Typ†	Max	Units	Conditions
120	TckH2dtV	SYNC XMIT (MASTER & SLAVE) Clock high to data out valid	PIC16**C**65	—	—	80	ns	
			PIC16**LC**65	—	—	100	ns	
121	Tckrf	Clock out rise time and fall time (Master Mode)	PIC16**C**65	—	—	45	ns	
			PIC16**LC**65	—	—	50	ns	
122	Tdtrf	Data out rise time and fall time	PIC16**C**65	—	—	45	ns	
			PIC16**LC**65	—	—	50	ns	

†: Data in “Typ” column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 19-12: USART SYNCHRONOUS RECEIVE (MASTER/SLAVE) TIMING

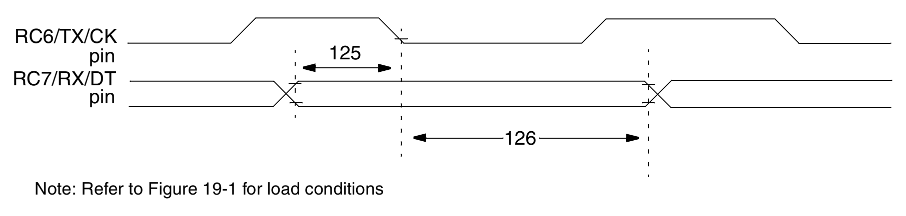


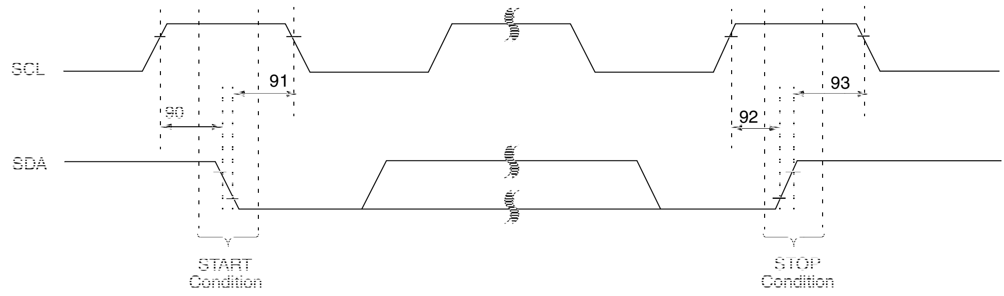
TABLE 19-12: USART SYNCHRONOUS RECEIVE REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
125	TdtV2ckL	SYNC RCV (MASTER & SLAVE) Data setup before CK ↓ (DT setup time)	15	—	—	ns	
126	TckL2dtl	Data hold after CK ↓ (DT hold time)	15	—	—	ns	

†: Data in “Typ” column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Applicable Devices	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67

FIGURE 20-10: I^{2}C BUS START/STOP BITS TIMING



Note: Refer to Figure 20-1 for load conditions

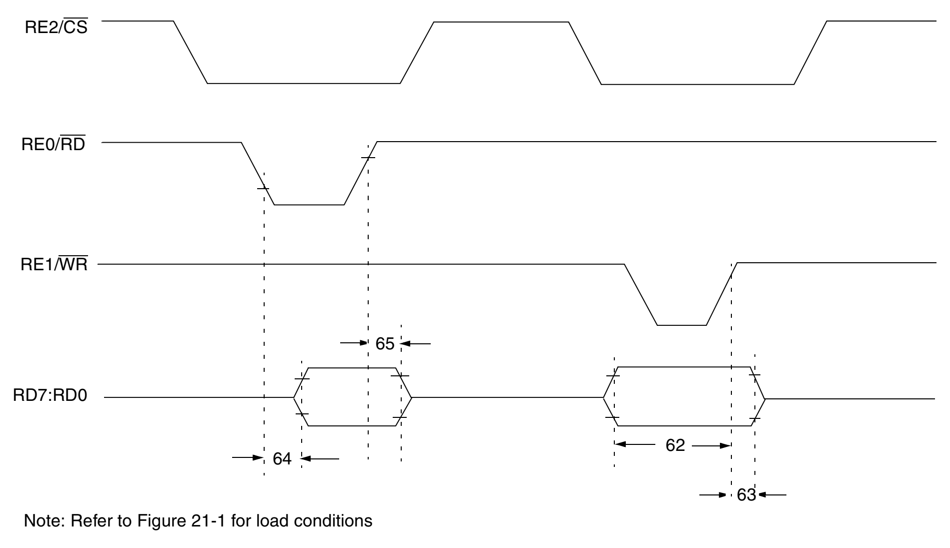
TABLE 20-9: I^{2}C BUS START/STOP BITS REQUIREMENTS

Parameter No.	Sym	Characteristic		Min	Typ	Max	Units	Conditions
90*	TSU:STA	START condition	100 kHz mode	4700	—	—	ns	Only relevant for repeated START condition
		Setup time	400 kHz mode	600	—	—		
91*	THD:STA	START condition	100 kHz mode	4000	—	—	ns	After this period the first clock pulse is generated
		Hold time	400 kHz mode	600	—	—		
92*	TSU:STO	STOP condition	100 kHz mode	4700	—	—	ns	
		Setup time	400 kHz mode	600	—	—		
93	THD:STO	STOP condition	100 kHz mode	4000	—	—	ns	
		Hold time	400 kHz mode	600	—	—		

* These parameters are characterized but not tested.

Applicable Devices	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67

FIGURE 21-8: PARALLEL SLAVE PORT TIMING (PIC16CR65)



Note: Refer to Figure 21-1 for load conditions

TABLE 21-7: PARALLEL SLAVE PORT REQUIREMENTS (PIC16CR65)

Parameter No.	Sym	Characteristic		Min	Typ†	Max	Units	Conditions
62*	TdtV2wrH	Data in valid before $\overline{\text{WR}}$↑ or $\overline{\text{CS}}$↑ (setup time)		20	—	—	ns	
63*	TwrH2dtI	$\overline{\text{WR}}$↑ or $\overline{\text{CS}}$↑ to data–in invalid (hold time)	PIC16**CR**65	20	—	—	ns	
			PIC16**LCR**65	35	—	—	ns	
64	TrdL2dtV	$\overline{\text{RD}}$↓ and $\overline{\text{CS}}$↓ to data–out valid		—	—	80	ns	
65*	TrdH2dtI	$\overline{\text{RD}}$↑ or $\overline{\text{CS}}$↑ to data–out invalid		10	—	30	ns	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Applicable Devices	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67

DC CHARACTERISTICS	**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ T_A ≤ +125°C for extended, -40°C ≤ T_A ≤ +85°C for industrial and 0°C ≤ T_A ≤ +70°C for commercial Operating voltage V_{DD} range as described in DC spec Section 22.1 and Section 22.2						
Param No.	**Characteristic**	**Sym**	**Min**	**Typ †**	**Max**	**Units**	**Conditions**
	Output High Voltage						
D090	I/O ports (Note 3)	V_{OH}	V_{DD}-0.7	-	-	V	I_{OH} = -3.0 mA, V_{DD} = 4.5V, -40°C to +85°C
D090A			V_{DD}-0.7	-	-	V	I_{OH} = -2.5 mA, V_{DD} = 4.5V, -40°C to +125°C
D092	OSC2/CLKOUT (RC osc config)		V_{DD}-0.7	-	-	V	I_{OH} = -1.3 mA, V_{DD} = 4.5V, -40°C to +85°C
D092A			V_{DD}-0.7	-	-	V	I_{OH} = -1.0 mA, V_{DD} = 4.5V, -40°C to +125°C
D150*	**Open-Drain High Voltage**	V_{OD}	-	-	14	V	RA4 pin
	Capacitive Loading Specs on Output Pins						
D100	OSC2 pin	C_{OSC2}	-	-	15	pF	In XT, HS and LP modes when external clock is used to drive OSC1.
D101	All I/O pins and OSC2 (in RC mode)	C_{IO}	-	-	50	pF	
D102	SCL, SDA in I^2C mode	Cb	-	-	400	pF	

* These parameters are characterized but not tested.

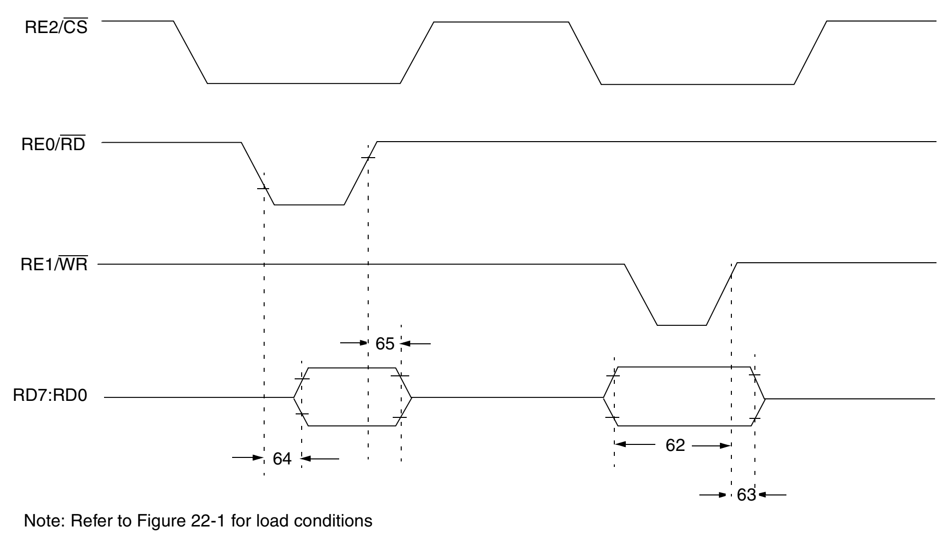
† Data in “Typ” column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C6X be driven with external clock in RC mode.

2: The leakage current on the $\overline{MCLR}$/V_{PP} pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as current sourced by the pin.

FIGURE 22-8: PARALLEL SLAVE PORT TIMING (PIC16C67)



Note: Refer to Figure 22-1 for load conditions

TABLE 22-7: PARALLEL SLAVE PORT REQUIREMENTS (PIC16C67)

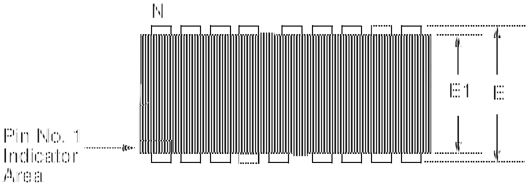
Parameter No.	Sym	Characteristic		Min	Typ†	Max	Units	Conditions
62*	TdtV2wrH	Data in valid before $\overline{\text{WR}}\uparrow$ or $\overline{\text{CS}}\uparrow$ (setup time)		20 25	— —	— —	ns ns	 Extended Range Only
63*	TwrH2dtI	$\overline{\text{WR}}\uparrow$ or $\overline{\text{CS}}\uparrow$ to data–in invalid (hold time)	PIC16**C**67	20	—	—	ns	
			PIC16**LC**67	35	—	—	ns	
64	TrdL2dtV	$\overline{\text{RD}}\downarrow$ and $\overline{\text{CS}}\downarrow$ to data–out valid		— —	— —	80 90	ns ns	 Extended Range Only
65*	TrdH2dtI	$\overline{\text{RD}}\uparrow$ or $\overline{\text{CS}}\uparrow$ to data–out invalid		10	—	30	ns	

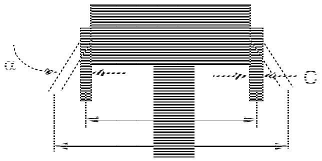
* These parameters are characterized but not tested.

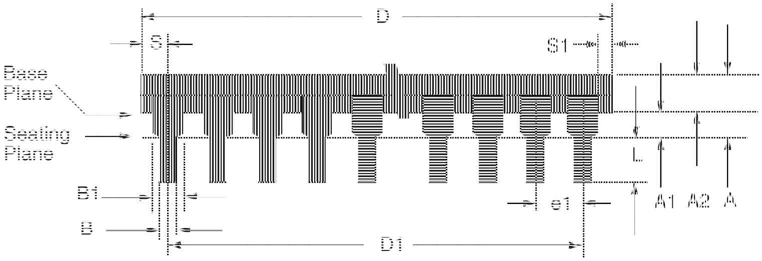
† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

24.3 40-Lead Plastic Dual In-line (600 mil) (P)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



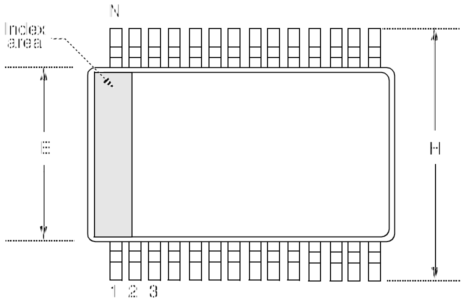


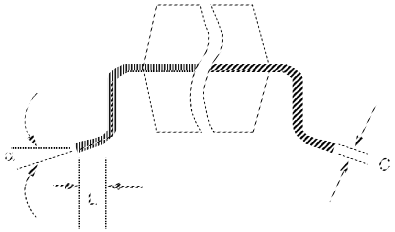


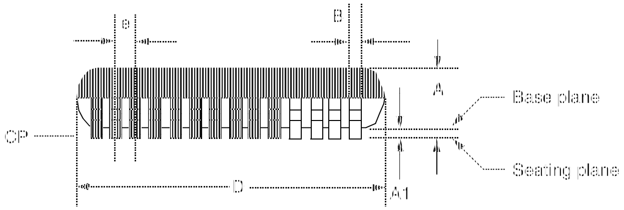
Package Group: Plastic Dual In-Line (PLA)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	–	5.080		–	0.200	
A1	0.381	–		0.015	–	
A2	3.175	4.064		0.125	0.160	
B	0.355	0.559		0.014	0.022	
B1	1.270	1.778	**Typical**	0.050	0.070	**Typical**
C	0.203	0.381	**Typical**	0.008	0.015	**Typical**
D	51.181	52.197		2.015	2.055	
D1	48.260	48.260	**Reference**	1.900	1.900	**Reference**
E	15.240	15.875		0.600	0.625	
E1	13.462	13.970		0.530	0.550	
e1	2.489	2.591	**Typical**	0.098	0.102	**Typical**
eA	15.240	15.240	**Reference**	0.600	0.600	**Reference**
eB	15.240	17.272		0.600	0.680	
L	2.921	3.683		0.115	0.145	
N	40	40		40	40	
S	1.270	–		0.050	–	
S1	0.508	–		0.020	–	

24.10 28-Lead Plastic Surface Mount (SSOP - 209 mil Body 5.30 mm) (SS)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging







Package Group: Plastic SSOP						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	8°		0°	8°	
A	1.730	1.990		0.068	0.078	
A1	0.050	0.210		0.002	0.008	
B	0.250	0.380		0.010	0.015	
C	0.130	0.220		0.005	0.009	
D	10.070	10.330		0.396	0.407	
E	5.200	5.380		0.205	0.212	
e	0.650	0.650	**Reference**	0.026	0.026	**Reference**
H	7.650	7.900		0.301	0.311	
L	0.550	0.950		0.022	0.037	
N	28	28		28	28	
CP	-	0.102		-	0.004	

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