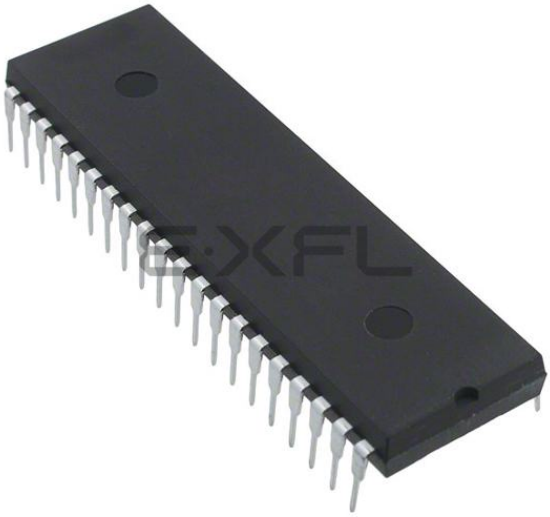

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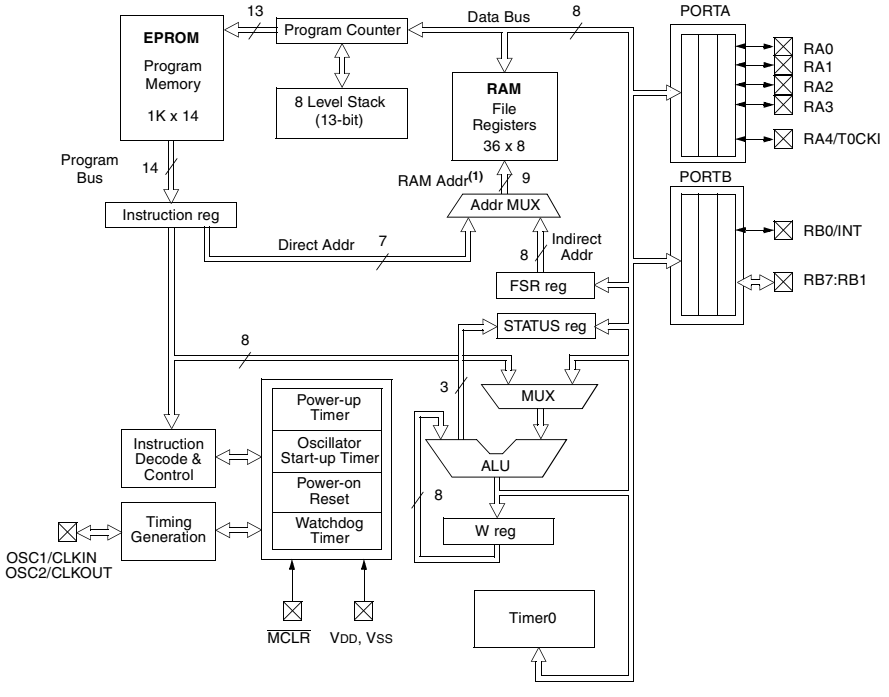
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	I²C, SPI
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	33
Program Memory Size	3.5KB (2K x 14)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 6V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	40-DIP (0.600", 15.24mm)
Supplier Device Package	40-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16c64a-04i-p

FIGURE 3-1: PIC16C61 BLOCK DIAGRAM



Note 1: Higher order bits are from the STATUS register.

TABLE 3-1: PIC16C61 PINOUT DESCRIPTION

Pin Name	DIP Pin#	SOIC Pin#	Pin Type	Buffer Type	Description
OSC1/CLKIN	16	16	I	ST/CMOS(1)	Oscillator crystal input/external clock source input.
OSC2/CLKOUT	15	15	O	—	Oscillator crystal output. Connects to crystal or resonator in crystal oscillator mode. In RC mode, the pin outputs CLKOUT which has 1/4 the frequency of OSC1, and denotes the instruction cycle rate.
$\overline{MCLR}$/VPP	4	4	I/P	ST	Master clear reset input or programming voltage input. This pin is an active low reset to the device.
					PORTA is a bi-directional I/O port.
RA0	17	17	I/O	TTL	
RA1	18	18	I/O	TTL	
RA2	1	1	I/O	TTL	
RA3	2	2	I/O	TTL	
RA4/T0CKI	3	3	I/O	ST	RA4 can also be the clock input to the Timer0 timer/counter. Output is open drain type.
					PORTB is a bi-directional I/O port. PORTB can be software programmed for internal weak pull-up on all inputs.
RB0/INT	6	6	I/O	TTL/ST(2)	RB0 can also be the external interrupt pin.
RB1	7	7	I/O	TTL	
RB2	8	8	I/O	TTL	
RB3	9	9	I/O	TTL	
RB4	10	10	I/O	TTL	Interrupt on change pin.
RB5	11	11	I/O	TTL	Interrupt on change pin.
RB6	12	12	I/O	TTL/ST(3)	Interrupt on change pin. Serial programming clock.
RB7	13	13	I/O	TTL/ST(3)	Interrupt on change pin. Serial programming data.
VSS	5	5	P	—	Ground reference for logic and I/O pins.
VDD	14	14	P	—	Positive supply for logic and I/O pins.

Legend: I = input O = output I/O = input/output P = power
— = Not used TTL = TTL input ST = Schmitt Trigger input

Note 1: This buffer is a Schmitt Trigger input when configured in RC oscillator mode and a CMOS input otherwise.
2: This buffer is a Schmitt Trigger input when configured as the external interrupt.
3: This buffer is a Schmitt Trigger input when used in serial programming mode.

4.2.2.5 PIR1 REGISTER

Applicable Devices												
61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67

This register contains the individual flag bits for the peripheral interrupts.

Note: Interrupt flag bits get set when an interrupt condition occurs regardless of the state of its corresponding enable bit or the global enable bit, GIE (INTCON<7>). User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

FIGURE 4-16: PIR1 REGISTER FOR PIC16C62/62A/R62 (ADDRESS 0Ch)

R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	—	SSPIF	CCP1IF	TMR2IF	TMR1IF
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n = Value at POR reset

bit 7-6: **Reserved**: Always maintain these bits clear.

bit 5-4: **Unimplemented**: Read as '0'

bit 3: **SSPIF**: Synchronous Serial Port Interrupt Flag bit
1 = The transmission/reception is complete (must be cleared in software)
0 = Waiting to transmit/receive

bit 2: **CCP1IF**: CCP1 Interrupt Flag bit
Capture Mode
1 = A TMR1 register capture occurred (must be cleared in software)
0 = No TMR1 register capture occurred
Compare Mode
1 = A TMR1 register compare match occurred (must be cleared in software)
0 = No TMR1 register compare match occurred
PWM Mode
Unused in this mode

bit 1: **TMR2IF**: TMR2 to PR2 Match Interrupt Flag bit
1 = TMR2 to PR2 match occurred (must be cleared in software)
0 = No TMR2 to PR2 match occurred

bit 0: **TMR1IF**: TMR1 Overflow Interrupt Flag bit
1 = TMR1 register overflow occurred (must be cleared in software)
0 = No TMR1 register overflow occurred

Interrupt flag bits get set when an interrupt condition occurs regardless of the state of its corresponding enable bit or the global enable bit, GIE (INTCON<7>). User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

5.0 I/O PORTS

Applicable Devices													
61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67

Some pins for these I/O ports are multiplexed with an alternate function(s) for the peripheral features on the device. In general, when a peripheral is enabled, that pin may not be used as a general purpose I/O pin.

5.1 PORTA and TRISA Register

Applicable Devices													
61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67

All devices have a 6-bit wide PORTA, except for the PIC16C61 which has a 5-bit wide PORTA.

Pin RA4/T0CKI is a Schmitt Trigger input and an open drain output. All other RA port pins have TTL input levels and full CMOS output drivers. All pins have data direction bits (TRIS registers) which can configure these pins as output or input.

Setting a bit in the TRISA register puts the corresponding output driver in a hi-impedance mode. Clearing a bit in the TRISA register puts the contents of the output latch on the selected pin.

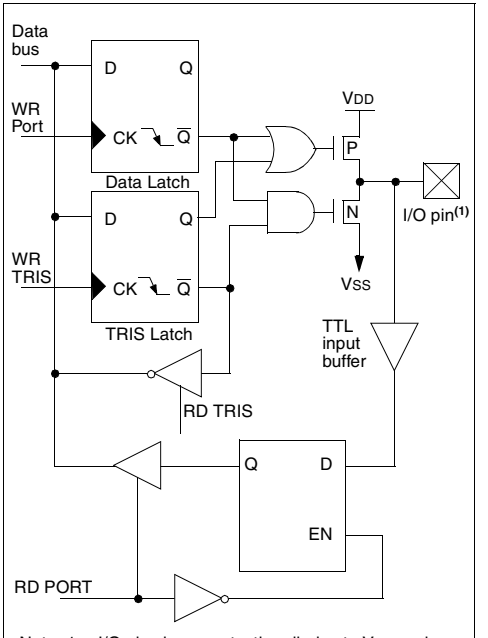
Reading PORTA register reads the status of the pins whereas writing to it will write to the port latch. All write operations are read-modify-write operations. Therefore, a write to a port implies that the port pins are read, this value is modified, and then written to the port data latch.

Pin RA4 is multiplexed with Timer0 module clock input to become the RA4/T0CKI pin.

EXAMPLE 5-1: INITIALIZING PORTA

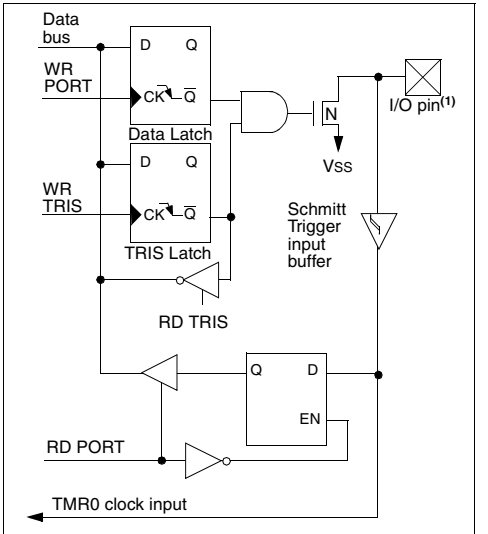
```
BCF     STATUS, RP0  ;
BCF     STATUS, RP1  ; PIC16C66/67 only
CLRF    PORTA        ; Initialize PORTA by
                     ; clearing output
                     ; data latches
BSF     STATUS, RP0  ; Select Bank 1
MOVLW   0xCF         ; Value used to
                     ; initialize data
                     ; direction
MOVWF   TRISA        ; Set RA<3:0> as inputs
                     ; RA<5:4> as outputs
                     ; TRISA<7:6> are always
                     ; read as '0'.
```

FIGURE 5-1: BLOCK DIAGRAM OF THE RA3:RA0 PINS AND THE RA5 PIN



Note 1: I/O pins have protection diodes to VDD and VSS.
2: The PIC16C61 does not have an RA5 pin.

FIGURE 5-2: BLOCK DIAGRAM OF THE RA4/T0CKI PIN



Note 1: I/O pin has protection diodes to VSS only.

5.3 PORTC and TRISC Register

Applicable Devices													
61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67

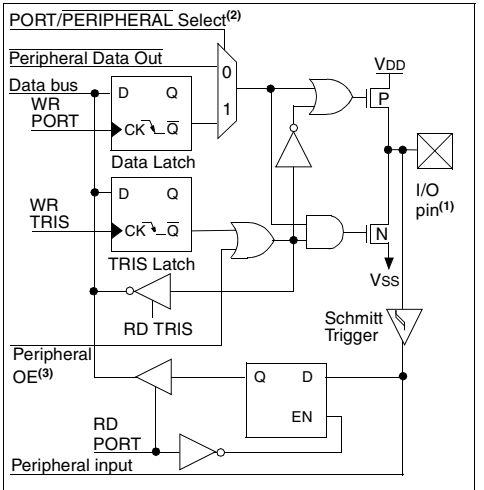
PORTC is an 8-bit wide bi-directional port. Each pin is individually configurable as an input or output through the TRISC register. PORTC is multiplexed with several peripheral functions (Table 5-5). PORTC pins have Schmitt Trigger input buffers.

When enabling peripheral functions, care should be taken in defining TRIS bits for each PORTC pin. Some peripherals override the TRIS bit to make a pin an output, while other peripherals override the TRIS bit to make a pin an input. Since the TRIS bit override is in effect while the peripheral is enabled, read-modify-write instructions (`BSF, BCF, XORWF`) with TRISC as destination should be avoided. The user should refer to the corresponding peripheral section for the correct TRIS bit settings.

EXAMPLE 5-3: INITIALIZING PORTC

```
BCF     STATUS, RP0   ;
BCF     STATUS, RP1   ; PIC16C66/67 only
CLRF    PORTC         ; Initialize PORTC by
                      ; clearing output
                      ; data latches
BSF     STATUS, RP0   ; Select Bank 1
MOVLW   0xCF          ; Value used to
                      ; initialize data
                      ; direction
MOVWF   TRISC         ; Set RC<3:0> as inputs
                      ; RC<5:4> as outputs
                      ; RC<7:6> as inputs
```

FIGURE 5-6: PORTC BLOCK DIAGRAM



Note 1: I/O pins have diode protection to VDD and VSS.
2: Port/Peripheral select signal selects between port data and peripheral output.
3: Peripheral OE (output enable) is only activated if peripheral select is active.

TABLE 5-5: PORTC FUNCTIONS FOR PIC16C62/64

Name	Bit#	Buffer Type	Function
RC0/T1OSI/T1CKI	bit0	ST	Input/output port pin or Timer1 oscillator input or Timer1 clock input
RC1/T1OSO	bit1	ST	Input/output port pin or Timer1 oscillator output
RC2/CCP1	bit2	ST	Input/output port pin or Capture1 input/Compare1 output/PWM1 output
RC3/SCK/SCL	bit3	ST	RC3 can also be the synchronous serial clock for both SPI and I^2C modes.
RC4/SDI/SDA	bit4	ST	RC4 can also be the SPI Data In (SPI mode) or data I/O (I^2C mode).
RC5/SDO	bit5	ST	Input/output port pin or synchronous serial port data output
RC6	bit6	ST	Input/output port pin
RC7	bit7	ST	Input/output port pin

Legend: ST = Schmitt Trigger input

TABLE 10-5: REGISTERS ASSOCIATED WITH PWM AND TIMER2

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets
0Bh,8Bh 10Bh,18Bh	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000u
0Ch	PIR1	PSPIF(2)	(3)	RCIF(1)	TXIF(1)	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
0Dh(4)	PIR2	—	—	—	—	—	—	—	CCP2IF	---- --- 0	---- --- 0
8Ch	PIE1	PSPIE(2)	(3)	RCIE(1)	TXIE(1)	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
8Dh(4)	PIE2	—	—	—	—	—	—	—	CCP2IE	---- --- 0	---- --- 0
87h	TRISC	PORTC Data Direction register								1111 1111	1111 1111
11h	TMR2	Timer2 module's register								0000 0000	0000 0000
92h	PR2	Timer2 module's Period register								1111 1111	1111 1111
12h	T2CON	—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000 0000	-000 0000
15h	CCPR1L	Capture/Compare/PWM1 (LSB)								xxxx xxxx	uuuu uuuu
16h	CCPR1H	Capture/Compare/PWM1 (MSB)								xxxx xxxx	uuuu uuuu
17h	CCP1CON	—	—	CCP1X	CCP1Y	CCP1M3	CCP1M2	CCP1M1	CCP1M0	--00 0000	--00 0000
1Bh(4)	CCPR2L	Capture/Compare/PWM2 (LSB)								xxxx xxxx	uuuu uuuu
1Ch(4)	CCPR2H	Capture/Compare/PWM2 (MSB)								xxxx xxxx	uuuu uuuu
1Dh(4)	CCP2CON	—	—	CCP2X	CCP2Y	CCP2M3	CCP2M2	CCP2M1	CCP2M0	--00 0000	--00 0000

Legend: x = unknown, u = unchanged, - = unimplemented locations read as '0'. Shaded cells are not used in this mode.

Note 1: These bits are associated with the USART module, which is implemented on the PIC16C63/R63/65/65A/R65/66/67 only.

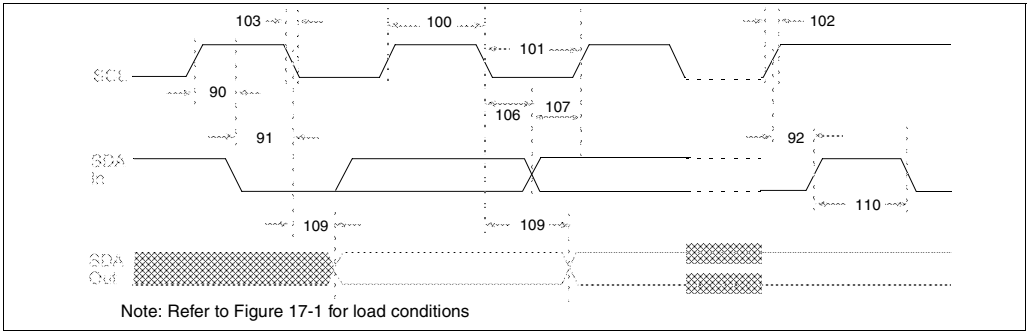
2: Bits PSPIE and PSPIF are reserved on the PIC16C62/62A/R62/63/R63/66, always maintain these bits clear.

3: The PIR1<6> and PIE1<6> bits are reserved, always maintain these bits clear.

4: These registers are associated with the CCP2 module, which is only implemented on the PIC16C63/R63/65/65A/R65/66/67.

Applicable Devices	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67

FIGURE 17-10: I^2C BUS DATA TIMING



Note: Refer to Figure 17-1 for load conditions

TABLE 17-10: I^2C BUS DATA REQUIREMENTS

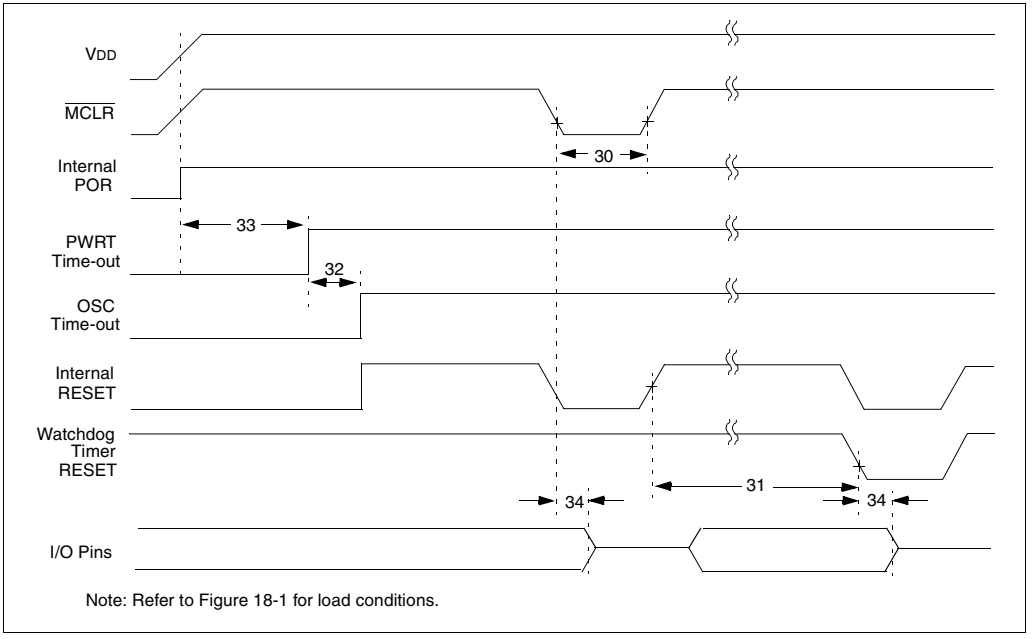
Parameter No.	Sym	Characteristic		Min	Max	Units	Conditions
100	THIGH	Clock high time	100 kHz mode	4.0	—	μs	Device must operate at a minimum of 1.5 MHz
			400 kHz mode	0.6	—	μs	Device must operate at a minimum of 10 MHz
			SSP Module	1.5TCY	—		
101	TLOW	Clock low time	100 kHz mode	4.7	—	μs	Device must operate at a minimum of 1.5 MHz
			400 kHz mode	1.3	—	μs	Device must operate at a minimum of 10 MHz
			SSP Module	1.5TCY	—		
102	TR	SDA and SCL rise time	100 kHz mode	—	1000	ns	
			400 kHz mode	20 + 0.1Cb	300	ns	Cb is specified to be from 10 to 400 pF
103	TF	SDA and SCL fall time	100 kHz mode	—	300	ns	
			400 kHz mode	20 + 0.1Cb	300	ns	Cb is specified to be from 10 to 400 pF
90	TSU:STA	START condition setup time	100 kHz mode	4.7	—	μs	Only relevant for repeated START condition
			400 kHz mode	0.6	—	μs	
91	THD:STA	START condition hold time	100 kHz mode	4.0	—	μs	After this period the first clock pulse is generated
			400 kHz mode	0.6	—	μs	
106	THD:DAT	Data input hold time	100 kHz mode	0	—	ns	
			400 kHz mode	0	0.9	μs	
107	TSU:DAT	Data input setup time	100 kHz mode	250	—	ns	Note 2
			400 kHz mode	100	—	ns	
92	TSU:STO	STOP condition setup time	100 kHz mode	4.7	—	μs	
			400 kHz mode	0.6	—	μs	
109	TAA	Output valid from clock	100 kHz mode	—	3500	ns	Note 1
			400 kHz mode	—	—	ns	
110	TBUF	Bus free time	100 kHz mode	4.7	—	μs	Time the bus must be free before a new transmission can start
			400 kHz mode	1.3	—	μs	
	Cb	Bus capacitive loading		—	400	pF	

Note 1: As a transmitter, the device must provide this internal minimum delay time to bridge the undefined region (min. 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

2: A fast-mode (400 kHz) I^2C-bus device can be used in a standard-mode (100 kHz) I^2C-bus system, but the requirement tsu;DAT ≥ 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line TR max. + tsu;DAT = 1000 + 250 = 1250 ns (according to the standard-mode I^2C bus specification) before the SCL line is released.

Applicable Devices	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67

FIGURE 18-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING



Note: Refer to Figure 18-1 for load conditions.

FIGURE 18-5: BROWN-OUT RESET TIMING

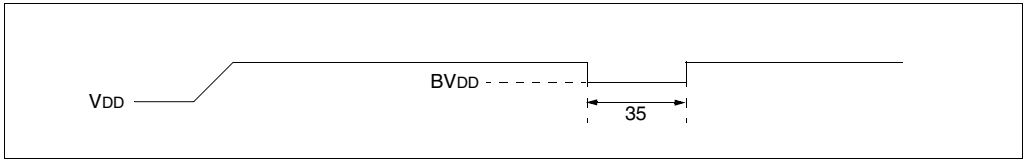


TABLE 18-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, POWER-UP TIMER, AND BROWN-OUT RESET REQUIREMENTS

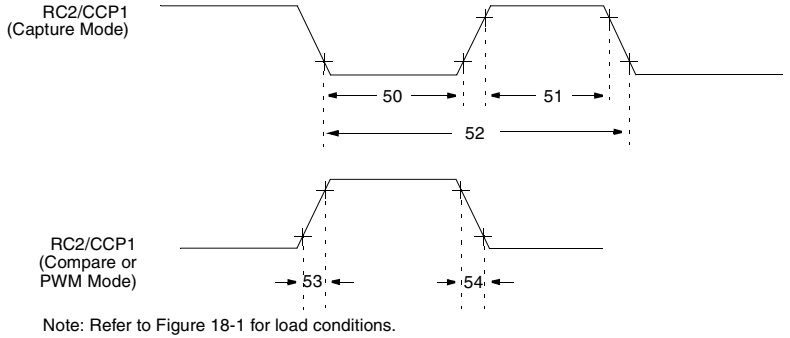
Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
30	TmcL	MCLR Pulse Width (low)	2	—	—	µs	VDD = 5V, -40°C to +125°C
31*	Twdt	Watchdog Timer Time-out Period (No Prescaler)	7	18	33	ms	VDD = 5V, -40°C to +125°C
32	Tost	Oscillation Start-up Timer Period	—	1024TOSC	—	—	TOSC = OSC1 period
33*	Tpwrt	Power-up Timer Period	28	72	132	ms	VDD = 5V, -40°C to +125°C
34	TIOZ	I/O Hi-impedance from MCLR Low or WDT Reset	—	—	2.1	µs	
35	TBOR	Brown-out Reset Pulse Width	100	—	—	µs	VDD ≤ BVDD (param. D005)

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Applicable Devices	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67

FIGURE 18-7: CAPTURE/COMPARE/PWM TIMINGS (CCP1)



Note: Refer to Figure 18-1 for load conditions.

TABLE 18-6: CAPTURE/COMPARE/PWM REQUIREMENTS (CCP1)

Parameter No.	Sym	Characteristic			Min	Typ†	Max	Units	Conditions
50*	TccL	CCP1 input low time	No Prescaler		0.5TCY + 20	—	—	ns	
			With Prescaler	PIC16**C**62A/R62/64A/R64	10	—	—	ns	
				PIC16**LC**62A/R62/64A/R64	20	—	—	ns	
51*	TccH	CCP1 input high time	No Prescaler		0.5TCY + 20	—	—	ns	
			With Prescaler	PIC16**C**62A/R62/64A/R64	10	—	—	ns	
				PIC16**LC**62A/R62/64A/R64	20	—	—	ns	
52*	TccP	CCP1 input period			$\frac{3T_{CY} + 40}{N}$	—	—	ns	N = prescale value (1,4 or 16)
53*	TccR	CCP1 output rise time		PIC16**C**62A/R62/64A/R64	—	10	25	ns	
				PIC16**LC**62A/R62/64A/R64	—	25	45	ns	
54*	TccF	CCP1 output fall time		PIC16**C**62A/R62/64A/R64	—	10	25	ns	
				PIC16**LC**62A/R62/64A/R64	—	25	45	ns	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Applicable Devices	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67

19.3 DC Characteristics: PIC16C65-04 (Commercial, Industrial)
PIC16C65-10 (Commercial, Industrial)
PIC16C65-20 (Commercial, Industrial)
PIC16LC65-04 (Commercial, Industrial)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial and 0°C ≤ TA ≤ +70°C for commercial Operating voltage VDD range as described in DC spec Section 19.1 and Section 19.2				
Param No.	**Characteristic**	**Sym**	**Min**	**Typ †**	**Max**	**Units**	**Conditions**
	Input Low Voltage						
	I/O ports	VIL					
D030	with TTL buffer		VSS	-	0.15VDD	V	For entire VDD range
D030A			VSS	-	0.8V	V	4.5V ≤ VDD ≤ 5.5V
D031	with Schmitt Trigger buffer		VSS	-	0.2VDD	V	
D032	$\overline{MCLR}$, OSC1(in RC mode)		Vss	-	0.2VDD	V	
D033	OSC1 (in XT, HS and LP)		Vss	-	0.3VDD	V	Note1
	Input High Voltage						
	I/O ports	VIH		-			
D040	with TTL buffer		2.0	-	VDD	V	4.5V ≤ VDD ≤ 5.5V
D040A			0.25VDD + 0.8V	-	VDD	V	For entire VDD range
D041	with Schmitt Trigger buffer		0.8VDD	-	VDD		For entire VDD range
D042	$\overline{MCLR}$		0.8VDD	-	VDD	V	
D042A	OSC1 (XT, HS and LP)		0.7 VDD	-	VDD	V	Note1
D043	OSC1 (in RC mode)		0.9VDD	-	VDD	V	
D070	PORTB weak pull-up current	IPURB	50	250	400	µA	VDD = 5V, VPIN = VSS
	Input Leakage Current (Notes 2, 3)						
D060	I/O ports	IIL	-	-	±1	µA	Vss ≤ VPIN ≤ VDD, Pin at hi-impedance
D061	$\overline{MCLR}$, RA4/T0CKI		-	-	±5	µA	Vss ≤ VPIN ≤ VDD
D063	OSC1		-	-	±5	µA	Vss ≤ VPIN ≤ VDD, XT, HS, and LP osc configuration
	Output Low Voltage						
D080	I/O ports	VOL	-	-	0.6	V	IOL = 8.5 mA, VDD = 4.5V, -40°C to +85°C
D083	OSC2/CLKOUT (RC osc config)		-	-	0.6	V	IOL = 1.6 mA, VDD = 4.5V, -40°C to +85°C
	Output High Voltage						
D090	I/O ports (Note 3)	VOH	VDD-0.7	-	-	V	IOH = -3.0 mA, VDD = 4.5V, -40°C to +85°C
D092	OSC2/CLKOUT (RC osc config)		VDD-0.7	-	-	V	IOH = -1.3 mA, VDD = 4.5V, -40°C to +85°C
D150*	**Open-Drain High Voltage**	VOD	-	-	14	V	RA4 pin

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C6X be driven with external clock in RC mode.

2: The leakage current on the $\overline{MCLR}$/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as current sourced by the pin.

Applicable Devices	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67

20.3 DC Characteristics: PIC16C63/65A-04 (Commercial, Industrial, Extended) PIC16C63/65A-10 (Commercial, Industrial, Extended) PIC16C63/65A-20 (Commercial, Industrial, Extended) PIC16LC63/65A-04 (Commercial, Industrial)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +125°C for extended, -40°C ≤ TA ≤ +85°C for industrial and 0°C ≤ TA ≤ +70°C for commercial Operating voltage VDD range as described in DC spec Section 20.1 and Section 20.2				
Param No.	**Characteristic**	**Sym**	**Min**	**Typ †**	**Max**	**Units**	**Conditions**
	Input Low Voltage						
	I/O ports	VIL					
D030	with TTL buffer		VSS	-	0.15VDD	V	For entire VDD range
D030A			VSS	-	0.8V	V	4.5V ≤ VDD ≤ 5.5V
D031	with Schmitt Trigger buffer		VSS	-	0.2VDD	V	
D032	$\overline{MCLR}$, OSC1 (in RC mode)		Vss	-	0.2VDD	V	
D033	OSC1 (in XT, HS and LP)		Vss	-	0.3VDD	V	Note1
	Input High Voltage						
	I/O ports	VIH		-			
D040	with TTL buffer		2.0	-	VDD	V	4.5V ≤ VDD ≤ 5.5V
D040A			0.25VDD + 0.8V	-	VDD	V	For entire VDD range
D041	with Schmitt Trigger buffer		0.8VDD	-	VDD	V	For entire VDD range
D042	$\overline{MCLR}$		0.8VDD	-	VDD	V	
D042A	OSC1 (XT, HS and LP)		0.7VDD	-	VDD	V	Note1
D043	OSC1 (in RC mode)		0.9VDD	-	VDD	V	
D070	PORTB weak pull-up current	IPURB	50	250	400	µA	VDD = 5V, VPIN = VSS
	Input Leakage Current (Notes 2, 3)						
D060	I/O ports	IIL	-	-	±1	µA	Vss ≤ VPIN ≤ VDD, Pin at hi-impedance
D061	$\overline{MCLR}$, RA4/T0CKI		-	-	±5	µA	Vss ≤ VPIN ≤ VDD
D063	OSC1		-	-	±5	µA	Vss ≤ VPIN ≤ VDD, XT, HS and LP osc configuration
	Output Low Voltage						
D080	I/O ports	VOL	-	-	0.6	V	IOL = 8.5 mA, VDD = 4.5V, -40°C to +85°C
D080A			-	-	0.6	V	IOL = 7.0 mA, VDD = 4.5V, -40°C to +125°C
D083	OSC2/CLKOUT (RC osc config)		-	-	0.6	V	IOL = 1.6 mA, VDD = 4.5V, -40°C to +85°C
D083A			-	-	0.6	V	IOL = 1.2 mA, VDD = 4.5V, -40°C to +125°C

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

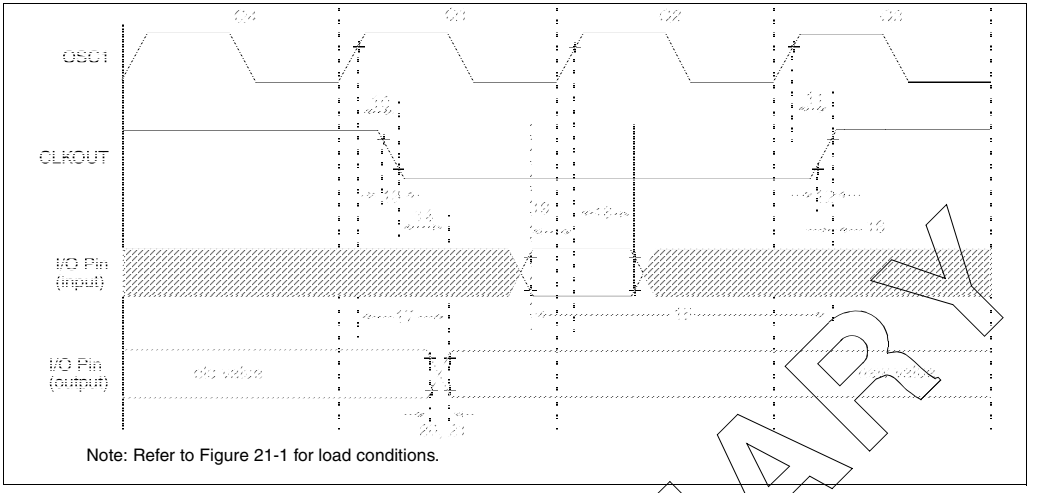
Note 1: In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C6X be driven with external clock in RC mode.

2: The leakage current on the $\overline{MCLR}$/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as current sourced by the pin.

Applicable Devices	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67

FIGURE 21-3: CLKOUT AND I/O TIMING



Note: Refer to Figure 21-1 for load conditions.

TABLE 21-3: CLKOUT AND I/O TIMING REQUIREMENTS

Param No.	Sym	Characteristic		Min	Typ†	Max	Units	Conditions
10*	TosH2ckL	OSC1↑ to CLKOUT↓		—	75	200	ns	Note 1
11*	TosH2ckH	OSC1↑ to CLKOUT↑		—	75	200	ns	Note 1
12*	TckR	CLKOUT rise time		—	35	100	ns	Note 1
13*	TckF	CLKOUT fall time		—	35	100	ns	Note 1
14*	TckL2ioV	CLKOUT ↓ to Port out valid		—	—	0.5TCY + 20	ns	Note 1
15*	TioV2ckH	Port in valid before CLKOUT ↑		Tosc + 200	—	—	ns	Note 1
16*	TckH2ioI	Port in hold after CLKOUT ↑		0	—	—	ns	Note 1
17*	TosH2ioV	OSC1↑ (Q1 cycle) to Port out valid		—	50	150	ns	
18*	TosH2ioI	OSC1↑ (Q2 cycle) to Port input invalid (I/O in hold time)	PIC16**CR**63/R65	100	—	—	ns	
			PIC16**LCR**63/R65	200	—	—	ns	
19*	TioV2osH	Port input valid to OSC1↑ (I/O in setup time)		0	—	—	ns	
20*	TioR	Port output rise time	PIC16**CR**63/R65	—	10	40	ns	
			PIC16**LCR**63/R65	—	—	80	ns	
21*	TioF	Port output fall time	PIC16**CR**63/R65	—	10	40	ns	
			PIC16**LCR**63/R65	—	—	80	ns	
22††*	Tinp	INT pin high or low time		TCY	—	—	ns	
23††*	Trbp	RB7:RB4 change INT high or low time		TCY	—	—	ns	

* These parameters are characterized but not tested.

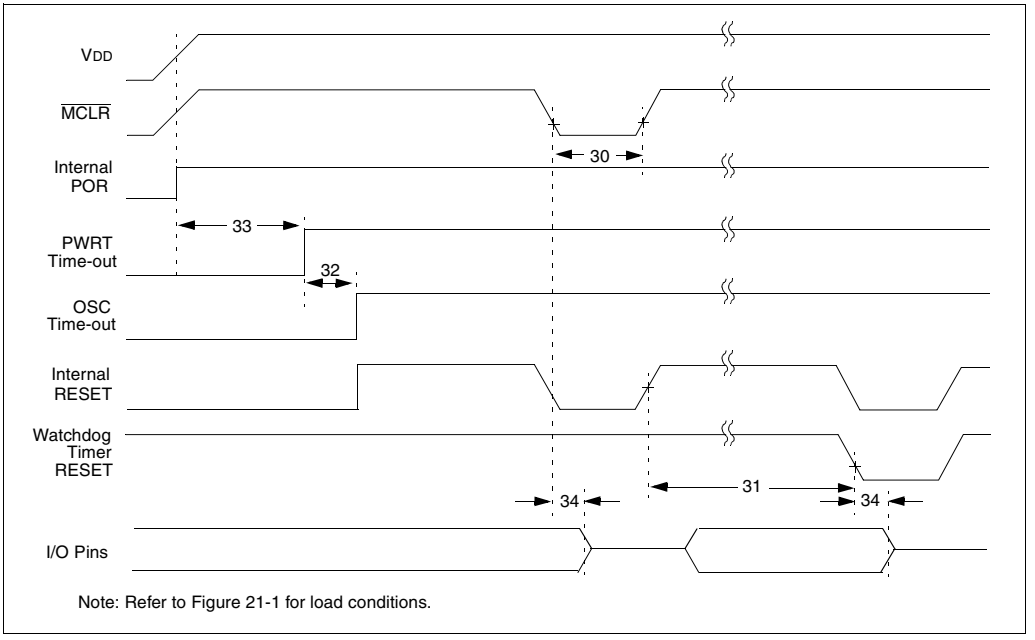
† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

†† These parameters are asynchronous events not related to any internal clock edge.

Note 1: Measurements are taken in RC Mode where CLKOUT output is 4 x TOSC.

Applicable Devices	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67

FIGURE 21-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING



Note: Refer to Figure 21-1 for load conditions.

FIGURE 21-5: BROWN-OUT RESET TIMING

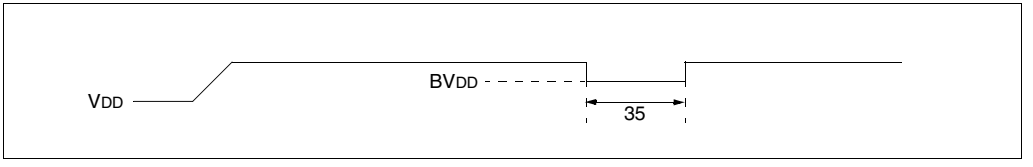


TABLE 21-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, POWER-UP TIMER, AND BROWN-OUT RESET REQUIREMENTS

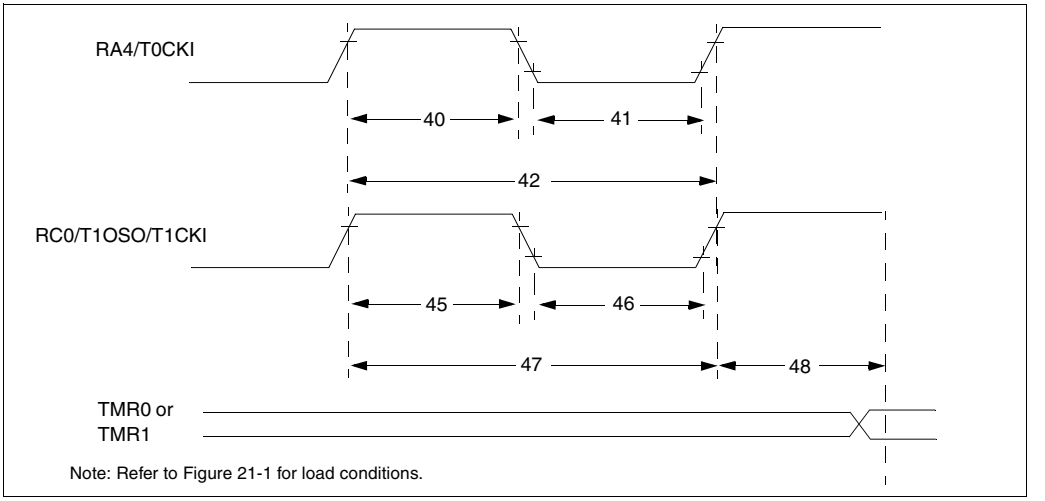
Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
30	TmcL	$\overline{MCLR}$ Pulse Width (low)	2	—	—	µs	VDD = 5V, -40°C to +125°C
31*	Twdt	Watchdog Timer Time-out Period (No Prescaler)	7	18	33	ms	VDD = 5V, -40°C to +125°C
32	Tost	Oscillation Start-up Timer Period	—	1024 TOSC	—	—	TOSC = OSC1 period
33*	Tpwrt	Power-up Timer Period	28	72	132	ms	VDD = 5V, -40°C to +125°C
34	TIOZ	I/O Hi-impedance from $\overline{MCLR}$ Low or WDT reset	—	—	2.1	µs	
35	TBOR	Brown-out Reset Pulse Width	100	—	—	µs	VDD ≤ BVDD (D005)

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Applicable Devices	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67

FIGURE 21-6: TIMER0 AND TIMER1 EXTERNAL CLOCK TIMINGS



Note: Refer to Figure 21-1 for load conditions.

TABLE 21-5: TIMER0 AND TIMER1 EXTERNAL CLOCK REQUIREMENTS

Param No.	Sym	Characteristic			Min	Typ†	Max	Units	Conditions
40*	Tt0H	T0CKI High Pulse Width		No Prescaler	0.5TCY + 20	—	—	ns	Must also meet parameter 42
				With Prescaler	10	—	—	ns	
41*	Tt0L	T0CKI Low Pulse Width		No Prescaler	0.5TCY + 20	—	—	ns	Must also meet parameter 42
				With Prescaler	10	—	—	ns	
42*	Tt0P	T0CKI Period		No Prescaler	TCY + 40	—	—	ns	
				With Prescaler	Greater of: 20 or TCY + 40 / N	—	—	ns	N = prescale value (2, 4, ..., 256)
45*	Tt1H	T1CKI High Time	Synchronous, Prescaler = 1		0.5TCY + 20	—	—	ns	Must also meet parameter 47
			Synchronous, Prescaler = 2,4,8	PIC16**C**6X	15	—	—	ns	
				PIC16**LC**6X	25	—	—	ns	
			Asynchronous	PIC16**C**6X	30	—	—	ns	
				PIC16**LC**6X	50	—	—	ns	
46*	Tt1L	T1CKI Low Time	Synchronous, Prescaler = 1		0.5TCY + 20	—	—	ns	Must also meet parameter 47
			Synchronous, Prescaler = 2,4,8	PIC16**C**6X	15	—	—	ns	
				PIC16**LC**6X	25	—	—	ns	
			Asynchronous	PIC16**C**6X	30	—	—	ns	
				PIC16**LC**6X	50	—	—	ns	
47*	Tt1P	T1CKI input period	Synchronous	PIC16**C**6X	Greater of: 30 OR TCY + 40 / N	—	—	ns	N = prescale value (1, 2, 4, 8)
				PIC16**LC**6X	Greater of: 50 OR TCY + 40 / N				N = prescale value (1, 2, 4, 8)
			Asynchronous	PIC16**C**6X	60	—	—	ns	
				PIC16**LC**6X	100	—	—	ns	
	Ft1	Timer1 oscillator input frequency range (oscillator enabled by setting bit T1OSCEN)			DC	—	200	kHz	
48	TCKEZtmr1	Delay from external clock edge to timer increment			2Tosc	—	7Tosc	—	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Applicable Devices	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67

22.4 Timing Parameter Symbology

The timing parameter symbols have been created following one of the following formats:

1. TppS2ppS
2. TppS
3. TCC:ST (I^2C specifications only)
4. Ts (I^2C specifications only)

T			
F	Frequency	T	Time

Lowercase letters (pp) and their meanings:

pp			
cc	CCP1	osc	OSC1
ck	CLKOUT	rd	$\overline{RD}$
cs	$\overline{CS}$	rw	$\overline{RD}$ or $\overline{WR}$
di	SDI	sc	SCK
do	SDO	ss	$\overline{SS}$
dt	Data in	t0	T0CKI
io	I/O port	t1	T1CKI
mc	$\overline{MCLR}$	wr	$\overline{WR}$

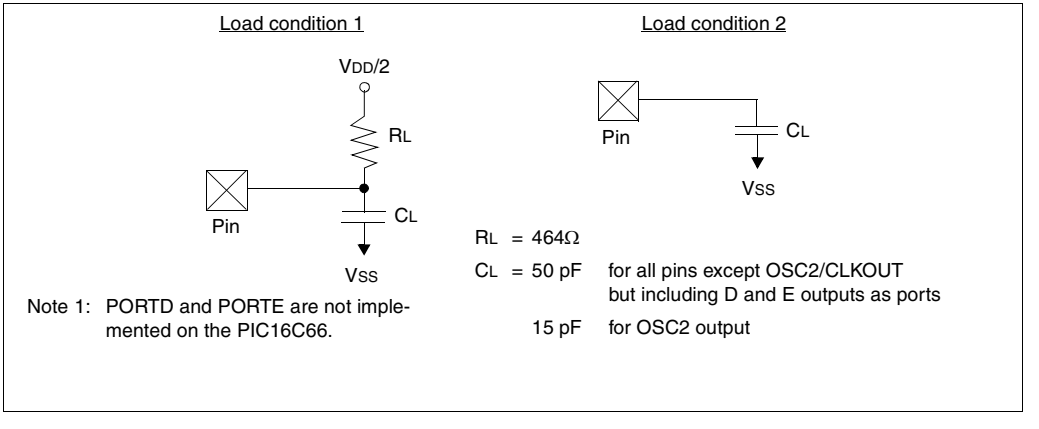
Uppercase letters and their meanings:

S			
F	Fall	P	Period
H	High	R	Rise
I	Invalid (Hi-impedance)	V	Valid
L	Low	Z	Hi-impedance
I^2C only			
AA	output access	High	High
BUF	Bus free	Low	Low

TCC:ST (I^2C specifications only)

CC			
HD	Hold	SU	Setup
ST			
DAT	DATA input hold	STO	STOP condition
STA	START condition		

FIGURE 22-1: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS



Note 1: PORTD and PORTE are not implemented on the PIC16C66.

Applicable Devices	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67

FIGURE 22-9: SPI MASTER MODE TIMING (CKE = 0)

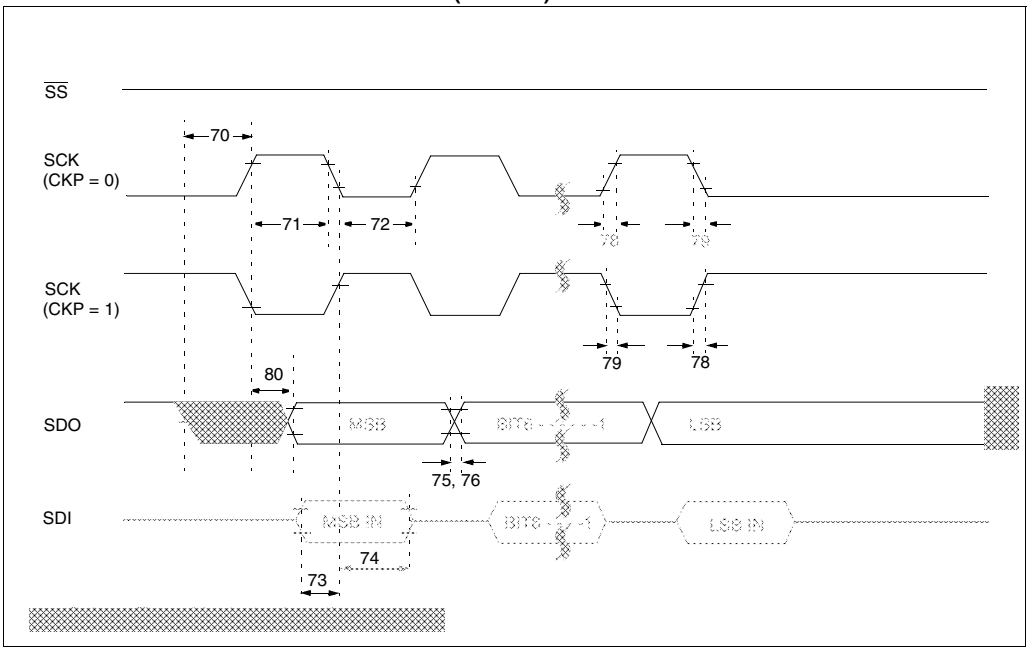
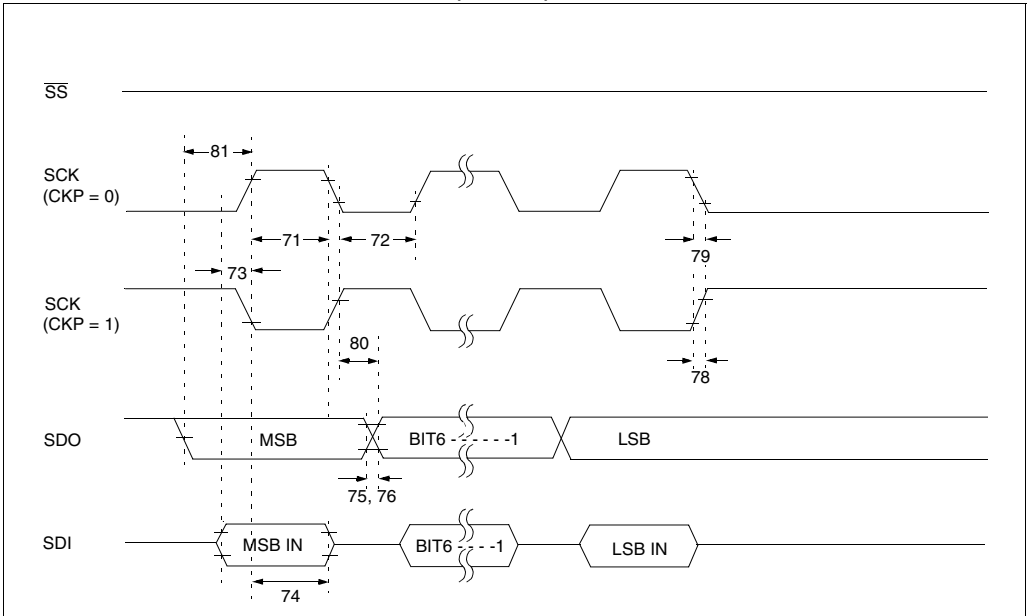


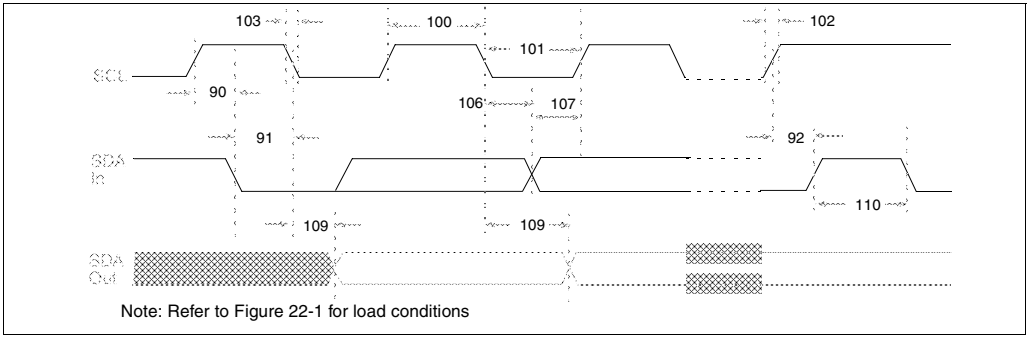
FIGURE 22-10: SPI MASTER MODE TIMING (CKE = 1)



Refer to Figure 22-1 for load conditions.

Applicable Devices	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67

FIGURE 22-14: I²C BUS DATA TIMING



Note: Refer to Figure 22-1 for load conditions

TABLE 22-10: I²C BUS DATA REQUIREMENTS

Parameter No.	Sym	Characteristic		Min	Max	Units	Conditions
100*	THIGH	Clock high time	100 kHz mode	4.0	—	µs	Device must operate at a minimum of 1.5 MHz
			400 kHz mode	0.6	—	µs	Device must operate at a minimum of 10 MHz
			SSP Module	1.5TCY	—		
101*	TLOW	Clock low time	100 kHz mode	4.7	—	µs	Device must operate at a minimum of 1.5 MHz
			400 kHz mode	1.3	—	µs	Device must operate at a minimum of 10 MHz
			SSP Module	1.5TCY	—		
102*	TR	SDA and SCL rise time	100 kHz mode	—	1000	ns	
			400 kHz mode	20 + 0.1Cb	300	ns	Cb is specified to be from 10-400 pF
103*	TF	SDA and SCL fall time	100 kHz mode	—	300	ns	
			400 kHz mode	20 + 0.1Cb	300	ns	Cb is specified to be from 10-400 pF
90*	TSU:STA	START condition setup time	100 kHz mode	4.7	—	µs	Only relevant for repeated START condition
			400 kHz mode	0.6	—	µs	
91*	THD:STA	START condition hold time	100 kHz mode	4.0	—	µs	After this period the first clock pulse is generated
			400 kHz mode	0.6	—	µs	
106*	THD:DAT	Data input hold time	100 kHz mode	0	—	ns	
			400 kHz mode	0	0.9	µs	
107*	TSU:DAT	Data input setup time	100 kHz mode	250	—	ns	Note 2
			400 kHz mode	100	—	ns	
92*	TSU:STO	STOP condition setup time	100 kHz mode	4.7	—	µs	
			400 kHz mode	0.6	—	µs	
109*	TAA	Output valid from clock	100 kHz mode	—	3500	ns	Note 1
			400 kHz mode	—	—	ns	
110*	TBUF	Bus free time	100 kHz mode	4.7	—	µs	Time the bus must be free before a new transmission can start
			400 kHz mode	1.3	—	µs	
	Cb	Bus capacitive loading		—	400	pF	

* These parameters are characterized but not tested.

Note 1: As a transmitter, the device must provide this internal minimum delay time to bridge the undefined region (min. 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

2: A fast-mode (400 kHz) I²C-bus device can be used in a standard-mode (100 kHz) I²C-bus system, but the requirement Tsu:DAT ≥ 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line TR max.+tsu;DAT = 1000 + 250 = 1250 ns (according to the standard-mode I²C bus specification) before the SCL line is released.

Applicable Devices	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67

FIGURE 23-25: TYPICAL IDD vs. FREQUENCY (LP MODE, 25°C)

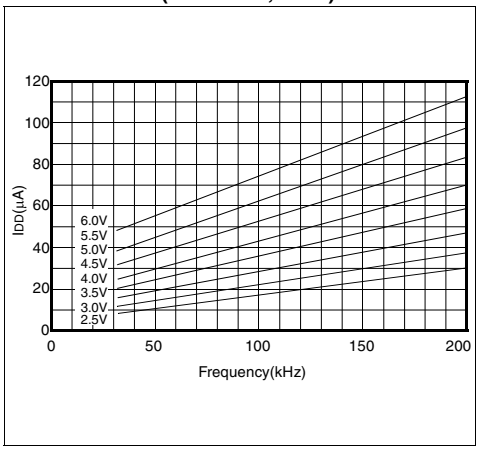


FIGURE 23-26: MAXIMUM IDD vs. FREQUENCY (LP MODE, 85°C TO -40°C)

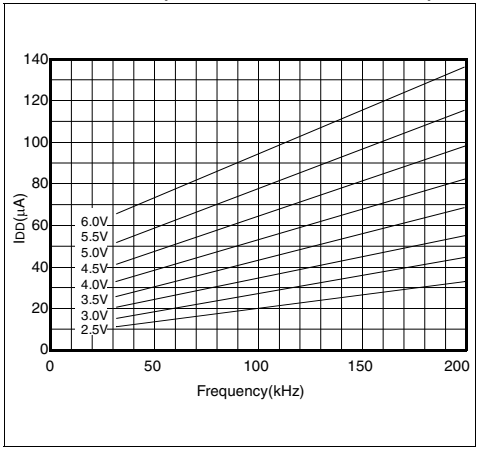


FIGURE 23-27: TYPICAL IDD vs. FREQUENCY (XT MODE, 25°C)

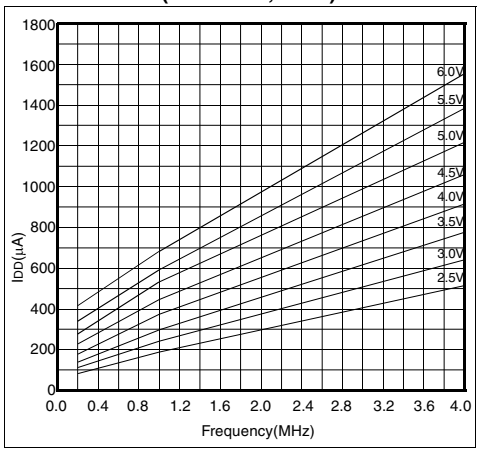
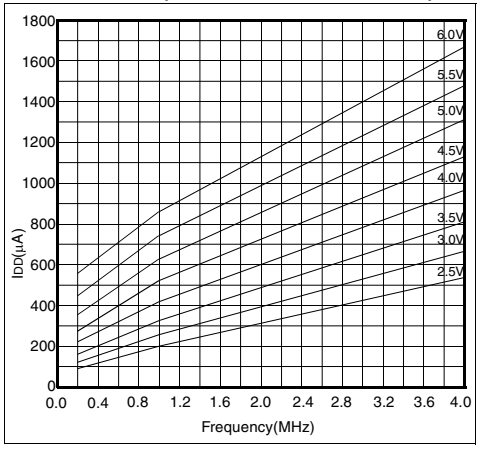


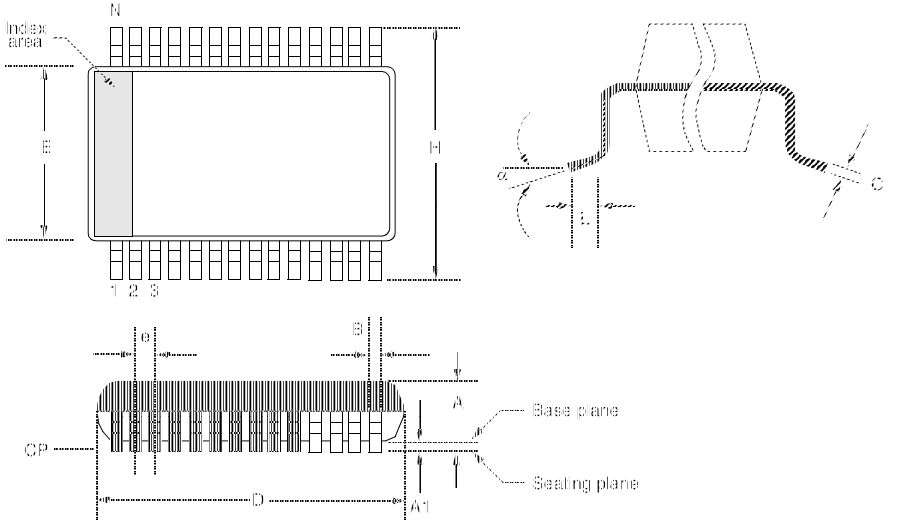
FIGURE 23-28: MAXIMUM IDD vs. FREQUENCY (XT MODE, -40°C TO 85°C)



Data based on matrix samples. See first page of this section for details.

24.10 28-Lead Plastic Surface Mount (SSOP - 209 mil Body 5.30 mm) (SS)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Package Group: Plastic SSOP						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	8°		0°	8°	
A	1.730	1.990		0.068	0.078	
A1	0.050	0.210		0.002	0.008	
B	0.250	0.380		0.010	0.015	
C	0.130	0.220		0.005	0.009	
D	10.070	10.330		0.396	0.407	
E	5.200	5.380		0.205	0.212	
e	0.650	0.650	**Reference**	0.026	0.026	**Reference**
H	7.650	7.900		0.301	0.311	
L	0.550	0.950		0.022	0.037	
N	28	28		28	28	
CP	-	0.102		-	0.004	

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1. Set your modem to 8-bit, No parity, and One stop (8N1). This is not the normal CompuServe setting which is 7E1.
2. Dial your local CompuServe access number.
3. Depress the **<Enter>** key and a garbage string will appear because CompuServe is expecting a 7E1 setting.
4. Type +, depress the **<Enter>** key and "`Host Name:`" will appear.
5. Type MCHIPBBS, depress the **<Enter>** key and you will be connected to the Microchip BBS.

In the United States, to find the CompuServe phone number closest to you, set your modem to 7E1 and dial (800) 848-4480 for 300-2400 baud or (800) 331-7166 for 9600-14400 baud connection. After the system responds with "`Host Name:`", type `NETWORK`, depress the **<Enter>** key and follow CompuServe's directions.

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