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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	33
Program Memory Size	7KB (4K x 14)
Program Memory Type	ОТР
EEPROM Size	-
RAM Size	192 x 8
Voltage - Supply (Vcc/Vdd)	$4V \sim 6V$
Data Converters	- ·
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	44-PLCC (16.59x16.59)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16c65a-04-l

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Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other resets ⁽³⁾
Bank 0											
00h ⁽¹⁾	INDF	Addressing	this location	uses conter	ts of FSR to	address data	a memory (n	ot a physical	register)	0000 0000	0000 0000
01h	TMR0	Timer0 mod	lule's registe	r						xxxx xxxx	uuuu uuuu
02h ⁽¹⁾	PCL	Program Co	ounter's (PC)	Least Signi	ficant Byte					0000 0000	0000 0000
03h ⁽¹⁾	STATUS	IRP	RP1	RP0	TO	PD	Z	DC	С	0001 1xxx	000q quuu
04h ⁽¹⁾	FSR	Indirect dat	ndirect data memory address pointer							xxxx xxxx	uuuu uuuu
05h	PORTA	_	_	PORTA Dat	a Latch wher	n written: PO	RTA pins wh	en read		xx xxxx	uu uuuu
06h	PORTB	PORTB Da	ta Latch whe	n written: PC	ORTB pins wi	nen read				xxxx xxxx	uuuu uuuu
07h	PORTC	PORTC Da	ta Latch whe	n written: PO	ORTC pins w	hen read				xxxx xxxx	uuuu uuuu
08h ⁽⁵⁾	PORTD	PORTD Da	ORTD Data Latch when written: PORTD pins when read							xxxx xxxx	uuuu uuuu
09h ⁽⁵⁾	PORTE	—	—	—	—	—	RE2	RE1	RE0	xxx	uuu
0Ah ^(1,2)	PCLATH	—	— — Write Buffer for the upper 5 bits of the Program Counter							0 0000	0 0000
0Bh ⁽¹⁾	INTCON	GIE	PEIE	TOIE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 0000
0Ch	PIR1	PSPIF ⁽⁶⁾	(4)	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
0Dh	PIR2	—	—			—	—	—	CCP2IF	0	0
0Eh	TMR1L	Holding reg	Holding register for the Least Significant Byte of the 16-bit TMR1 register							xxxx xxxx	uuuu uuuu
0Fh	TMR1H	Holding reg	ister for the I	Most Signific	ant Byte of th	ne 16-bit TMF	R1 register			xxxx xxxx	uuuu uuuu
10h	T1CON	—	_	T1CKPS1	T1CKPS0	T1OSCEN	T1SYNC	TMR1CS	TMR10N	00 0000	uu uuuu
11h	TMR2	Timer2 mod	lule's registe	r						0000 0000	0000 0000
12h	T2CON	—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000 0000	-000 0000
13h	SSPBUF	Synchronou	us Serial Por	t Receive Bu	ffer/Transmit	Register				xxxx xxxx	uuuu uuuu
14h	SSPCON	WCOL	SSPOV	SSPEN	СКР	SSPM3	SSPM2	SSPM1	SSPM0	0000 0000	0000 0000
15h	CCPR1L	Capture/Co	mpare/PWM	1 (LSB)						xxxx xxxx	uuuu uuuu
16h	CCPR1H	Capture/Co	mpare/PWM	1 (MSB)						xxxx xxxx	uuuu uuuu
17h	CCP1CON	—	—	CCP1X	CCP1Y	CCP1M3	CCP1M2	CCP1M1	CCP1M0	00 0000	00 0000
18h	RCSTA	SPEN	RX9	SREN	CREN	_	FERR	OERR	RX9D	0000 -00x	0000 -00x
19h	TXREG	USART Tra	nsmit Data F	legister						0000 0000	0000 0000
1Ah	RCREG	USART Re	ceive Data R	egister						0000 0000	0000 0000
1Bh	CCPR2L	Capture/Co	mpare/PWM	2 (LSB)						xxxx xxxx	uuuu uuuu
1Ch	CCPR2H	Capture/Co	mpare/PWM	2 (MSB)						xxxx xxxx	uuuu uuuu
1Dh	CCP2CON	—	—	CCP2X	CCP2Y	CCP2M3	CCP2M2	CCP2M1	CCP2M0	00 0000	00 0000
1Eh-1Fh	-	Unimpleme	nted							—	—

TABLE 4-6: SPECIAL FUNCTION REGISTERS FOR THE PIC16C66/67

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented location read as '0'. Shaded locations are unimplemented, read as '0'.

Note 1: These registers can be addressed from any bank.

2: The upper byte of the Program Counter (PC) is not directly accessible. PCLATH is a holding register for the PC whose contents are transferred to the upper byte of the program counter. (PC<12:8>)

3: Other (non power-up) resets include external reset through MCLR and the Watchdog Timer reset.

4: PIE1<6> and PIR1<6> are reserved on the PIC16C66/67, always maintain these bits clear.

5: PORTD, PORTE, TRISD, and TRISE are not implemented on the PIC16C66, read as '0'.

6: PSPIF (PIR1<7>) and PSPIE (PIE1<7>) are reserved on the PIC16C66, maintain these bits clear.

4.2.2.2 OPTION REGISTER

Applicable Devices

61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

The OPTION register is a readable and writable register which contains various control bits to configure the TMR0/WDT prescaler, the external INT interrupt, TMR0, and the weak pull-ups on PORTB. Note: To achieve a 1:1 prescaler assignment for TMR0 register, assign the prescaler to the Watchdog Timer.

R/W-1 R/W-1 R/W-1 R/W-1 R/W-1 R/W-1 R/W-1 R/W-1 RBPU INTEDG TOCS T0SE PSA PS2 PS1 PS0 R = Readable bit W = Writable bit bit7 bit0 U = Unimplemented bit, read as '0' n = Value at POR reset bit 7: RBPU: PORTB Pull-up Enable bit 1 = PORTB pull-ups are disabled 0 = PORTB pull-ups are enabled by individual port latch values INTEDG: Interrupt Edge Select bit bit 6: 1 = Interrupt on rising edge of RB0/INT pin 0 = Interrupt on falling edge of RB0/INT pin bit 5: TOCS: TMR0 Clock Source Select bit 1 = Transition on RA4/T0CKI pin 0 = Internal instruction cycle clock (CLKOUT) TOSE: TMR0 Source Edge Select bit bit 4. 1 = Increment on high-to-low transition on RA4/T0CKI pin 0 = Increment on low-to-high transition on RA4/T0CKI pin PSA: Prescaler Assignment bit bit 3: 1 = Prescaler is assigned to the WDT 0 = Prescaler is assigned to the Timer0 module bit 2-0: PS2:PS0: Prescaler Rate Select bits Bit Value TMR0 Rate WDT Rate 000 1:1 1:2 001 1:2 1 · 4 1:4 010 1:8 1:8 011 1:16 100 1:32 1:16 1:32 101 1:64 1:64 110 1:128 1:128 111 1:256

FIGURE 4-10: OPTION REGISTER (ADDRESS 81h, 181h)

						-					
R/W-0	B/W-0	U-0	U-0	B/W-0	R/W-0	B/W-0	R/W-0				
PSPIF				SSPIF	CCP1IF	TMR2IF	TMR1IF	R = Readable bit			
bit7							bit0				
bit 7: PSPIF: Parallel Slave Port Interrupt Flag bit 1 = A read or a write operation has taken place (must be cleared in software) 0 = No read or write operation has taken place											
bit 6:	Reserved: Always maintain this bit clear.										
bit 5-4:	Unimplemented: Read as '0'										
bit 3:	•										
bit 2:	 bit 2: CCP1IF: CCP1 Interrupt Flag bit Capture Mode A TMR1 register capture occurred (must be cleared in software) No TMR1 register capture occurred Compare Mode A TMR1 register compare match occurred (must be cleared in software) No TMR1 register compare match occurred (must be cleared in software) No TMR1 register compare match occurred										
bit 1:	1 = TMR2	MR2 to PR to PR2 mat R2 to PR2	ch occurre	d (must be	bit cleared in so	ftware)					
bit 0:	1 = TMR1	MR1 Overf register ove R1 register	erflow occu		be cleared in	software)					
global		GIE (INTC						s corresponding enable bit or the rrupt flag bits are clear prior to			

FIGURE 4-18: PIR1 REGISTER FOR PIC16C64/64A/R64 (ADDRESS 0Ch)

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets
0Bh,8Bh 10Bh,18Bh	INTCON	GIE	PEIE	TOIE	INTE	RBIE	TOIF	INTF	RBIF	0000 000x	0000 000u
0Ch	PIR1	PSPIF ⁽²⁾	(3)	RCIF ⁽¹⁾	TXIF ⁽¹⁾	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000	0000
0Dh ⁽⁴⁾	PIR2	—	_	_	_	_	_	_	CCP2IF		 0
8Ch	PIE1	PSPIE ⁽²⁾	(3)	RCIE ⁽¹⁾	TXIE ⁽¹⁾	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000	0000
8Dh ⁽⁴⁾	PIE2	—	_	-	_	-	_	-	CCP2IE		 0
87h	TRISC	C PORTC Data Direction register									1111 1111
11h	TMR2	Timer2 m	Timer2 module's register								0000
92h	PR2	Timer2 m	iodule's Per	iod register						1111 1111	1111 1111
12h	T2CON	—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000 0000	-000 0000
15h	CCPR1L	Capture/0	Compare/P	VM1 (LSB)	1					xxxx xxxx	uuuu uuuu
16h	CCPR1H	Capture/0	Compare/P	VM1 (MSB)					xxxx xxxx	นนนน นนนน
17h	CCP1CON	—	—	CCP1X	CCP1Y	CCP1M3	CCP1M2	CCP1M1	CCP1M0	00 0000	00 0000
1Bh ⁽⁴⁾	CCPR2L	Capture/0	Compare/P	VM2 (LSB)	1		1			xxxx xxxx	นนนน นนนน
1Ch ⁽⁴⁾	CCPR2H	Capture/0	Compare/P\	VM2 (MSB)					xxxx xxxx	นนนน นนนน
1Dh ⁽⁴⁾	CCP2CON	-	—	CCP2X	CCP2Y	CCP2M3	CCP2M2	CCP2M1	CCP2M0	00 0000	00 0000

TABLE 10-5: REGISTERS ASSOCIATED WITH PWM AND TIMER2

 Legend:
 x = unknown, u = unchanged, - = unimplemented locations read as '0'. Shaded cells are not used in this mode.

 Note
 1:
 These bits are associated with the USART module, which is implemented on the PIC16C63/R63/65/65A/R65/66/67 only.

2: Bits PSPIE and PSPIF are reserved on the PIC16C62/62A/R62/63/R63/66, always maintain these bits clear.

3: The PIR1<6> and PIE1<6> bits are reserved, always maintain these bits clear.

4: These registers are associated with the CCP2 module, which is only implemented on the PIC16C63/R63/65/65A/R65/66/67.

11.2 <u>SPI Mode for PIC16C62/62A/R62/63/</u> R63/64/64A/R64/65/65A/R65

This section contains register definitions and operational characteristics of the SPI module for the PIC16C62, PIC16C62A, PIC16CR62, PIC16C63, PIC16CR63, PIC16C64A, PIC16CR64, PIC16CR64, PIC16C65, PIC16C65A, PIC16CR65.

FIGURE 11-1: SSPSTAT: SYNC SERIAL PORT STATUS REGISTER (ADDRESS 94h)

U-0	U-0	R-0	B-0	B-0	R-0	B-0	B-0			
_	_	D/A	P	S	R/W	UA	BF	R = Readable bit		
bit7			1			<u>I</u>	bit0	W = Writable bit U = Unimplemented bit, read as '0' - n =Value at POR reset		
bit 7-6:	Unimpl	emented	Read as	'0'						
 bit 5: D/Ā: Data/Address bit (I²C mode only) 1 = Indicates that the last byte received or transmitted was data 0 = Indicates that the last byte received or transmitted was address 										
bit 4:	 bit 4: P: Stop bit (I²C mode only. This bit is cleared when the SSP module is disabled, SSPEN is cleared) 1 = Indicates that a stop bit has been detected last (this bit is '0' on RESET) 0 = Stop bit was not detected last 									
bit 3:	 S: Start bit (I²C mode only. This bit is cleared when the SSP module is disabled, SSPEN is cleared) 1 = Indicates that a start bit has been detected last (this bit is '0' on RESET) 0 = Start bit was not detected last 									
bit 2:	This bit	holds the o the next ad	R/W bit i	ation (I ² C r nformation stop bit, or	following the	e last addre	ess match. T	his bit is valid from the address		
bit 1:	1 = Indi	cates that	the user	it I ² C mode needs to up to be upda	odate the add	dress in the	SSPADD re	egister		
bit 0:	BF: Buf	fer Full St	atus bit							
	1 = Rec		olete, SSF	es) PBUF is full SSPBUF is						
	1 = Trar		ogress, S	SPBUF is f PBUF is err						

To enable the serial port, SSP Enable bit, SSPEN (SSPCON<5>) must be set. To reset or reconfigure SPI mode, clear bit SSPEN, re-initialize the SSPCON register, and then set bit SSPEN. This configures the SDI, SDO, SCK, and \overline{SS} pins as serial port pins. For the pins to behave as the serial port function, they must have their data direction bits (in the TRISC register) appropriately programmed. That is:

- SDI must have TRISC<4> set
- SDO must have TRISC<5> cleared
- SCK (Master mode) must have TRISC<3> cleared
- SCK (Slave mode) must have TRISC<3> set
- SS must have TRISA<5> set

Any serial port function that is not desired may be overridden by programming the corresponding data direction (TRIS) register to the opposite value. An example would be in master mode where you are only sending data (to a display driver), then both SDI and \overline{SS} could be used as general purpose outputs by clearing their corresponding TRIS register bits.

Figure 11-10 shows a typical connection between two microcontrollers. The master controller (Processor 1) initiates the data transfer by sending the SCK signal. Data is shifted out of both shift registers on their programmed clock edge, and latched on the opposite edge of the clock. Both processors should be programmed to same Clock Polarity (CKP), then both controllers would send and receive data at the same time. Whether the data is meaningful (or dummy data) depends on the application firmware. This leads to three scenarios for data transmission:

- · Master sends data Slave sends dummy data
- Master sends data Slave sends data
- · Master sends dummy data Slave sends data

The master can initiate the data transfer at any time because it controls the SCK. The master determines when the slave (Processor 2) is to broadcast data by the firmware protocol.

In master mode the data is transmitted/received as soon as the SSPBUF register is written to. If the SPI is only going to receive, the SCK output could be disabled (programmed as an input). The SSPSR register will continue to shift in the signal present on the SDI pin at the programmed clock rate. As each byte is received, it will be loaded into the SSPBUF register as if a normal received byte (interrupts and status bits appropriately set). This could be useful in receiver applications as a "line activity monitor" mode.

In slave mode, the data is transmitted and received as the external clock pulses appear on SCK. When the last bit is latched the interrupt flag bit SSPIF (PIR1<3>) is set.

The clock polarity is selected by appropriately programming bit CKP (SSPCON<4>). This then would give waveforms for SPI communication as shown in Figure 11-11, Figure 11-12, and Figure 11-13 where the MSB is transmitted first. In master mode, the SPI clock rate (bit rate) is user programmable to be one of the following:

- Fosc/4 (or Tcy)
- Fosc/16 (or 4 Tcy)
- Fosc/64 (or 16 Tcy)
- Timer2 output/2

This allows a maximum bit clock frequency (at 20 MHz) of 5 MHz. When in slave mode the external clock must meet the minimum high and low times.

In sleep mode, the slave can transmit and receive data and wake the device from sleep.

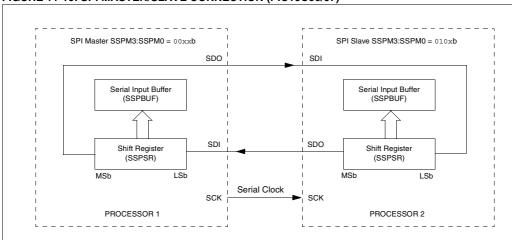


FIGURE 11-10: SPI MASTER/SLAVE CONNECTION (PIC16C66/67)

TABLE 12-10: REGISTERS ASSOCIATED WITH SYNCHRONOUS SLAVE TRANSMISSION

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
0Ch	PIR1	PSPIF ⁽¹⁾	(2)	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
18h	RCSTA	SPEN	RX9	SREN	CREN	_	FERR	OERR	RX9D	0000 -00x	0000 -00x
19h	TXREG	USART Tra	ansmit R	egister						0000 0000	0000 0000
8Ch	PIE1	PSPIE ⁽¹⁾	(2)	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
98h	TXSTA	CSRC	TX9	TXEN	SYNC	_	BRGH	TRMT	TX9D	0000 -010	0000 -010
99h	SPBRG	RG Baud Rate Generator Register								0000 0000	0000 0000

Legend: x = unknown, - = unimplemented locations read as '0'. Shaded cells are not used for Synchronous Slave Transmission.

Note 1: PSPIF and PSPIE are reserved on the PIC16C63/R63/66, always maintain these bits clear.

2: PIR1<6> and PIE1<6> are reserved, always maintain these bits clear.

Value on Value on Address Name Bit 7 Bit 6 Bit 5 Bit 4 Bit 3 Bit 2 Bit 1 Bit 0 POR. all other BOR Resets PSPIF⁽¹⁾ 0Ch PIR1 RCIF TXIF SSPIF CCP1IF TMR2IF TMR1IF 0000 0000 0000 0000 (2) 18h RCSTA SPEN RX9 SREN CREN FFRR OFBB 0000 -00x 0000 -00x RX9D 0000 0000 0000 0000 1Ah RCREG USART Receive Register PSPIE⁽¹⁾ CCP1IE 0000 0000 0000 0000 8Ch PIE1 RCIE TXIE SSPIE TMR2IE TMR1IE (2) 0000 -010 0000 -010 98h TXSTA CSRC BRGH TRMT TX9D TX9 TXEN SYNC _ 0000 0000 0000 0000 SPBRG 99h Baud Rate Generator Register

TABLE 12-11: REGISTERS ASSOCIATED WITH SYNCHRONOUS SLAVE RECEPTION

Legend: x = unknown, - = unimplemented locations read as '0'. Shaded cells are not used for Synchronous Slave Reception.

Note 1: PSPIF and PSPIE are reserved on the PIC16C63/R63/66, always maintain these bits clear.

2: PIR1<6> and PIE1<6> are reserved, always maintain these bits clear.

13.5 Interrupts

Applicable Devices 61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

The PIC16C6X family has up to 11 sources of interrupt. The interrupt control register (INTCON) records individual interrupt requests in flag bits. It also has individual and global interrupt enable bits.

Note:	Individual interrupt flag bits are set regard-
	less of the status of their corresponding
	mask bit or global enable bit, GIE.

Global interrupt enable bit, GIE (INTCON<7>) enables (if set) all un-masked interrupts or disables (if cleared) all interrupts. When bit GIE is enabled, and an interrupt flag bit and mask bit are set, the interrupt will vector immediately. Individual interrupts can be disabled through their corresponding enable bits in the INTCON register. GIE is cleared on reset.

The "return from interrupt" instruction, RETFIE, exits the interrupt routine as well as sets the GIE bit, which re-enable interrupts.

The RB0/INT pin interrupt, the RB port change interrupt and the TMR0 overflow interrupt flag bits are contained in the INTCON register.

The peripheral interrupt flag bits are contained in special function registers PIR1 and PIR2. The corresponding interrupt enable bits are contained in special function registers PIE1 and PIE2 and the peripheral interrupt enable bit is contained in special function register INTCON.

When an interrupt is responded to, bit GIE is cleared to disable any further interrupts, the return address is pushed onto the stack and the PC is loaded with 0004h. Once in the interrupt service routine the source(s) of the interrupt can be determined by polling the interrupt flag bits. The interrupt flag bit(s) must be cleared in software before re-enabling interrupts to avoid recursive interrupts.

For external interrupt events, such as the RB0/INT pin or RB port change interrupt, the interrupt latency will be three or four instruction cycles. The exact latency depends when the interrupt event occurs (Figure 13-19). The latency is the same for one or two cycle instructions. Once in the interrupt service routine the source(s) of the interrupt can be determined by polling the interrupt flag bits. The interrupt flag bit(s) must be cleared in software before re-enabling interrupts to avoid infinite interrupt requests. Individual interrupt flag bits are set regardless of the status of their corresponding mask bit or the GIE bit.

- Note: For the PIC16C61/62/64/65, if an interrupt occurs while the Global Interrupt Enable bit, GIE is being cleared, bit GIE may unintentionally be re-enabled by the user's Interrupt Service Routine (the RETFIE instruction). The events that would cause this to occur are:
 - 1. An instruction clears the GIE bit while an interrupt is acknowledged
 - 2. The program branches to the Interrupt vector and executes the Interrupt Service Routine.
 - The Interrupt Service Routine completes with the execution of the RET-FIE instruction. This causes the GIE bit to be set (enables interrupts), and the program returns to the instruction after the one which was meant to disable interrupts.
 - 4. Perform the following to ensure that interrupts are globally disabled.

LOOP	BCF II	NTCON,GIE	;Disable Global				
			;Interrupt bit				
	BTFSC INTCON,GIE		;Global Interrupt				
			;Disabled?				
	GOTO	LOOP	;NO, try again				
	:		;Yes, continue				
			;with program flow				

13.7 <u>Watchdog Timer (WDT)</u>

Applicable Devices

61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

The Watchdog Timer is a free running on-chip RC oscillator which does not require any external components. This RC oscillator is separate from the RC oscillator of the OSC1/CLKIN pin. That means that the WDT will run, even if the clock on the OSC1/CLKIN and OSC2/ CLKOUT pins of the device has been stopped, for example, by execution of a SLEEP instruction. During normal operation, a WDT time-out generates a device reset. If the device is in SLEEP mode, a WDT time-out causes the device to wake-up and continue with normal operation (WDT Wake-up). The WDT can be permanently disabled by clearing configuration bit WDTE (Section 13.1).

13.7.1 WDT PERIOD

The WDT has a nominal time-out period of 18 ms, (with no prescaler). The time-out periods vary with temperature, VDD and process variations from part to part (see DC specs). If longer time-out periods are desired, a prescaler with a division ratio of up to 1:128 can be

FIGURE 13-20: WATCHDOG TIMER BLOCK DIAGRAM

assigned to the WDT under software control by writing to the OPTION register. Thus, time-out periods up to 2.3 seconds can be realized.

The CLRWDT and SLEEP instructions clear the WDT and the postscaler, if assigned to the WDT, and prevent it from timing out and generating a device RESET condition.

The $\overline{\text{TO}}$ bit in the STATUS register will be cleared upon a WDT time-out.

13.7.2 WDT PROGRAMMING CONSIDERATIONS

It should also be taken in account that under worst case conditions (VDD = Min., Temperature = Max., max. WDT prescaler) it may take several seconds before a WDT time-out occurs.

Note: When a CLRWDT instruction is executed and the prescaler is assigned to the WDT, the prescaler count will be cleared, but the prescaler assignment is not changed.

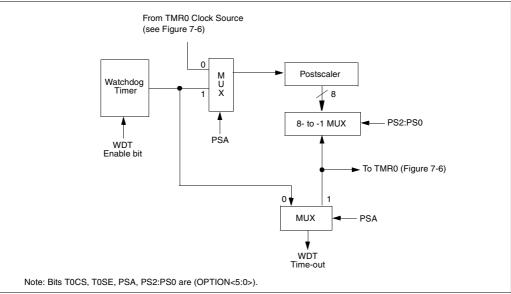


FIGURE 13-21: SUMMARY OF WATCHDOG TIMER REGISTERS

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
2007h	Config. bits	(1)	BODEN ⁽¹⁾	CP1	CP0	PWRTE ⁽¹⁾	WDTE	FOSC1	FOSC0
81h,181h	OPTION	RBPU	INTEDG	TOCS	TOSE	PSA	PS2	PS1	PS0

Legend: Shaded cells are not used by the Watchdog Timer.

Note 1: See Figure 13-1, Figure 13-2, and Figure 13-3 for details of these bits for the specific device.

Instruction Descriptions 14.1

Add Lite	ral and	w					
[<i>label</i>] A	DDLW	k					
$0 \le k \le 255$							
$(W) + k \rightarrow (W)$							
C, DC, Z							
11	111x	kkkk	kkkk				
The contents of the W register are added to the eight bit literal 'k' and the result is placed in the W register.							
1							
1							
Q1	Q2	Q3	Q4				
Decode	Read literal 'k'	Process data	Write to W				
After Inst	W = ruction	0x10 0x25					
	[<i>label</i>] Al $0 \le k \le 2\xi$ (W) + k - C, DC, Z 11 The conte added to the result is pl 1 1 Q1 Decode ADDLW Before In After Inst	$ \begin{array}{l lllllllllllllllllllllllllllllllllll$	$0 \le k \le 255$ (W) + k → (W) C, DC, Z $11 111x kkkk$ The contents of the W register added to the eight bit literal 'k' result is placed in the W register 1 1 2 2 2 2 2 2 2 2 2 2 2 2 2 3 2 2 2 2				

ANDLW	AND Lite	eral with	W					
Syntax:	[<i>label</i>] A	[<i>label</i>] ANDLW k						
Operands:	$0 \le k \le 25$	$0 \le k \le 255$						
Operation:	(W) .AND	D. (k) \rightarrow (W)					
Status Affected:	Z							
Encoding:	11	1001	kkkk	kkkk				
Description:	The contents of W register are AND'ed with the eight bit literal 'k'. The result is placed in the W register.							
Words:	1							
Cycles:	1							
Q Cycle Activity:	Q1	Q2	Q3	Q4				
	Decode	Read literal "k"	Process data	Write to W				
Example	ANDLW	0x5F						
	Before In	struction						
	After Inst		0xA3					
		W =	0x03					

ADDWF	Add W a	nd f						
Syntax:	[<i>label</i>] A	DDWF	f,d					
Operands:	$\begin{array}{l} 0 \leq f \leq 127 \\ d \in [0,1] \end{array}$							
Operation:	(W) + (f) \rightarrow (destination)							
Status Affected:	C, DC, Z							
Encoding:	00	0111	dfff	ffff				
Description:	Add the contents of the W register with register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'.							
Words:	1							
Cycles:	1							
Q Cycle Activity:	Q1	Q2	Q3	Q4				
	Decode	Read register 'f'	Process data	Write to destination				
Evennle	ADDUE	BOD	<u>.</u>					
Example	ADDWF		0					
	Before In	structior	ו 0x17					
	FSR = 0xC2							
	After Inst							
		W = FSR =	0xD9 0xC2					

ANDWF	AND W v	vith f		
Syntax:	[<i>label</i>] Al	NDWF	f,d	
Operands:	$\begin{array}{l} 0 \leq f \leq 12 \\ d \in [0,1] \end{array}$	7		
Operation:	(W) .AND	0. (f) \rightarrow (e	destinatio	on)
Status Affected:	Z			
Encoding:	0.0	0101	dfff	ffff
Description:	AND the W is 0 the res ter. If 'd' is register 'f'.	sult is stor 1 the res	red in the	W regis-
Words:	1			
Cycles:	1			
Q Cycle Activity:	Q1	Q2	Q3	Q4
	Decode	Read register 'f'	Process data	Write to destination
Example	ANDWF	FSR,	1	
	Before In			
		W = FSR =	0x17 0xC2	
	After Inst		0102	
		W =	0x17	
		FSR =	0x02	

Applicable Devices	61	60	601	Deo	60	Dec	61	611	DGA	65	65A	Dee	66	67
Applicable Devices	01	02	02A	n02	03	n03	04	04A	n04	05	05A	H00	00	07

		Standa	rd Operat	ing Co			ss otherwise stated)		
		Operatir	ng temper	ature	-40°C	S ≤ TA	$\Delta \leq +125^{\circ}C$ for extended,		
	RACTERISTICS				-40°C	≤ T/	$\Delta \leq +85^{\circ}$ C for industrial and		
	ARACIERISTICS				0°C	≤ T⁄	$A \leq +70^{\circ}C$ for commercial		
		Operatir	ng voltage	VDD r	ange as c	describe	ed in DC spec Section 15.1 and		
		Section 15.2.							
Param	Characteristic	Sym	Min	Typ†	Max	Units	Conditions		
No.									
	Output High Voltage								
D090	I/O ports (Note 3)	Voh	VDD-0.7	-	-	v	IOH = -3.0 mA,		
						-	$VDD = 4.5V, -40^{\circ}C \text{ to } +85^{\circ}C$		
D090A			VDD-0.7	-	-	v	IOH = -2.5 mA,		
							VDD = 4.5V, -40°C to +125°C		
D092	OSC2/CLKOUT (RC osc config)		VDD-0.7	-	-	V	IOH = -1.3 mA,		
							VDD = 4.5V, -40°C to +85°C		
D092A			VDD-0.7	-	-	V	IOH = -1.0 mA,		
							VDD = 4.5V, -40°C to +125°C		
D150*	Open-Drain High Voltage	Vod	-	-	14	V	RA4 pin		
	Capacitive Loading Specs on								
	Output Pins								
D100	OSC2 pin	Cosc2			15	pF	In XT, HS and LP modes when		
							external clock is used to drive		
							OSC1.		
D101	All I/O pins and OSC2 (in RC mode)	Cio			50	pF			

The parameters are characterized but not tested.

*

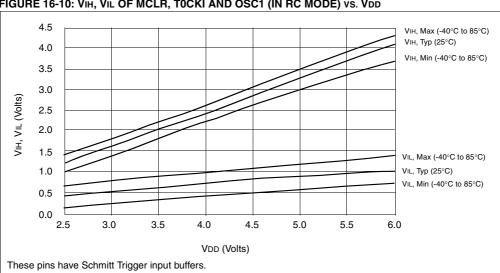
† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C6X be driven with external clock in RC mode.

 The leakage current on the MCLR/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as current sourced by the pin.

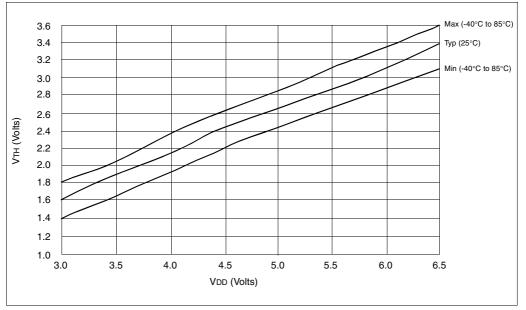
PIC16C6X



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FIGURE 16-10: VIH, VIL OF MCLR, TOCKI AND OSC1 (IN RC MODE) vs. VDD

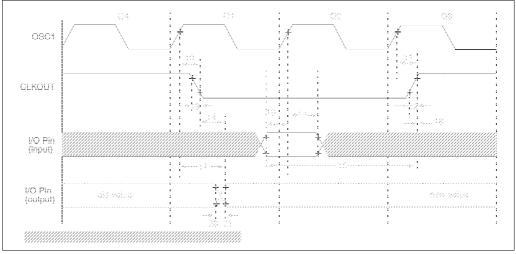




PIC16C6X

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FIGURE 18-3: CLKOUT AND I/O TIMING



CLKOUT AND I/O TIMING REQUIREMENTS TABLE 18-3:

Parameters	Sym	Characteristic		Min	Typ†	Max	Units	Conditions
10*	TosH2ckL	OSC1↑ to CLKOUT↓		-	75	200	ns	Note 1
11*	TosH2ckH	OSC1↑ to CLKOUT↑	OSC1↑ to CLKOUT↑		75	200	ns	Note 1
12*	TckR	CLKOUT rise time		_	35	100	ns	Note 1
13*	TckF	CLKOUT fall time		_	35	100	ns	Note 1
14*	TckL2ioV	CLKOUT ↓ to Port out valid		_	_	0.5TCY + 20	ns	Note 1
15*	TioV2ckH	Port in valid before CLKOUT \uparrow		Tosc + 200	_	_	ns	Note 1
16*	TckH2iol	Port in hold after CLKOUT \uparrow		0	_	_	ns	Note 1
17*	TosH2ioV	OSC1 [↑] (Q1 cycle) to Port out va	OSC1↑ (Q1 cycle) to Port out valid			150	ns	
18*	TosH2iol	OSC1 [↑] (Q2 cycle) to Port input invalid (I/O in hold time)	PIC16 C 62A/ R62/64A/R64	100	—	—	ns	
			PIC16 LC 62A/ R62/64A/R64	200	_	_	ns	
19*	TioV2osH	Port input valid to OSC1 [↑] (I/O in	setup time)	0	_	_	ns	
20*	TioR	Port output rise time	PIC16 C 62A/ R62/64A/R64	—	10	40	ns	
			PIC16 LC 62A/ R62/64A/R64	_	_	80	ns	
21*	TioF	Port output fall time	PIC16 C 62A/ R62/64A/R64	—	10	40	ns	
			PIC16 LC 62A/ R62/64A/R64	_	-	80	ns	
22††*	Tinp	RB0/INT pin high or low time		Тсү	_	_	ns	
23††*	Trbp	RB7:RB4 change int high or low	Тсү	—	—	ns		

These parameters are characterized but not tested.

t Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

†† These parameters are asynchronous events not related to any internal clock edge.

Note 1: Measurements are taken in RC Mode where CLKOUT output is 4 x TOSC.

Applicable Devices 61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

22.0 ELECTRICAL CHARACTERISTICS FOR PIC16C66/67

Absolute Maximum Ratings (†)

Ambient temperature under bias	55°C to +125°C
Storage temperature	
Voltage on any pin with respect to Vss (except VDD, MCLR, and RA4)	0.3V to (VDD + 0.3V)
Voltage on VDD with respect to Vss	-0.3V to +7.5V
Voltage on MCLR with respect to Vss (Note 2)	
Voltage on RA4 with respect to Vss	0V to +14V
Total power dissipation (Note 1)	1.0W
Maximum current out of VSS pin	
Maximum current into VDD pin	250 mA
Input clamp current, Iк (VI < 0 or VI > VDD)	±20 mA
Output clamp current, loк (Vo < 0 or Vo > VDD)	±20 mA
Maximum output current sunk by any I/O pin	25 mA
Maximum output current sourced by any I/O pin	25 mA
Maximum current sunk by PORTA, PORTB, and PORTE (Note 3) (combined)	200 mA
Maximum current sourced by PORTA, PORTB, and PORTE (Note 3) (combined)	
Maximum current sunk by PORTC and PORTD (Note 3) (combined)	200 mA
Maximum current sourced by PORTC and PORTD (Note 3) (combined)	200 mA
Note 1: Power dissipation is calculated as follows: Pdis = VDD x {IDD - \sum IOH} + \sum {(VDD-Vd	OH) X IOH} + Σ (VOI X IOL)

- Note 2: Voltage spikes below Vss at the MCLR/VPP pin, inducing currents greater than 80 mA, may cause latch-up. Thus, a series resistor of 50-100Ω should be used when applying a "low" level to the MCLR/VPP pin rather than pulling this pin directly to Vss.
- Note 3: PORTD and PORTE not available on the PIC16C66.

† NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 22-1: CROSS REFERENCE OF DEVICE SPECS FOR OSCILLATOR CONFIGURATIONS AND FREQUENCIES OF OPERATION (COMMERCIAL DEVICES)

osc	PIC16C66-04 PIC16C67-04	PIC16C66-10 PIC16C67-10	PIC16C66-20 PIC16C67-20	PIC16LC66-04 PIC16LC67-04	JW Devices
RC	VDD: 4.0V to 6.0V IDD: 5 mA max. at 5.5V IPD: 16 µA max. at 4V Freq: 4 MHz max.	VDD: 4.5V to 5.5V IDD: 2.7 mA typ. at 5.5V IPD: 1.5 μA typ. at 4V Freq: 4 MHz max.	VDD: 4.5V to 5.5V IDD: 2.7 mA typ. at 5.5V IPD: 1.5 μA typ. at 4V Freq: 4 MHz max.	VDD: 2.5V to 6.0V IDD: 3.8 mA max. at 3V IPD: 5 μA max. at 3V Freq: 4 MHz max.	VDD: 4.0V to 6.0V IDD: 5 mA max. at 5.5V IPD: 16 μA max. at 4V Freq: 4 MHz max.
ХТ	VDD: 4.0V to 6.0V IDD: 5 mA max. at 5.5V IPD: 16 μA max. at 4V Freq: 4 MHz max.	VDD: 4.5V to 5.5V IDD: 2.7 mA typ. at 5.5V IPD: 1.5 μA typ. at 4V Freq: 4 MHz max.	VDD: 4.5V to 5.5V IDD: 2.7 mA typ. at 5.5V IPD: 1.5 μA typ. at 4V Freq: 4 MHz max.	VDD: 2.5V to 6.0V IDD: 3.8 mA max. at 3V IPD: 5 μA max. at 3V Freq: 4 MHz max.	VDD: 4.0V to 6.0V IDD: 5 mA max. at 5.5V IPD: 16 μA max. at 4V Freq: 4 MHz max.
HS	VDD: 4.5V to 5.5V IDD: 13.5 mA typ. at 5.5V	VDD: 4.5V to 5.5V IDD: 10 mA max. at 5.5V	VDD: 4.5V to 5.5V IDD: 20 mA max. at 5.5V	Not recommended for use in HS mode	VDD: 4.5V to 5.5V IDD: 20 mA max. at 5.5V
	IPD: 1.5 μA typ. at 4.5V Freg: 4 MHz max.	IPD 1.5 μA typ. at 4.5V Freg: 10 MHz max.	IPD: 1.5 μA typ. at 4.5V Freg: 20 MHz max.	use in his mode	IPD: 1.5 μA typ. at 4.5V Freg: 20 MHz max.
LP	VDD: 4.0V to 6.0V IDD: 52.5 μA typ. at 32 kHz, 4.0V IPD: 0.9 μA typ. at 4.0V Freq: 200 kHz max.	Not recommended for use in LP mode	Not recommended for use in LP mode	VDD: 2.5V to 6.0V IDD: 48 μA max. at 32 kHz, 3.0V IPD: 5 μA max. at 3.0V Freq: 200 kHz max.	VDD: 2.5V to 6.0V IDD: 48 μA max. at 32 kHz, 3.0V

The shaded sections indicate oscillator selections which are tested for functionality, but not for MIN/MAX specifications. It is recommended that the user select the device type that ensures the specifications required.

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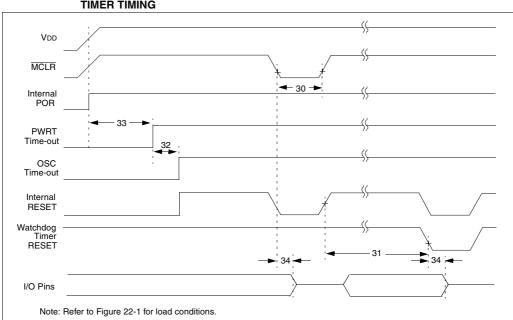


FIGURE 22-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING

FIGURE 22-5: BROWN-OUT RESET TIMING

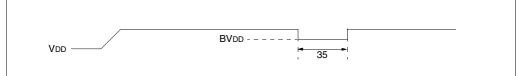


TABLE 22-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, POWER-UP TIMER, AND BROWN-OUT RESET REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Тур†	Max	Units	Conditions
30	TmcL	MCLR Pulse Width (low)	2	—		μs	VDD = 5V, -40°C to +125°C
31*	Twdt	Watchdog Timer Time-out Period (No Prescaler)	7	18	33	ms	VDD = 5V, -40°C to +125°C
32	Tost	Oscillation Start-up Timer Period	-	1024 Tosc		_	TOSC = OSC1 period
33*	Tpwrt	Power-up Timer Period	28	72	132	ms	VDD = 5V, -40°C to +125°C
34	Tioz	I/O Hi-impedance from MCLR Low or WDT reset		_	2.1	μs	
35	TBOR	Brown-out Reset Pulse Width	100	—		μs	V DD \leq BVDD (D005)

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

PIC16C6X

Applicable Devices 61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

FIGURE 22-14: I²C BUS DATA TIMING

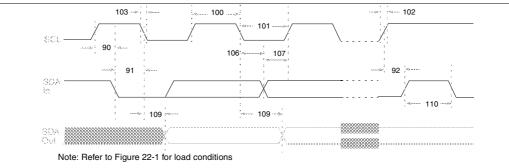


TABLE 22-10: I²C BUS DATA REQUIREMENTS

Parameter No.	Sym	Characteristic		Min	Max	Units	Conditions
100*	Тнідн	Clock high time	100 kHz mode	4.0	-	μs	Device must operate at a mini- mum of 1.5 MHz
			400 kHz mode	0.6	_	μs	Device must operate at a mini- mum of 10 MHz
			SSP Module	1.5TCY	—		
101*	TLOW	Clock low time	100 kHz mode	4.7	_	μs	Device must operate at a mini- mum of 1.5 MHz
			400 kHz mode	1.3	_	μs	Device must operate at a mini- mum of 10 MHz
			SSP Module	1.5Tcy	—		
102*	TR	SDA and SCL rise	100 kHz mode	-	1000	ns	
		time	400 kHz mode	20 + 0.1Cb	300	ns	Cb is specified to be from 10-400 pF
103*	TF	SDA and SCL fall time	100 kHz mode	—	300	ns	
			400 kHz mode	20 + 0.1Cb	300	ns	Cb is specified to be from 10-400 pF
90*	TSU:STA	START condition	100 kHz mode	4.7	—	μs	Only relevant for repeated
		setup time	400 kHz mode	0.6	—	μs	START condition
91*	THD:STA	START condition hold	100 kHz mode	4.0	—	μs	After this period the first clock
		time	400 kHz mode	0.6	—	μs	pulse is generated
106*	THD:DAT	Data input hold time	100 kHz mode	0	—	ns	
			400 kHz mode	0	0.9	μs	
107*	TSU:DAT	Data input setup time	100 kHz mode	250	—	ns	Note 2
			400 kHz mode	100	—	ns	
92*	Tsu:sto	STOP condition setup	100 kHz mode	4.7	—	μs	
		time	400 kHz mode	0.6	—	μs	
109*	TAA	Output valid from	100 kHz mode	_	3500	ns	Note 1
		clock	400 kHz mode	—	—	ns	
110*	TBUF	Bus free time	100 kHz mode	4.7	—	μs	Time the bus must be free
			400 kHz mode	1.3	—	μs	before a new transmission can start
	Cb	Bus capacitive loading		—	400	pF	

These parameters are characterized but not tested.

Note 1: As a transmitter, the device must provide this internal minimum delay time to bridge the undefined region (min. 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

2: A fast-mode (400 kHz) I²C-bus device can be used in a standard-mode (100 kHz) I²C-bus system, but the requirement Tsu:DAT ≥ 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line TR max.+tsu;DAT = 1000 + 250 = 1250 ns (according to the standard-mode I²C bus specification) before the SCL line is released. Applicable Devices 61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

FIGURE 22-15: USART SYNCHRONOUS TRANSMISSION (MASTER/SLAVE) TIMING

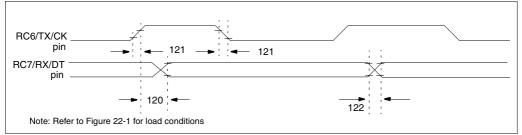


TABLE 22-11: USART SYNCHRONOUS TRANSMISSION REQUIREMENTS

Parameter No.	Sym	Characteristic		Min	Тур†	Max	Units	Conditions
120*	TckH2dtV	SYNC XMIT (MASTER & SLAVE)	PIC16 C 66/67		—	80	ns	
		Clock high to data out valid	PIC16 LC 66/67	-	—	100	ns	
121*	Tckrf	ckrf Clock out rise time and fall time			—	45	ns	
	(Master Mode)	(Master Mode)	PIC16LC66/67		—	50	ns	
122*	Tdtrf	Data out rise time and fall time	PIC16 C 66/67	_	—	45	ns	
	Ī		PIC16LC66/67	_	—	50	ns	

* These parameters are characterized but not tested.

†: Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 22-16: USART SYNCHRONOUS RECEIVE (MASTER/SLAVE) TIMING

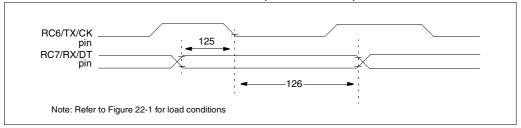


TABLE 22-12: USART SYNCHRONOUS RECEIVE REQUIREMENTS

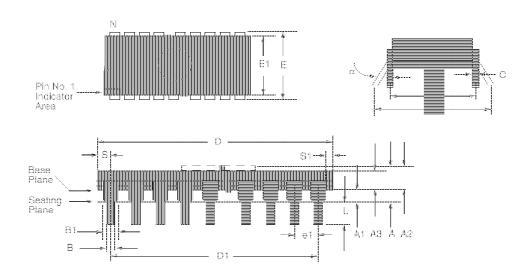
Parameter No.	Sym	Characteristic	Min	Тур†	Max	Units	Conditions
125*	TdtV2ckL	SYNC RCV (MASTER & SLAVE) Data setup before CK \downarrow (DT setup time)	15		_	ns	
126*	TckL2dtl	Data hold after CK \downarrow (DT hold time)	15	_	_	ns	

These parameters are characterized but not tested.

†: Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.



Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Pa	ckage Group: (Ceramic CERDIP I	Dual In-Line (C	DP)		
		Millimeters			Inches		
Symbol	Min	Мах	Notes	Min	Мах	Notes	
α	0°	10°		0°	10°		
А	4.318	5.715		0.170	0.225		
A1	0.381	1.778		0.015	0.070		
A2	3.810	4.699		0.150	0.185		
A3	3.810	4.445		0.150	0.175		
В	0.355	0.585		0.014	0.023		
B1	1.270	1.651	Typical	0.050	0.065	Typical	
С	0.203	0.381	Typical	0.008	0.015	Typical	
D	51.435	52.705		2.025	2.075		
D1	48.260	48.260	Reference	1.900	1.900	Reference	
E	15.240	15.875		0.600	0.625		
E1	12.954	15.240		0.510	0.600		
e1	2.540	2.540	Reference	0.100	0.100	Reference	
eA	14.986	16.002	Typical	0.590	0.630	Typical	
eB	15.240	18.034		0.600	0.710		
L	3.175	3.810		0.125	0.150		
N	40	40		40	40		
S	1.016	2.286		0.040	0.090		
S1	0.381	1.778		0.015	0.070		

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