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### Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	I <sup>2</sup> C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	33
Program Memory Size	7KB (4K x 14)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	192 x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 6V
Data Converters	-
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Through Hole
Package / Case	40-DIP (0.600", 15.24mm)
Supplier Device Package	40-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16c65a-04-p

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#### **TABLE 3-3:** PIC16C64/64A/R64/65/65A/R65/67 PINOUT DESCRIPTION

Pin Name	DIP Pin#	PLCC Pin#	TQFP MQFP Pin#	Pin Type	Buffer Type	Description
OSC1/CLKIN	13	14	30	Ι	ST/CMOS(3)	Oscillator crystal input/external clock source input.
OSC2/CLKOUT	14	15	31	0	_	Oscillator crystal output. Connects to crystal or resonator in crystal oscillator mode. In RC mode, the pin outputs CLK- OUT which has 1/4 the frequency of OSC1, and denotes the instruction cycle rate.
MCLR/Vpp	1	2	18	I/P	ST	Master clear reset input or programming voltage input. This pin is an active low reset to the device.
						PORTA is a bi-directional I/O port.
RA0	2	3	19	I/O	TTL	
RA1	3	4	20	I/O	TTL	
RA2	4	5	21	I/O	TTL	
RA3	5	6	22	I/O	TTL	
RA4/T0CKI	6	7	23	I/O	ST	RA4 can also be the clock input to the Timer0 timer/counter. Output is open drain type.
RA5/SS	7	8	24	I/O	TTL	RA5 can also be the slave select for the synchronous serial port.
						PORTB is a bi-directional I/O port. PORTB can be software programmed for internal weak pull-up on all inputs.
RB0/INT	33	36	8	I/O	TTL/ST(4)	RB0 can also be the external interrupt pin.
RB1	34	37	9	I/O	TTL	
RB2	35	38	10	I/O	TTL	
RB3	36	39	11	I/O	TTL	
RB4	37	41	14	I/O	TTL	Interrupt on change pin.
RB5	38	42	15	I/O	TTL	Interrupt on change pin.
RB6	39	43	16	I/O	TTL/ST <sup>(5)</sup>	Interrupt on change pin. Serial programming clock.
RB7	40	44	17	I/O	TTL/ST <sup>(5)</sup>	Interrupt on change pin. Serial programming data.
						PORTC is a bi-directional I/O port.
RC0/T1OSO <sup>(1)</sup> /T1CKI	15	16	32	I/O	ST	RC0 can also be the Timer1 oscillator output <sup>(1)</sup> or Timer1 clock input.
RC1/T1OSI <sup>(1)</sup> /CCP2 <sup>(2)</sup>	16	18	35	I/O	ST	RC1 can also be the Timer1 oscillator input <sup>(1)</sup> or Capture2 input/Compare2 output/PWM2 output <sup>(2)</sup> .
RC2/CCP1	17	19	36	I/O	ST	RC2 can also be the Capture1 input/Compare1 out- put/PWM1 output.
RC3/SCK/SCL	18	20	37	I/O	ST	RC3 can also be the synchronous serial clock input/out- put for both SPI and I <sup>2</sup> C modes.
RC4/SDI/SDA	23	25	42	I/O	ST	RC4 can also be the SPI Data In (SPI mode) or data I/O (I <sup>2</sup> C mode).
RC5/SDO	24	26	43	I/O	ST	RC5 can also be the SPI Data Out (SPI mode).
RC6/TX/CK <sup>(2)</sup>	25	27	44	I/O	ST	RC6 can also be the USART Asynchronous Transmit <sup>(2)</sup> or Synchronous Clock <sup>(2)</sup> .
RC7/RX/DT <sup>(2)</sup>	26	29	1	I/O	ST	RC7 can also be the USART Asynchronous Receive <sup>(2)</sup> or Synchronous Data <sup>(2)</sup> .
Legend: I = input C	) = outp	ut	I/C	) = input/	output	P = power

— = Not used TTL = TTL input

ST = Schmitt Trigger input Note 1: Pin functions T1OSO and T1OSI are reversed on the PIC16C64.

2: CCP2 and the USART are not available on the PIC16C64/64A/R64.

3: This buffer is a Schmitt Trigger input when configured in RC oscillator mode and a CMOS input otherwise.

4: This buffer is a Schmitt Trigger input when configured as the external interrupt.

5: This buffer is a Schmitt Trigger input when used in serial programming mode.

6: This buffer is a Schmitt Trigger input when configured as general purpose I/O and a TTL input when used in the Parallel Slave Port mode (for interfacing to a microprocessor bus).

Example 4-1 shows the calling of a subroutine in page 1 of the program memory. This example assumes that the PCLATH is saved and restored by the interrupt service routine (if interrupts are used).

#### EXAMPLE 4-1: CALL OF A SUBROUTINE IN PAGE 1 FROM PAGE 0

ORG 0x5	00	
BSF	PCLATH, 3	;Select page 1 (800h-FFFh)
BCF	PCLATH,4	;Only on >4K devices
CALL	SUB1_P1	;Call subroutine in
	:	;page 1 (800h-FFFh)
	:	
	:	
ORG 0x9	00	
SUB1_P1	:	;called subroutine
	:	;page 1 (800h-FFFh)
	:	
RETURN		;return to Call subroutine ;in page 0 (000h-7FFh)

#### 4.5 Indirect Addressing, INDF and FSR Registers

Applicable	e Devices

61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67
----	----	-----	-----	----	-----	----	-----	-----	----	-----	-----	----	----

The INDF register is not a physical register. Addressing the INDF register will cause indirect addressing.

Indirect addressing is possible by using the INDF register. Any instruction using the INDF register actually accesses the register pointed to by the File Select Register, FSR. Reading the INDF register itself indirectly (FSR = '0') will produce 00h. Writing to the INDF register indirectly results in a no-operation (although status bits may be affected). An effective 9-bit address is obtained by concatenating the 8-bit FSR register and the IRP bit (STATUS<7>), as shown in Figure 4-25.

A simple program to clear RAM location 20h-2Fh using indirect addressing is shown in Example 4-2.

#### EXAMPLE 4-2: INDIRECT ADDRESSING

NEXT	movlw movwf clrf incf btfss	0x20 FSR INDF FSR,F FSR,4	;initialize pointer ; to RAM ;clear INDF register ;inc pointer ;all done?
	goto	NEXT	;NO, clear next
CONTINUE			
	:		;YES, continue

#### FIGURE 4-25: DIRECT/INDIRECT ADDRESSING



### 5.7 Parallel Slave Port

#### Applicable Devices

#### 61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

PORTD operates as an 8-bit wide parallel slave port (microprocessor port) when control bit PSPMODE (TRISE<4>) is set. In slave mode it is asynchronously readable and writable by the external world through  $\overline{\text{RD}}$  control input (RE0/ $\overline{\text{RD}}$ ) and  $\overline{\text{WR}}$  control input pin (RE1/ $\overline{\text{WR}}$ ).

It can directly interface to an 8-bit microprocessor data bus. The external microprocessor can read or write the PORTD latch as an 8-bit latch. Setting PSPMODE enables port pin RE0/RD to be the RD input, RE1/WR to be the WR input and RE2/CS to be the CS (chip select) input. For this functionality, the corresponding data direction bits of the TRISE register (TRISE<2:0>) must be configured as inputs (set).

There are actually two 8-bit latches, one for data-out (from the PIC16/17) and one for data input. The user writes 8-bit data to PORTD data latch and reads data from the port pin latch (note that they have the same address). In this mode, the TRISD register is ignored since the microprocessor is controlling the direction of data flow.

A write to the PSP occurs when both the  $\overline{CS}$  and  $\overline{WR}$  lines are first detected low. When either the  $\overline{CS}$  or  $\overline{WR}$  lines become high (level triggered), then the Input Buffer Full status flag bit IBF (TRISE<7>) is set on the Q4 clock cycle, following the next Q2 cycle, to signal the write is complete (Figure 5-12). The interrupt flag bit PSPIF (PIR1<7>) is also set on the same Q4 clock cycle. IBF can only be cleared by reading the PORTD input latch. The input Buffer Overflow status flag bit IBOV (TRISE<5>) is set if a second write to the Parallel Slave Port is attempted when the previous byte has not been read out of the buffer.

A read from the PSP occurs when both the  $\overline{CS}$  and  $\overline{RD}$  lines are first detected low. The Output Buffer Full status flag bit OBF (TRISE<6>) is cleared immediately (Figure 5-13) indicating that the PORTD latch is waiting to be read by the external bus. When either the  $\overline{CS}$  or  $\overline{RD}$  pin becomes high (level triggered), the interrupt flag bit PSPIF is set on the Q4 clock cycle, following the next Q2 cycle, indicating that the read is complete. OBF remains low until data is written to PORTD by the user firmware.

When not in Parallel Slave Port mode, the IBF and OBF bits are held clear. However, if flag bit IBOV was previously set, it must be cleared in firmware.

An interrupt is generated and latched into flag bit PSPIF when a read or write operation is completed. PSPIF must be cleared by the user in firmware and the interrupt can be disabled by clearing the interrupt enable bit PSPIE (PIE1<7>).

#### FIGURE 5-11: PORTD AND PORTE AS A PARALLEL SLAVE PORT



Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets
0Bh,8Bh 10Bh,18Bh	INTCON	GIE	PEIE	TOIE	INTE	RBIE	TOIF	INTF	RBIF	0000 000x	0000 000u
0Ch	PIR1	PSPIF <sup>(2)</sup>	(3)	RCIF <sup>(1)</sup>	TXIF <sup>(1)</sup>	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000	0000
0Dh <sup>(4)</sup>	PIR2	—	—	—	-	—	—	—	CCP2IF		
8Ch	PIE1	PSPIE <sup>(2)</sup>	(3)	RCIE <sup>(1)</sup>	TXIE <sup>(1)</sup>	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000	0000
8Dh <sup>(4)</sup>	PIE2	—	_	_	_	_	_	_	CCP2IE		
87h	TRISC	PORTC I	Data Direction	on register						1111 1111	1111 1111
11h	TMR2	Timer2 m	iodule's reg	ister						0000	0000
92h	PR2	Timer2 m	iodule's Per	iod register						1111 1111	1111 1111
12h	T2CON	—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000 0000	-000 0000
15h	CCPR1L	Capture/0	Compare/P	WM1 (LSB)				L		xxxx xxxx	uuuu uuuu
16h	CCPR1H	Capture/0	Compare/P	WM1 (MSB	)					xxxx xxxx	uuuu uuuu
17h	CCP1CON	—	_	CCP1X	CCP1Y	CCP1M3	CCP1M2	CCP1M1	CCP1M0	00 0000	00 0000
1Bh <sup>(4)</sup>	CCPR2L	Capture/0	Compare/P	WM2 (LSB)		·		·	·	xxxx xxxx	սսսս սսսս
1Ch <sup>(4)</sup>	CCPR2H	Capture/0	Compare/P	WM2 (MSB	)					xxxx xxxx	սսսս սսսս
1Dh <sup>(4)</sup>	CCP2CON	—	_	CCP2X	CCP2Y	CCP2M3	CCP2M2	CCP2M1	CCP2M0	00 0000	00 0000

### TABLE 10-5: REGISTERS ASSOCIATED WITH PWM AND TIMER2

 Legend:
 x = unknown, u = unchanged, - = unimplemented locations read as '0'. Shaded cells are not used in this mode.

 Note
 1:
 These bits are associated with the USART module, which is implemented on the PIC16C63/R63/65/65A/R65/66/67 only.

2: Bits PSPIE and PSPIF are reserved on the PIC16C62/62A/R62/63/R63/66, always maintain these bits clear.

3: The PIR1<6> and PIE1<6> bits are reserved, always maintain these bits clear.

4: These registers are associated with the CCP2 module, which is only implemented on the PIC16C63/R63/65/65A/R65/66/67.

Steps to follow when setting up an Asynchronous Transmission:

- 1. Initialize the SPBRG register for the appropriate baud rate. If a high speed baud rate is desired, then set bit BRGH. (Section 12.1).
- 2. Enable the asynchronous serial port by clearing bit SYNC and setting bit SPEN.
- 3. If interrupts are desired, then set enable bit TXIE.
- 4. If 9-bit transmission is desired, then set transmit bit TX9.

- 5. Enable the transmission by setting bit TXEN, which will also set bit TXIF.
- 6. If 9-bit transmission is selected, the ninth bit should be loaded in bit TX9D.
- 7. Load data to the TXREG register (starts transmission).

## FIGURE 12-8: ASYNCHRONOUS MASTER TRANSMISSION



#### FIGURE 12-9: ASYNCHRONOUS MASTER TRANSMISSION (BACK TO BACK)



#### TABLE 12-6: REGISTERS ASSOCIATED WITH ASYNCHRONOUS TRANSMISSION

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
0Ch	PIR1	PSPIF <sup>(1)</sup>	(2)	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
18h	RCSTA	SPEN	RX9	SREN	CREN	_	FERR	OERR	RX9D	0000 -00x	0000 -00x
19h	TXREG	USART Tra	ansmit R		0000 0000	0000 0000					
8Ch	PIE1	PSPIE <sup>(1)</sup>	(2)	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
98h	TXSTA	CSRC	ТХ9	TXEN	SYNC	_	BRGH	TRMT	TX9D	0000 -010	0000 -010
99h	SPBRG	SPBRG Baud Rate Generator Register									0000 0000

Legend: x = unknown, - = unimplemented locations read as '0'. Shaded cells are not used for Asynchronous Transmission.

Note 1: PSPIF and PSPIE are reserved on the PIC16C63/R63/66, always maintain these bits clear.

2: PIR1<6> and PIE1<6> are reserved, always maintain these bits clear.

#### 12.3 USART Synchronous Master Mode

#### Applicable Devices

#### 61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

In Synchronous Master mode the data is transmitted in a half-duplex manner i.e., transmission and reception do not occur at the same time. When transmitting data the reception is inhibited and vice versa. Synchronous mode is entered by setting bit SYNC (TXSTA<4>). In addition enable bit SPEN (RCSTA<7>) is set in order to configure the RC6 and RC7 I/O pins to CK (clock) and DT (data) lines respectively. The Master mode indicates that the processor transmits the master clock on the CK line. The Master mode is entered by setting bit CSRC (TXSTA<7>).

#### 12.3.1 USART SYNCHRONOUS MASTER TRANSMISSION

The USART transmitter block diagram is shown in Figure 12-7. The heart of the transmitter is the transmit (serial) shift register (TSR). The shift register obtains its data from the read/write transmit buffer register, TXREG. The TXREG register is loaded with data in software. The TSR register is not loaded until the last bit has been transmitted from the previous load. As soon as the last bit is transmitted, the TSR register is loaded with new data from the TXREG register (if available). Once the TXREG register transfers the data to the TSR register (occurs in one Tcycle), the TXREG register is empty and interrupt flag bit TXIF (PIR1<4>) is set. This interrupt can be enabled/disabled by setting/clearing enable bit TXIE (PIE1<4>). Flag bit TXIF will be set regardless of the status of enable bit TXIE and cannot be cleared in software. It will clear only when new data is loaded into the TXREG register. While flag bit TXIF indicates the status of the TXREG register, another bit, TRMT (TXSTA<1>), shows the status of the TSR register. Status bit TRMT is a read only bit which is set when the TSR register is empty. No interrupt logic is tied to this bit, so the user has to poll this bit in order to determine if the TSR register is empty. The TSR register is not mapped in data memory so it is not available to the user.

Transmission is enabled by setting enable bit TXEN (TXSTA<5>). The actual transmission will not occur until the TXREG register has been loaded with data. The first data bit will be shifted out on the next available rising edge of the clock on the CK line. Data out is stable around the falling edge of the synchronous clock (Figure 12-12). The transmission can also be started by first loading the TXREG register and then setting enable bit TXEN (Figure 12-13). This is advantageous when slow baud rates are selected, since the BRG is kept in reset when bits TXEN. CREN, and SREN are clear. Setting enable bit TXEN will start the BRG, creating a shift clock immediately. Normally when transmission is first started, the TSR register is empty, so a transfer to the TXREG register will result in an immediate transfer to TSR resulting in an empty TXREG register. Back-to-back transfers are possible.

Clearing enable bit TXEN, during a transmission, will cause the transmission to be aborted and will reset the transmitter. The DT and CK pins will revert to hi-impedance. If, during a transmission, either bit CREN or bit SREN is set the transmission is aborted and the DT pin reverts to a hi-impedance state (for a reception). The CK pin will remain an output if bit CSRC is set (internal clock). The transmitter logic however, is not reset although it is disconnected from the pins. In order to reset the transmitter, the user has to clear enable bit TXEN. If enable bit SREN is set (to interrupt an on going transmission and receive a single word), then after the single word is received, enable bit SREN will be cleared, and the serial port will revert back to transmitting since enable bit TXEN is still set. The DT line will immediately switch from hi-impedance receive mode to transmit and start driving. To avoid this, enable bit TXEN should be cleared.

In order to select 9-bit transmission, bit TX9 (TXSTA<6>) should be set and the ninth bit should be written to bit TX9D (TXSTA<0>). The ninth bit must be written before writing the 8-bit data to the TXREG register. This is because a data write to the TXREG register can result in an immediate transfer of the data to the TSR register (if the TSR is empty). If the TSR register was empty and the TXREG register was written before writing the "new" TX9D, the "present" value of bit TX9D is loaded.

Steps to follow when setting up a Synchronous Master Transmission:

- 1. Initialize the SPBRG register for the appropriate baud rate (Section 12.1).
- 2. Enable the synchronous master serial port by setting bits SYNC, SPEN, and CSRC.
- 3. If interrupts are desired, then set enable bit  $\ensuremath{\mathsf{TXIE}}$  .
- 4. If 9-bit transmission is desired, then set bit TX9.
- 5. Enable the transmission by setting enable bit TXEN.
- 6. If 9-bit transmission is selected, the ninth bit should be loaded in bit TX9D.
- 7. Start transmission by loading data to the TXREG register.

TABLE 13-9:	STATUS BITS AND THEIR SIGNIFICANCE FOR
	PIC16C62A/R62/63/R63/64A/R64/65A/R65/66/67

POR	BOR	то	PD	
0	x	1	1	Power-on Reset
0	x	0	x	Illegal, TO is set on a Power-on Reset
0	x	x	0	Illegal, PD is set on a Power-on Reset
1	0	x	x	Brown-out Reset
1	1	0	1	WDT Reset
1	1	0	0	WDT Wake-up
1	1	u	u	MCLR reset during normal operation
1	1	1	0	MCLR reset during SLEEP or interrupt wake-up from SLEEP

Legend: x = unknown, u = unchanged

### TABLE 13-10: RESET CONDITION FOR SPECIAL REGISTERS ON PIC16C61/62/64/65

	Program Counter	STATUS	PCON <sup>(2)</sup>
Power-on Reset	000h	0001 1xxx	0 -
MCLR reset during normal operation	000h	000u uuuu	u-
MCLR reset during SLEEP	000h	0001 0uuu	u-
WDT Reset	000h	0000 luuu	u-
WDT Wake-up	PC + 1	uuu0 0uuu	u-
Interrupt wake-up from SLEEP	PC + 1 <sup>(1)</sup>	uuul 0uuu	u-

Legend: u = unchanged, x = unknown, - = unimplemented bit read as '0'.

Note 1: When the wake-up is due to an interrupt and the global enable bit, GIE is set, the PC is loaded with the interrupt vector (0004h) after execution of PC+1.

2: The PCON register is not implemented on the PIC16C61.

#### TABLE 13-11: RESET CONDITION FOR SPECIAL REGISTERS ON PIC16C62A/R62/63/R63/64A/R64/65A/R65/66/67

	Program Counter	STATUS	PCON
Power-on Reset	000h	0001 1xxx	0x
MCLR reset during normal operation	000h	000u uuuu	uu
MCLR reset during SLEEP	000h	0001 0uuu	uu
WDT Reset	000h	0000 luuu	uu
Brown-out Reset	000h	0001 luuu	u0
WDT Wake-up	PC + 1	uuu0 0uuu	uu
Interrupt wake-up from SLEEP	PC + 1 <sup>(1)</sup>	uuul 0uuu	uu

Legend: u = unchanged, x = unknown, - = unimplemented bit read as '0'.

Note 1: When the wake-up is due to an interrupt and global enable bit, GIE is set, the PC is loaded with the interrupt vector (0004h) after execution of PC+1.

BCF	Bit Clear	f							
Syntax:	[ <i>label</i> ] BC	CF f,b							
Operands:	$\begin{array}{l} 0 \leq f \leq 12 \\ 0 \leq b \leq 7 \end{array}$	7							
Operation:	$0 \rightarrow (f < b;$	>)							
Status Affected:	None								
Encoding:	01	00bb	bfff	ffff					
Description:	Bit 'b' in re	gister 'f' is	s cleared.						
Words:	1								
Cycles:	1								
Q Cycle Activity:	Q1	Q2	Q3	Q4					
	Decode	Read register 'f'	Process data	Write register 'f'					
Example	BCF	FLAG_	REG, 7						
	Before Instruction FLAG_REG = 0xC7 After Instruction FLAG_REG = 0x47								

BTFSC	Bit Test,	Skip if Cl	ear							
Syntax:	[ <i>label</i> ] BT	FSC f,b								
Operands:	$0 \le f \le 12$	7								
	$0 \le b \le 7$									
Operation:	skip if (f<	b>) = 0								
Status Affected:	None									
Encoding:	01	10bb	bfff	ffff						
Description:	If bit 'b' in register 'f' is '1' then the next instruction is executed. If bit 'b', in register 'f', is '0' then the next instruction is discarded, and a NOP is executed instead, making this a 2Tcy instruction.									
Words:	1									
Cycles:	1(2)									
Q Cycle Activity:	Q1	Q2	Q3	Q4						
	Decode	Read register 'f'	Process data	No- Operation						
If Skip:	(2nd Cyc	le)								
	Q1	Q2	Q3	Q4						
	No- Operation	No- Operation	No- Operation	No- Operation						
Example	HERE FALSE TRUE	BTFSC GOTO •	FLAG,1 PROCESS_	_CODE						
	Before In	struction PC = a	ddress H	ERE						
	After Inst		- 0							

BSF	Bit Set f										
Syntax:	[ <i>label</i> ] BS	SF f,b									
Operands:	$\begin{array}{l} 0 \leq f \leq 12 \\ 0 \leq b \leq 7 \end{array}$	$\begin{array}{l} 0 \leq f \leq 127 \\ 0 \leq b \leq 7 \end{array}$									
Operation:	$1 \rightarrow (f < b >)$										
Status Affected:	None										
Encoding:	01	01bb	bfff	ffff							
Description:	Bit 'b' in re	gister 'f' is	s set.								
Words:	1										
Cycles:	1										
Q Cycle Activity:	Q1	Q2	Q3	Q4							
	Decode	Read register 'f'	Process data	Write register 'f'							
Example	BSF	FLAG_F	REG, 7								
	Before Instruction										
	After Instruction										
		FLAG_RE	EG = 0x8A	4							

PC = address TRUE if FLAG<1>=1, PC = address FALSE

Applicable Devices 61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

## 15.5 <u>Timing Diagrams and Specifications</u>

#### FIGURE 15-2: EXTERNAL CLOCK TIMING



### TABLE 15-2: EXTERNAL CLOCK TIMING REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Тур†	Мах	Units	Conditions
	Fosc	External CLKIN Frequency	DC	-	4	MHz	XT and RC osc mode
		(Note 1)	DC	_	4	MHz	HS osc mode (-04)
			DC	_	20	MHz	HS osc mode (-20)
			DC	_	200	kHz	LP osc mode
		Oscillator Frequency	DC	-	4	MHz	RC osc mode
		(Note 1)	0.1	_	4	MHz	XT osc mode
			1	_	4	MHz	HS osc mode (-04)
			1		20	MHz	HS osc mode (-20)
1	Tosc	External CLKIN Period	250	—	—	ns	XT and RC osc mode
		(Note 1)	250	—	—	ns	HS osc mode (-04)
			50	—	—	ns	HS osc mode (-20)
			5	_	—	μS	LP osc mode
		Oscillator Period	250	_	—	ns	RC osc mode
		(Note 1)	250	—	10,000	ns	XT osc mode
			250	—	1,000	ns	HS osc mode (-04)
			50	—	1,000	ns	HS osc mode (-20)
			5	_	—	μS	LP osc mode
2	Тсү	Instruction Cycle Time (Note 1)	1.0	Тсү	DC	μS	TCY = 4/Fosc
3	TosL,	External Clock in (OSC1) High or	50	—	—	ns	XT oscillator
	IosH	Low lime	2.5	—	—	μS	LP oscillator
			10	_	—	ns	HS oscillator
4	TosR,	External Clock in (OSC1) Rise or	25	—	—	ns	XT oscillator
	IOSF	Fall lime	50	—	—	ns	LP oscillator
			15	_	—	ns	HS oscillator

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Instruction cycle period (TcY) equals four times the input oscillator time-base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min." values with an external clock applied to the OSC1/CLKIN pin. When an external clock input is used, the "Max." cycle time limit is "DC" (no clock) for all devices.

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#### TABLE 17-8: SPI MODE REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Typ†	Мах	Units	Conditions
70	TssL2scH, TssL2scL	$\overline{SS}\downarrow$ to SCK $\downarrow$ or SCK $\uparrow$ input	Тсү	_	l	ns	
71	TscH	SCK input high time (slave mode)	TCY + 20	_	_	ns	
72	TscL	SCK input low time (slave mode)	Tcy + 20	—		ns	
73	TdiV2scH, TdiV2scL	Setup time of SDI data input to SCK edge	50	_		ns	
74	TscH2diL, TscL2diL	Hold time of SDI data input to SCK edge	50	_		ns	
75	TdoR	SDO data output rise time	_	10	25	ns	
76	TdoF	SDO data output fall time		10	25	ns	
77	TssH2doZ	SS↑ to SDO output hi-impedance	10	—	50	ns	
78	TscR	SCK output rise time (master mode)		10	25	ns	
79	TscF	SCK output fall time (master mode)	_	10	25	ns	
80	TscH2doV, TscL2doV	SDO data output valid after SCK edge	_	_	50	ns	

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

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	• •		<b>UL</b> , .		00		• •	• • • •		~~			00	•••

		Standard Operating Conditions (unless otherwise stated)								
		Operatio	na tomnor	ature	-40°	C < '	$T_{\Lambda} < \pm 125^{\circ}C$ for extended			
		operadi	ig temper	ature	/ +0 /0º	$T_{A} \leq 1.95^{\circ}C$ for industrial and				
DC CH/	ARACTERISTICS				$-40 \text{ C} \leq 14 \leq +60 \text{ C}$ for non-metric					
		<b>•</b>								
		Operating voltage VDD range as described in DC spec Section 18.1 and								
		Section	18.2			ц				
Param	Characteristic	Sym	Min	Тур	Max	Units	Conditions			
No.				1						
	Output High Voltage									
D090	I/O ports (Note 3)	VOH	VDD-0.7	-	-	V	IOH = -3.0 mA, VDD = 4.5V,			
							-40°C to +85°C			
D090A			VDD-0.7	-	-	V	IOH = -2.5 mA, VDD = 4.5V,			
							-40°C to +125°C			
D092	OSC2/CLKOUT (RC osc config)		VDD-0.7	-	-	v	IOH = -1.3 mA, VDD = 4.5V,			
							-40°C to +85°C			
D092A			VDD-0.7	-	-	v	IOH = -1.0 mA, VDD = 4.5V,			
							-40°C to +125°C			
D150*	Open-Drain High Voltage	Vod	-	-	14	V	RA4 pin			
	Capacitive Loading Specs on Out-									
	put Pins									
D100	OSC2 pin	Cosc <sub>2</sub>	-	-	15	pF	In XT, HS and LP modes when			
							external clock is used to drive			
							OSC1.			
D101	All I/O pins and OSC2 (in RC mode)	Cio	-	-	50	pF				
D102	SCL, SDA in I <sup>2</sup> C mode	Cb	-	-	400	pF				

These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C6X be driven with external clock in RC mode.

2: The leakage current on the MCLR/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as current sourced by the pin.

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#### 19.2 DC Characteristics: PIC16LC65-04 (Commercial, Industrial)

	Standard Operating Conditions (unless otherwise stated)												
DC CH	ARACTERISTICS	Operatir	ng temp	perature	e -40	°C ≤	$IA \le +85^{\circ}C$ for industrial and						
				i	0-0	,	$IA \leq +70^{\circ}C$ for commercial						
Param No.	Characteristic	Sym	Min	Тур†	Max	Units	Conditions						
D001	Supply Voltage	Vdd	3.0	-	6.0	V	LP, XT, RC osc configuration (DC - 4 MHz)						
D002*	RAM Data Retention Voltage (Note 1)	Vdr	-	1.5	-	V							
D003	VDD start voltage to ensure internal Power-on Reset signal	VPOR	-	Vss	-	V	See section on Power-on Reset for details						
D004*	VDD rise rate to ensure internal Power-on Reset signal	SVDD	0.05	-	-	V/ms	See section on Power-on Reset for details						
D010	Supply Current (Note 2, 5)	IDD	-	2.0	3.8	mA	XT, RC osc configuration Fosc = 4 MHz, VDD = 3.0V (Note 4)						
D010A			-	22.5	105	μA	LP osc configuration Fosc = 32 kHz, VDD = 4.0V, WDT disabled						
D020	Power-down Current	IPD	-	7.5	800	μA	VDD = 3.0V, WDT enabled, -40°C to +85°C						
D021	(Note 3, 5)		-	0.9	800	μA	VDD = 3.0V, WDT disabled, 0°C to +70°C						
D021A			-	0.9	800	μA	VDD = $3.0V$ , WDT disabled, $-40^{\circ}C$ to $+85^{\circ}C$						

These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.

The test conditions for all IDD measurements in active operation mode are:

OSC1 = external square wave, from rail to rail; all I/O pins tristated, pulled to VDD,

 $\overline{MCLR} = VDD$ ; WDT enabled/disabled as specified.

- 3: The power down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and Vss.
- 4: For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula Ir = VDD/2Rext (mA) with Rext in kOhm.
- 5: Timer1 oscillator (when enabled) adds approximately 20 μA to the specification. This value is from characterization and is for design guidance only. This is not tested.

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## FIGURE 19-3: CLKOUT AND I/O TIMING



TABLE 19-3-	CLKOUT AND I/O TIMING REQUIREMENTS.
TADLL 13-3.	

Parameter	Sym	Characteristic		Min	Typ†	Max	Units	Conditions
No.								
10*	TosH2ckL	OSC1↑ to CLKOUT↓		_	75	200	ns	Note 1
11*	TosH2ckH	OSC1↑ to CLKOUT↑		—	75	200	ns	Note 1
12*	TckR	CLKOUT rise time	—	35	100	ns	Note 1	
13*	TckF	CLKOUT fall time		—	35	100	ns	Note 1
14*	TckL2ioV	CLKOUT $\downarrow$ to Port out valid		—		0.5TCY + 20	ns	Note 1
15*	TioV2ckH	Port in valid before CLKOUT ↑	Port in valid before CLKOUT 1			_	ns	Note 1
16*	TckH2iol	Port in hold after CLKOUT $\uparrow$	0		_	ns	Note 1	
17*	TosH2ioV	OSC1 <sup>↑</sup> (Q1 cycle) to Port out v	valid	—	50	150	ns	
18*	TosH2iol	OSC1↑ (Q2 cycle) to Port	PIC16 <b>C</b> 65	100		_	ns	
		input invalid (I/O in hold time)	PIC16 <b>LC</b> 65	200		_	ns	
19*	TioV2osH	Port input valid to OSC1 <sup>↑</sup> (I/O i	n setup time)	0		_	ns	
20*	TioR	Port output rise time	PIC16 <b>C</b> 65	—	10	25	ns	
			PIC16 <b>LC</b> 65	—		60	ns	
21*	TioF	Port output fall time	PIC16 <b>C</b> 65	—	10	25	ns	
			PIC16 <b>LC</b> 65	—		60	ns	
22††*	Tinp	RB0/INT pin high or low time	pin high or low time		-	—	ns	
23††*	Trbp	RB7:RB4 change int high or low	w time	TCY	_	_	ns	

\* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

these parameters are asynchronous events not related to any internal clock edge.

Note 1: Measurements are taken in RC Mode where CLKOUT output is 4 x Tosc.

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### FIGURE 19-6: CAPTURE/COMPARE/PWM TIMINGS (CCP1 AND CCP2)

TABLE 19-6: CAPTURE/COMPARE/PWM REQUIREMENTS (CCP1 AND CCP2)

Parameter No.	Sym	Characteristic			Min	Тур†	Max	Units	Conditions
50*	TccL	CCP1 and CCP2	No Prescaler		0.5TCY + 20	—		ns	
		input low time	uput low time With Prescaler		10	—	_	ns	
				PIC16 <b>LC</b> 65	20	—	—	ns	
51*	TccH	CCP1 and CCP2	No Prescaler		0.5TCY + 20	—	—	ns	
	input high time	input high time	With Prescaler	PIC16 <b>C</b> 65	10	_	_	ns	
				PIC16 <b>LC</b> 65	20	—	—	ns	
52*	TccP	CCP1 and CCP2 in	nput period		<u>3Tcy + 40</u> N	-	—	ns	N = prescale value (1,4, or 16)
53	TccR	CCP1 and CCP2 c	output rise time	PIC16 <b>C</b> 65	—	10	25	ns	
				PIC16 <b>LC</b> 65	_	25	45	ns	
54	TccF	CCP1 and CCP2 c	output fall time	PIC16 <b>C</b> 65	_	10	25	ns	
				PIC16 <b>LC</b> 65	_	25	45	ns	

\* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Applicable Devices 61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67



## FIGURE 21-7: CAPTURE/COMPARE/PWM TIMINGS (CCP1 AND CCP2)

#### TABLE 21-6: CAPTURE/COMPARE/PWM REQUIREMENTS (CCP1 AND CCP2)

Param No.	Sym	Characteristic	Min	Тур†	Max	Units	Conditions		
50*	TccL	CCP1 and CCP2	No Prescaler		0.5TCY + 20	_	_	ns	
		input low time	With Prescaler	PIC16CR63/R65	10	—	—	ns	
				PIC16LCR63/R65	20	—	_	ns	
51*	TccH	CCP1 and CCP2	No Prescaler		0.5TCY + 20	—	_	ns	
	input high time	With Prescaler	PIC16CR63/R65	10		_	ns		
				PIC16LCR63/R65	20		_	ns	
52*	TccP	CCP1 and CCP2 ir	nput period		<u>3Tcy + 40</u> N		-	ns	N = prescale value (1,4, or 16)
53*	TccR	CCP1 and CCP2 o	utput rise time	PIC16CR63/R65	—	10	25	ns	
				PIC16LCR63/R65	—	25	45	ns	
54*	TccF	CCP1 and CCP2 o	utput fall time	PIC16CR63/R65	—	10	25	ns	
				PIC16LCR63/R65	_	25	45	ns	

\* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

### Applicable Devices 61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

## FIGURE 22-14: I<sup>2</sup>C BUS DATA TIMING



### TABLE 22-10: I<sup>2</sup>C BUS DATA REQUIREMENTS

Parameter	Sym	Characteristic		Min	Max	Units	Conditions
No.							
100*	THIGH	Clock high time	100 kHz mode	4.0	—	μs	Device must operate at a mini- mum of 1.5 MHz
			400 kHz mode	0.6	_	μs	Device must operate at a mini- mum of 10 MHz
			SSP Module	1.5TCY	_		
101*	TLOW	Clock low time	100 kHz mode	4.7	—	μs	Device must operate at a mini- mum of 1.5 MHz
			400 kHz mode	1.3	—	μs	Device must operate at a mini- mum of 10 MHz
			SSP Module	1.5TCY	—		
102*	TR	SDA and SCL rise	100 kHz mode	—	1000	ns	
		time	400 kHz mode	20 + 0.1Cb	300	ns	Cb is specified to be from 10-400 pF
103*	TF	SDA and SCL fall time	100 kHz mode	_	300	ns	
			400 kHz mode	20 + 0.1Cb	300	ns	Cb is specified to be from 10-400 pF
90*	TSU:STA	START condition	100 kHz mode	4.7	—	μs	Only relevant for repeated
		setup time	400 kHz mode	0.6	_	μs	START condition
91*	THD:STA	START condition hold	100 kHz mode	4.0	—	μs	After this period the first clock
		time	400 kHz mode	0.6	—	μs	pulse is generated
106*	THD:DAT	Data input hold time	100 kHz mode	0	—	ns	_
			400 kHz mode	0	0.9	μs	
107*	TSU:DAT	Data input setup time	100 kHz mode	250	—	ns	Note 2
			400 kHz mode	100	—	ns	
92*	TSU:STO	STOP condition setup	100 kHz mode	4.7	—	μs	_
		time	400 kHz mode	0.6	_	μs	
109*	TAA	Output valid from	100 kHz mode	—	3500	ns	Note 1
		clock	400 kHz mode	—	—	ns	
110*	TBUF	Bus free time	100 kHz mode	4.7	_	μS	Time the bus must be free
			400 kHz mode	1.3	—	μs	betore a new transmission can start
	Cb	Bus capacitive loading		—	400	pF	

These parameters are characterized but not tested.

Note 1: As a transmitter, the device must provide this internal minimum delay time to bridge the undefined region (min. 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

2: A fast-mode (400 kHz) I<sup>2</sup>C-bus device can be used in a standard-mode (100 kHz) I<sup>2</sup>C-bus system, but the requirement Tsu:DAT ≥ 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line TR max.+tsu;DAT = 1000 + 250 = 1250 ns (according to the standard-mode I<sup>2</sup>C bus specification) before the SCL line is released.







Data based on matrix samples. See first page of this section for details.

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#### FIGURE 23-29: TYPICAL IDD vs. FREQUENCY (HS MODE, 25°C)



#### FIGURE 23-30: MAXIMUM IDD vs. FREQUENCY (HS MODE, -40°C TO 85°C)



### 24.9 28-Lead Ceramic Side Brazed Dual In-Line with Window (300 mil) (JW)

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Package Group: Ceramic Side Brazed Dual In-Line (CER)							
Symbol	Millimeters			Inches			
	Min	Max	Notes	Min	Max	Notes	
α	0°	10°		0°	10°		
А	3.937	5.030		0.155	0.198		
A1	1.016	1.524		0.040	0.060		
A2	2.921	3.506		0.115	0.138		
A3	1.930	2.388		0.076	0.094		
В	0.406	0.508		0.016	0.020		
B1	1.219	1.321	Typical	0.048	0.052		
С	0.228	0.305	Typical	0.009	0.012		
D	35.204	35.916		1.386	1.414		
D1	32.893	33.147	Reference	1.295	1.305		
E	7.620	8.128		0.300	0.320		
E1	7.366	7.620		0.290	0.300		
e1	2.413	2.667	Typical	0.095	0.105		
eA	7.366	7.874	Reference	0.290	0.310		
eB	7.594	8.179		0.299	0.322		
L	3.302	4.064		0.130	0.160		
Ν	28	28		28	28		
S	1.143	1.397		0.045	0.055		
S1	0.533	0.737		0.021	0.029		

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