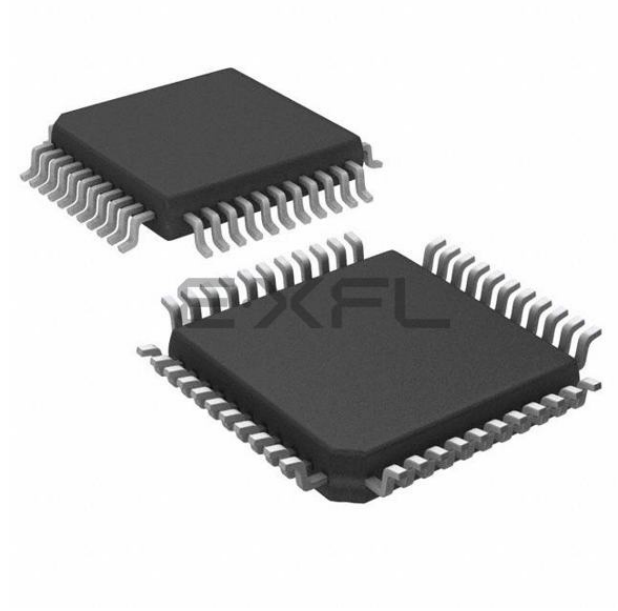

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	33
Program Memory Size	7KB (4K x 14)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	192 x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 6V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-QFP
Supplier Device Package	44-MQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16c65a-04i-pq

4.2.2.3 INTCON REGISTER

Applicable Devices													
61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67

The INTCON Register is a readable and writable register which contains the various enable and flag bits for the TMR0 register overflow, RB port change and external RB0/INT pin interrupts.

Note: Interrupt flag bits get set when an interrupt condition occurs regardless of the state of its corresponding enable bit or the global enable bit, GIE (INTCON<7>).

FIGURE 4-11: INTCON REGISTER (ADDRESS 0Bh, 8Bh, 10Bh 18Bh)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-x
GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n = Value at POR reset
x = unknown

bit 7: **GIE:**(1) Global Interrupt Enable bit
1 = Enables all un-masked interrupts
0 = Disables all interrupts

bit 6: **PEIE:**(2) Peripheral Interrupt Enable bit
1 = Enables all un-masked peripheral interrupts
0 = Disables all peripheral interrupts

bit 5: **T0IE:** TMR0 Overflow Interrupt Enable bit
1 = Enables the TMR0 overflow interrupt
0 = Disables the TMR0 overflow interrupt

bit 4: **INTE:** RB0/INT External Interrupt Enable bit
1 = Enables the RB0/INT external interrupt
0 = Disables the RB0/INT external interrupt

bit 3: **RBIE:** RB Port Change Interrupt Enable bit
1 = Enables the RB port change interrupt
0 = Disables the RB port change interrupt

bit 2: **T0IF:** TMR0 Overflow Interrupt Flag bit
1 = TMR0 register overflowed (must be cleared in software)
0 = TMR0 register did not overflow

bit 1: **INTF:** RB0/INT External Interrupt Flag bit
1 = The RB0/INT external interrupt occurred (must be cleared in software)
0 = The RB0/INT external interrupt did not occur

bit 0: **RBIF:** RB Port Change Interrupt Flag bit
1 = At least one of the RB7:RB4 pins changed state (see Section 5.2 to clear the interrupt)
0 = None of the RB7:RB4 pins have changed state

Note 1: For the PIC16C61/62/64/65, if an interrupt occurs while the GIE bit is being cleared, the GIE bit may unintentionally be re-enabled by the RETFIE instruction in the user's Interrupt Service Routine. Refer to Section 13.5 for a detailed description.
2: The PEIE bit (bit6) is unimplemented on the PIC16C61, read as '0'.

Interrupt flag bits get set when an interrupt condition occurs regardless of the state of its corresponding enable bit or the global enable bit, GIE (INTCON<7>). User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

5.3 PORTC and TRISC Register

Applicable Devices													
61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67

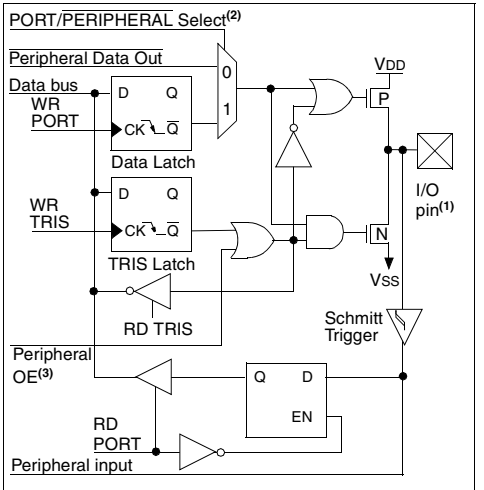
PORTC is an 8-bit wide bi-directional port. Each pin is individually configurable as an input or output through the TRISC register. PORTC is multiplexed with several peripheral functions (Table 5-5). PORTC pins have Schmitt Trigger input buffers.

When enabling peripheral functions, care should be taken in defining TRIS bits for each PORTC pin. Some peripherals override the TRIS bit to make a pin an output, while other peripherals override the TRIS bit to make a pin an input. Since the TRIS bit override is in effect while the peripheral is enabled, read-modify-write instructions (`BSF, BCF, XORWF`) with TRISC as destination should be avoided. The user should refer to the corresponding peripheral section for the correct TRIS bit settings.

EXAMPLE 5-3: INITIALIZING PORTC

```
BCF     STATUS, RP0   ;
BCF     STATUS, RP1   ; PIC16C66/67 only
CLRF    PORTC         ; Initialize PORTC by
                      ; clearing output
                      ; data latches
BSF     STATUS, RP0   ; Select Bank 1
MOVLW   0xCF          ; Value used to
                      ; initialize data
                      ; direction
MOVWF   TRISC         ; Set RC<3:0> as inputs
                      ; RC<5:4> as outputs
                      ; RC<7:6> as inputs
```

FIGURE 5-6: PORTC BLOCK DIAGRAM



Note 1: I/O pins have diode protection to VDD and VSS.
2: Port/Peripheral select signal selects between port data and peripheral output.
3: Peripheral OE (output enable) is only activated if peripheral select is active.

TABLE 5-5: PORTC FUNCTIONS FOR PIC16C62/64

Name	Bit#	Buffer Type	Function
RC0/T1OSI/T1CKI	bit0	ST	Input/output port pin or Timer1 oscillator input or Timer1 clock input
RC1/T1OSO	bit1	ST	Input/output port pin or Timer1 oscillator output
RC2/CCP1	bit2	ST	Input/output port pin or Capture1 input/Compare1 output/PWM1 output
RC3/SCK/SCL	bit3	ST	RC3 can also be the synchronous serial clock for both SPI and I^2C modes.
RC4/SDI/SDA	bit4	ST	RC4 can also be the SPI Data In (SPI mode) or data I/O (I^2C mode).
RC5/SDO	bit5	ST	Input/output port pin or synchronous serial port data output
RC6	bit6	ST	Input/output port pin
RC7	bit7	ST	Input/output port pin

Legend: ST = Schmitt Trigger input

6.0 OVERVIEW OF TIMER MODULES

Applicable Devices													
61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67

All PIC16C6X devices have three timer modules except for the PIC16C61, which has one timer module. Each module can generate an interrupt to indicate that an event has occurred (i.e., timer overflow). Each of these modules are detailed in the following sections. The timer modules are:

- Timer0 module (Section 7.0)
- Timer1 module (Section 8.0)
- Timer2 module (Section 9.0)

6.1 Timer0 Overview

Applicable Devices													
61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67

The Timer0 module is a simple 8-bit overflow counter. The clock source can be either the internal system clock (Fosc/4) or an external clock. When the clock source is an external clock, the Timer0 module can be selected to increment on either the rising or falling edge.

The Timer0 module also has a programmable prescaler option. This prescaler can be assigned to either the Timer0 module or the Watchdog Timer. Bit PSA (OPTION<3>) assigns the prescaler, and bits PS2:PS0 (OPTION<2:0>) determine the prescaler value. TMR0 can increment at the following rates: 1:1 when the prescaler is assigned to Watchdog Timer, 1:2, 1:4, 1:8, 1:16, 1:32, 1:64, 1:128, and 1:256.

Synchronization of the external clock occurs after the prescaler. When the prescaler is used, the external clock frequency may be higher then the device's frequency. The maximum frequency is 50 MHz, given the high and low time requirements of the clock.

6.2 Timer1 Overview

Applicable Devices													
61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67

Timer1 is a 16-bit timer/counter. The clock source can be either the internal system clock (Fosc/4), an external clock, or an external crystal. Timer1 can operate as either a timer or a counter. When operating as a counter (external clock source), the counter can either operate synchronized to the device or asynchronously to the device. Asynchronous operation allows Timer1 to operate during sleep, which is useful for applications that require a real-time clock as well as the power savings of SLEEP mode.

TImer1 also has a prescaler option which allows TMR1 to increment at the following rates: 1:1, 1:2, 1:4, and 1:8. TMR1 can be used in conjunction with the Capture/Compare/PWM module. When used with a CCP module, Timer1 is the time-base for 16-bit capture or 16-bit compare and must be synchronized to the device.

6.3 Timer2 Overview

Applicable Devices													
61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67

Timer2 is an 8-bit timer with a programmable prescaler and a programmable postscaler, as well as an 8-bit Period Register (PR2). Timer2 can be used with the CCP module (in PWM mode) as well as the Baud Rate Generator for the Synchronous Serial Port (SSP). The prescaler option allows Timer2 to increment at the following rates: 1:1, 1:4, and 1:16.

The postscaler allows TMR2 register to match the period register (PR2) a programmable number of times before generating an interrupt. The postscaler can be programmed from 1:1 to 1:16 (inclusive).

6.4 CCP Overview

Applicable Devices													
61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67

The CCP module(s) can operate in one of three modes: 16-bit capture, 16-bit compare, or up to 10-bit Pulse Width Modulation (PWM).

Capture mode captures the 16-bit value of TMR1 into the CCPRxH:CCPRxL register pair. The capture event can be programmed for either the falling edge, rising edge, fourth rising edge, or sixteenth rising edge of the CCPx pin.

Compare mode compares the TMR1H:TMR1L register pair to the CCPRxH:CCPRxL register pair. When a match occurs, an interrupt can be generated and the output pin CCPx can be forced to a given state (High or Low) and Timer1 can be reset. This depends on control bits CCPxM3:CCPxM0.

PWM mode compares the TMR2 register to a 10-bit duty cycle register (CCPRxH:CCPRxL<5:4>) as well as to an 8-bit period register (PR2). When the TMR2 register = Duty Cycle register, the CCPx pin will be forced low. When TMR2 = PR2, TMR2 is cleared to 00h, an interrupt can be generated, and the CCPx pin (if an output) will be forced high.

7.3 Prescaler

Applicable Devices													
61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67

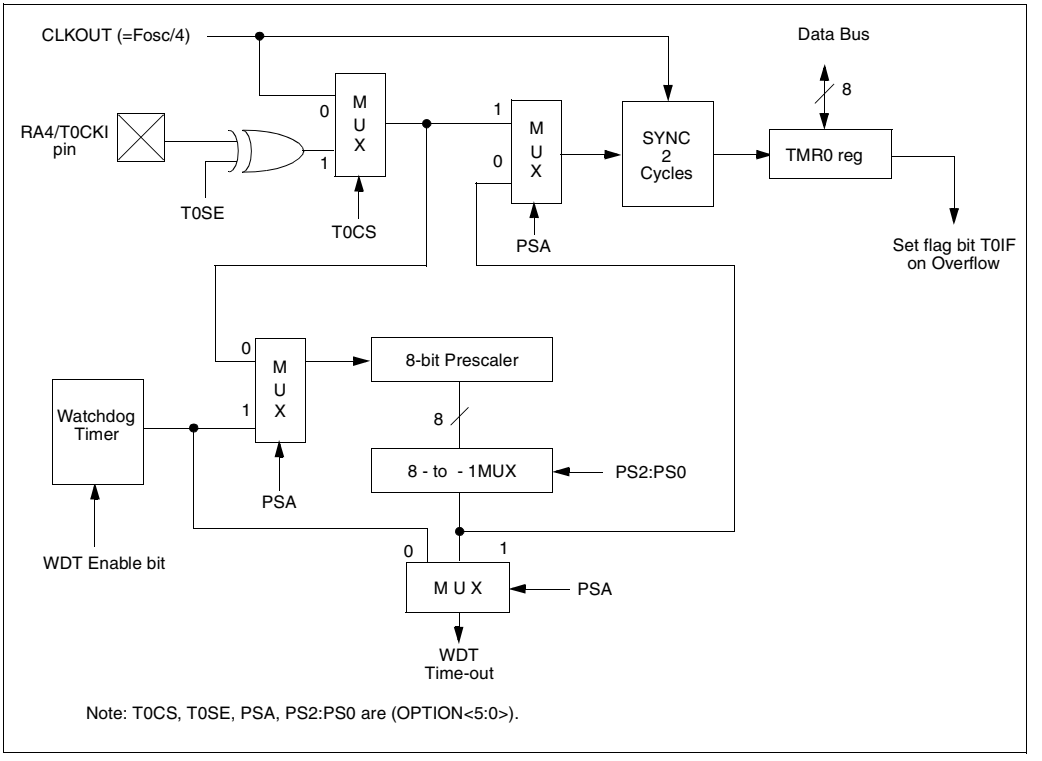
An 8-bit counter is available as a prescaler for the Timer0 module or as a postscaler for the Watchdog Timer (WDT), respectively (Figure 7-6). For simplicity, this counter is being referred to as "prescaler" throughout this data sheet. Note that the prescaler may be used by either the Timer0 module or the Watchdog Timer, but not both. Thus, a prescaler assignment for the Timer0 module means that there is no prescaler for the Watchdog Timer, and vice-versa.

The PSA and PS2:PS0 bits (OPTION<3:0>) determine the prescaler assignment and prescale ratio.

When assigned to the Timer0 module, all instructions writing to the TMR0 register (e.g. `CLRF TMR0`, `MOVWF TMR0`, `BSF TMR0,bitx`) will clear the prescaler count. When assigned to the Watchdog Timer, a `CLRWDT` instruction will clear the Watchdog Timer and the prescaler count. The prescaler is not readable or writable.

Note:	Writing to TMR0 when the prescaler is assigned to Timer0 will clear the prescaler count, but will not change the prescaler assignment.

FIGURE 7-6: BLOCK DIAGRAM OF THE TIMER0/WDT PRESCALER



Note: T0CS, T0SE, PSA, PS2:PS0 are (OPTION<5:0>).

8.3 Timer1 Operation in Asynchronous Counter Mode

Applicable Devices													
61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67

If control bit $\overline{\text{T1SYNC}}$ (T1CON<2>) is set, the external clock input is not synchronized. The timer continues to increment asynchronous to the internal phase clocks. The timer will continue to run during SLEEP and generate an interrupt on overflow which will wake the processor. However, special precautions in software are needed to read-from or write-to the Timer1 register pair, TMR1L and TMR1H (Section 8.3.2).

In asynchronous counter mode, Timer1 cannot be used as a time-base for capture or compare operations.

8.3.1 EXTERNAL CLOCK INPUT TIMING WITH UNSYNCHRONIZED CLOCK

If control bit $\overline{\text{T1SYNC}}$ is set, the timer will increment completely asynchronously. The input clock must meet certain minimum high time and low time requirements, as specified in timing parameters (45 - 47).

8.3.2 READING AND WRITING TMR1 IN ASYNCHRONOUS COUNTER MODE

Reading TMR1H or TMR1L, while the timer is running from an external asynchronous clock, will ensure a valid read (taken care of in hardware). However, the user should keep in mind that reading the 16-bit timer in two 8-bit values itself poses certain problems since the timer may overflow between the reads.

For writes, it is recommended that the user simply stop the timer and write the desired values. A write contention may occur by writing to the timer registers while the register is incrementing. This may produce an unpredictable value in the timer register.

Reading the 16-bit value requires some care. Example 8-1 is an example routine to read the 16-bit timer value. This is useful if the timer cannot be stopped.

EXAMPLE 8-1: READING A 16-BIT FREE-RUNNING TIMER

```
;  All Interrupts are disabled
    MOVF    TMR1H,  W       ;Read high byte
    MOVWF   TMPH            ;
    MOVF    TMR1L,  W       ;Read low byte
    MOVWF   TMPL            ;
    MOVF    TMR1H,  W       ;Read high byte
    SUBWF   TMPH,   W       ;Sub 1st read
                            ;with 2nd read
    BTFSC   STATUS,Z        ;is result = 0
    GOTO    CONTINUE        ;Good 16-bit read
; TMR1L may have rolled over between the read
; of the high and low bytes. Reading the high
; and low bytes now will read a good value.
    MOVF    TMR1H,  W       ;Read high byte
    MOVWF   TMPH            ;
    MOVF    TMR1L,  W       ;Read low byte
    MOVWF   TMPL            ;
;   Re-enable Interrupt (if required)
CONTINUE                    ;Continue with
    :                       ;your code
```

8.4 Timer1 Oscillator

Applicable Devices													
61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67

A crystal oscillator circuit is built in-between pins T1OSI (input) and T1OSO (amplifier output). It is enabled by setting control bit T1OSCEN (T1CON<3>). The oscillator is a low power oscillator rated up to 200 kHz. It will continue to run during SLEEP. It is primarily intended for a 32 kHz crystal. Table 8-1 shows the capacitor selection for the Timer1 oscillator.

The Timer1 oscillator is identical to the LP oscillator. The user must allow a software time delay to ensure proper oscillator start-up.

TABLE 8-1: CAPACITOR SELECTION FOR THE TIMER1 OSCILLATOR

Osc Type	Freq	C1	C2
LP	32 kHz	33 pF	33 pF
	100 kHz	15 pF	15 pF
	200 kHz	15 pF	15 pF
These values are for design guidance only.			
Crystals Tested:			
32.768 kHz	Epson C-001R32.768K-A		± 20 PPM
100 kHz	Epson C-2 100.00 KC-P		± 20 PPM
200 kHz	STD XTL 200.000 kHz		± 20 PPM

Note 1: Higher capacitance increases the stability of oscillator but also increases the start-up time.

2: Since each resonator/crystal has its own characteristics, the user should consult the resonator/crystal manufacturer for appropriate values of external components.

TABLE 10-5: REGISTERS ASSOCIATED WITH PWM AND TIMER2

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets
0Bh,8Bh 10Bh,18Bh	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000u
0Ch	PIR1	PSPIF(2)	(3)	RCIF(1)	TXIF(1)	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
0Dh(4)	PIR2	—	—	—	—	—	—	—	CCP2IF	---- --- 0	---- --- 0
8Ch	PIE1	PSPIE(2)	(3)	RCIE(1)	TXIE(1)	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
8Dh(4)	PIE2	—	—	—	—	—	—	—	CCP2IE	---- --- 0	---- --- 0
87h	TRISC	PORTC Data Direction register								1111 1111	1111 1111
11h	TMR2	Timer2 module's register								0000 0000	0000 0000
92h	PR2	Timer2 module's Period register								1111 1111	1111 1111
12h	T2CON	—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000 0000	-000 0000
15h	CCPR1L	Capture/Compare/PWM1 (LSB)								xxxx xxxx	uuuu uuuu
16h	CCPR1H	Capture/Compare/PWM1 (MSB)								xxxx xxxx	uuuu uuuu
17h	CCP1CON	—	—	CCP1X	CCP1Y	CCP1M3	CCP1M2	CCP1M1	CCP1M0	--00 0000	--00 0000
1Bh(4)	CCPR2L	Capture/Compare/PWM2 (LSB)								xxxx xxxx	uuuu uuuu
1Ch(4)	CCPR2H	Capture/Compare/PWM2 (MSB)								xxxx xxxx	uuuu uuuu
1Dh(4)	CCP2CON	—	—	CCP2X	CCP2Y	CCP2M3	CCP2M2	CCP2M1	CCP2M0	--00 0000	--00 0000

Legend: x = unknown, u = unchanged, - = unimplemented locations read as '0'. Shaded cells are not used in this mode.

Note 1: These bits are associated with the USART module, which is implemented on the PIC16C63/R63/65/65A/R65/66/67 only.

2: Bits PSPIE and PSPIF are reserved on the PIC16C62/62A/R62/63/R63/66, always maintain these bits clear.

3: The PIR1<6> and PIE1<6> bits are reserved, always maintain these bits clear.

4: These registers are associated with the CCP2 module, which is only implemented on the PIC16C63/R63/65/65A/R65/66/67.

12.1.1 SAMPLING

The data on the RC7/RX/DT pin is sampled three times by a majority detect circuit to determine if a high or a low level is present at the RX pin. If bit BRGH (TXSTA<2>) is clear (i.e., at the low baud rates), the sampling is done on the seventh, eighth and ninth falling edges of a x16 clock (Figure 12-3). If bit BRGH is set (i.e., at the high baud rates), the sampling is done on the 3 clock edges preceding the second rising edge after the first falling edge of a x4 clock (Figure 12-4 and Figure 12-5).

FIGURE 12-3: RX PIN SAMPLING SCHEME (BRGH = 0) PIC16C63/R63/65/65A/R65)

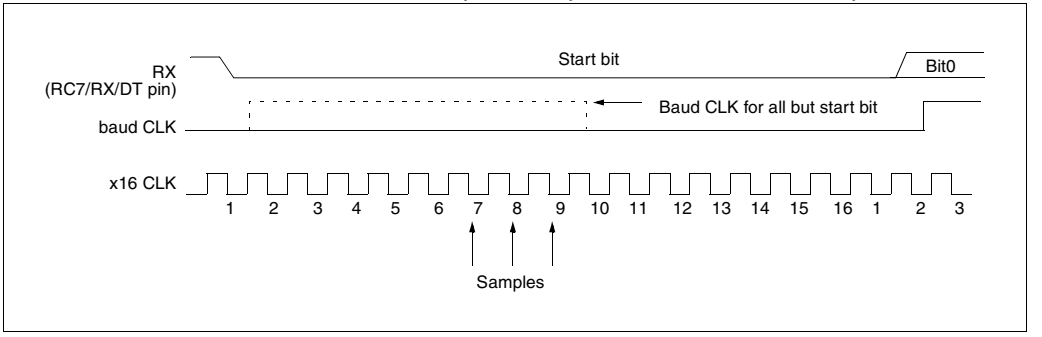


FIGURE 12-4: RX PIN SAMPLING SCHEME (BRGH = 1) (PIC16C63/R63/65/65A/R65)

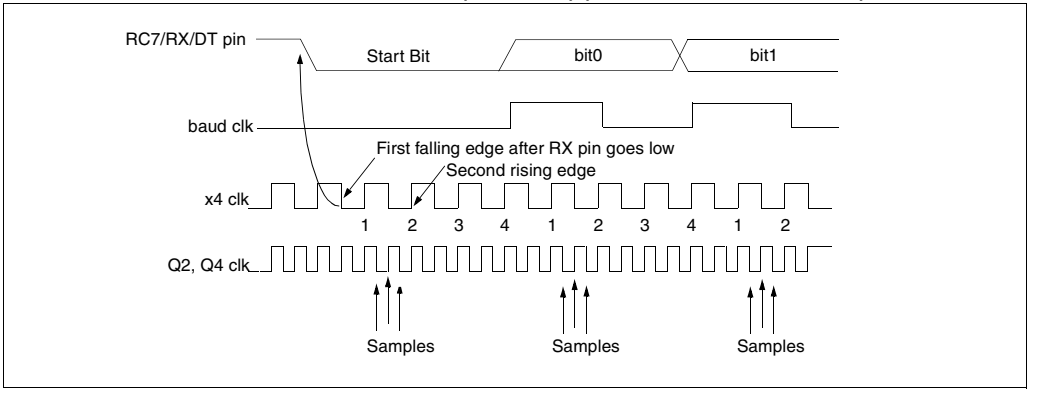


FIGURE 12-5: RX PIN SAMPLING SCHEME (BRGH = 1) (PIC16C63/R63/65/65A/R65)

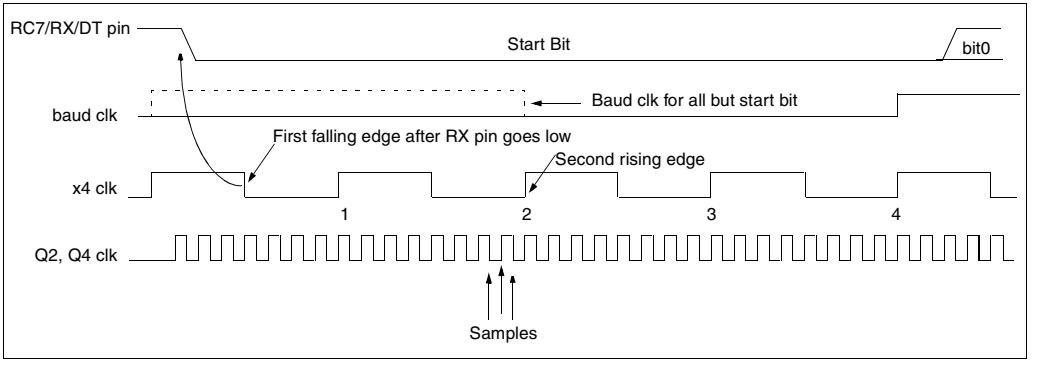


TABLE 12-8: REGISTERS ASSOCIATED WITH SYNCHRONOUS MASTER TRANSMISSION

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
0Ch	PIR1	PSPIF(1)	(2)	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
18h	RCSTA	SPEN	RX9	SREN	CREN	—	FERR	OERR	RX9D	0000 -00x	0000 -00x
19h	TXREG	USART Transmit Register								0000 0000	0000 0000
8Ch	PIE1	PSPIE(1)	(2)	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
98h	TXSTA	CSRC	TX9	TXEN	SYNC	—	BRGH	TRMT	TX9D	0000 -010	0000 -010
99h	SPBRG	Baud Rate Generator Register								0000 0000	0000 0000

Legend: x = unknown, - = unimplemented locations read as '0'. Shaded cells are not used for Synchronous Master Transmission.
Note 1: PSPIE and PSPIF are reserved on the PIC16C63/R63/66, always maintain these bits clear.
2: PIE1<6> and PIR1<6> are reserved, always maintain these bits clear.

FIGURE 12-12: SYNCHRONOUS TRANSMISSION

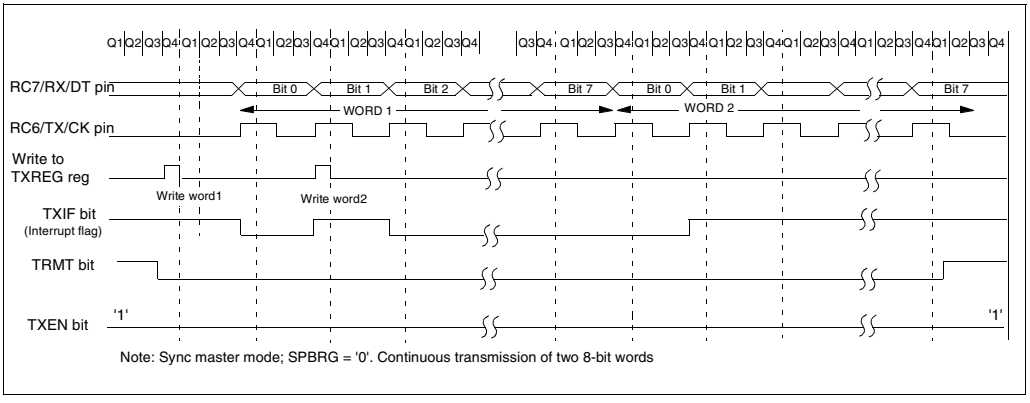
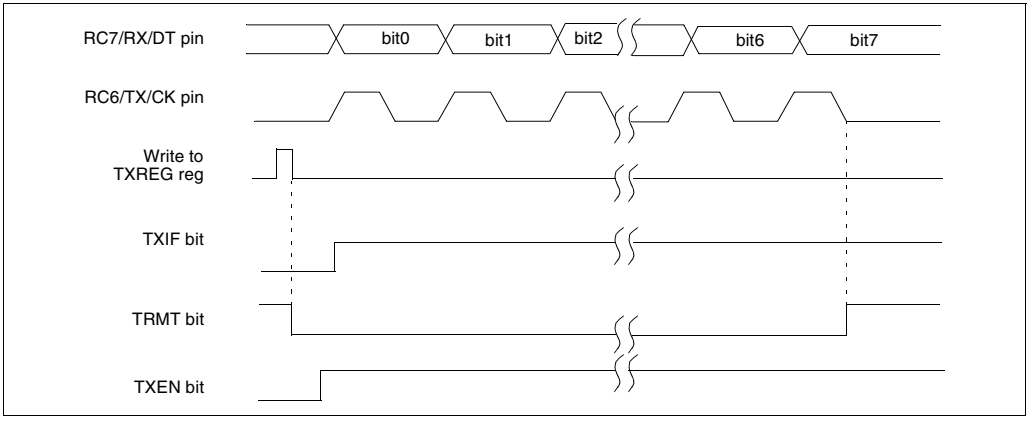


FIGURE 12-13: SYNCHRONOUS TRANSMISSION THROUGH TXEN



BCF **Bit Clear f**

Syntax: [*label*] BCF f,b

Operands: $0 \le f \le 127$
$0 \le b \le 7$

Operation: $0 \rightarrow (f<b>)$

Status Affected: None

Encoding:

01	00bb	bfff	ffff

Description: Bit 'b' in register 'f' is cleared.

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process data	Write register 'f'

Example

```
BCF     FLAG_REG, 7
```

Before Instruction
FLAG_REG = 0xC7
After Instruction
FLAG_REG = 0x47

BSF **Bit Set f**

Syntax: [*label*] BSF f,b

Operands: $0 \le f \le 127$
$0 \le b \le 7$

Operation: $1 \rightarrow (f<b>)$

Status Affected: None

Encoding:

01	01bb	bfff	ffff

Description: Bit 'b' in register 'f' is set.

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process data	Write register 'f'

Example

```
BSF     FLAG_REG,   7
```

Before Instruction
FLAG_REG = 0x0A
After Instruction
FLAG_REG = 0x8A

BTFSC **Bit Test, Skip if Clear**

Syntax: [*label*] BTFSC f,b

Operands: $0 \le f \le 127$
$0 \le b \le 7$

Operation: skip if $(f<b>) = 0$

Status Affected: None

Encoding:

01	10bb	bfff	ffff

Description: If bit 'b' in register 'f' is '1' then the next instruction is executed.
If bit 'b', in register 'f', is '0' then the next instruction is discarded, and a NOP is executed instead, making this a 2TCY instruction.

Words: 1

Cycles: 1(2)

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process data	No-Operation

If Skip: (2nd Cycle)

Q1	Q2	Q3	Q4
No-Operation	No-Operation	No-Operation	No-Operation

Example

```
HERE    BTFSC   FLAG,1
FALSE   GOTO    PROCESS_CODE
TRUE    •
        •
        •
```

Before Instruction
PC = address HERE
After Instruction
if FLAG<1> = 0,
PC = address TRUE
if FLAG<1>=1,
PC = address FALSE

Applicable Devices	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67

FIGURE 16-2: TYPICAL RC OSCILLATOR FREQUENCY VS. VDD

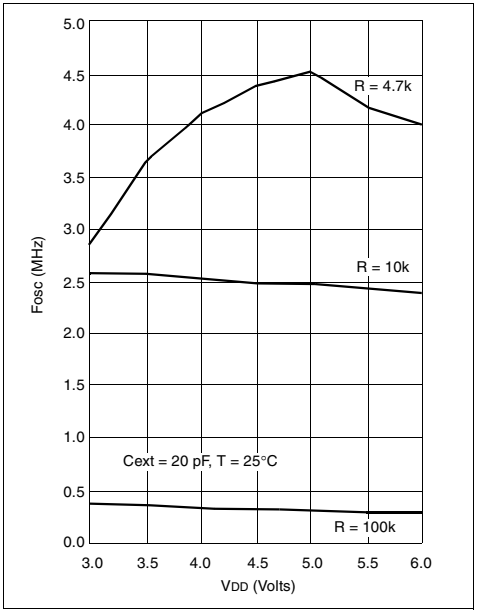


FIGURE 16-3: TYPICAL RC OSCILLATOR FREQUENCY VS. VDD

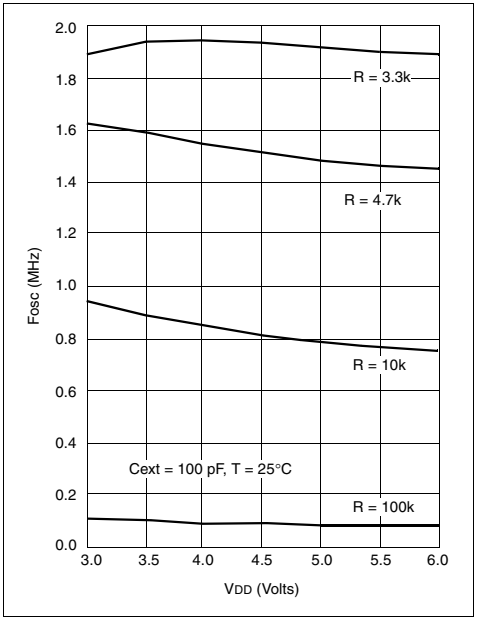


FIGURE 16-4: TYPICAL RC OSCILLATOR FREQUENCY VS. VDD

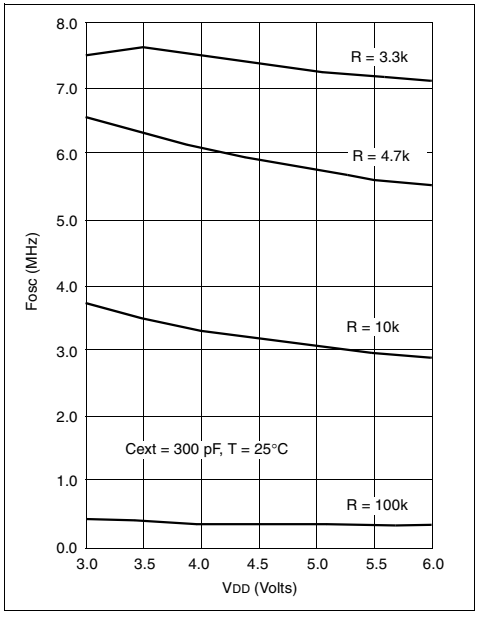
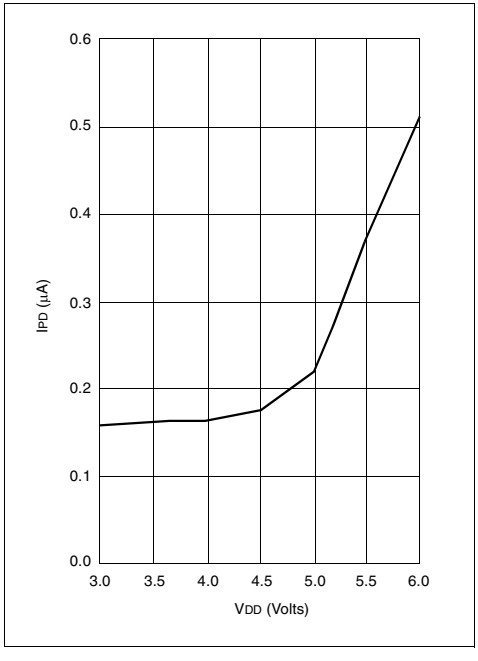


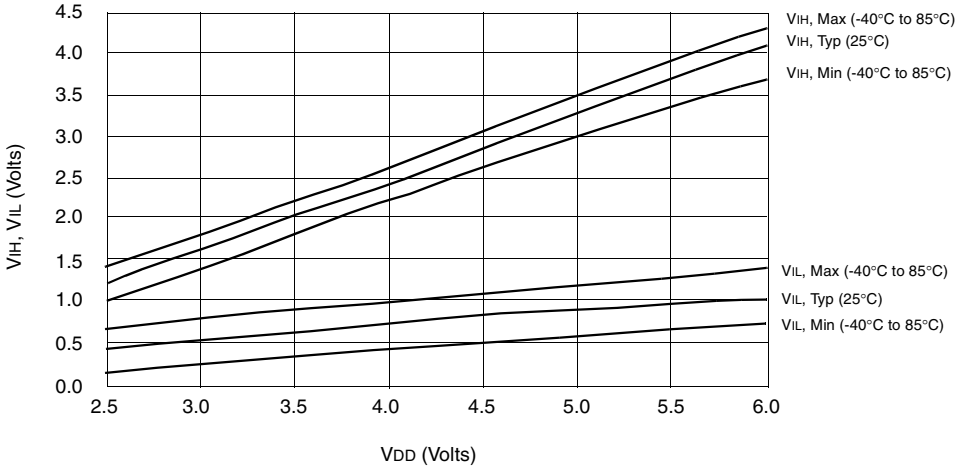
FIGURE 16-5: TYPICAL IPD VS. VDD WATCHDOG TIMER DISABLED 25°C



Data based on matrix samples. See first page of this section for details.

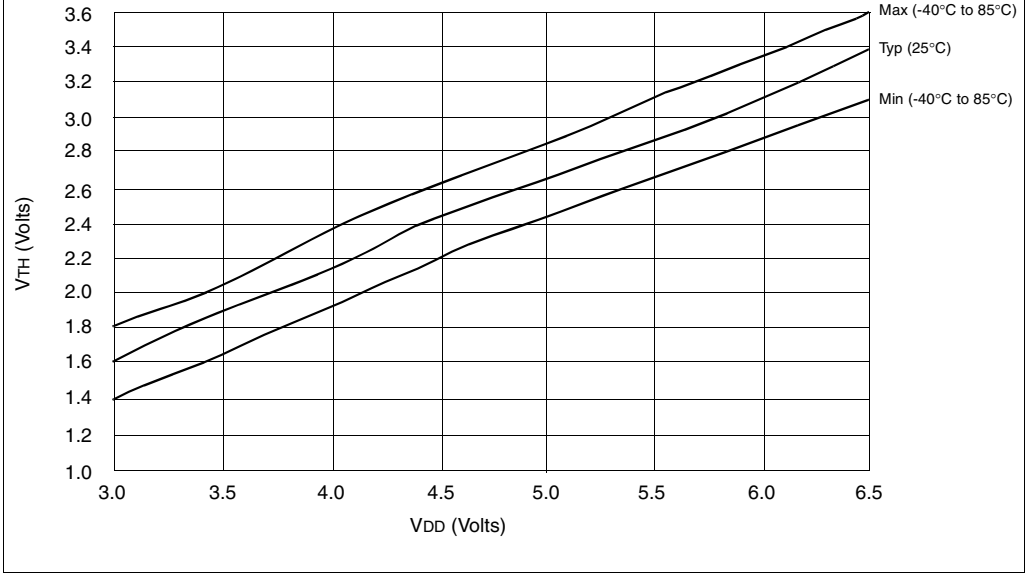
Applicable Devices	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67

FIGURE 16-10: VIH, VIL OF $\overline{MCLR}$, T0CKI AND OSC1 (IN RC MODE) VS. VDD



These pins have Schmitt Trigger input buffers.

FIGURE 16-11: VTH (INPUT THRESHOLD VOLTAGE) OF OSC1 INPUT (IN XT, HS, AND LP MODES) VS. VDD



Data based on matrix samples. See first page of this section for details.

Applicable Devices	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67

NOTES:

Applicable Devices	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67

DC CHARACTERISTICS

Standard Operating Conditions (unless otherwise stated)
Operating temperature -40°C ≤ TA ≤ +85°C for industrial and
0°C ≤ TA ≤ +70°C for commercial
Operating voltage VDD range as described in DC spec Section 19.1 and Section 19.2

Param No.	Characteristic	Sym	Min	Typ †	Max	Units	Conditions
	Capacitive Loading Specs on Output Pins						
D100	OSC2 pin	COSC2	-	-	15	pF	In XT, HS and LP modes when external clock is used to drive OSC1.
D101	All I/O pins and OSC2 (in RC mode)	CIO	-	-	50	pF	
D102	SCL, SDA in I^2C mode	Cb	-	-	400	pF	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

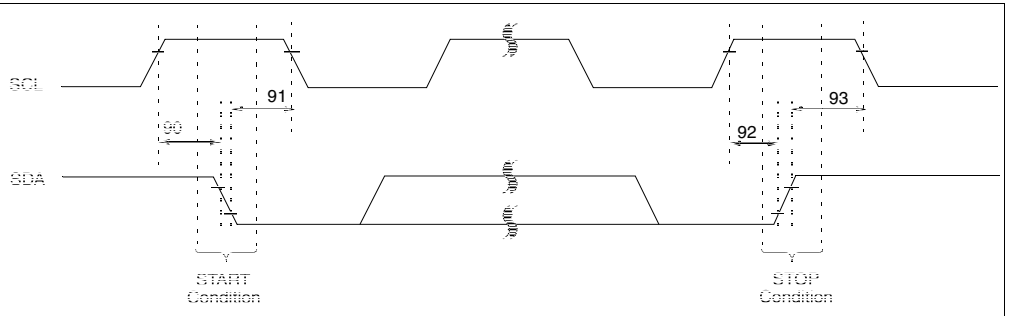
Note 1: In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C6X be driven with external clock in RC mode.

2: The leakage current on the $\overline{MCLR}$/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as current sourced by the pin.

Applicable Devices	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67

FIGURE 20-10: I^2C BUS START/STOP BITS TIMING



Note: Refer to Figure 20-1 for load conditions

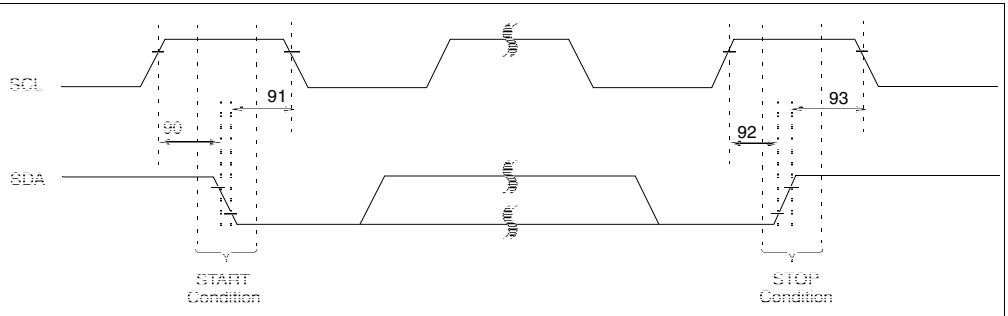
TABLE 20-9: I^2C BUS START/STOP BITS REQUIREMENTS

Parameter No.	Sym	Characteristic		Min	Typ	Max	Units	Conditions
90*	TSU:STA	START condition Setup time	100 kHz mode	4700	—	—	ns	Only relevant for repeated START condition
			400 kHz mode	600	—	—		
91*	THD:STA	START condition Hold time	100 kHz mode	4000	—	—	ns	After this period the first clock pulse is generated
			400 kHz mode	600	—	—		
92*	TSU:STO	STOP condition Setup time	100 kHz mode	4700	—	—	ns	
			400 kHz mode	600	—	—		
93	THD:STO	STOP condition Hold time	100 kHz mode	4000	—	—	ns	
			400 kHz mode	600	—	—		

* These parameters are characterized but not tested.

Applicable Devices	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67

FIGURE 22-13: I^2C BUS START/STOP BITS TIMING



Note: Refer to Figure 22-1 for load conditions

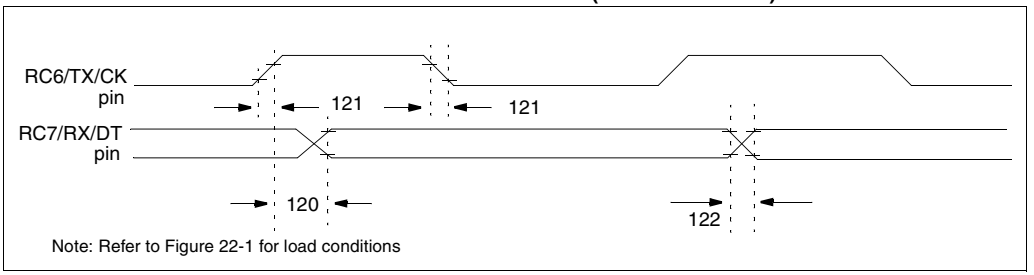
TABLE 22-9: I^2C BUS START/STOP BITS REQUIREMENTS

Parameter No.	Sym	Characteristic		Min	Typ	Max	Units	Conditions
90*	TSU:STA	START condition Setup time	100 kHz mode	4700	—	—	ns	Only relevant for repeated START condition
			400 kHz mode	600	—	—		
91*	THD:STA	START condition Hold time	100 kHz mode	4000	—	—	ns	After this period the first clock pulse is generated
			400 kHz mode	600	—	—		
92*	TSU:STO	STOP condition Setup time	100 kHz mode	4700	—	—	ns	
			400 kHz mode	600	—	—		
93	THD:STO	STOP condition Hold time	100 kHz mode	4000	—	—	ns	
			400 kHz mode	600	—	—		

* These parameters are characterized but not tested.

Applicable Devices	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67

FIGURE 22-15: USART SYNCHRONOUS TRANSMISSION (MASTER/SLAVE) TIMING



Note: Refer to Figure 22-1 for load conditions

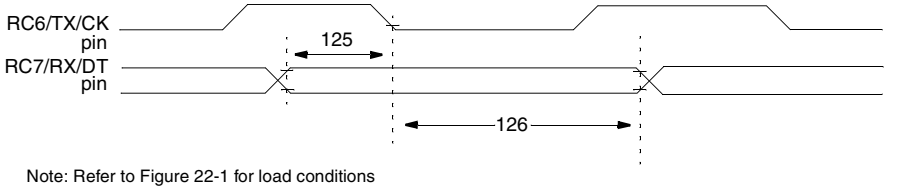
TABLE 22-11: USART SYNCHRONOUS TRANSMISSION REQUIREMENTS

Parameter No.	Sym	Characteristic		Min	Typ†	Max	Units	Conditions
120*	TckH2dtV	SYNC XMIT (MASTER & SLAVE) Clock high to data out valid	PIC16**C**66/67	—	—	80	ns	
			PIC16**LC**66/67	—	—	100	ns	
121*	Tckrf	Clock out rise time and fall time (Master Mode)	PIC16**C**66/67	—	—	45	ns	
			PIC16**LC**66/67	—	—	50	ns	
122*	Tdtrf	Data out rise time and fall time	PIC16**C**66/67	—	—	45	ns	
			PIC16**LC**66/67	—	—	50	ns	

* These parameters are characterized but not tested.

†: Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 22-16: USART SYNCHRONOUS RECEIVE (MASTER/SLAVE) TIMING



Note: Refer to Figure 22-1 for load conditions

TABLE 22-12: USART SYNCHRONOUS RECEIVE REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
125*	TdtV2ckL	SYNC RCV (MASTER & SLAVE) Data setup before CK ↓ (DT setup time)	15	—	—	ns	
126*	TckL2dtl	Data hold after CK ↓ (DT hold time)	15	—	—	ns	

* These parameters are characterized but not tested.

†: Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Applicable Devices	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67

FIGURE 23-3: TYPICAL IPD vs. VDD @ 25°C (WDT ENABLED, RC MODE)

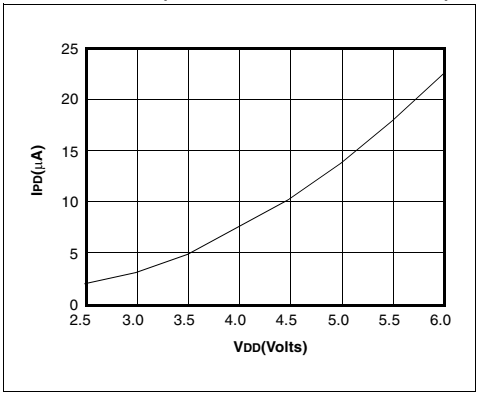


FIGURE 23-4: MAXIMUM IPD vs. VDD (WDT ENABLED, RC MODE)

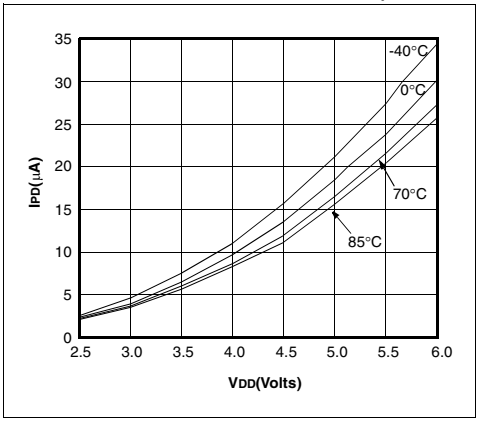
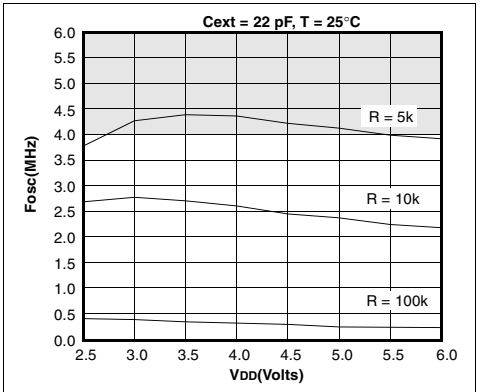


FIGURE 23-5: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD



Shaded area is beyond recommended range.

FIGURE 23-6: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD

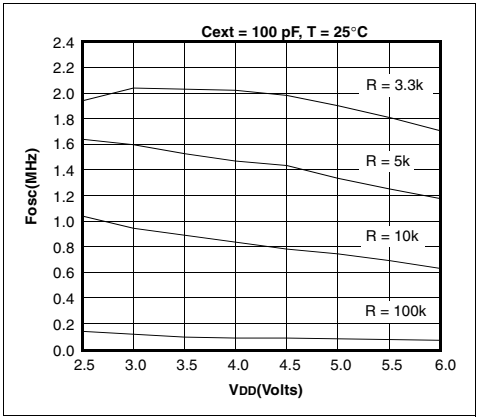
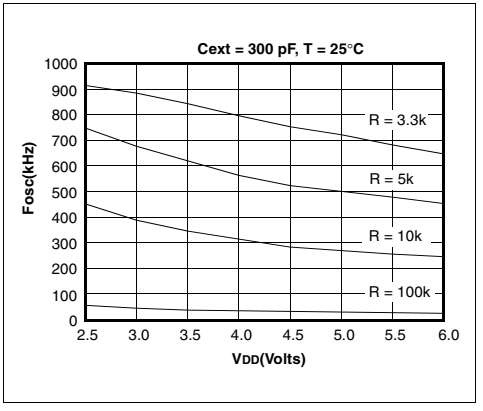


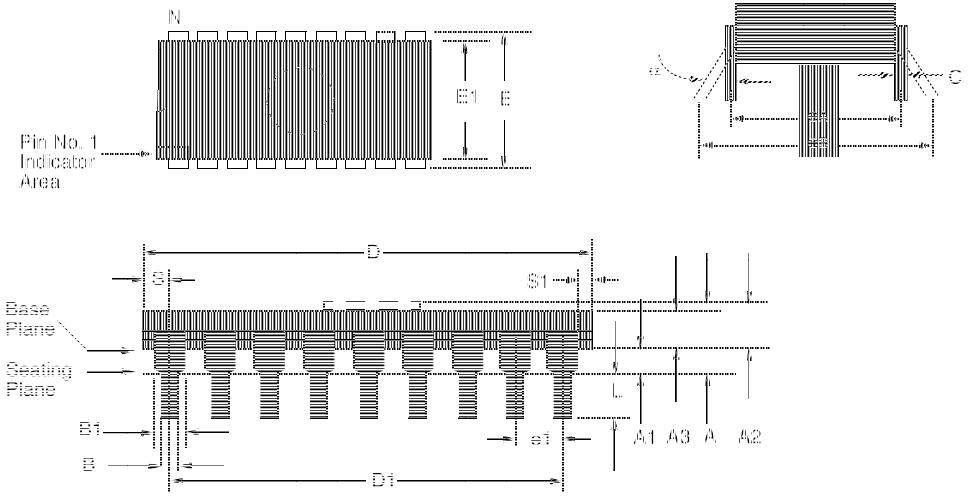
FIGURE 23-7: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD



Data based on matrix samples. See first page of this section for details.

24.6 18-Lead Ceramic CERDIP Dual In-line with Window (300 mil) (JW)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Package Group: Ceramic CERDIP Dual In-Line (CDP)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	—	5.080		—	0.200	
A1	0.381	1.778		0.015	0.070	
A2	3.810	4.699		0.150	0.185	
A3	3.810	4.445		0.150	0.175	
B	0.355	0.585		0.014	0.023	
B1	1.270	1.651	**Typical**	0.050	0.065	**Typical**
C	0.203	0.381	**Typical**	0.008	0.015	**Typical**
D	22.352	23.622		0.880	0.930	
D1	20.320	20.320	**Reference**	0.800	0.800	**Reference**
E	7.620	8.382		0.300	0.330	
E1	5.588	7.874		0.220	0.310	
e1	2.540	2.540	**Reference**	0.100	0.100	**Reference**
eA	7.366	8.128	**Typical**	0.290	0.320	**Typical**
eB	7.620	10.160		0.300	0.400	
L	3.175	3.810		0.125	0.150	
N	18	18		18	18	
S	0.508	1.397		0.020	0.055	
S1	0.381	1.270		0.015	0.050	

Figure 11-2: SSPCON: Sync Serial Port Control Register (Address 14h) 85
Figure 11-3: SSP Block Diagram (SPI Mode) 86
Figure 11-4: SPI Master/Slave Connection 87
Figure 11-5: SPI Mode Timing, Master Mode or Slave Mode w/o $\overline{SS}$ Control 88
Figure 11-6: SPI Mode Timing, Slave Mode with $\overline{SS}$ Control 88
Figure 11-7: SSPSTAT: Sync Serial Port Status Register (Address 94h)(PIC16C66/67) 89
Figure 11-8: SSPCON: Sync Serial Port Control Register (Address 14h)(PIC16C66/67) 90
Figure 11-9: SSP Block Diagram (SPI Mode) (PIC16C66/67) 91
Figure 11-10: SPI Master/Slave Connection (PIC16C66/67) 92
Figure 11-11: SPI Mode Timing, Master Mode (PIC16C66/67) 93
Figure 11-12: SPI Mode Timing (Slave Mode With CKE = 0) (PIC16C66/67) 93
Figure 11-13: SPI Mode Timing (Slave Mode With CKE = 1) (PIC16C66/67) 94
Figure 11-14: Start and Stop Conditions 95
Figure 11-15: 7-bit Address Format 96
Figure 11-16: I^2C 10-bit Address Format 96
Figure 11-17: Slave-receiver Acknowledge 96
Figure 11-18: Data Transfer Wait State 96
Figure 11-19: Master-transmitter Sequence 97
Figure 11-20: Master-receiver Sequence 97
Figure 11-21: Combined Format 97
Figure 11-22: Multi-master Arbitration (Two Masters) 98
Figure 11-23: Clock Synchronization 98
Figure 11-24: SSP Block Diagram (I^2C Mode) 99
Figure 11-25: I^2C Waveforms for Reception (7-bit Address) 101
Figure 11-26: I^2C Waveforms for Transmission (7-bit Address) 102
Figure 11-27: Operation of the I^2C Module in IDLE_MODE, RCV_MODE or XMIT_MODE 104
Figure 12-1: TXSTA: Transmit Status and Control Register (Address 98h) 105
Figure 12-2: RCSTA: Receive Status and Control Register (Address 18h) 106
Figure 12-3: RX Pin Sampling Scheme (BRGH = 0) PIC16C63/R63/65/65A/R65) 110
Figure 12-4: RX Pin Sampling Scheme (BRGH = 1) (PIC16C63/R63/65/65A/R65) 110
Figure 12-5: RX Pin Sampling Scheme (BRGH = 1) (PIC16C63/R63/65/65A/R65) 110
Figure 12-6: RX Pin Sampling Scheme (BRGH = 0 or = 1) (PIC16C66/67) 111
Figure 12-7: USART Transmit Block Diagram 112
Figure 12-8: Asynchronous Master Transmission 113
Figure 12-9: Asynchronous Master Transmission (Back to Back) 113
Figure 12-10: USART Receive Block Diagram 114
Figure 12-11: Asynchronous Reception 114
Figure 12-12: Synchronous Transmission 117
Figure 12-13: Synchronous Transmission through TXEN 117
Figure 12-14: Synchronous Reception (Master Mode, SREN) 119
Figure 13-1: Configuration Word for PIC16C61 123
Figure 13-2: Configuration Word for PIC16C62/64/65 124
Figure 13-3: Configuration Word for PIC16C62A/R62/63/R63/64A/R64/ 65A/R65/66/67 124
Figure 13-4: Crystal/Ceramic Resonator Operation (HS, XT or LP OSC Configuration) 125
Figure 13-5: External Clock Input Operation (HS, XT or LP OSC Configuration) 125
Figure 13-6: External Parallel Resonant Crystal Oscillator Circuit 127
Figure 13-7: External Series Resonant Crystal Oscillator Circuit 127
Figure 13-8: RC Oscillator Mode 127
Figure 13-9: Simplified Block Diagram of On-chip Reset Circuit 128
Figure 13-10: Brown-out Situations 129
Figure 13-11: Time-out Sequence on Power-up ($\overline{MCLR}$ not Tied to VDD): Case 1 134
Figure 13-12: Time-out Sequence on Power-up ($\overline{MCLR}$ Not Tied To VDD): Case 2 134
Figure 13-13: Time-out Sequence on Power-up ($\overline{MCLR}$ Tied to VDD) 134
Figure 13-14: External Power-on Reset Circuit (For Slow VDD Power-up) 135
Figure 13-15: External Brown-out Protection Circuit 1 135
Figure 13-16: External Brown-out Protection Circuit 2 135
Figure 13-17: Interrupt Logic for PIC16C61 137
Figure 13-18: Interrupt Logic for PIC16C6X 137
Figure 13-19: INT Pin Interrupt Timing 138
Figure 13-20: Watchdog Timer Block Diagram 140
Figure 13-21: Summary of Watchdog Timer Registers 140
Figure 13-22: Wake-up from Sleep Through Interrupt 142
Figure 13-23: Typical In-circuit Serial Programming Connection 142
Figure 14-1: General Format for Instructions 143
Figure 16-1: Load Conditions for Device Timing Specifications 168
Figure 16-2: External Clock Timing 169
Figure 16-3: CLKOUT and I/O Timing 170
Figure 16-4: Reset, Watchdog Timer, Oscillator Start-up Timer and Power-up Timer Timing 171
Figure 16-5: Timer0 External Clock Timings 172
Figure 17-1: Typical RC Oscillator Frequency vs. Temperature 173
Figure 17-2: Typical RC Oscillator Frequency vs. VDD 174
Figure 17-3: Typical RC Oscillator Frequency vs. VDD 174
Figure 17-4: Typical RC Oscillator Frequency vs. VDD 174
Figure 17-5: Typical IPD vs. VDD Watchdog Timer Disabled 25°C 174
Figure 17-6: Typical IPD vs. VDD Watchdog Timer Enabled 25°C 175
Figure 17-7: Maximum IPD vs. VDD Watchdog Disabled 175
Figure 17-8: Maximum IPD vs. VDD Watchdog Enabled* 176
Figure 17-9: VTH (Input Threshold Voltage) of I/O Pins vs. VDD 176

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1. Set your modem to 8-bit, No parity, and One stop (8N1). This is not the normal CompuServe setting which is 7E1.
2. Dial your local CompuServe access number.
3. Depress the **<Enter>** key and a garbage string will appear because CompuServe is expecting a 7E1 setting.
4. Type +, depress the **<Enter>** key and "`Host Name:`" will appear.
5. Type MCHIPBBS, depress the **<Enter>** key and you will be connected to the Microchip BBS.

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