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Applications of "Embedded - Microcontrollers"
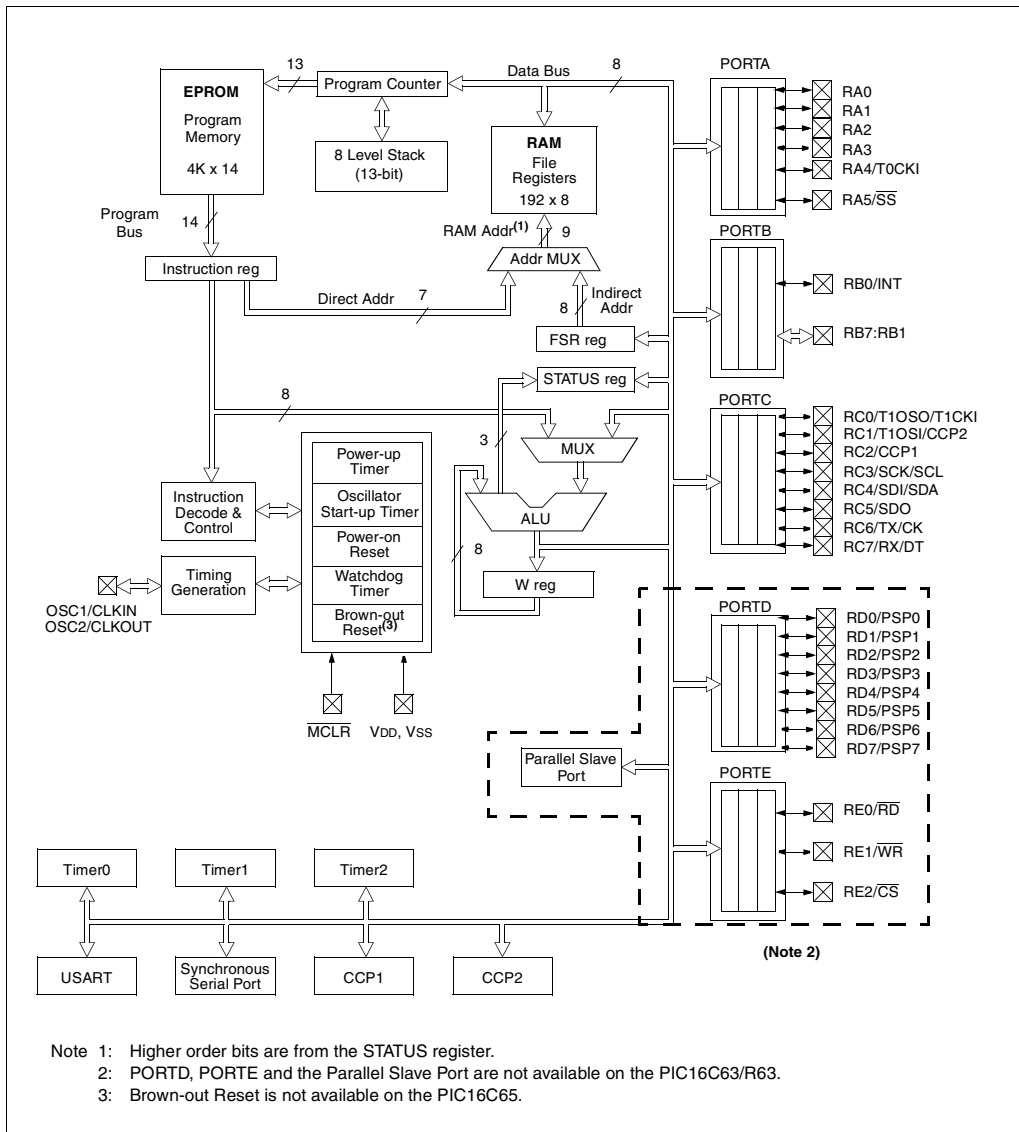
Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	33
Program Memory Size	7KB (4K x 14)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	192 x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 6V
Data Converters	-
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	44-PLCC (16.59x16.59)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16c65a-20-l

NOTES:

PIC16C6X

FIGURE 3-3: PIC16C63/R63/65/65A/R65 BLOCK DIAGRAM

Note 1: Higher order bits are from the STATUS register.
2: PORTD, PORTE and the Parallel Slave Port are not available on the PIC16C63/R63.
3: Brown-out Reset is not available on the PIC16C65.

TABLE 4-2: SPECIAL FUNCTION REGISTERS FOR THE PIC16C62/62A/R62

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other resets[3]
Bank 0											
00h[1]	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								0000 0000	0000 0000
01h	TMR0	Timer0 module's register								xxxx xxxx	uuuu uuuu
02h[1]	PCL	Program Counter's (PC) Least Significant Byte								0000 0000	0000 0000
03h[1]	STATUS	IRP[5]	RP1[5]	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	000q quuu
04h[1]	FSR	Indirect data memory address pointer								xxxx xxxx	uuuu uuuu
05h	PORTA	—	—	PORTA Data Latch when written: PORTA pins when read						--xx xxxx	--uu uuuu
06h	PORTB	PORTB Data Latch when written: PORTB pins when read								xxxx xxxx	uuuu uuuu
07h	PORTC	PORTC Data Latch when written: PORTC pins when read								xxxx xxxx	uuuu uuuu
08h	—	Unimplemented								—	—
09h	—	Unimplemented								—	—
0Ah[1,2]	PCLATH	—	—	—	Write Buffer for the upper 5 bits of the Program Counter					---0 0000	---0 0000
0Bh[1]	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000u
0Ch	PIR1	(6)	(6)	—	—	SSPIF	CCP1IF	TMR2IF	TMR1IF	00-- 0000	00-- 0000
0Dh	—	Unimplemented								—	—
0Eh	TMR1L	Holding register for the Least Significant Byte of the 16-bit TMR1 register								xxxx xxxx	uuuu uuuu
0Fh	TMR1H	Holding register for the Most Significant Byte of the 16-bit TMR1 register								xxxx xxxx	uuuu uuuu
10h	T1CON	—	—	T1CKPS1	T1CKPS0	T1OSCEN	$\overline{T1SYNC}$	TMR1CS	TMR1ON	--00 0000	--uu uuuu
11h	TMR2	Timer2 module's register								0000 0000	0000 0000
12h	T2CON	—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000 0000	-000 0000
13h	SSPBUF	Synchronous Serial Port Receive Buffer/Transmit Register								xxxx xxxx	uuuu uuuu
14h	SSPCON	WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0	0000 0000	0000 0000
15h	CCPR1L	Capture/Compare/PWM1 (LSB)								xxxx xxxx	uuuu uuuu
16h	CCPR1H	Capture/Compare/PWM1 (MSB)								xxxx xxxx	uuuu uuuu
17h	CCP1CON	—	—	CCP1X	CCP1Y	CCP1M3	CCP1M2	CCP1M1	CCP1M0	--00 0000	--00 0000
18h-1Fh	—	Unimplemented								—	—

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented location read as '0'.
Shaded locations are unimplemented, read as '0'.

Note 1: These registers can be addressed from either bank.
2: The upper byte of the Program Counter (PC) is not directly accessible. PCLATH is a holding register for the PC whose contents are transferred to the upper byte of the program counter. (PC<12:8>)
3: Other (non power-up) resets include external reset through $\overline{MCLR}$ and the Watchdog Timer reset.
4: The $\overline{BOR}$ bit is reserved on the PIC16C62, always maintain this bit set.
5: The IRP and RP1 bits are reserved on the PIC16C62/62A/R62, always maintain these bits clear.
6: PIE1<7:6> and PIR1<7:6> are reserved on the PIC16C62/62A/R62, always maintain these bits clear.

TABLE 4-4: **SPECIAL FUNCTION REGISTERS FOR THE PIC16C64/64A/R64 (Cont.'d)**

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other resets[3]
Bank 1											
80h[1]	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								0000 0000	0000 0000
81h	OPTION	$\overline{RBPU}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
82h[1]	PCL	Program Counter's (PC) Least Significant Byte								0000 0000	0000 0000
83h[1]	STATUS	IRP[5]	RP1[5]	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	000q quuu
84h[1]	FSR	Indirect data memory address pointer								xxxx xxxx	uuuu uuuu
85h	TRISA	—	—	PORTA Data Direction Register						--11 1111	--11 1111
86h	TRISB	PORTB Data Direction Register								1111 1111	1111 1111
87h	TRISC	PORTC Data Direction Register								1111 1111	1111 1111
88h	TRISD	PORTD Data Direction Register								1111 1111	1111 1111
89h	TRISE	IBF	OBF	IBOV	PSPMODE	—	PORTE Data Direction Bits			0000 -111	0000 -111
8Ah[1,2]	PCLATH	—	—	—	Write Buffer for the upper 5 bits of the Program Counter					---0 0000	---0 0000
8Bh[1]	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000u
8Ch	PIE1	PSPIE	(6)	—	—	SSPIE	CCP1IE	TMR2IE	TMR1IE	00-- 0000	00-- 0000
8Dh	—	Unimplemented								—	—
8Eh	PCON	—	—	—	—	—	—	$\overline{POR}$	$\overline{BOR}$[4]	---- --qq	---- --uu
8Fh	—	Unimplemented								—	—
90h	—	Unimplemented								—	—
91h	—	Unimplemented								—	—
92h	PR2	Timer2 Period Register								1111 1111	1111 1111
93h	SSPADD	Synchronous Serial Port (I2C mode) Address Register								0000 0000	0000 0000
94h	SSPSTAT	—	—	D/$\overline{A}$	P	S	R/$\overline{W}$	UA	BF	--00 0000	--00 0000
95h-9Fh	—	Unimplemented								—	—

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented location read as '0'.
Shaded locations are unimplemented, read as '0'.

Note 1: These registers can be addressed from either bank.
2: The upper byte of the Program Counter (PC) is not directly accessible. PCLATH is a holding register for the PC whose contents are transferred to the upper byte of the program counter. (PC<12:8>)
3: Other (non power-up) resets include external reset through $\overline{MCLR}$ and the Watchdog Timer reset.
4: The $\overline{BOR}$ bit is reserved on the PIC16C64, always maintain this bit set.
5: The IRP and RP1 bits are reserved on the PIC16C64/64A/R64, always maintain these bits clear.
6: PIE1<6> and PIR1<6> are reserved on the PIC16C64/64A/R64, always maintain these bits clear.

7.2 Using Timer0 with External Clock

Applicable Devices

61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67

When an external clock input is used for Timer0, it must meet certain requirements. The requirements ensure the external clock can be synchronized with the internal phase clock (TOSC). Also, there is a delay in the actual incrementing of Timer0 after synchronization.
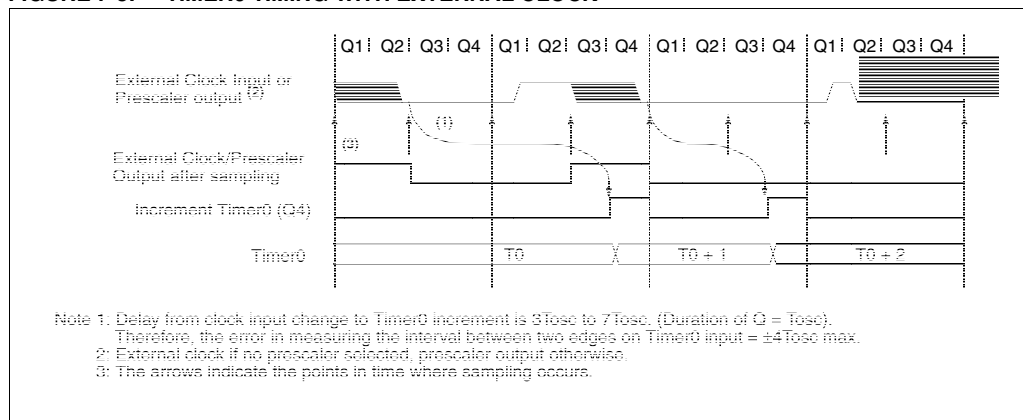
7.2.1 EXTERNAL CLOCK SYNCHRONIZATION

When no prescaler is used, the external clock input is the same as the prescaler output. The synchronization of T0CKI with the internal phase clocks is accomplished by sampling the prescaler output on the Q2 and Q4 cycles of the internal phase clocks (Figure 7-5). Therefore, it is necessary for T0CKI to be high for at least 2Tosc (and a small RC delay of 20 ns) and low for at least 2Tosc (and a small RC delay of 20 ns). Refer to the electrical specification of the desired device.

When a prescaler is used, the external clock input is divided by the asynchronous ripple-counter type prescaler so that the prescaler output is symmetrical. For the external clock to meet the sampling requirement, the ripple-counter must be taken into account. Therefore, it is necessary for T0CKI to have a period of at least 4Tosc (and a small RC delay of 40 ns) divided by the prescaler value. The only requirement on T0CKI high and low time is that they do not violate the minimum pulse width requirement of 10 ns. Refer to parameters 40, 41 and 42 in the electrical specification of the desired device.

7.2.2 TIMER0 INCREMENT DELAY

Since the prescaler output is synchronized with the internal clocks, there is a small delay from the time the external clock edge occurs to the time the Timer0 module is actually incremented. Figure 7-5 shows the delay from the external clock edge to the timer incrementing.

FIGURE 7-5: TIMER0 TIMING WITH EXTERNAL CLOCK

Note 1: Delay from clock input change to Timer0 increment is 3Tosc to 7Tosc. (Duration of Q = Tosc).
Therefore, the error in measuring the interval between two edges on Timer0 input = ±4Tosc max.
2: External clock if no prescaler selected, prescaler output otherwise.
3: The arrows indicate the points in time where sampling occurs.

11.2   SPI Mode for PIC16C62/62A/R62/63/ R63/64/64A/R64/65/65A/R65

This section contains register definitions and operational characteristics of the SPI module for the PIC16C62, PIC16C62A, PIC16CR62, PIC16C63, PIC16CR63, PIC16C64, PIC16C64A, PIC16CR64, PIC16C65, PIC16C65A, PIC16CR65.

FIGURE 11-1:   SSPSTAT: SYNC SERIAL PORT STATUS REGISTER (ADDRESS 94h)

U-0	U-0	R-0	R-0	R-0	R-0	R-0	R-0
—	—	D/$\overline{\text{A}}$	P	S	R/$\overline{\text{W}}$	UA	BF

bit7   bit0

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n =Value at POR reset

bit 7-6: **Unimplemented:** Read as '0'

bit 5: **D/$\overline{\text{A}}$**: Data/Address bit (I^2C mode only)
1 = Indicates that the last byte received or transmitted was data
0 = Indicates that the last byte received or transmitted was address

bit 4: **P**: Stop bit (I^2C mode only. This bit is cleared when the SSP module is disabled, SSPEN is cleared)
1 = Indicates that a stop bit has been detected last (this bit is '0' on RESET)
0 = Stop bit was not detected last

bit 3: **S**: Start bit (I^2C mode only. This bit is cleared when the SSP module is disabled, SSPEN is cleared)
1 = Indicates that a start bit has been detected last (this bit is '0' on RESET)
0 = Start bit was not detected last

bit 2: **R/$\overline{\text{W}}$**: Read/Write bit information (I^2C mode only)
This bit holds the R/W bit information following the last address match. This bit is valid from the address match to the next start bit, stop bit, or $\overline{\text{ACK}}$ bit.
1 = Read
0 = Write

bit 1: **UA**: Update Address (10-bit I^2C mode only)
1 = Indicates that the user needs to update the address in the SSPADD register
0 = Address does not need to be updated

bit 0: **BF**: Buffer Full Status bit

Receive (SPI and I^2C modes)
1 = Receive complete, SSPBUF is full
0 = Receive not complete, SSPBUF is empty

Transmit (I^2C mode only)
1 = Transmit in progress, SSPBUF is full
0 = Transmit complete, SSPBUF is empty

Applicable Devices														
61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67

PIC16C6X

Figure 11-19 and Figure 11-20 show Master-transmitter and Master-receiver data transfer sequences.

When a master does not wish to relinquish the bus (by generating a STOP condition), a repeated START condition (Sr) must be generated. This condition is identical to the start condition (SDA goes high-to-low while SCL is high), but occurs after a data transfer acknowledge pulse (not the bus-free state). This allows a master to send "commands" to the slave and then receive the requested information or to address a different slave device. This sequence is shown in Figure 11-21.
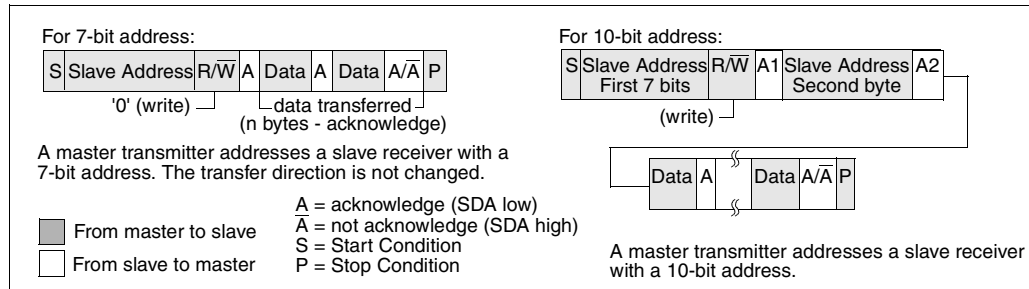
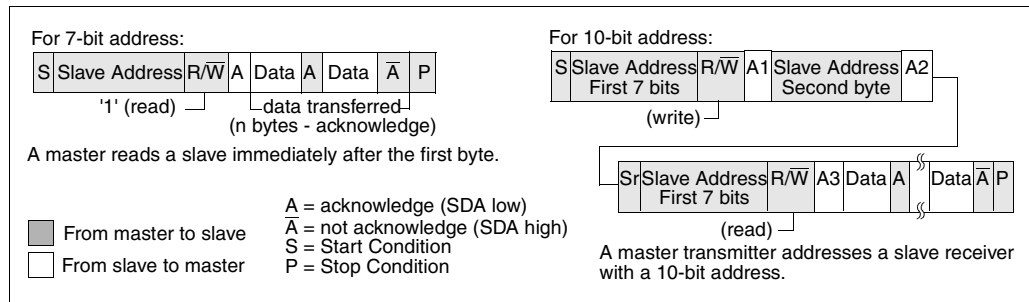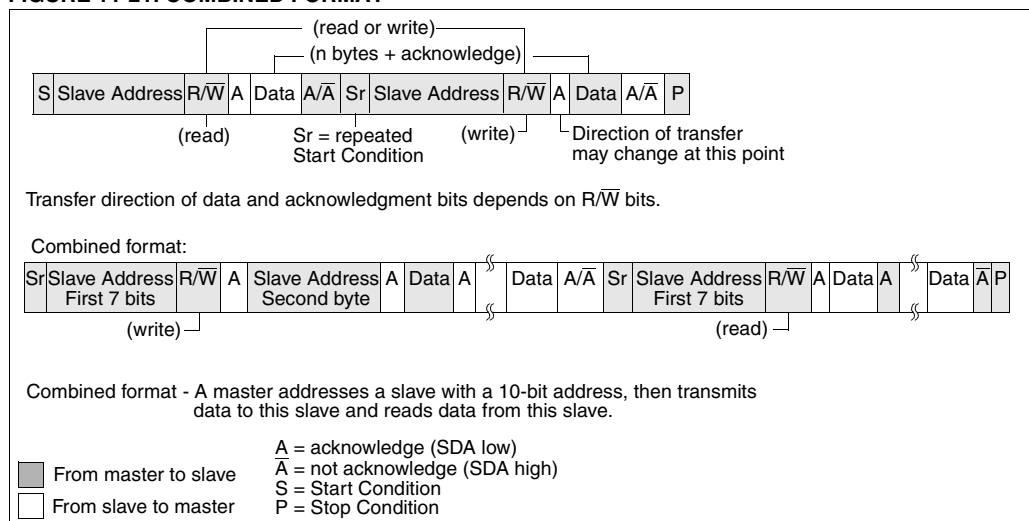### FIGURE 11-19: MASTER-TRANSMITTER SEQUENCE

For 7-bit address:

| S | Slave Address | R/$\overline{W}$ | A | Data | A | Data | A/$\overline{A}$ | P |

'0' (write) — data transferred (n bytes - acknowledge)

A master transmitter addresses a slave receiver with a 7-bit address. The transfer direction is not changed.

From master to slave
From slave to master

A = acknowledge (SDA low)
$\overline{A}$ = not acknowledge (SDA high)
S = Start Condition
P = Stop Condition

For 10-bit address:

| S | Slave Address First 7 bits | R/$\overline{W}$ | A1 | Slave Address Second byte | A2 |

(write)

| Data | A | Data | A/$\overline{A}$ | P |

A master transmitter addresses a slave receiver with a 10-bit address.

FIGURE 11-20: MASTER-RECEIVER SEQUENCE

For 7-bit address:

| S | Slave Address | R/$\overline{W}$ | A | Data | A | Data | $\overline{A}$ | P |

'1' (read) — data transferred (n bytes - acknowledge)

A master reads a slave immediately after the first byte.

From master to slave
From slave to master

A = acknowledge (SDA low)
$\overline{A}$ = not acknowledge (SDA high)
S = Start Condition
P = Stop Condition

For 10-bit address:

| S | Slave Address First 7 bits | R/$\overline{W}$ | A1 | Slave Address Second byte | A2 |

(write)

| Sr | Slave Address First 7 bits | R/$\overline{W}$ | A3 | Data | A | Data | $\overline{A}$ | P |

(read)

A master transmitter addresses a slave receiver with a 10-bit address.

FIGURE 11-21: COMBINED FORMAT

(read or write)
(n bytes + acknowledge)

| S | Slave Address | R/$\overline{W}$ | A | Data | A/$\overline{A}$ | Sr | Slave Address | R/$\overline{W}$ | A | Data | A/$\overline{A}$ | P |

(read)   Sr = repeated Start Condition   (write)   Direction of transfer may change at this point

Transfer direction of data and acknowledgment bits depends on R/$\overline{W}$ bits.

Combined format:

| Sr | Slave Address First 7 bits | R/$\overline{W}$ | A | Slave Address Second byte | A | Data | A | Data | A/$\overline{A}$ | Sr | Slave Address First 7 bits | R/$\overline{W}$ | A | Data | A | Data | $\overline{A}$ | P |

(write)   (read)

Combined format - A master addresses a slave with a 10-bit address, then transmits data to this slave and reads data from this slave.

From master to slave
From slave to master

A = acknowledge (SDA low)
$\overline{A}$ = not acknowledge (SDA high)
S = Start Condition
P = Stop Condition

13.0 SPECIAL FEATURES OF THE CPU

Applicable Devices

61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67

What sets a microcontroller apart from other processors are special circuits to deal with the needs of real-time applications. The PIC16CXX family has a host of such features intended to maximize system reliability, minimize cost through elimination of external components, provide power saving operating modes and offer code protection. These are:

- Oscillator selection
- Reset
  - Power-on Reset (POR)
  - Power-up Timer (PWRT)
  - Oscillator Start-up Timer (OST)
  - Brown-out Reset (BOR)
- Interrupts
- Watchdog Timer (WDT)
- SLEEP mode
- Code protection
- ID locations
- In-circuit serial programming

The PIC16CXX has a Watchdog Timer which can be shut off only through configuration bits. It runs off its own RC oscillator for added reliability. There are two timers that offer necessary delays on power-up. One is the Oscillator Start-up Timer (OST), intended to keep the chip in RESET until the crystal oscillator is stable. The other is the Power-up Timer (PWRT), which provides a fixed delay of 72 ms (nominal) on power-up only, designed to keep the part in reset while the power supply stabilizes. With these two timers on-chip, most applications need no external reset circuitry.

SLEEP mode is designed to offer a very low current power-down mode. The user can wake from SLEEP through external reset, Watchdog Timer Wake-up or through an interrupt. Several oscillator options are also made available to allow the part to fit the application. The RC oscillator option saves system cost while the LP crystal option saves power. A set of configuration bits are used to select various options.

13.1 Configuration Bits

Applicable Devices

61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67

The configuration bits can be programmed (read as '0') or left unprogrammed (read as '1') to select various device configurations. These bits are mapped in program memory location 2007h.

The user will note that address 2007h is beyond the user program memory space. In fact, it belongs to the special test/configuration memory space (2000h - 3FFFh), which can be accessed only during programming.

FIGURE 13-1: CONFIGURATION WORD FOR PIC16C61

—	—	—	—	—	—	—	—	—	CP0	PWRTE	WDTE	FOSC1	FOSC0

bit13   bit0

Register: CONFIG
Address: 2007h

bit 13-5: **Unimplemented**: Read as '1'

bit 4: **CP0**: Code protection bit
1 = Code protection off
0 = All memory is code protected, but 00h - 3Fh is writable

bit 3: **PWRTE**: Power-up Timer Enable bit
1 = Power-up Timer enabled
0 = Power-up Timer disabled

bit 2: **WDTE**: Watchdog Timer Enable bit
1 = WDT enabled
0 = WDT disabled

bit 1-0: **FOSC1:FOSC0**: Oscillator Selection bits
11 = RC oscillator
10 = HS oscillator
01 = XT oscillator
00 = LP oscillator

13.8   Power-down Mode (SLEEP)

Applicable Devices

61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67

Power-down mode is entered by executing a SLEEP instruction.

If enabled, the Watchdog Timer will be cleared but keeps running, status bit $\overline{PD}$ (STATUS<3>) is cleared, status bit $\overline{TO}$ (STATUS<4>) is set, and the oscillator driver is turned off. The I/O ports maintain the status they had before the SLEEP instruction was executed (driving high, low, or hi-impedance).

For lowest current consumption in this mode, place all I/O pins at either VDD, or VSS, ensure no external circuitry is drawing current from the I/O pin, and disable external clocks. Pull all I/O pins, that are hi-impedance inputs, high or low externally to avoid switching currents caused by floating inputs. The T0CKI input should also be at VDD or VSS for lowest current consumption. The contribution from on-chip pull-ups on PORTB should be considered.

The $\overline{MCLR}$/VPP pin must be at a logic high level (VIHMC).

13.8.1   WAKE-UP FROM SLEEP

The device can wake from SLEEP through one of the following events:

1.   External reset input on $\overline{MCLR}$/VPP pin.
2.   Watchdog Timer Wake-up (if WDT was enabled).
3.   Interrupt from RB0/INT pin, RB port change, or some peripheral interrupts.

External $\overline{MCLR}$ Reset will cause a device reset. All other events are considered a continuation of program execution and cause a "wake-up". The $\overline{TO}$ and $\overline{PD}$ bits in the STATUS register can be used to determine the cause of device reset. The $\overline{PD}$ bit, which is set on power-up is cleared when SLEEP is invoked. The $\overline{TO}$ bit is cleared if WDT time-out occurred (and caused wake-up).

The following peripheral interrupts can wake the device from SLEEP:

1.   TMR1 interrupt. Timer1 must be operating as an asynchronous counter.
2.   SSP (Start/Stop) bit detect interrupt.
3.   SSP transmit or receive in slave mode (SPI/I^{2}C).
4.   CCP capture mode interrupt.
5.   Parallel Slave Port read or write.
6.   USART TX or RX (synchronous slave mode).

Other peripherals can not generate interrupts since during SLEEP, no on-chip Q clocks are present.

When the SLEEP instruction is being executed, the next instruction (PC + 1) is pre-fetched. For the device to wake-up through an interrupt event, the corresponding interrupt enable bit must be set (enabled). Wake-up is regardless of the state of the GIE bit. If the GIE bit is clear (disabled), the device continues execution at the instruction after the SLEEP instruction. If the GIE bit is set (enabled), the device executes the instruction after the SLEEP instruction and then branches to the interrupt address (0004h). In cases where the execution of the instruction following SLEEP is not desirable, the user should have a NOP after the SLEEP instruction.
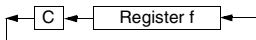
13.8.2   WAKE-UP USING INTERRUPTS

When global interrupts are disabled (GIE cleared) and any interrupt source has both its interrupt enable bit and interrupt flag bit set, one of the following will occur:

- If the interrupt occurs **before** the execution of a SLEEP instruction, the SLEEP instruction will complete as a NOP. Therefore, the WDT and WDT postscaler will not be cleared, the $\overline{TO}$ bit will not be set and $\overline{PD}$ bits will not be cleared.

- If the interrupt occurs **during or after** the execution of a SLEEP instruction, the device will immediately wake up from sleep. The SLEEP instruction will be completely executed before the wake-up. Therefore, the WDT and WDT postscaler will be cleared, the $\overline{TO}$ bit will be set and the $\overline{PD}$ bit will be cleared.

Even if the flag bits were checked before executing a SLEEP instruction, it may be possible for flag bits to become set before the SLEEP instruction completes. To determine whether a SLEEP instruction executed, test the $\overline{PD}$ bit. If the $\overline{PD}$ bit is set, the SLEEP instruction was executed as a NOP.

To ensure that the WDT is cleared, a CLRWDT instruction should be executed before a SLEEP instruction.

RLF	**Rotate Left f through Carry**
Syntax:	[*label*] RLF f,d
Operands:	0 ≤ f ≤ 127 d ∈ [0,1]
Operation:	See description below
Status Affected:	C

Encoding:	00	1101	dfff	ffff

Description: The contents of register 'f' are rotated one bit to the left through the Carry Flag. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is stored back in register 'f'.

Words:	1
Cycles:	1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process data	Write to destination

Example   RLF   REG1,0
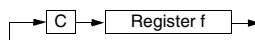
Before Instruction
REG1   =   1110 0110
C   =   0
After Instruction
REG1   =   1110 0110
W   =   1100 1100
C   =   1

RRF	**Rotate Right f through Carry**
Syntax:	[*label*] RRF f,d
Operands:	0 ≤ f ≤ 127 d ∈ [0,1]
Operation:	See description below
Status Affected:	C

Encoding:	00	1100	dfff	ffff

Description: The contents of register 'f' are rotated one bit to the right through the Carry Flag. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'.

Words:	1
Cycles:	1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process data	Write to destination

Example   RRF   REG1,0

Before Instruction
REG1   =   1110 0110
C   =   0
After Instruction
REG1   =   1110 0110
W   =   0111 0011
C   =   0

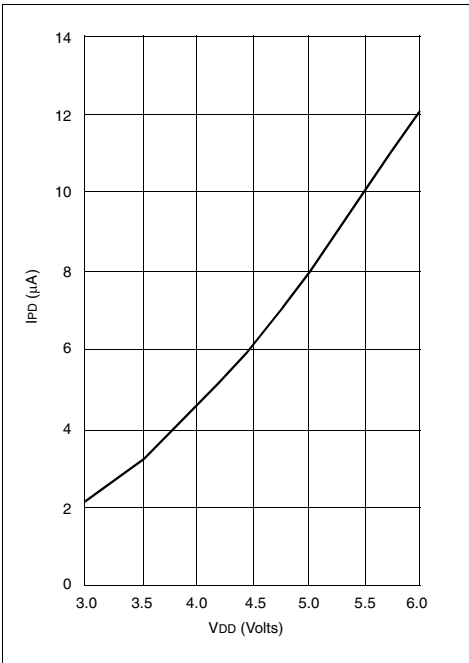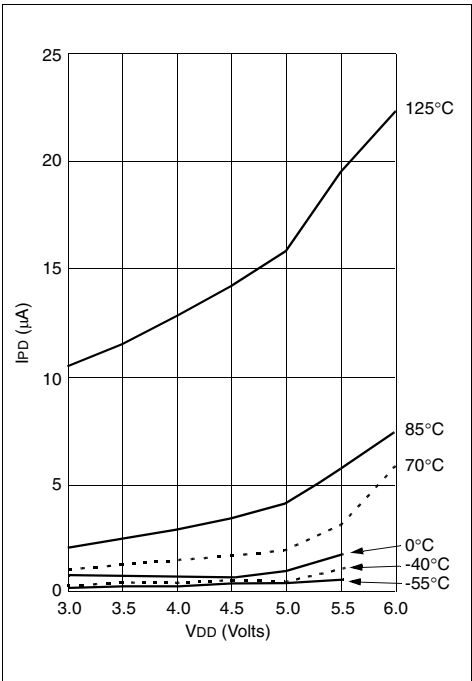**FIGURE 16-6: TYPICAL IPD VS. VDD WATCHDOG TIMER ENABLED 25°C**

FIGURE 16-7: MAXIMUM IPD VS. VDD WATCHDOG DISABLED

Data based on matrix samples. See first page of this section for details.

PIC16C6X

17.3   DC Characteristics: PIC16C62/64-04 (Commercial, Industrial)
PIC16C62/64-10 (Commercial, Industrial)
PIC16C62/64-20 (Commercial, Industrial)
PIC16LC62/64-04 (Commercial, Industrial)

DC CHARACTERISTICS		Standard Operating Conditions (unless otherwise stated)					
		Operating temperature -40°C $\leq$ TA $\leq$ +85°C for industrial and 0°C $\leq$ TA $\leq$ +70°C for commercial Operating voltage VDD range as described in DC spec Section 17.1 and Section 17.2					
Param No.	Characteristic	Sym	Min	Typ†	Max	Units	Conditions
	Input Low Voltage						
	I/O ports	VIL					
D030	with TTL buffer		VSS	-	0.15VDD	V	For entire VDD range
D030A			VSS	-	0.8V	V	4.5V $\leq$ VDD $\leq$ 5.5V
D031	with Schmitt Trigger buffer		VSS	-	0.2VDD	V	
D032	$\overline{MCLR}$, OSC1 (in RC mode)		VSS	-	0.2VDD	V	
D033	OSC1 (in XT, HS and LP)		VSS	-	0.3VDD	V	Note1
	Input High Voltage						
	I/O ports	VIH					
D040	with TTL buffer		2.0	-	VDD	V	4.5V $\leq$ VDD $\leq$ 5.5V
D040A			0.25VDD + 0.8V	-	VDD	V	For entire VDD range
D041	with Schmitt Trigger buffer		0.8VDD	-	VDD		For entire VDD range
D042	$\overline{MCLR}$		0.8VDD	-	VDD	V	
D042A	OSC1 (XT, HS and LP)		0.7VDD	-	VDD	V	Note1
D043	OSC1 (in RC mode)		0.9VDD	-	VDD	V	
D070	PORTB weak pull-up current	IPURB	50	200	400	µA	VDD = 5V, VPIN = VSS
	Input Leakage Current (Notes 2, 3)						
D060	I/O ports	IIL	-	-	±1	µA	VSS $\leq$ VPIN $\leq$ VDD, Pin at hi-impedance
D061	$\overline{MCLR}$, RA4/T0CKI		-	-	±5	µA	VSS $\leq$ VPIN $\leq$ VDD
D063	OSC1		-	-	±5	µA	VSS $\leq$ VPIN $\leq$ VDD, XT, HS and LP osc configuration
	Output Low Voltage						
D080	I/O ports	VOL	-	-	0.6	V	IOL = 8.5 mA, VDD = 4.5V, -40°C to +85°C
D083	OSC2/CLKOUT (RC osc config)		-	-	0.6	V	IOL = 1.6 mA, VDD = 4.5V, -40°C to +85°C
	Output High Voltage						
D090	I/O ports (Note 3)	VOH	VDD-0.7	-	-	V	IOH = -3.0 mA, VDD = 4.5V, -40°C to +85°C
D092	OSC2/CLKOUT (RC osc config)		VDD-0.7	-	-	V	IOH = -1.3 mA, VDD = 4.5V, -40°C to +85°C
D150*	**Open-Drain High Voltage**	VOD	-	-	14	V	RA4 pin

*   These parameters are characterized but not tested.

†   Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C6X be driven with external clock in RC mode.

2: The leakage current on the $\overline{MCLR}$/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as current sourced by the pin.

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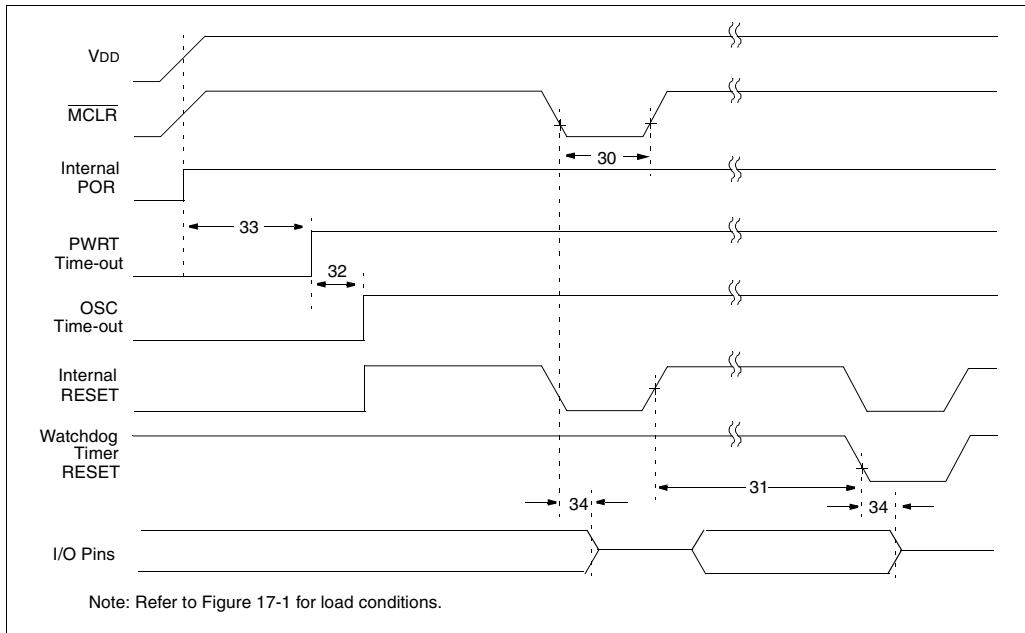**FIGURE 17-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING**

Note: Refer to Figure 17-1 for load conditions.

TABLE 17-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
30*	TmcL	MCLR Pulse Width (low)	100	—	—	ns	VDD = 5V, -40°C to +85°C
31*	Twdt	Watchdog Timer Time-out Period (No Prescaler)	7	18	33	ms	VDD = 5V, -40°C to +85°C
32	Tost	Oscillation Start-up Timer Period	—	1024TOSC	—	—	TOSC = OSC1 period
33*	Tpwrt	Power-up Timer Period	28	72	132	ms	VDD = 5V, -40°C to +85°C
34*	TIOZ	I/O Hi-impedance from MCLR Low	—	—	100	ns	

*   These parameters are characterized but not tested.

†   Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

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FIGURE 17-7: PARALLEL SLAVE PORT TIMING (PIC16C64)

Note: Refer to Figure 17-1 for load conditions
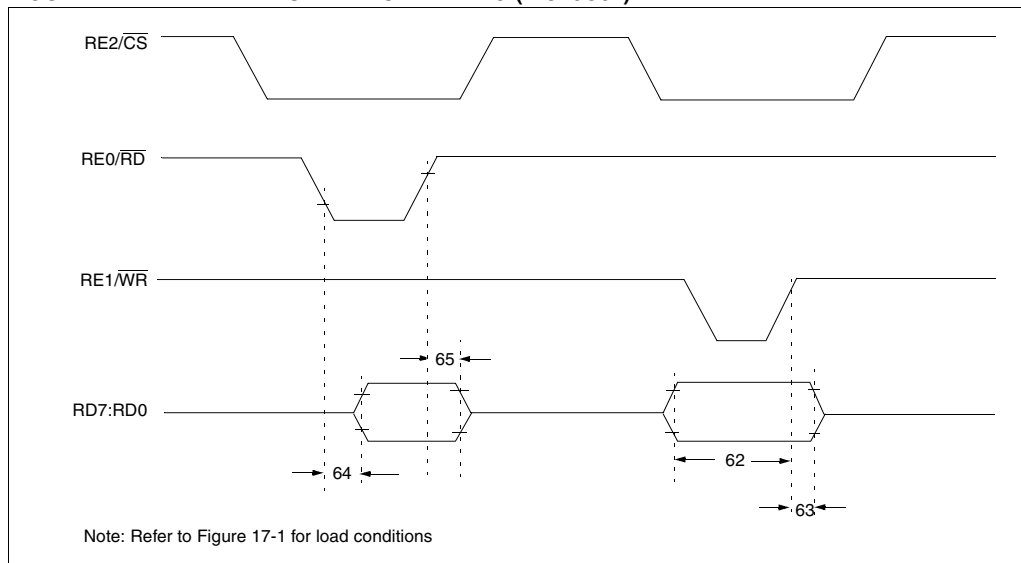
TABLE 17-7: PARALLEL SLAVE PORT REQUIREMENTS (PIC16C64)

Parameter No.	Sym	Characteristic		Min	Typ†	Max	Units	Conditions
62	TdtV2wrH	Data in valid before $\overline{WR}\uparrow$ or $\overline{CS}\uparrow$ (setup time)		20	—	—	ns	
63*	TwrH2dtl	$\overline{WR}\uparrow$ or $\overline{CS}\uparrow$ to data–in invalid (hold time)	PIC16**C**64	20	—	—	ns	
			PIC16**LC**64	35	—	—	ns	
64	TrdL2dtV	$\overline{RD}\downarrow$ and $\overline{CS}\downarrow$ to data-out valid		—	—	80	ns	
65	TrdH2dtl	$\overline{RD}\uparrow$ or $\overline{CS}\uparrow$ to data–out invalid		10	—	30	ns	

*   These parameters are characterized but not tested.

†   Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

18.5   Timing Diagrams and Specifications

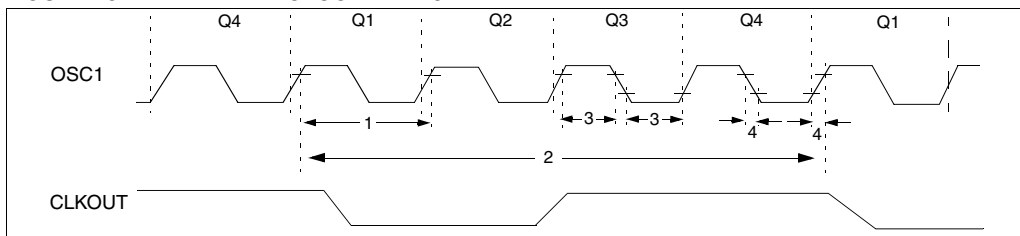### FIGURE 18-2:   EXTERNAL CLOCK TIMING

TABLE 18-2:   EXTERNAL CLOCK TIMING REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
	Fosc	**External CLKIN Frequency** (Note 1)	DC	—	4	MHz	XT and RC osc mode
			DC	—	4	MHz	HS osc mode (-04)
			DC	—	10	MHz	HS osc mode (-10)
			DC	—	20	MHz	HS osc mode (-20)
			DC	—	200	kHz	LP osc mode
		Oscillator Frequency (Note 1)	DC	—	4	MHz	RC osc mode
			0.1	—	4	MHz	XT osc mode
			4	—	20	MHz	HS osc mode
			5	—	200	kHz	LP osc mode
1	Tosc	**External CLKIN Period** (Note 1)	250	—	—	ns	XT and RC osc mode
			250	—	—	ns	HS osc mode (-04)
			100	—	—	ns	HS osc mode (-10)
			50	—	—	ns	HS osc mode (-20)
			5	—	—	µs	LP osc mode
		Oscillator Period (Note 1)	250	—	—	ns	RC osc mode
			250	—	10,000	ns	XT osc mode
			250	—	250	ns	HS osc mode (-04)
			100	—	250	ns	HS osc mode (-10)
			50	—	250	ns	HS osc mode (-20)
			5	—	—	µs	LP osc mode
2	TCY	**Instruction Cycle Time (Note 1)**	200	TCY	DC	ns	TCY = 4/Fosc
3	TosL, TosH	**External Clock in (OSC1) High or Low Time**	100	—	—	ns	XT oscillator
			2.5	—	—	µs	LP oscillator
			15	—	—	ns	HS oscillator
4	TosR, TosF	**External Clock in (OSC1) Rise or Fall Time**	—	—	25	ns	XT oscillator
			—	—	50	ns	LP oscillator
			—	—	15	ns	HS oscillator

†   Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Instruction cycle period (TCY) equals four times the input oscillator time-base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min." values with an external clock applied to the OSC1/CLKIN pin. When an external clock input is used, the "Max." cycle time limit is "DC" (no clock) for all devices.

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FIGURE 18-6:   TIMER0 AND TIMER1 EXTERNAL CLOCK TIMINGS

Note: Refer to Figure 18-1 for load conditions.
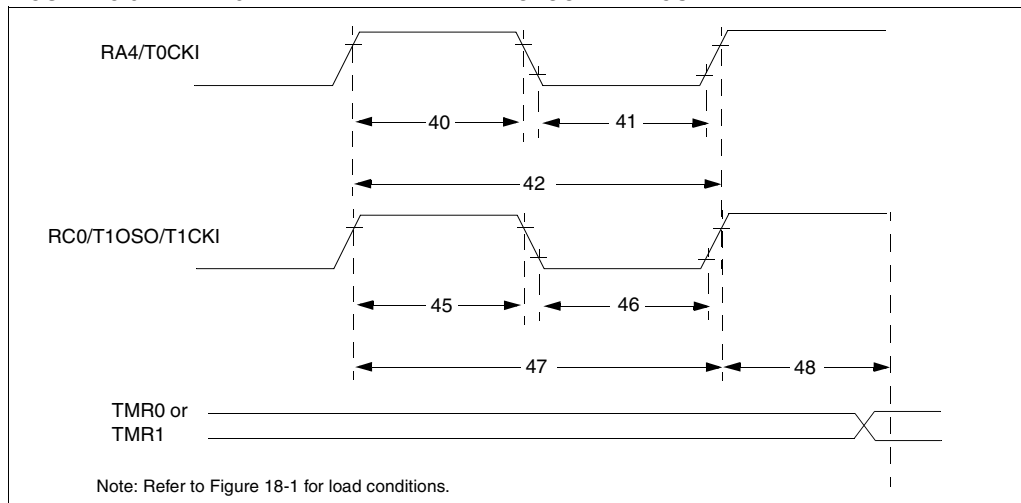
TABLE 18-5:   TIMER0 AND TIMER1 EXTERNAL CLOCK REQUIREMENTS

Param No.	Sym	Characteristic			Min	Typ†	Max	Units	Conditions
40*	Tt0H	T0CKI High Pulse Width	No Prescaler		$0.5 T_{CY} + 20$	—	—	ns	Must also meet parameter 42
			With Prescaler		10	—	—	ns	
41*	Tt0L	T0CKI Low Pulse Width	No Prescaler		$0.5 T_{CY} + 20$	—	—	ns	Must also meet parameter 42
			With Prescaler		10	—	—	ns	
42*	Tt0P	T0CKI Period	No Prescaler		$T_{CY} + 40$	—	—	ns	
			With Prescaler		Greater of: 20 or $\frac{T_{CY} + 40}{N}$	—	—	ns	N = prescale value (2, 4, ..., 256)
45*	Tt1H	T1CKI High Time	Synchronous, Prescaler = 1		$0.5 T_{CY} + 20$	—	—	ns	Must also meet parameter 47
			Synchronous, Prescaler = 2,4,8	PIC16**C**6X	15	—	—	ns	
				PIC16**LC**6X	25	—	—	ns	
			Asynchronous	PIC16**C**6X	30	—	—	ns	
				PIC16**LC**6X	50	—	—	ns	
46*	Tt1L	T1CKI Low Time	Synchronous, Prescaler = 1		$0.5 T_{CY} + 20$	—	—	ns	Must also meet parameter 47
			Synchronous, Prescaler = 2,4,8	PIC16**C**6X	15	—	—	ns	
				PIC16**LC**6X	25	—	—	ns	
			Asynchronous	PIC16**C**6X	30	—	—	ns	
				PIC16**LC**6X	50	—	—	ns	
47*	Tt1P	T1CKI input period	Synchronous	PIC16**C**6X	Greater of: 30 OR $\frac{T_{CY} + 40}{N}$	—	—	ns	N = prescale value (1, 2, 4, 8)
				PIC16**LC**6X	Greater of: 50 OR $\frac{T_{CY} + 40}{N}$				N = prescale value (1, 2, 4, 8)
			Asynchronous	PIC16**C**6X	60	—	—	ns	
				PIC16**LC**6X	100	—	—	ns	
	Ft1	Timer1 oscillator input frequency range (oscillator enabled by setting bit T1OSCEN)			DC	—	200	kHz	
48	TCKEZtmr1	Delay from external clock edge to timer increment			2Tosc	—	7Tosc	—	

*   These parameters are characterized but not tested.

†   Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

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19.3   DC Characteristics: PIC16C65-04   (Commercial, Industrial)
**   PIC16C65-10   (Commercial, Industrial)**
**   PIC16C65-20   (Commercial, Industrial)**
**   PIC16LC65-04 (Commercial, Industrial)**

DC CHARACTERISTICS		**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial and 0°C ≤ TA ≤ +70°C for commercial Operating voltage VDD range as described in DC spec Section 19.1 and Section 19.2					
Param No.	Characteristic	Sym	Min	Typ †	Max	Units	Conditions
	Input Low Voltage						
	I/O ports	VIL					
D030	with TTL buffer		Vss	-	0.15VDD	V	For entire VDD range
D030A			Vss	-	0.8V	V	4.5V ≤ VDD ≤ 5.5V
D031	with Schmitt Trigger buffer		Vss	-	0.2VDD	V	
D032	MCLR, OSC1(in RC mode)		Vss	-	0.2VDD	V	
D033	OSC1 (in XT, HS and LP)		Vss	-	0.3VDD	V	Note1
	Input High Voltage						
	I/O ports	VIH		-			
D040	with TTL buffer		2.0	-	VDD	V	4.5V ≤ VDD ≤ 5.5V
D040A			0.25VDD+ 0.8V	-	VDD	V	For entire VDD range
D041	with Schmitt Trigger buffer		0.8VDD	-	VDD		For entire VDD range
D042	MCLR		0.8VDD	-	VDD	V	
D042A	OSC1 (XT, HS and LP)		0.7 VDD	-	VDD	V	Note1
D043	OSC1 (in RC mode)		0.9VDD	-	VDD	V	
D070	PORTB weak pull-up current	IPURB	50	250	400	µA	VDD = 5V, VPIN = VSS
	Input Leakage Current (Notes 2, 3)						
D060	I/O ports	IIL	-	-	±1	µA	Vss ≤ VPIN ≤ VDD, Pin at hi-impedance
D061	MCLR, RA4/T0CKI		-	-	±5	µA	Vss ≤ VPIN ≤ VDD
D063	OSC1		-	-	±5	µA	Vss ≤ VPIN ≤ VDD, XT, HS, and LP osc configuration
	Output Low Voltage						
D080	I/O ports	VOL	-	-	0.6	V	IOL = 8.5 mA, VDD = 4.5V, -40°C to +85°C
D083	OSC2/CLKOUT (RC osc config)		-	-	0.6	V	IOL = 1.6 mA, VDD = 4.5V, -40°C to +85°C
	Output High Voltage						
D090	I/O ports (Note 3)	VOH	VDD-0.7	-	-	V	IOH = -3.0 mA, VDD = 4.5V, -40°C to +85°C
D092	OSC2/CLKOUT (RC osc config)		VDD-0.7	-	-	V	IOH = -1.3 mA, VDD = 4.5V, -40°C to +85°C
D150*	**Open-Drain High Voltage**	VOD	-	-	14	V	RA4 pin

*   These parameters are characterized but not tested.

†   Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C6X be driven with external clock in RC mode.

2: The leakage current on the MCLR/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as current sourced by the pin.

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19.4   Timing Parameter Symbology

The timing parameter symbols have been created following one of the following formats:

1. TppS2ppS   3. TCC:ST   (I^{2}C specifications only)
2. TppS   4. Ts   (I^{2}C specifications only)

T				
F	Frequency		T	Time

Lowercase letters (pp) and their meanings:

pp				
cc	CCP1		osc	OSC1
ck	CLKOUT		rd	$\overline{RD}$
cs	$\overline{CS}$		rw	$\overline{RD}$ or $\overline{WR}$
di	SDI		sc	SCK
do	SDO		ss	$\overline{SS}$
dt	Data in		t0	T0CKI
io	I/O port		t1	T1CKI
mc	$\overline{MCLR}$		wr	$\overline{WR}$

Uppercase letters and their meanings:

S				
F	Fall		P	Period
H	High		R	Rise
I	Invalid (Hi-impedance)		V	Valid
L	Low		Z	Hi-impedance
I^{2}C only				
AA	output access		High	High
BUF	Bus free		Low	Low

TCC:ST (I^{2}C specifications only)

CC				
HD	Hold		SU	Setup
ST				
DAT	DATA input hold		STO	STOP condition
STA	START condition			

FIGURE 19-1:   LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS

Load condition 1

Load condition 2

R_L = 464Ω

C_L = 50 pF   for all pins except OSC2/CLKOUT
                 but including D and E outputs as ports

       15 pF   for OSC2 output
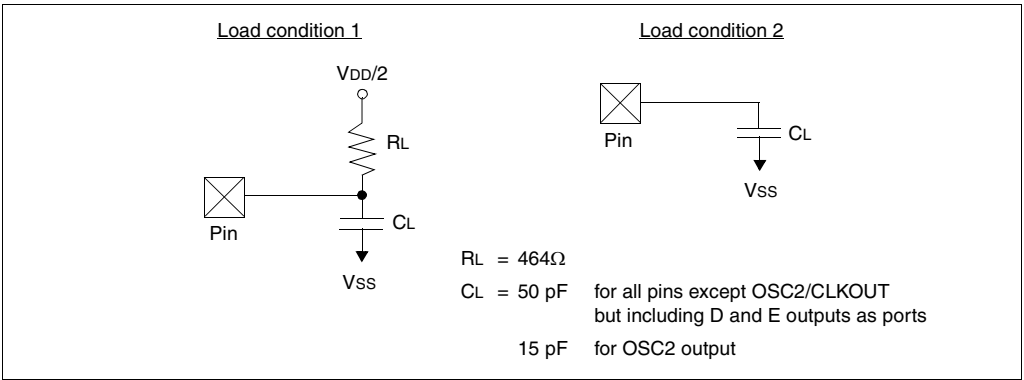
PIC16C6X

22.3   DC Characteristics: PIC16C66/67-04 (Commercial, Industrial, Extended)
PIC16C66/67-10 (Commercial, Industrial, Extended)
PIC16C66/67-20 (Commercial, Industrial, Extended)
PIC16LC66/67-04 (Commercial, Industrial)

DC CHARACTERISTICS	Standard Operating Conditions (unless otherwise stated)						
	Operating temperature $-40°C \le T_A \le +125°C$ for extended, $-40°C \le T_A \le +85°C$ for industrial and $0°C \le T_A \le +70°C$ for commercial						
	Operating voltage V_{DD} range as described in DC spec Section 22.1 and Section 22.2						
Param No.	Characteristic	Sym	Min	Typ †	Max	Units	Conditions
	Input Low Voltage						
	I/O ports	V_{IL}					
D030	with TTL buffer		V_{SS}	-	$0.15V_{DD}$	V	For entire V_{DD} range
D030A			V_{SS}	-	0.8V	V	$4.5V \le V_{DD} \le 5.5V$
D031	with Schmitt Trigger buffer		V_{SS}	-	$0.2V_{DD}$	V	
D032	$\overline{MCLR}$, OSC1 (in RC mode)		V_{SS}	-	$0.2V_{DD}$	V	
D033	OSC1 (in XT, HS and LP)		V_{SS}	-	$0.3V_{DD}$	V	Note1
	Input High Voltage						
	I/O ports	V_{IH}		-			
D040	with TTL buffer		2.0	-	V_{DD}	V	$4.5V \le V_{DD} \le 5.5V$
D040A			$0.25V_{DD}$ + 0.8V	-	V_{DD}	V	For entire V_{DD} range
D041	with Schmitt Trigger buffer		$0.8V_{DD}$	-	V_{DD}	V	For entire V_{DD} range
D042	$\overline{MCLR}$		$0.8V_{DD}$	-	V_{DD}	V	
D042A	OSC1 (XT, HS and LP)		$0.7V_{DD}$	-	V_{DD}	V	Note1
D043	OSC1 (in RC mode)		$0.9V_{DD}$	-	V_{DD}	V	
D070	PORTB weak pull-up current	I_{PURB}	50	250	400	µA	$V_{DD} = 5V$, $V_{PIN} = V_{SS}$
	Input Leakage Current (Notes 2, 3)						
D060	I/O ports	I_{IL}	-	-	±1	µA	$V_{SS} \le V_{PIN} \le V_{DD}$, Pin at hi-impedance
D061	$\overline{MCLR}$, RA4/T0CKI		-	-	±5	µA	$V_{SS} \le V_{PIN} \le V_{DD}$
D063	OSC1		-	-	±5	µA	$V_{SS} \le V_{PIN} \le V_{DD}$, XT, HS and LP osc configuration
	Output Low Voltage						
D080	I/O ports	V_{OL}	-	-	0.6	V	$I_{OL} = 8.5$ mA, $V_{DD} = 4.5V$, -40°C to +85°C
D080A			-	-	0.6	V	$I_{OL} = 7.0$ mA, $V_{DD} = 4.5V$, -40°C to +125°C
D083	OSC2/CLKOUT (RC osc config)		-	-	0.6	V	$I_{OL} = 1.6$ mA, $V_{DD} = 4.5V$, -40°C to +85°C
D083A			-	-	0.6	V	$I_{OL} = 1.2$ mA, $V_{DD} = 4.5V$, -40°C to +125°C

*   These parameters are characterized but not tested.

†   Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1:   In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C6X be driven with external clock in RC mode.

2:    The leakage current on the $\overline{MCLR}$/Vpp pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3:    Negative current is defined as current sourced by the pin.

Applicable Devices	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67

DC CHARACTERISTICS	Standard Operating Conditions (unless otherwise stated)
	Operating temperature -40°C $\leq$ TA $\leq$ +125°C for extended, -40°C $\leq$ TA $\leq$ +85°C for industrial and 0°C $\leq$ TA $\leq$ +70°C for commercial Operating voltage VDD range as described in DC spec Section 22.1 and Section 22.2

Param No.	Characteristic	Sym	Min	Typ †	Max	Units	Conditions
	Output High Voltage						
D090	I/O ports (Note 3)	VOH	VDD-0.7	-	-	V	IOH = -3.0 mA, VDD = 4.5V, -40°C to +85°C
D090A			VDD-0.7	-	-	V	IOH = -2.5 mA, VDD = 4.5V, -40°C to +125°C
D092	OSC2/CLKOUT (RC osc config)		VDD-0.7	-	-	V	IOH = -1.3 mA, VDD = 4.5V, -40°C to +85°C
D092A			VDD-0.7	-	-	V	IOH = -1.0 mA, VDD = 4.5V, -40°C to +125°C
D150*	**Open-Drain High Voltage**	VOD	-	-	14	V	RA4 pin
	Capacitive Loading Specs on Output Pins						
D100	OSC2 pin	COSC2	-	-	15	pF	In XT, HS and LP modes when external clock is used to drive OSC1.
D101	All I/O pins and OSC2 (in RC mode)	CIO	-	-	50	pF	
D102	SCL, SDA in I²C mode	Cb	-	-	400	pF	

*   These parameters are characterized but not tested.

†   Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C6X be driven with external clock in RC mode.

2: The leakage current on the $\overline{\text{MCLR}}$/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as current sourced by the pin.