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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	33
Program Memory Size	7KB (4K x 14)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	192 x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 6V
Data Converters	-
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Through Hole
Package / Case	40-DIP (0.600", 15.24mm)
Supplier Device Package	40-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16c65a-20-p

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FIGURE 4-8: PIC16C66/67 DATA MEMORY MAP

(4)		(*)	1	(*)	1		
Indirect addr.(*)	00h	Indirect addr.(*)	80h	Indirect addr. ^(*)	100h	Indirect addr. ^(*)	180
TMR0	01h	OPTION	81h	TMR0	101h	OPTION	181
PCL	02h	PCL	82h	PCL	102h	PCL	182
STATUS	03h	STATUS	83h	STATUS	103h	STATUS	183
FSR	04h	FSR	84h	FSR	104h	FSR	184
PORTA	05h	TRISA	85h		105h		185
PORTB	06h	TRISB	86h	PORTB	106h	TRISB	186
PORTC	07h	TRISC	87h		107h		187
PORTD (1)	08h	TRISD (1)	88h		108h		188
PORTE (1)	09h	TRISE (1)	89h		109h		189
PCLATH	0Ah	PCLATH	8Ah	PCLATH	10Ah	PCLATH	18/
INTCON	0Bh	INTCON	8Bh	INTCON	10Bh	INTCON	18E
PIR1	0Ch	PIE1	8Ch		10Ch		180
PIR2	0Dh	PIE2	8Dh		10Dh		180
TMR1L	0Eh	PCON	8Eh		10Eh		18
TMR1H	0Fh		8Fh		10Fh		18
T1CON	10h		90h		110h		190
TMR2	11h		91h		111h		191
T2CON	12h	PR2	92h		112h		192
SSPBUF	13h	SSPADD	93h		113h		193
SSPCON	14h	SSPSTAT	94h		114h		194
CCPR1L	15h		95h		115h		195
CCPR1H	16h		96h		116h	a .	196
CCP1CON	17h		97h	General	117h	General	197
RCSTA	18h	TXSTA	98h	Register	118h	Register	198
TXREG	19h	SPBRG	99h	16 Bytes	119h	16 Bytes	199
RCREG	1Ah		9Ah		11Ah		19/
CCPR2L	1Bh		9Bh		11Bh		19
CCPR2H	1Ch		9Ch		11Ch		190
CCP2CON	1Dh		9Dh		11Dh		19
	1Eh		9Eh		11Eh		198
	1Fh		9Fh		11Fh		19
	20h		A0h		120h		1A
General Purpose Register 96 Bytes		General Purpose Register 80 Bytes	EEh	General Purpose Register 80 Bytes	16Eb	General Purpose Register 80 Bytes	1E
,		accesses 70h-7Fh	F0h	accesses 70h-7Fh	170h	accesses 70h-7Fh	1F(
Deals 0	7Fh	III Balik U	FFh	Bank 0	17Fh	Bank 3	1FI
Bank 0 Unimplemente Not a physical hese registers are	ed data me register. not impler	Bank 1 mory locations, read	as '0'. 6C66.	Bank 2		Bank 3	
Note: The u	pper 16 by	ytes of data memo	ory in bar	iks 1, 2, and 3 are	mapped i	n Bank 0. This may	y requ

4.2.2.7 PIR2 REGISTER

Applicable Devices 61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

This register contains the CCP2 interrupt flag bit.

Note: Interrupt flag bits get set when an interrupt condition occurs regardless of the state of its corresponding enable bit or the global enable bit, GIE (INTCON<7>). User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

FIGURE 4-21: PIR2 REGISTER (ADDRESS 0Dh)



11.2 <u>SPI Mode for PIC16C62/62A/R62/63/</u> R63/64/64A/R64/65/65A/R65

This section contains register definitions and operational characteristics of the SPI module for the PIC16C62, PIC16C62A, PIC16CR62, PIC16C63, PIC16CR63, PIC16C64A, PIC16CR64, PIC16CR64, PIC16C65, PIC16C65A, PIC16CR65.

FIGURE 11-1: SSPSTAT: SYNC SERIAL PORT STATUS REGISTER (ADDRESS 94h)

U-0	U-0	R-0	R-0	R-0	R-0	R-0	R-0									
—		D/A	Р	S	R/W	UA	BF	R = Readable bit								
bit7							bit0	W = Writable bit								
								as '0'								
								- n =Value at POR reset								
bit 7-6:	Unimp	emented	Read as	'0'												
bit 5:	 D/Ā: Data/Address bit (l²C mode only) 1 = Indicates that the last byte received or transmitted was data 															
	 1 = Indicates that the last byte received or transmitted was data 0 = Indicates that the last byte received or transmitted was address 															
hit 4	P. Ston	P : Stop bit (I ² C mode only. This bit is cleared when the SSP module is disabled, SSPEN is cleared)														
ын 4.	1 = Indi	 1 = Indicates that a stop bit has been detected last (this bit is '0' on RESET) 2 Step bit was act detected last 														
	0 = Sto	= Stop bit was not detected last														
bit 3:	S: Start	bit (I ² C m	node only.	This bit is o	cleared wher	the SSP n	nodule is disa	abled, SSPEN is cleared)								
	1 = Indi 0 = Sta	1 = Indicates that a start bit has been detected last (this bit is '0' on RESET) 0 = Start bit was not detected last														
hit 2.	e − eta R/W· B	0 = Start bit was not detected last $\mathbf{R}\overline{\mathbf{W}}$: Bead/Write bit information (I ² C mode only)														
DR E.	This bit	holds the	R/W bit i	nformation	following the	alast addre	ess match. Th	nis bit is valid from the address								
	match t	o the next	start bit, s	stop bit, or	ACK bit.											
	1 = Rea 0 = Wri	ad te														
hit 1·		 date Addr	ess (10-hi	t I ² C mode	only)											
2.1.11	1 = Indi	cates that	the user i	needs to up	date the add	dress in the	SSPADD reg	gister								
	0 = Adc	lress does	s not need	to be upda	ited											
bit 0:	BF: But	fer Full St	atus bit													
	Receive	e (SPI and	I I ² C mode	es)												
	1 = Rec 0 - Rec	ceive com	plete, SSP	'BUF is tull SSPRLIE is	emntv											
	Transm	it (I ² C mo	de only)	001 001 13	Subry											
	1 = Trai	nsmit in pr	ogress, S	SPBUF is f	ull											
	0 = Trai	nsmit com	plete, SSF	PBUF is err	pty											

FIGURE 13-2: CONFIGURATION WORD FOR PIC16C62/64/65

— bit13			-	-	_	_	CP1	CP0	PWRTE	WDTE	FOSC1	FOSC0 bit0	Register: Address	CONFIG 2007h
bit 13-6:	Unimpleme	nted: Re	ead a	s '1'										
bit 5-4:	CP1:CP0 : C 11 = Code p 10 = Upper I 01 = Upper 3 00 = All men	ode Pro protection half of pr 3/4th of mory is c	tectio n off rograi progra code p	n bits m men am me protect	nory co mory c ed	de pro	tected otected							
bit 3:	PWRTE : Pov 1 = Power-up 0 = Power-up	wer-up T p Timer p Timer	Fimer enabl disab	Enable led led	e bit									
bit 2:	WDTE: Wate 1 = WDT ena 0 = WDT dis	chdog Ti abled abled	imer E	Enable	bit									
bit 1-0:	FOSC1:FOS 11 = RC osc 10 = HS osc 01 = XT osc 00 = LP osc	SCO: Oso cillator cillator cillator illator illator	cillato	r Seleo	tion bi	ts								

FIGURE 13-3: CONFIGURATION WORD FOR PIC16C62A/R62/63/R63/64A/R64/65A/R65/66/67

CP1	CP0	CP1	CP0	CP1	CP0	-	BODEN	CP1	CP0	PWRTE	WDTE	FOSC1	FOSC0	Register:	CONFIG	
bit13													bit0	Address	2007h	
bit 13- bit 5:4	8: CP 11 10 01 00	 <i>i</i> = Code protection bits^{ic/} <i>i</i> = Code protection off <i>i</i> = Upper half of program memory code protected <i>i</i> = Upper 3/4th of program memory code protected <i>i</i> = All memory is code protected 														
bit 7:	Un	Jnimplemented: Read as '1'														
bit 6:	BC 1 = 0 =	ODEN: Brown-out Reset Enable bit ⁽¹⁾ = Brown-out Reset enabled = Brown-out Reset disabled														
bit 3:	PV 1 = 0 =	V RTE : Power-up Timer Enable bit ⁽¹⁾ = Power-up Timer disabled D = Power-up Timer enabled														
bit 2:	WI 1 = 0 =	DTE : W WDT (WDT (atchdog enablec disablec	g Timer I d	Enable	e bit										
bit 1-0	D: FC 11 10 01 00	FOSC1:FOSC0: Oscillator Selection bits 11 = RC oscillator 10 = HS oscillator 01 = XT oscillator 00 = LP oscillator														
Note	1: En En 2: All	abling E sure the of the (Brown-o e Powe CP1:CF	out Res r-up Tir 90 pairs	et auto ner is e have t	matical nabled o be giv	ly enable anytime ven the s	es Powe Brown ame va	er-up T I-out Re alue to	imer (PV eset is ei impleme	VRT) re nabled. int the o	egardle: code pr	ss of the sotection s	value of bit P	WRTE.	

-

TABLE 13-1: CERAMIC RESONATORS PIC16C61

Ranges Te	Ranges Tested:												
Mode	Freq	OSC1	OSC2										
XT	455 kHz	47 - 100 pF	47 - 100 pF										
	2.0 MHz	15 - 68 pF	15 - 68 pF										
	4.0 MHz	15 - 68 pF	15 - 68 pF										
HS	8.0 MHz	15 - 68 pF	15 - 68 pF										
16.0 MHz 10 - 47 pF 10 - 47 pF													
These values are for design guidance only. See													
note	es at bottom of page	ge.											
Resonator	rs Used:												
455 kHz	Panasonic EF	D-A455K04B	± 0.3%										
2.0 MHz	Murata Erie CS	SA2.00MG	± 0.5%										
4.0 MHz	Murata Erie CS	SA4.00MG	± 0.5%										
8.0 MHz	Murata Erie CS	SA8.00MT	$\pm 0.5\%$										
16.0 MHz	16.0 MHz Murata Erie CSA16.00MX ± 0.5%												
All reso	nators used did r	ot have built-in	capacitors.										

TABLE 13-2: CERAMIC RESONATORS PIC16C62/62A/R62/63/R63/64/ 64A/R64/65/65A/R65/66/67

Ranges Te	Ranges Tested:												
Mode	Freq	OSC1	OSC2										
XT	455 kHz	68 - 100 pF	68 - 100 pF										
	2.0 MHz	15 - 68 pF	15 - 68 pF										
	4.0 MHz	15 - 68 pF	15 - 68 pF										
HS	8.0 MHz	10 - 68 pF	10 - 68 pF										
16.0 MHz 10 - 22 pF 10 - 22 pF													
The note	These values are for design guidance only. See notes at bottom of page.												
Resonato	rs Used:												
455 kHz	Panasonic E	FO-A455K04B	$\pm 0.3\%$										
2.0 MHz	Murata Erie	CSA2.00MG	$\pm 0.5\%$										
4.0 MHz	Murata Erie	CSA4.00MG	$\pm 0.5\%$										
8.0 MHz	Murata Erie	CSA8.00MT	± 0.5%										
16.0 MHz	Murata Erie	CSA16.00MX	$\pm 0.5\%$										
All reso	onators used die	d not have built-in	capacitors.										

TABLE 13-3: CAPACITOR SELECTION FOR CRYSTAL OSCILLATOR FOR PIC16C61

Mode	Freq	OSC1	OSC2								
LP	32 kHz	33 - 68 pF	33 - 68 pF								
	200 kHz	15 - 47 pF	15 - 47 pF								
XT	100 kHz	47 - 100 pF	47 - 100 pF								
	500 kHz	20 - 68 pF	20 - 68 pF								
	1 MHz	15 - 68 pF	15 - 68 pF								
	2 MHz	15 - 47 pF	15 - 47 pF								
	4 MHz	15 - 33 pF	15 - 33 pF								
HS	8 MHz	15 - 47 pF	15 - 47 pF								
	20 MHz	15 - 47 pF	15 - 47 pF								
Th	These values are for design guidance only. See										
no	tes at bottom o	f page.									

TABLE 13-4: CAPACITOR SELECTION FOR CRYSTAL OSCILLATOR FOR PIC16C62/62A/R62/63/R63/64/ 64A/R64/65/65A/R65/66/67

Оѕс Туре	Crystal Freq	Cap. Range C1	Cap. Range C2							
LP	32 kHz	33 pF	33 pF							
	200 kHz	15 pF	15 pF							
XT	200 kHz	47-68 pF	47-68 pF							
	1 MHz	15 pF	15 pF							
	4 MHz	15 pF	15 pF							
HS	4 MHz	15 pF	15 pF							
	8 MHz	15-33 pF	15-33 pF							
	20 MHz	15-33 pF	15-33 pF							
These values are for design guidance only. Se										
notes		payo.								
	Crys	stais Used								
30 147	Encon C-00	11D22 768K-A	+ 20 DDM							

32 kHz	Epson C-001R32.768K-A	± 20 PPM
200 kHz	STD XTL 200.000KHz	± 20 PPM
1 MHz	ECS ECS-10-13-1	± 50 PPM
4 MHz	ECS ECS-40-20-1	± 50 PPM
8 MHz	EPSON CA-301 8.000M-C	± 30 PPM
20 MHz	EPSON CA-301 20.000M-C	± 30 PPM

Note 1: Recommended values of C1 and C2 are identical to the ranges tested Table 13-1 and Table 13-2.

2: Higher capacitance increases the stability of oscillator but also increases the start-up time.

3: Since each resonator/crystal has its own characteristics, the user should consult the resonator/crystal manufacturer for appropriate values of external components.

4: Rs may be required in HS mode as well as XT mode to avoid overdriving crystals with low drive level specification.

Register	Applicable Devices											Power-o Brow Re	on Reset n-out set	MCLR Reset during: – normal operation – SLEEP WDT Reset	Wake-up via interrupt or WDT Wake-up			
TRISD	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67	1111	1111	1111 1111	uuuu uuuu
TRISE	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67	0000	-111	0000 -111	uuuu -uuu
PIE1	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67	00	0000	00 0000	uu uuuu
	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67	0000	0000	0000 0000	uuuu uuuu
PIE2	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67		0	0	u
PCON	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67		0u	uu	uu
1 CON	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67		0 -	u-	u-
PR2	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67	1111	1111	1111 1111	1111 1111
SSPADD	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67	0000	0000	0000 0000	uuuu uuuu
SSPSTAT	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67	0 0	0000	00 0000	uu uuuu
TXSTA	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67	0000	-010	0000 -010	uuuu -uuu
SPBRG	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67	0000	0000	0000 0000	uuuu uuuu

TABLE 13-12: INITIALIZATION CONDITIONS FOR ALL REGISTERS (Cont.'d)

Legend: u = unchanged, x = unknown, -= unimplemented bit read as '0', q = value depends on condition.

Note 1: One or more bits in INTCON, PIR1 and/or PIR2 will be affected (to cause wake-up).

2: When the wake-up is due to an interrupt and the global enable bit, GIE is set, the PC is loaded with the interrupt vector (0004h) after execution of PC + 1.

3: See Table 13-10 and Table 13-11 for reset value for specific conditions.

FIGURE 13-11: TIME-OUT SEQUENCE ON POWER-UP (MCLR NOT TIED TO VDD): CASE 1



FIGURE 13-12: TIME-OUT SEQUENCE ON POWER-UP (MCLR NOT TIED TO VDD): CASE 2



FIGURE 13-13: TIME-OUT SEQUENCE ON POWER-UP (MCLR TIED TO VDD)



Increme	nt f, Skip	if O		IORLW	Inclusive	OR Lite	eral with	w		
[label]	INCFSZ	f,d		Syntax:	[label]	IORLW	k			
$0 \le f \le 12$.7			Operands:	$0 \le k \le 2$	55				
$d \in [0,1]$				Operation:	(W) .OR.	$k \rightarrow (W)$)			
(f) + 1 \rightarrow	(destinat	ion),		Status Affected:	Z					
Nono	suit – U			Encoding:	11	1000	kkkk	kkkk		
00	1111	dfff	ffff	Description:	The conte OR'ed with	nts of the	W register t bit literal	r is 'k'. The		
The conte mented. If	nts of regi: 'd' is 0 the	ster 'f' are e result is p	incre- placed in	Manda.	result is pl	aced in th	ie W regist	ier.		
the W regi placed bac	ster. If 'd' i ck in reaist	s 1 the res er 'f'.	sult is	words:	1					
If the resu executed.	It is 1, the If the resu	next instru It is 0. a N	ction is OP is exe-	Cycles:	1	00	00	04		
cuted inste	ead makin	g it a 2Tcy	instruc-	Q Cycle Activity:	Q1	Q2	Q3	Q4		
1					Decode	Read literal 'k'	Process data	Write to W		
1(2)										
Q1	Q2	Q3	Q4	Example	IORLW	0x35				
Decode	Read	Process	Write to		Before In	struction	ΟχΘΑ			
	register 'f'	data	destination		After Instruction W = 0xBF					
(2nd Cyc	le)									
Q1	Q2	Q3	Q4			Z =	I			
No- Operation	No- Operation	No- Operation	No- Operation							
HERE CONTINU Before In PC After Inst CNT if CNT if CNT PC if CNT	INCFS GOTO UE • • • • • • • • • • • • • • • • • • •	ress HERE T + 1 ress CONT	NT, 1 DP INUE							
	Increment [label] $0 \le f \le 12$ $d \in [0,1]$ (f) + 1 \rightarrow skip if ress None 00 The contermented. If the W regipted back if the result executed. cuted instation. 1 1(2) Q1 Decode (2nd Cyce Q1 No- Operation HERE CONTINU Before Inn PC After Instation if CNT PC	Increment f, Skip [label] INCFSZ $0 \le f \le 127$ $d \in [0,1]$ (f) + 1 \rightarrow (destinat skip if result = 0 None 00 1111 The contents of regis mented. If 'd' is 0 the the W register. If 'd' is placed back in regist If the result is 1, the executed. If the result cuted instead making tion. 1 1(2) Q1 Q2 Decode Read register 'f' (2nd Cycle) Q1 Q2 Decode Read register 'f' (2nd Cycle) Q1 Q2 No- Operation Operation HERE INCFS GOTO CONTINUE • • • Before Instruction CNT = CNT if CNT= 0, PC = addi if CNT≠ 0, PC = addi	Increment f, Skip if 0 [label] INCFSZ f,d $0 \le f \le 127$ $d \in [0,1]$ (f) + 1 -> (destination), skip if result = 0 None 00 1111 dfff The contents of register 'f' are mented. If 'd' is 0 the result is p the W register. If 'd' is 1 the result is 0, the result is 1, the next instru- executed. If the result is 0, the Next cuted instead making it a 2Tcv tion. 1 1(2) Q1 Q2 Q3 Decode Read register 'f' Process data (2nd Cycle) Q1 Q2 Q3 No- Operation Operation Operation HERE INCFSZ CL CONTINUE • • Before Instruction PC = address HERE After Instruction CNT = CNT + 1 if CNT= 0, PC = address CONT if CNT = 0, PC = address HERE	Increment f, Skip if 0[label] INCFSZ f,d $0 \le f \le 127$ $d \in [0,1]$ (f) + 1 \rightarrow (destination), skip if result = 0None00111101dfffThe contents of register 'f' are incremented. If 'd' is 0 the result is placed in the Wregister. If 'd' is 1 the result is placed back in register 'f'.If the result is 1, the next instruction is executed instead making it a 2TCY instruction.11(2)Q1Q2Q3Q4DecodeRead register 'f'Process dataWrite to destination(2nd Cycle)Q1Q2Q1Q2Q3Q4No- No- OperationMERE GOTO CONTINUE •No- No- No- No- No- CONTINUE •Before Instruction PC = address HEREAfter Instruction CNT = CNT + 1 if CNT = 0, PC PC PC CPC = address HERE + 1	Increment f, Skip if 0IORLW $[label]$ INCFSZ f,dSyntax: $0 \le f \le 127$ Operands:Operands: $d \in [0,1]$ Operation),Skip if result = 0NoneStatus Affected: 00 1111dfff 00 1111dfffThe contents of register 'f' are incremented. If 'd' is 0 the result is placed in the W register. If 'd is 1 the result is placed back in register 'f'.Words:If the result is 1, the next instruction is executed in the executed in the variation of the register 'f'.Words:11(2)Q1Q2Q1Q2Q3Q4DecodeRead register 'f'Process destinationWrite to destination(2nd Cycle)Q1Q2Q3Q1Q2Q3Q4None OperationNo- OperationNo- OperationHEREINCFSZ (CONTINUE + -CNT, 1 GOTO LOOPCONTINUE + Before Instruction PC=PC=Address HERE After Instruction CNT = CNT + 1 if CNT = 0, PCPC=address CONTINUE if CNT = 0, PC=PC=address HERE + 11	Increment f, Skip if 0IORLWInclusive $[label]$ INCFSZ f,dSyntax: $[label]$ $0 \leq f \leq 127$ $d \in [0,1]$ Operation),Skip if result = 0(f) + 1 \rightarrow (destination),Skip if result = 0Operation:(W) .OR.None $0 \circ 1111$ dfffffffThe contents of register 'f' are incremented. If 'd' is 0 the result is placed inDescription:The contents of register 'f'.The contents of register 'f'.If the result is 0, a NOP is executed instead making it a 2TCY instruction.Words:11(2)Q1Q2Q3Q4DecodeRead register 'TProcess destinationWirite to destination1ICIORLWExample1DecodeRead register 'TNo- Operation1Q1Q2Q3Q4DecodeRead register 'TNo- OperationNo- Operation1Marce Stere contrinueIORLWHEREINCFSZ GOTO LOOPCONTCONTINUE• •••Before Instruction CNT = OTT =CNT + 1 if CNT= 0, PC = address HERE + 1PC=address HERE + 1	Increment f, Skip if 0Inclusive OR Litter $[label]$ INCFSZ f,dSyntax: $[label]$ IORLW $0 \le f \le 127$ $d \in [0,1]$ Operation $0 \le k \le 255$ $d \in [0,1]$ Operation $0 \le k \le 255$ Operation:(W) .OR. $k \rightarrow (W)$ $(f) + 1 \rightarrow (destination), skip if result = 0$ None $0 \le k \le 255$ Operation:(W) .OR. $k \rightarrow (W)$ $0 \circ 1111$ dfffffffInclusive OR LitterZThe contents of register 'f are incremented. If d' is 0 the result is placed in the W register. If d' is 1 the result is placed in the W register. If d' is 1 the result is placed in the weight secuted instead making it a 2TCY instruction.Description:The contents of the eight result is placed in the eight result is placed back in register 'f.11(2)Q1Q2Q3Q4 $Q = Q1$ Q2Q3Q4 $Q = CQ3$ $Q = CQ3$ $Q = Q1$ Q2Q3Q4 $Q = CQ3$ $Q = Q3$ $Q = Q1$ Q2Q3Q4 $Q = CQ3$ $Q = Q3$ $Q = Q1$ Q2Q3Q4 $Q = CQ3$ $Q = Q3$ $Q = Q1$ Q2Q3Q4 $Q = Q3$ $Q = Q3$ $Q = Q1$ Q2Q3Q4 $Q = Z = Z$ $Q = Z = Z$ $Q = Q1$ Q2Q3Q4 $Q = Z = Z$ $Z = Z$ $Q = Q1$ Q2Q3Q4 $Q = Z = Z$ $Z = Z$ $Q = Q1$ Q2Q3Q4 $Q = Z = Z$ $Z = Z$ $Q = Q1$ Q2Q3Q4 $Q = Z = Z$ $Z = Z = Z$ $Q = Q1$	Increment f, Skip if 0 $[label]$ INCFSZ f,d $[label]$ INCFSZ f,d $0 \le f \le 127$ $0 \le f \le 127$ $d \in [0,1]$ (f) + 1 \rightarrow (destination), skip if result = 0None $0 \le 1111$ $dfff$ 111 $dfff$ ffffThe contents of register 'f' are incremented. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed in the W register if' d' is 1 the result is placed in the result is 0, a NOP is executed. If the result is 0, a NOP is executed. If the result is 0, a NOP is executed. If the result is 0, a NOP is executed. If the result is 0, a NOP is executed. If the result is 0, a NOP is executed. If the result is 0, a NOP is executed. If the result is 0, a NOP is executed. If the result is 0, and Destinon11(2)Q1Q1Q2Q3Q4 $Decode$ $Read$ $Pcodes$ $Read$ $Process$ Q1Q2Q3Q1Q2Q3Q1Q2Q3Q1Q2Q3Q1Q2Q3Q1Q2Q3Q1Q2Q3Q1Q2Q3Q2Q3Q4 $W = 0xBF$ Z $Z = 1$		

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FIGURE 15-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING

TABLE 15-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Тур†	Max	Units	Conditions
30*	TmcL	MCLR Pulse Width (low)	200	—	—	ns	VDD = 5V, -40°C to +125°C
31*	Twdt	Watchdog Timer Time-out Period (No Prescaler)	7	18	33	ms	VDD = 5V, -40°C to +125°C
32	Tost	Oscillation Start-up Timer Period	—	1024Tosc	—		TOSC = OSC1 period
33*	Tpwrt	Power-up Timer Period	28	72	132	ms	$VDD = 5V, -40^{\circ}C \text{ to } +125^{\circ}C$
34*	Tıoz	I/O Hi-impedance from MCLR Low	—	—	100	ns	

* These parameters are characterized but not tested.

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17.1 DC Characteristics: PIC16C62/64-04 (Commercial, Industrial) PIC16C62/64-10 (Commercial, Industrial) PIC16C62/64-20 (Commercial, Industrial)

		Standa	rd Ope	rating	Condi	tions (ı	unless otherwise stated)
DC CHAR	ACTERISTICS	Operatir	ng temp	erature	e -4()°C ≤	\leq TA \leq +85°C for industrial and
					0°0	C ≤	\leq TA \leq +70°C for commercial
Param No.	Characteristic	Sym	Min	Тур†	Max	Units	Conditions
D001	Supply Voltage	Vdd	4.0	-	6.0	V	XT, RC and LP osc configuration
D001A			4.5	-	5.5	V	HS osc configuration
D002*	RAM Data Retention Voltage (Note 1)	Vdr	-	1.5	-	V	
D003	VDD start voltage to ensure internal Power- on Reset signal	VPOR	-	Vss	-	V	See section on Power-on Reset for details
D004*	VDD rise rate to ensure internal Power-on Reset signal	Svdd	0.05	-	-	V/ms	See section on Power-on Reset for details
D010	Supply Current (Note 2, 5)	IDD	-	2.7	5.0	mA	XT, RC, osc configuration FOSC = 4 MHz, VDD = 5.5V (Note 4)
D013			-	13.5	30	mA	HS osc configuration Fosc = 20 MHz, VDD = 5.5V
D020 D021 D021A	Power-down Current (Note 3, 5)	IPD	- - -	10.5 1.5 1.5	42 21 24	μΑ μΑ μΑ	$\label{eq:VDD} \begin{array}{l} VDD=4.0V, WDT \mbox{ enabled}, -40^\circ C \mbox{ to } +85^\circ C \\ VDD=4.0V, WDT \mbox{ disabled}, -0^\circ C \mbox{ to } +70^\circ C \\ VDD=4.0V, WDT \mbox{ disabled}, -40^\circ C \mbox{ to } +85^\circ C \end{array}$

These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.

The test conditions for all IDD measurements in active operation mode are:

OSC1 = external square wave, from rail to rail; all I/O pins tristated, pulled to VDD

 $\overline{MCLR} = VDD$; WDT enabled/disabled as specified.

3: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSs.

- 4: For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula Ir = VDD/2Rext (mA) with Rext in kOhm.
- 5: Timer1 oscillator (when enabled) adds approximately 20 μA to the specification. This value is from characterization and is for design guidance only. This is not tested.

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FIGURE 19-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING

TABLE 19-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Тур†	Мах	Units	Conditions
30*	TmcL	MCLR Pulse Width (low)	100	—	I	ns	VDD = 5V, -40°C to +85°C
31*	Twdt	Watchdog Timer Time-out Period (No Prescaler)	7	18	33	ms	$VDD = 5V$, $-40^{\circ}C$ to $+85^{\circ}C$
32	Tost	Oscillation Start-up Timer Period		1024Tosc		—	TOSC = OSC1 period
33*	Tpwrt	Power-up Timer Period or WDT reset	28	72	132	ms	VDD = 5V, -40°C to +85°C
34	Tioz	I/O Hi-impedance from MCLR Low	-	—	100	ns	

These parameters are characterized but not tested.

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TABLE 19-8: SPI MODE REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Typ†	Мах	Units	Conditions
70	TssL2scH, TssL2scL	\overline{SS} ↓ to SCK↓ or SCK↑ input	Тсү	_	l	ns	
71	TscH	SCK input high time (slave mode)	TCY + 20	_	_	ns	
72	TscL	SCK input low time (slave mode)	Tcy + 20	—		ns	
73	TdiV2scH, TdiV2scL	Setup time of SDI data input to SCK edge	50	_		ns	
74	TscH2diL, TscL2diL	Hold time of SDI data input to SCK edge	50	_		ns	
75	TdoR	SDO data output rise time	_	10	25	ns	
76	TdoF	SDO data output fall time		10	25	ns	
77	TssH2doZ	SS↑ to SDO output hi-impedance	10	—	50	ns	
78	TscR	SCK output rise time (master mode)		10	25	ns	
79	TscF	SCK output fall time (master mode)	_	10	25	ns	
80	TscH2doV, TscL2doV	SDO data output valid after SCK edge	_	_	50	ns	

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FIGURE 19-9: I²C BUS START/STOP BITS TIMING



TABLE 19-9: I²C BUS START/STOP BITS REQUIREMENTS

Parameter No.	Sym	Characteristic		Min	Тур	Мах	Units	Conditions	
90	TSU:STA	START condition	100 kHz mode	4700	—	-	ne	Only relevant for repeated START	
		Setup time	400 kHz mode	600	—	—	113	condition	
91	THD:STA	START condition	100 kHz mode	4000	—	—	20	After this period the first clock	
		Hold time	400 kHz mode	600	_	_	115	pulse is generated	
92	TSU:STO	STOP condition	100 kHz mode	4700	_	_	ne		
		Setup time	400 kHz mode	600	—	—	115		
93	THD:STO	STOP condition	100 kHz mode	4000	—	—	ne		
		Hold time	400 kHz mode	600	—	—	115		

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FIGURE 21-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING

FIGURE 21-5: BROWN-OUT RESET TIMING



TABLE 21-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, POWER-UP TIMER, AND BROWN-OUT RESET REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Тур†	Мах	Units	Conditions
-							
30	TmcL	MCLR Pulse Width (low)	2	—	—	μs	VDD = 5V, -40°C to +125°C
31*	Twdt	Watchdog Timer Time-out Period (No Prescaler)	7	18	33	ms	VDD = 5V, -40°C to +125°C
32	Tost	Oscillation Start-up Timer Period		1024 Tosc	—	—	TOSC = OSC1 period
33*	Tpwrt	Power-up Timer Period	28	72	132	ms	VDD = 5V, -40°C to +125°C
34	Tıoz	I/O Hi-impedance from MCLR Low or WDT reset		_	2.1	μs	
35	TBOR	Brown-out Reset Pulse Width	100	_	—	μs	$VDD \le BVDD$ (D005)

* These parameters are characterized but not tested.

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FIGURE 21-7: CAPTURE/COMPARE/PWM TIMINGS (CCP1 AND CCP2)

TABLE 21-6: CAPTURE/COMPARE/PWM REQUIREMENTS (CCP1 AND CCP2)

Param No.	Sym	Characteristic			Min	Тур†	Max	Units	Conditions
50*	50* TccL CCP1 and CCP2 input low time		No Prescaler		0.5Tcy + 20	_	_	ns	
			With Prescaler	PIC16CR63/R65	10	—	—	ns	
				PIC16LCR63/R65	20	—	_	ns	
51*	51* TccH CCP1 and CCP2		No Prescaler		0.5TCY + 20	—	_	ns	
	input high time	input high time	With Prescaler	PIC16 CR 63/R65	10		_	ns	
				PIC16LCR63/R65	20		_	ns	
52*	TccP	CCP1 and CCP2 ir	nput period		<u>3Tcy + 40</u> N		-	ns	N = prescale value (1,4, or 16)
53*	TccR	CCP1 and CCP2 o	utput rise time	PIC16 CR 63/R65	—	10	25	ns	
				PIC16LCR63/R65	—	25	45	ns	
54*	TccF	CCP1 and CCP2 output fall time		PIC16 CR 63/R65	—	10	25	ns	
				PIC16LCR63/R65	_	25	45	ns	

* These parameters are characterized but not tested.



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24.4 18-Lead Plastic Surface Mount (SOIC - Wide, 300 mil Body) (SO)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging







	Package Group: Plastic SOIC (SO)											
		Millimeters		Inches								
Symbol	Min	Мах	Notes	Min	Мах	Notes						
α	0°	8 °		0°	8°							
A	2.362	2.642		0.093	0.104							
A1	0.101	0.300		0.004	0.012							
В	0.355	0.483		0.014	0.019							
С	0.241	0.318		0.009	0.013							
D	11.353	11.735		0.447	0.462							
E	7.416	7.595		0.292	0.299							
е	1.270	1.270	Reference	0.050	0.050	Reference						
Н	10.007	10.643		0.394	0.419							
h	0.381	0.762		0.015	0.030							
L	0.406	1.143		0.016	0.045							
N	18	18		18	18							
CP	_	0.102		_	0.004							

24.9 28-Lead Ceramic Side Brazed Dual In-Line with Window (300 mil) (JW)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Package Group: Ceramic Side Brazed Dual In-Line (CER)										
0h.al		Millimeters			Inches						
Symbol	Min	Max	Notes	Min	Max	Notes					
α	0°	10°		0°	10°						
А	3.937	5.030		0.155	0.198						
A1	1.016	1.524		0.040	0.060						
A2	2.921	3.506		0.115	0.138						
A3	1.930	2.388		0.076	0.094						
В	0.406	0.508		0.016	0.020						
B1	1.219	1.321	Typical	0.048	0.052						
С	0.228	0.305	Typical	0.009	0.012						
D	35.204	35.916		1.386	1.414						
D1	32.893	33.147	Reference	1.295	1.305						
E	7.620	8.128		0.300	0.320						
E1	7.366	7.620		0.290	0.300						
e1	2.413	2.667	Typical	0.095	0.105						
eA	7.366	7.874	Reference	0.290	0.310						
eB	7.594	8.179		0.299	0.322						
L	3.302	4.064		0.130	0.160						
Ν	28	28		28	28						
S	1.143	1.397		0.045	0.055						
S1	0.533	0.737		0.021	0.029						

24.11 44-Lead Plastic Leaded Chip Carrier (Square) (PLCC)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Package Group: Plastic Leaded Chip Carrier (PLCC)										
		Millimeters		Inches							
Symbol	Min	Мах	Notes	Min	Max	Notes					
А	4.191	4.572		0.165	0.180						
A1	2.413	2.921		0.095	0.115						
D	17.399	17.653		0.685	0.695						
D1	16.510	16.663		0.650	0.656						
D2	15.494	16.002		0.610	0.630						
D3	12.700	12.700	Reference	0.500	0.500	Reference					
E	17.399	17.653		0.685	0.695						
E1	16.510	16.663		0.650	0.656						
E2	15.494	16.002		0.610	0.630						
E3	12.700	12.700	Reference	0.500	0.500	Reference					
Ν	44	44		44	44						
CP	_	0.102		_	0.004						
LT	0.203	0.381		0.008	0.015						

24.13 44-Lead Plastic Surface Mount (TQFP 10x10 mm Body 1.0/0.10 mm Lead Form) (TQ)



Package Group: Plastic TQFP											
		Millimeters		Inches							
Symbol	Min	Max	Notes	Min	Мах	Notes					
Α	1.00	1.20		0.039	0.047						
A1	0.05	0.15		0.002	0.006						
A2	0.95	1.05		0.037	0.041						
D	11.75	12.25		0.463	0.482						
D1	9.90	10.10		0.390	0.398						
E	11.75	12.25		0.463	0.482						
E1	9.90	10.10		0.390	0.398						
L	0.45	0.75		0.018	0.030						
е	0.80	BSC		0.031	BSC						
b	0.30	0.45		0.012	0.018						
b1	0.30	0.40		0.012	0.016						
С	0.09	0.20		0.004	0.008						
c1	0.09	0.16		0.004	0.006						
Ν	44	44		44	44						
Θ	0°	7 °		0°	7 °						

Note 1: Dimensions D1 and E1 do not include mold protrusion. Allowable mold protrusion is 0.25m/m (0.010") per side. D1 and E1 dimensions including mold mismatch.

2: Dimension "b" does not include Dambar protrusion, allowable Dambar protrusion shall be 0.08m/m (0.003")max.

3: This outline conforms to JEDEC MS-026.