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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

### Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	I <sup>2</sup> C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	33
Program Memory Size	7KB (4K x 14)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	192 x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 6V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	44-PLCC (16.59x16.59)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16c65a-20i-l

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Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other resets <sup>(3)</sup>
Bank 2											
100h <sup>(1)</sup>	INDF	Addressing	Addressing this location uses contents of FSR to address data memory (not a physical register) 0000 0000								0000 0000
101h	TMR0	Timer0 mod	lule's registe	r						xxxx xxxx	uuuu uuuu
102h <sup>(1)</sup>	PCL	Program Co	ounter's (PC)	Least Signi	ficant Byte					0000 0000	0000 0000
103h <sup>(1)</sup>	STATUS	IRP	RP1	RP0	TO	PD	Z	DC	С	0001 1xxx	000q quuu
104h <sup>(1)</sup>	FSR	Indirect data	a memory ac	Idress pointe	er					xxxx xxxx	uuuu uuuu
105h	—	Unimpleme	nted							—	—
106h	PORTB	PORTB Dat	a Latch whe	n written: PC	ORTB pins wi	nen read				xxxx xxxx	uuuu uuuu
107h	—	Unimpleme	nted							—	—
108h	—	Unimpleme	nted							_	_
109h	—	Unimpleme	nted							—	—
10Ah <sup>(1,2)</sup>	PCLATH	—			Write Buffer	for the uppe	r 5 bits of the	e Program C	ounter	0 0000	0 0000
10Bh <sup>(1)</sup>	INTCON	GIE	PEIE	TOIE	INTE	RBIE	TOIF	INTF	RBIF	0000 000x	0000 000u
10Ch- 10Fh	_	Unimplemented								—	—
Bank 3	Bank 3										
180h <sup>(1)</sup>	INDF	Addressing	this location	uses conter	nts of FSR to	address data	a memory (n	ot a physical	register)	0000 0000	0000 0000
181h	OPTION	RBPU	INTEDG	TOCS	TOSE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
182h <sup>(1)</sup>	PCL	Program Co	ounter's (PC)	Least Sigr	nificant Byte					0000 0000	0000 0000
183h <sup>(1)</sup>	STATUS	IRP	RP1	RP0	TO	PD	z	DC	С	0001 1xxx	000q quuu
184h <sup>(1)</sup>	FSR	Indirect data	a memory ac	Idress pointe	ər					xxxx xxxx	uuuu uuuu
185h	_	Unimpleme	nted							_	_
186h	TRISB	PORTB Dat	a Direction I	Register						1111 1111	1111 1111
187h	_	Unimpleme	nted							—	—
188h	_	Unimpleme	Unimplemented							—	_
189h	-	Unimpleme	nted							—	-
18Ah <sup>(1,2)</sup>	PCLATH	—			Write Buffer	for the uppe	r 5 bits of the	e Program C	ounter	0 0000	0 0000
18Bh <sup>(1)</sup>	INTCON	GIE	GIE         PEIE         TOIE         INTE         RBIE         TOIF         INTF         RBIF         0000 0000x         00								
18Ch- 19Fh	-	Unimpleme	nted							-	-

### TABLE 4-6: SPECIAL FUNCTION REGISTERS FOR THE PIC16C66/67 (Cont.'d)

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented location read as '0'. Shaded locations are unimplemented, read as '0'.

Note 1: These registers can be addressed from any bank.

2: The upper byte of the Program Counter (PC) is not directly accessible. PCLATH is a holding register for the PC whose contents are transferred to the upper byte of the program counter. (PC<12:8>)

3: Other (non power-up) resets include external reset through MCLR and the Watchdog Timer reset.

4: PIE1<6> and PIR1<6> are reserved on the PIC16C66/67, always maintain these bits clear.

5: PORTD, PORTE, TRISD, and TRISE are not implemented on the PIC16C66, read as '0'.

6: PSPIF (PIR1<7>) and PSPIE (PIE1<7>) are reserved on the PIC16C66, maintain these bits clear.

#### 7.0 TIMER0 MODULE

#### Applicable Devices

61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

The Timer0 module has the following features:

- 8-bit timer/counter register, TMR0
  - Read and write capability
  - Interrupt on overflow from FFh to 00h
- 8-bit software programmable prescaler
- Internal or external clock select
- Edge select for external clock

Figure 7-1 is a simplified block diagram of the Timer0 module.

Timer mode is selected by clearing bit T0CS (OPTION<5>). In timer mode, the Timer0 module will increment every instruction cycle (without prescaler). If TMR0 register is written, the increment is inhibited for the following two instruction cycles (Figure 7-2 and Figure 7-3). The user can work around this by writing an adjusted value to the TMR0 register.

Counter mode is selected by setting bit TOCS. In this mode, Timer0 will increment either on every rising or falling edge of pin RA4/T0CKI. The incrementing edge is determined by the source edge select bit T0SE (OPTION<4>). Clearing bit TOSE selects the rising edge. Restrictions on the external clock input are discussed in detail in Section 7.2.

The prescaler is mutually exclusively shared between the Timer0 module and the Watchdog Timer. The prescaler assignment is controlled in software by control bit PSA (OPTION<3>). Clearing bit PSA will assign the prescaler to the Timer0 module. The prescaler is not readable or writable. When the prescaler is assigned to the Timer0 module, prescale values of 1:2, 1:4, ..., 1:256 are selectable. Section 7.3 details the operation of the prescaler.

#### 7.1 TMR0 Interrupt

#### Applicable Devices

61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

The TMR0 interrupt is generated when the register (TMR0) overflows from FFh to 00h. This overflow sets interrupt flag bit T0IF (INTCON<2>). The interrupt can be masked by clearing enable bit T0IE (INTCON<5>). Flag bit T0IF must be cleared in software by the TImer0 interrupt service routine before re-enabling this interrupt. The TMR0 interrupt cannot wake the processor from SLEEP since the timer is shut off during SLEEP. Figure 7-4 displays the Timer0 interrupt timing.



#### FIGURE 7-2: TIMER0 TIMING: INTERNAL CLOCK/NO PRESCALER



### TABLE 9-1: REGISTERS ASSOCIATED WITH TIMER2 AS A TIMER/COUNTER

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Valu PC BC	e on: )R, )R	Valu all o res	e on ther ets
0Bh,8Bh 10Bh,18Bh	INTCON	GIE	PEIE	TOIE	INTE	RBIE	TOIF	INTF	RBIF	0000	000x	0000	000u
0Ch	PIR1	PSPIF <sup>(2)</sup>	(3)	RCIF <sup>(1)</sup>	TXIF <sup>(1)</sup>	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000	0000	0000	0000
8Ch	PIE1	PSPIE <sup>(2)</sup>	(3)	RCIE <sup>(1)</sup>	TXIE <sup>(1)</sup>	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000	0000	0000	0000
11h	TMR2	Timer2 m	Timer2 module's register								0000	0000	0000
12h	T2CON		TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000	0000	-000	0000
92h	PR2	R2 Timer2 Period register								1111	1111	1111	1111

Legend: x = unknown, u = unchanged, - = unimplemented locations read as '0'. Shaded cells are not used by Timer2.

Note 1: The USART is implemented on the PIC16C63/R63/65/65A/R65/66/67 only.

2: Bits PSPIE and PSPIF are reserved on the PIC16C62/62A/R62/63/R63/66, always maintain these bits clear.

3: PIR1<6> and PIE1<6> are reserved, always maintain these bits clear.

SUBWF	Subtract	W from f							
Syntax:	[ label ]	SUBWF	f,d						
Operands:	$\begin{array}{l} 0 \leq f \leq 12 \\ d \in [0,1] \end{array}$	7							
Operation:	(f) - (W) –	→ (destina	tion)						
Status Affected:	C, DC, Z								
Encoding:	00	0010	dfff	ffff					
Description:	Subtract (2's complement method) W reg- ister from register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'.								
Words:	1								
Cycles:	1								
Q Cycle Activity:	Q1	Q2	Q3	Q4					
	Decode	Read register 'f'	Process data	Write to destination					
Example 1:	SUBWF	REG1,1							
	Before Ins	struction							
	REG1	=	3						
	W	=	2						
	z	=	?						
	After Instr	uction							
	REG1	=	1						
	W C	=	2 1: result is	positive					
	Z	=	0	P					
Example 2:	Before Ins	struction							
	REG1	=	2						
	W C	=	2 ?						
	Z	=	?						
	After Instr	uction							
	REG1	=	0						
	C V	=	2 1; result is	zero					
	Z	=	1						
Example 3:	Before Ins	struction							
	REG1	=	1						
	C	=	2 ?						
	Z	=	?						
	After Instr	uction							
	REG1	=	0xFF						
	C	=	∠ 0; result is	negative					
	Z	=	0						

SWAPF	Swap Ni	bbles in t	f						
Syntax:	[label]	SWAPF f	,d						
Operands:	$\begin{array}{l} 0 \leq f \leq 127 \\ d  \in  [0,1] \end{array}$								
Operation:	$(f<3:0>) \rightarrow (destination<7:4>),$ $(f<7:4>) \rightarrow (destination<3:0>)$								
Status Affected:	None								
Encoding:	00	1110	dfff	ffff					
Description:	The upper and lower nibbles of register 'f' are exchanged. If 'd' is 0 the result is placed in W register. If 'd' is 1 the result is placed in register 'f'.								
Words:	1								
Cycles:	1								
Q Cycle Activity:	Q1	Q2	Q3	Q4					
	Decode	Read register 'f'	Proces data	s Write to destination					
Example	SWAPF	REG,	0						
	Before In	struction							
		REG1	= C	xA5					
	After Inst	ruction							
		REG1 W	= C = C	)xA5 )x5A					

TRIS	Load TRIS Register								
Syntax:	[label]	TRIS	f						
Operands:	$5 \leq f \leq 7$								
Operation:	(W) $\rightarrow$ TRIS register f;								
Status Affected:	None								
Encoding:	00	0000	0110	Offf					
Description:	The instruction is supported for code compatibility with the PIC16C5X prod- ucts. Since TRIS registers are read- able and writable, the user can directly address them.								
Words:	1								
Cycles:	1								
Example									
	To maintain upward compatibility with future PIC16CXX products, do not use this instruction.								

## 18.0 ELECTRICAL CHARACTERISTICS FOR PIC16C62A/R62/64A/R64

#### Absolute Maximum Ratings †

Ambient temperature under bias	55°C to +125°C
Storage temperature	65°C to +150°C
Voltage on any pin with respect to Vss (except VDD, MCLR, and RA4)	0.3V to (VDD + 0.3V)
Voltage on VDD with respect to Vss	0.3V to +7.5V
Voltage on MCLR with respect to Vss (Note 2)	0V to +14V
Voltage on RA4 with respect to Vss	0V to +14V
Total power dissipation (Note 1)	1.0W
Maximum current out of Vss pin	
Maximum current into VDD pin	250 mA
Input clamp current, Iik (VI < 0 or VI > VDD)	±20 mA
Output clamp current, Ioκ (Vo < 0 or Vo > VDD)	±20 mA
Maximum output current sunk by any I/O pin	25 mA
Maximum output current sourced by any I/O pin	25 mA
Maximum current sunk by PORTA, PORTB, and PORTE (combined)	200 mA
Maximum current sourced by PORTA, PORTB, and PORTE (combined)	
Maximum current sunk by PORTC and PORTD (combined)	200 mA
Maximum current sourced by PORTC and PORTD (combined)	200 mA

**Note 1:** Power dissipation is calculated as follows: Pdis = VDD x {IDD -  $\sum$  IOH} +  $\sum$  {(VDD-VOH) x IOH} +  $\sum$ (VOI x IOL)

Note 2: Voltage spikes below Vss at the MCLR pin, inducing currents greater than 80 mA, may cause latch-up. Thus, a series resistor of 50-100Ω should be used when applying a "low" level to the MCLR pin rather than pulling this pin directly to Vss.

† NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

#### TABLE 18-1: CROSS REFERENCE OF DEVICE SPECS FOR OSCILLATOR CONFIGURATIONS AND FREQUENCIES OF OPERATION (COMMERCIAL DEVICES)

osc	PIC16C62A-04 PIC16CR62-04 PIC16C64A-04 PIC16CR64-04	PIC16C62A-10 PIC16CR62-10 PIC16C64A-10 PIC16CR64-10	PIC16C62A-20 PIC16CR62-20 PIC16C64A-20 PIC16CR64-20	PIC16LC62A-04 PIC16LCR62-04 PIC16LC64A-04 PIC16LCR64-04	JW Devices
RC	VDD: 4.0V to 6.0V IDD: 5 mA max. at 5.5V IPD: 16 μA max. at 4V Freq:4 MHz max.	VDD: 4.5V to 5.5V IDD: 2.0 mA typ. at 5.5V IPD: 1.5 μA typ. at 4V Freq: 4 MHz max.	VDD: 4.5V to 5.5V IDD: 2.0 mA typ. at 5.5V IPD: 1.5 μA typ. at 4V Freq: 4 MHz max.	VDD: 2.5V to 6.0V IDD: 3.8 mA max. at 3.0V IPD: 5 µA max. at 3V Freq: 4 MHz max.	VDD: 4.0V to 6.0V IDD: 5 mA max. at 5.5V IPD: 16 μA max. at 4V Freq:4 MHz max.
ХТ	VDD: 4.0V to 6.0V IDD: 5 mA max. at 5.5V IPD: 16 μA max. at 4V Freq: 4 MHz max.	VDD: 4.5V to 5.5V IDD: 2.0 mA typ. at 5.5V IPD: 1.5 $\mu A$ typ. at 4V Freq: 4 MHz max.	VDD: 4.5V to 5.5V IDD: 2.0 mA typ. at 5.5V IPD: 1.5 μA typ. at 4V Freq: 4 MHz max.	VDD: 2.5V to 6.0V IDD: 3.8 mA max. at 3.0V IPD: 5 µA max. at 3.0V Freq: 4 MHz max.	VDD: 4.0V to 6.0V IDD: 5 mA max. at 5.5V IPD: 16 μA max. at 4V Freq: 4 MHz max.
HS	VDD: 4.5V to 5.5V IDD: 13.5 mA typ. at 5.5V IPD: 1.5 μA typ. at 4.5V Freq: 4 MHz max.	VDD: 4.5V to 5.5V IDD: 10 mA max. at 5.5V IPD: 1.5 μA typ. at 4.5V Freq: 10 MHz max.	VDD: 4.5V to 5.5V IDD: 20 mA max. at 5.5V IPD: 1.5 μA typ. at 4.5V Freq: 20 MHz max.	Not recommended for use in HS mode	VDD: 4.5V to 5.5V IDD: 20 mA max. at 5.5V IPD: 1.5 μA typ. at 4.5V Freq: 20 MHz max.
LP	VDD: 4.0V to 6.0V IDD: 52.5 μA typ. at 32 kHz, 4.0V IPD: 0.9 μA typ. at 4.0V Freq: 200 kHz max.	Not recommended for use in LP mode	Not recommended for use in LP mode	VDD: 2.5V to 6.0V IDD: 48 μA max. at 32 kHz, 3.0V IPD: 5 μA max. at 3.0V Freq: 200 kHz max.	VDD: 2.5V to 6.0V IDD: 48 μA max. at 32 kHz, 3.0V IPD: 5 μA max. at 3.0V Freq: 200 kHz max.

The shaded sections indicate oscillator selections which are tested for functionality, but not for MIN/MAX specifications. It is recommended that the user select the device type that ensures the specifications required.

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Applicable Devices 61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

### FIGURE 18-3: CLKOUT AND I/O TIMING



#### **CLKOUT AND I/O TIMING REQUIREMENTS TABLE 18-3:**

Parameters	Sym	Characteristic		Min	Typ†	Max	Units	Conditions
10*	TosH2ckL	OSC1↑ to CLKOUT↓		—	75	200	ns	Note 1
11*	TosH2ckH	OSC1↑ to CLKOUT↑	—	75	200	ns	Note 1	
12*	TckR	CLKOUT rise time		—	35	100	ns	Note 1
13*	TckF	CLKOUT fall time		—	35	100	ns	Note 1
14*	TckL2ioV	CLKOUT $\downarrow$ to Port out valid		—		0.5TCY + 20	ns	Note 1
15*	TioV2ckH	Port in valid before CLKOUT $\uparrow$		Tosc + 200		—	ns	Note 1
16*	TckH2iol	Port in hold after CLKOUT 1		0		—	ns	Note 1
17*	TosH2ioV	OSC1 <sup>↑</sup> (Q1 cycle) to Port out va	lid	—	50	150	ns	
18*	TosH2iol	OSC1 <sup>↑</sup> (Q2 cycle) to Port input invalid (I/O in hold time)	PIC16 <b>C</b> 62A/ R62/64A/R64	100	_	—	ns	
			PIC16 <b>LC</b> 62A/ R62/64A/R64	200		_	ns	
19*	TioV2osH	Port input valid to OSC1 <sup>↑</sup> (I/O in	setup time)	0		—	ns	
20*	TioR	Port output rise time	PIC16 <b>C</b> 62A/ R62/64A/R64	-	10	40	ns	
			PIC16 <b>LC</b> 62A/ R62/64A/R64	-		80	ns	
21*	TioF	Port output fall time	PIC16 <b>C</b> 62A/ R62/64A/R64	-	10	40	ns	
			PIC16 <b>LC</b> 62A/ R62/64A/R64	-	—	80	ns	
22††*	Tinp	RB0/INT pin high or low time	Тсү	_	—	ns		
23††*	Trbp	RB7:RB4 change int high or low	time	Тсү	_	—	ns	

These parameters are characterized but not tested.

t Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**††** These parameters are asynchronous events not related to any internal clock edge.

Note 1: Measurements are taken in RC Mode where CLKOUT output is 4 x TOSC.



## FIGURE 19-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING

## TABLE 19-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Тур†	Мах	Units	Conditions
30*	TmcL	MCLR Pulse Width (low)	100	—	I	ns	VDD = 5V, -40°C to +85°C
31*	Twdt	Watchdog Timer Time-out Period (No Prescaler)	7	18	33	ms	$VDD = 5V$ , $-40^{\circ}C$ to $+85^{\circ}C$
32	Tost	Oscillation Start-up Timer Period		1024Tosc		-	TOSC = OSC1 period
33*	Tpwrt	Power-up Timer Period or WDT reset	28	72	132	ms	VDD = 5V, -40°C to +85°C
34	Tioz	I/O Hi-impedance from MCLR Low	-	—	100	ns	

These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Applicable Devices 61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

## FIGURE 19-9: I<sup>2</sup>C BUS START/STOP BITS TIMING



## TABLE 19-9: I<sup>2</sup>C BUS START/STOP BITS REQUIREMENTS

Parameter No.	Sym	Characteristic		Min	Тур	Мах	Units	Conditions	
90	TSU:STA	START condition	100 kHz mode	4700	—	-	ne	Only relevant for repeated START	
		Setup time	400 kHz mode	600	—	—	113	condition	
91	THD:STA	START condition	100 kHz mode	4000	—	—	ne	After this period the first clock	
		Hold time	400 kHz mode	600	_	_	115	pulse is generated	
92	TSU:STO	STOP condition	100 kHz mode	4700	—	—	ne		
		Setup time	400 kHz mode	600	—	—	115		
93	THD:STO	STOP condition	100 kHz mode	4000	—	—	ne		
		Hold time	400 kHz mode	600	—	—	115		

#### 20.2 DC Characteristics: PIC16LC63/65A-04 (Commercial, Industrial)

DC CHA	RACTERISTICS	$\begin{array}{llllllllllllllllllllllllllllllllllll$						
Param No.	Characteristic	Sym	Min	Тур†	Max	Units	Conditions	
D001	Supply Voltage	Vdd	2.5	-	6.0	V	LP, XT, RC osc configuration (DC - 4 MHz)	
D002*	RAM Data Retention Voltage (Note 1)	Vdr	-	1.5	-	V		
D003	VDD start voltage to ensure internal Power-on Reset signal	VPOR	-	Vss	-	V	See section on Power-on Reset for details	
D004*	VDD rise rate to ensure internal Power-on Reset signal	SVDD	0.05	-	-	V/ms	See section on Power-on Reset for details	
D005	Brown-out Reset Voltage	BVDD	3.7	4.0	4.3	V	BODEN configuration bit is enabled	
D010	Supply Current (Note 2, 5)	IDD	-	2.0	3.8	mA	XT, RC osc configuration Fosc = 4 MHz, VDD = 3.0V (Note 4)	
D010A			-	22.5	48	μA	LP osc configuration Fosc = 32 kHz, VDD = 3.0V, WDT disabled	
D015*	Brown-out Reset Current (Note 6)	$\Delta$ IBOR	-	350	425	μA	BOR enabled, VDD = 5.0V	
D020	Power-down Current	IPD	-	7.5	30	μA	VDD = 3.0V, WDT enabled, $-40^{\circ}C$ to $+85^{\circ}C$	
D021	(Note 3, 5)		-	0.9	5	μA	VDD = $3.0V$ , WDT disabled, $0^{\circ}C$ to $+70^{\circ}C$	
D021A			-	0.9	5	μA	VDD = $3.0V$ , WDT disabled, $-40^{\circ}C$ to $+85^{\circ}C$	
D023*	Brown-out Reset Current (Note 6)	$\Delta$ IBOR	-	350	425	μA	BOR enabled, VDD = 5.0V	

These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.

The test conditions for all IDD measurements in active operation mode are:

OSC1 = external square wave, from rail to rail; all I/O pins tristated, pulled to VDD,

- $\overline{MCLR} = VDD$ ; WDT enabled/disabled as specified.
- 3: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.
- 4: For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula Ir = VDD/2Rext (mA) with Rext in kOhm.
- 5: Timer1 oscillator (when enabled) adds approximately 20 μA to the specification. This value is from characterization and is for design guidance only. This is not tested.
- 6: The ∆ current is the additional current consumed when this peripheral is enabled. This current should be added to the base IDD or IPD measurement.

### Applicable Devices 61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

### FIGURE 20-11: I<sup>2</sup>C BUS DATA TIMING



### TABLE 20-10: I<sup>2</sup>C BUS DATA REQUIREMENTS

Parameter	Sym	Characteristic		Min	Max	Units	Conditions
No.							
100*	THIGH	Clock high time	100 kHz mode	4.0	—	μs	Device must operate at a mini- mum of 1.5 MHz
			400 kHz mode	0.6	_	μs	Device must operate at a mini- mum of 10 MHz
			SSP Module	1.5TCY	_		
101*	TLOW	Clock low time	100 kHz mode	4.7	—	μs	Device must operate at a mini- mum of 1.5 MHz
			400 kHz mode	1.3	—	μs	Device must operate at a mini- mum of 10 MHz
			SSP Module	1.5TCY	—		
102*	TR	SDA and SCL rise	100 kHz mode	—	1000	ns	
		time	400 kHz mode	20 + 0.1Cb	300	ns	Cb is specified to be from 10-400 pF
103*	TF	SDA and SCL fall time	100 kHz mode	—	300	ns	
			400 kHz mode	20 + 0.1Cb	300	ns	Cb is specified to be from 10-400 pF
90*	TSU:STA	START condition	100 kHz mode	4.7	—	μs	Only relevant for repeated
		setup time	400 kHz mode	0.6	_	μs	START condition
91*	THD:STA	START condition hold	100 kHz mode	4.0	—	μs	After this period the first clock
		time	400 kHz mode	0.6	—	μs	pulse is generated
106*	THD:DAT	Data input hold time	100 kHz mode	0	—	ns	_
			400 kHz mode	0	0.9	μs	
107*	TSU:DAT	Data input setup time	100 kHz mode	250	—	ns	Note 2
			400 kHz mode	100	—	ns	
92*	TSU:STO	STOP condition setup	100 kHz mode	4.7	—	μS	_
		time	400 kHz mode	0.6	_	μs	
109*	TAA	Output valid from	100 kHz mode	—	3500	ns	Note 1
		clock	400 kHz mode	—	—	ns	
110*	TBUF	Bus free time	100 kHz mode	4.7	_	μS	Time the bus must be free
			400 kHz mode	1.3	—	μs	betore a new transmission can start
	Cb	Bus capacitive loading		—	400	pF	

These parameters are characterized but not tested.

Note 1: As a transmitter, the device must provide this internal minimum delay time to bridge the undefined region (min. 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

2: A fast-mode (400 kHz) I<sup>2</sup>C-bus device can be used in a standard-mode (100 kHz) I<sup>2</sup>C-bus system, but the requirement Tsu:DAT ≥ 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line TR max.+tsu;DAT = 1000 + 250 = 1250 ns (according to the standard-mode I<sup>2</sup>C bus specification) before the SCL line is released.

#### FIGURE 20-12: USART SYNCHRONOUS TRANSMISSION (MASTER/SLAVE) TIMING



#### TABLE 20-11: USART SYNCHRONOUS TRANSMISSION REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Тур†	Max	Units	Conditions	
120*	TckH2dtV	SYNC XMIT (MASTER & SLAVE)	PIC16 <b>C</b> 63/65A		—	80	ns	
Clock	Clock high to data out valid	PIC16 <b>LC</b> 63/65A	-	—	100	ns		
121*	Tckrf Clock out rise time and fall time		PIC16 <b>C</b> 63/65A		_	45	ns	
		(Master Mode)	PIC16 <b>LC</b> 63/65A	-	—	50	ns	
122*	122* Tdtrf Data out rise time and fall time		PIC16 <b>C</b> 63/65A		_	45	ns	
			PIC16 <b>LC</b> 63/65A		—	50	ns	
* Thee	a naramatara	are characterized but not tested						

These parameters are characterized but not tested.

**†**: Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

#### FIGURE 20-13: USART SYNCHRONOUS RECEIVE (MASTER/SLAVE) TIMING



#### TABLE 20-12: USART SYNCHRONOUS RECEIVE REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Тур†	Max	Units	Conditions
125*	TdtV2ckL	$\frac{\text{SYNC RCV (MASTER \& SLAVE)}}{\text{Data setup before CK} \downarrow (\text{DT setup time})}$	15	_	_	ns	
126*	TckL2dtl	Data hold after CK $\downarrow$ (DT hold time)	15	—	_	ns	

These parameters are characterized but not tested.

**†**: Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

#### 21.2 DC Characteristics: PIC16LCR63/R65-04 (Commercial, Industrial)

DC CHA	RACTERISTICS	$\begin{array}{llllllllllllllllllllllllllllllllllll$							
Param No.	Characteristic	Sym	Min	Тур†	Max	Units	Conditions		
D001	Supply Voltage	Vdd	3.0	-	5.5	V	LP, XT, RC osc configuration (DC - 4 MHz)		
D002*	RAM Data Retention Voltage (Note 1)	Vdr	-	1.5	-	V			
D003	VDD start voltage to ensure internal Power-on Reset signal	VPOR	-	Vss	-	V	See section on Power-on Reset for details		
D004*	VDD rise rate to ensure internal Power-on Reset signal	SVDD	0.05	-	-	V/ms	See section on Power-on Reset for details		
D005	Brown-out Reset Voltage	BVDD	3.7	4.0	4.3	V	BODEN configuration bit is enabled		
D010	Supply Current (Note 2, 5)	IDD	-	2.0	3.8	mA	XT, RC osc configuration Fosc = 4 MHz, VDD = 3.0V (Note 4)		
D010A			-	22.5	48	μA	LP osc configuration Fosc = 32 kHz, VDD = 3.0V, WDT disabled		
D015*	Brown-out Reset Current (Note 6)	$\Delta$ IBOR	-	350	425	μA	BOR enabled, VDD = 5.0V		
D020	Power-down Current	IPD	-	7.5	30	μA	VDD = 3.0V, WDT enabled, $-40^{\circ}C$ to $+85^{\circ}C$		
D021	(Note 3, 5)		-	0.9	5	μA	VDD = $3.0V$ , WDT disabled, $0^{\circ}C$ to $+70^{\circ}C$		
D021A			-	0.9	5	μA	VDD = $3.0V$ , WDT disabled, $-40^{\circ}C$ to $+85^{\circ}C$		
D023*	Brown-out Reset Current (Note 6)	$\Delta$ IBOR	-	350	425	μA	BOR enabled, VDD = 5.0V		

These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.

The test conditions for all IDD measurements in active operation mode are:

OSC1 = external square wave, from rail to rail; all I/O pins tristated, pulled to VDD,

- $\overline{MCLR} = VDD$ ; WDT enabled/disabled as specified.
- 3: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.
- 4: For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula Ir = VDD/2Rext (mA) with Rext in kOhm.
- 5: Timer1 oscillator (when enabled) adds approximately 20 μA to the specification. This value is from characterization and is for design guidance only. This is not tested.
- 6: The ∆ current is the additional current consumed when this peripheral is enabled. This current should be added to the base IDD or IPD measurement.

## Applicable Devices 61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

### FIGURE 21-3: CLKOUT AND I/O TIMING



TABLE 21-3: CLKOUT AND I/O TIMING REQUIREMENT
---

Param	Sym	Characteristic	<	Min	Typt	Max	Units	Conditions
No.				$\langle - \rangle \langle$	$\sum$			
10*	TosH2ckL	OSC1↑ to CLKOUT↓		$\langle \mathcal{F} \rangle$	75	200	ns	Note 1
11*	TosH2ckH	OSC1↑ to CLKOUT↑			75	200	ns	Note 1
12*	TckR	CLKOUT rise time	$\sim  V $	$\searrow$	35	100	ns	Note 1
13*	TckF	CLKOUT fall time	$\sum$	> -	35	100	ns	Note 1
14*	TckL2ioV	CLKOUT ↓ to Port out valid	$   _{A} _{\wedge}$	[ _		0.5TCY + 20	ns	Note 1
15*	TioV2ckH	Port in valid before CLKOUT	$///\sim$	Tosc + 200	-	_	ns	Note 1
16*	TckH2iol	Port in hold after CLKOUT ↑	$\overline{\langle \langle \rangle}$	0	I	_	ns	Note 1
17*	TosH2ioV	OSC1 <sup>↑</sup> (Q1 cycle) to Port out val	id 🔪	—	50	150	ns	
18*	TosH2ioI	OSC11 (Q2 cycle) to Port input	P1C16CR63/R65	100		_	ns	
		invalid (I/O in hold time)	PIC16LCR63/R65	200		_	ns	
19*	TioV2osH	Port input valid to OSC11 (I/Q in	setup time)	0	_	—	ns	
20*	TioR	Port output rise time	PIC16CR63/R65	—	10	40	ns	
		$\frown$	PIC16LCR63/R65	_	-	80	ns	
21*	TioF	Port output fall time	PIC16CR63/R65	_	10	40	ns	
	$\langle$	$\langle \rangle \rangle$	PIC16LCR63/R65	—		80	ns	
22††*	Tinp	INT pin high or low time		Тсү	-	_	ns	
23††*	Trbp	RB7:RB2 change INT high or low	time	Тсү	_	—	ns	

These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

t† These parameters are asynchronous events not related to any internal clock edge.

Note 1: Measurements are taken in RC Mode where CLKOUT output is 4 x Tosc.

Applicable Devices 61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

## FIGURE 21-10: I<sup>2</sup>C BUS START/STOP BITS TIMING



#### I<sup>2</sup>C BUS START/STOP BITS REQUIREMENTS **TABLE 21-9:**

Parameter No.	Sym	Characteristic		Min	Тур	Мах	Units	Conditions
90*	TSU:STA	START condition	100 kHz mode	4700	—	-	<b>n</b> 0	Only relevant for repeated START
		Setup time	400 kHz mode	600	—	—	115	condition
91*	THD:STA	START condition	100 kHz mode	4000	—	—	ns	After this period the first clock pulse is generated
		Hold time	400 kHz mode	600	—	_	115	
92*	TSU:STO	STOP condition	100 kHz mode	4700	—	—	ne	
		Setup time	400 kHz mode	600	—	—	113	
93	THD:STO	STOP condition	100 kHz mode	4000	—	—	ne	
		Hold time	400 kHz mode	600	—	—	115	
* These na	ramotore are	characterized but not	t tostad					

These parameters are characterized but not tested.

## Applicable Devices 61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

### 22.4 Timing Parameter Symbology

The timing parameter symbols have been created following one of the following formats:

1. TppS2p	S	3. TCC:ST	(I <sup>2</sup> C specifications only)
2. TppS		4. Ts	(I <sup>2</sup> C specifications only)
Т			
F	Frequency	Т	Time
Lowerca	se letters (pp) and their meanings:	-	
рр			
сс	CCP1	OSC	OSC1
ck	CLKOUT	rd	RD
CS	CS	rw	RD or WR
di	SDI	SC	SCK
do	SDO	SS	SS
dt	Data in	tO	TOCKI
io	I/O port	t1	T1CKI
mc	MCLR	wr	WR
Upperca	se letters and their meanings:		
S			
F	Fall	Р	Period
Н	High	R	Rise
I	Invalid (Hi-impedance)	V	Valid
L	Low	Z	Hi-impedance
I <sup>2</sup> C only			
AA	output access	High	High
BUF	Bus free	Low	Low
Tcc:st (	<sup>2</sup> C specifications only)		
CC			
HD	Hold	SU	Setup
ST			
DAT	DATA input hold	STO	STOP condition
STA	START condition		
FIGURE 2	2-1: LOAD CONDITIONS FOR DEVICE	TIMING SP	ECIFICATIONS
	Load condition 1		Load condition 2
	VDD/2		
	Ĭ	>	
	$\leq$ RL	Pi	
	<		
	•		Vss
	'''' ↓ RL	<b>= 464</b> Ω	
	VSS CL	= 50 pF fc	or all pins except OSC2/CLKOUT
Note 1:	PORTD and PORTE are not imple-	b	ut including D and E outputs as ports
	· · · · · · · · · · · · · · · · · · ·	45.55	
	mented on the PIC16C66.	15 pr to	or OSC2 output
	mented on the PIC16C66.	15 pr to	

### 22.5 <u>Timing Diagrams and Specifications</u>

#### FIGURE 22-2: EXTERNAL CLOCK TIMING



#### TABLE 22-2: EXTERNAL CLOCK TIMING REQUIREMENTS

Param No.	Sym	Characteristic	Min	Тур†	Мах	Units	Conditions
	Fosc	External CLKIN Frequency	DC	_	4	MHz	XT and BC osc mode
		(Note 1)	DC	_	4	MHz	HS osc mode (-04)
			DC	_	10	MHz	HS osc mode (-10)
			DC	_	20	MHz	HS osc mode (-20)
			DC	_	200	kHz	LP osc mode
		Oscillator Frequency	DC	_	4	MHz	BC osc mode
		(Note 1)	0.1	_	4	MHz	XT osc mode
			4	_	20	MHz	HS osc mode
			5	_	200	kHz	LP osc mode
1	Tosc	External CLKIN Period	250	_	_	ns	XT and RC osc mode
		(Note 1)	250	_	_	ns	HS osc mode (-04)
			100	_	_	ns	HS osc mode (-10)
			50	_	_	ns	HS osc mode (-20)
			5	_	_	μS	LP osc mode
		Oscillator Period	250	_	_	ns	RC osc mode
		(Note 1)	250	_	10,000	ns	XT osc mode
			250	_	250	ns	HS osc mode (-04)
			100	_	250	ns	HS osc mode (-10)
			50	_	250	ns	HS osc mode (-20)
			5	_	_	μs	LP osc mode
2	TCY	Instruction Cycle Time (Note 1)	200	Тсү	DC	ns	Tcy = 4/Fosc
3*	TosL,	External Clock in (OSC1) High or	100	_	—	ns	XT oscillator
	TosH	Low Time	2.5	_	_	μs	LP oscillator
			15	—	—	ns	HS oscillator
4*	TosR,	External Clock in (OSC1) Rise or	_	—	25	ns	XT oscillator
	TosF	Fall Time	—	—	50	ns	LP oscillator
			—	—	15	ns	HS oscillator

These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Instruction cycle period (TcY) equals four times the input oscillator time-base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min." values with an external clock applied to the OSC1/CLKIN pin. When an external clock input is used, the "Max." cycle time limit is "DC" (no clock) for all devices.

Applicable Devices 61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

## FIGURE 22-13: I<sup>2</sup>C BUS START/STOP BITS TIMING



## TABLE 22-9: I<sup>2</sup>C BUS START/STOP BITS REQUIREMENTS

Parameter No.	Sym	Characteristic		Min	Тур	Мах	Units	Conditions
90*	TSU:STA	START condition	100 kHz mode	4700	—	—	ne	Only relevant for repeated START
		Setup time	400 kHz mode	600	—	—	113	condition
91*	THD:STA	START condition	100 kHz mode	4000	—	—	ne	After this period the first clock
		Hold time	400 kHz mode	600	_	_	115	pulse is generated
92*	TSU:STO	STOP condition	100 kHz mode	4700	_	_	ne	
		Setup time	400 kHz mode	600	_	_	115	
93	THD:STO	STOP condition	100 kHz mode	4000	—	—	ne	
		Hold time	400 kHz mode	600	—	—	115	

These parameters are characterized but not tested.

### Applicable Devices 61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

### FIGURE 22-14: I<sup>2</sup>C BUS DATA TIMING



### TABLE 22-10: I<sup>2</sup>C BUS DATA REQUIREMENTS

Parameter	Sym	Characteristic		Min	Max	Units	Conditions
No.							
100*	THIGH	Clock high time	100 kHz mode	4.0	—	μs	Device must operate at a mini- mum of 1.5 MHz
			400 kHz mode	0.6	_	μs	Device must operate at a mini- mum of 10 MHz
			SSP Module	1.5TCY	_		
101*	TLOW	Clock low time	100 kHz mode	4.7	—	μs	Device must operate at a mini- mum of 1.5 MHz
			400 kHz mode	1.3	—	μs	Device must operate at a mini- mum of 10 MHz
			SSP Module	1.5TCY	—		
102*	TR	SDA and SCL rise	100 kHz mode	—	1000	ns	
		time	400 kHz mode	20 + 0.1Cb	300	ns	Cb is specified to be from 10-400 pF
103*	TF	SDA and SCL fall time	100 kHz mode	—	300	ns	
			400 kHz mode	20 + 0.1Cb	300	ns	Cb is specified to be from 10-400 pF
90*	TSU:STA	START condition	100 kHz mode	4.7	—	μs	Only relevant for repeated
		setup time	400 kHz mode	0.6	_	μs	START condition
91*	THD:STA	START condition hold	100 kHz mode	4.0	—	μs	After this period the first clock
		time	400 kHz mode	0.6	—	μs	pulse is generated
106*	THD:DAT	Data input hold time	100 kHz mode	0	—	ns	_
			400 kHz mode	0	0.9	μs	
107*	TSU:DAT	Data input setup time	100 kHz mode	250	—	ns	Note 2
			400 kHz mode	100	—	ns	
92*	TSU:STO	STOP condition setup	100 kHz mode	4.7	—	μS	_
		time	400 kHz mode	0.6	_	μs	
109*	TAA	Output valid from	100 kHz mode	—	3500	ns	Note 1
		clock	400 kHz mode	—	—	ns	
110*	TBUF	Bus free time	100 kHz mode	4.7	_	μS	Time the bus must be free
			400 kHz mode	1.3	—	μs	betore a new transmission can start
	Cb	Bus capacitive loading		—	400	pF	

These parameters are characterized but not tested.

Note 1: As a transmitter, the device must provide this internal minimum delay time to bridge the undefined region (min. 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

2: A fast-mode (400 kHz) I<sup>2</sup>C-bus device can be used in a standard-mode (100 kHz) I<sup>2</sup>C-bus system, but the requirement Tsu:DAT ≥ 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line TR max.+tsu;DAT = 1000 + 250 = 1250 ns (according to the standard-mode I<sup>2</sup>C bus specification) before the SCL line is released.



FIGURE 23-23: TYPICAL XTAL STARTUP TIME vs. VDD (HS MODE, 25°C)



FIGURE 23-24: TYPICAL XTAL STARTUP TIME vs. Vdd (XT MODE, 25°C)



#### TABLE 23-2: CAPACITOR SELECTION FOR CRYSTAL OSCILLATORS

Osc Type	Crystal Freq	Cap. Range C1	Cap. Range C2		
LP	32 kHz	33 pF	33 pF		
	200 kHz	15 pF	15 pF		
ХТ	200 kHz	47-68 pF	47-68 pF		
	1 MHz	15 pF	15 pF		
	4 MHz	15 pF	15 pF		
HS	4 MHz	15 pF	15 pF		
	8 MHz	15-33 pF	15-33 pF		
	20 MHz	15-33 pF	15-33 pF		
Crystals Used					
32 kHz	Epson C-00	01R32.768K-A	± 20 PPM		
200 kHz	STD XTL 2	00.000KHz	± 20 PPM		
1 MHz	ECS ECS-1	± 50 PPM			
4 MHz	ECS ECS-4	± 50 PPM			
8 MHz	EPSON CA	± 30 PPM			
20 MHz	EPSON CA	-301 20.000M-C	± 30 PPM		

### F.7 PIC16C7XX Family of Devces

		PIC16C710	PIC16C71	PIC16C711	PIC16C715	PIC16C72	PIC16CR72 <sup>(1)</sup>
Clock	Maximum Frequency of Operation (MHz)	20	20	20	20	20	20
Memory	EPROM Program Memory (x14 words)	512	1K	1K	2К	2К	—
	ROM Program Memory (14K words)	_	_	_	_	_	2К
	Data Memory (bytes)	36	36	68	128	128	128
Peripherals	Timer Module(s)	TMR0	TMR0	TMR0	TMR0	TMR0, TMR1, TMR2	TMR0, TMR1, TMR2
	Capture/Compare/ PWM Module(s)	_	—	_	_	1	1
	Serial Port(s) (SPI/I <sup>2</sup> C, USART)	_	_	_	_	SPI/I <sup>2</sup> C	SPI/I <sup>2</sup> C
	Parallel Slave Port	_	_	_	_	_	—
	A/D Converter (8-bit) Channels	4	4	4	4	5	5
Features	Interrupt Sources	4	4	4	4	8	8
	I/O Pins	13	13	13	13	22	22
	Voltage Range (Volts)	3.0-6.0	3.0-6.0	3.0-6.0	3.0-5.5	2.5-6.0	3.0-5.5
	In-Circuit Serial Programming	Yes	Yes	Yes	Yes	Yes	Yes
	Brown-out Reset	Yes	—	Yes	Yes	Yes	Yes
	Packages	18-pin DIP, SOIC; 20-pin SSOP	18-pin DIP, SOIC	18-pin DIP, SOIC; 20-pin SSOP	18-pin DIP, SOIC; 20-pin SSOP	28-pin SDIP, SOIC, SSOP	28-pin SDIP, SOIC, SSOP

		PIC16C73A	PIC16C74A	PIC16C76	PIC16C77
Clock	Maximum Frequency of Oper- ation (MHz)	20	20	20	20
Memory	EPROM Program Memory (x14 words)	4K	4K	8K	8K
	Data Memory (bytes)	192	192	368	368
Peripherals	Timer Module(s)	TMR0, TMR1, TMR2	TMR0, TMR1, TMR2	TMR0, TMR1, TMR2	TMR0, TMR1, TMR2
	Capture/Compare/PWM Mod- ule(s)	2	2	2	2
	Serial Port(s) (SPI/I <sup>2</sup> C, USART)	SPI/I <sup>2</sup> C, USART	SPI/I <sup>2</sup> C, USART	SPI/I <sup>2</sup> C, USART	SPI/I <sup>2</sup> C, USART
	Parallel Slave Port	_	Yes	—	Yes
	A/D Converter (8-bit) Channels	5	8	5	8
Features	Interrupt Sources	11	12	11	12
	I/O Pins	22	33	22	33
	Voltage Range (Volts)	2.5-6.0	2.5-6.0	2.5-6.0	2.5-6.0
	In-Circuit Serial Programming	Yes	Yes	Yes	Yes
	Brown-out Reset	Yes	Yes	Yes	Yes
	Packages	28-pin SDIP, SOIC	40-pin DIP; 44-pin PLCC, MQFP, TQFP	28-pin SDIP, SOIC	40-pin DIP; 44-pin PLCC, MQFP, TQFP

All PIC16/17 Family devices have Power-on Reset, selectable Watchdog Timer, selectable code protect and high I/O current capability. All PIC16C7XX Family devices use serial programming with clock pin RB6 and data pin RB7.

Note 1: Please contact your local Microchip sales office for availability of these devices.