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Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	10MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	22
Program Memory Size	14KB (8K x 14)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	368 x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 6V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16c66-10i-so

TABLE 4-3: SPECIAL FUNCTION REGISTERS FOR THE PIC16C63/R63

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other resets ⁽³⁾
Bank 0											
00h ⁽¹⁾	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								0000 0000	0000 0000
01h	TMR0	Timer0 module's register								xxxx xxxx	uuuu uuuu
02h ⁽¹⁾	PCL	Program Counter's (PC) Least Significant Byte								0000 0000	0000 0000
03h ⁽¹⁾	STATUS	IRP ⁽⁴⁾	RP1 ⁽⁴⁾	RP0	T _O	P _D	Z	DC	C	0001 1xxx	000q quuu
04h ⁽¹⁾	FSR	Indirect data memory address pointer								xxxx xxxx	uuuu uuuu
05h	PORTA	—	—	PORTA Data Latch when written: PORTA pins when read						- -xx xxxx	- -uu uuuu
06h	PORTB	PORTB Data Latch when written: PORTB pins when read								xxxx xxxx	uuuu uuuu
07h	PORTC	PORTC Data Latch when written: PORTC pins when read								xxxx xxxx	uuuu uuuu
08h	—	Unimplemented								—	—
09h	—	Unimplemented								—	—
0Ah ^(1,2)	PCLATH	—	—	—	Write Buffer for the upper 5 bits of the Program Counter					- - - 0 0000	- - - 0 0000
0Bh ⁽¹⁾	INTCON	GIE	PEIE	TOIE	INTE	RBIE	TOIF	INTF	RBIF	0000 000x	0000 000u
0Ch	PIR1	(5)	(5)	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
0Dh	PIR2	—	—	—	—	—	—	—	CCP2IF	- - - - - 0	- - - - - 0
0Eh	TMR1L	Holding register for the Least Significant Byte of the 16-bit TMR1 register								xxxx xxxx	uuuu uuuu
0Fh	TMR1H	Holding register for the Most Significant Byte of the 16-bit TMR1 register								xxxx xxxx	uuuu uuuu
10h	T1CON	—	—	T1CKPS1	T1CKPS0	T1OSCEN	T1SYNC	TMR1CS	TMR1ON	- - 00 0000	- - uu uuuu
11h	TMR2	Timer2 module's register								0000 0000	0000 0000
12h	T2CON	—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	- 000 0000	- 000 0000
13h	SSPBUF	Synchronous Serial Port Receive Buffer/Transmit Register								xxxx xxxx	uuuu uuuu
14h	SSPCON	WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0	0000 0000	0000 0000
15h	CCPR1L	Capture/Compare/PWM1 (LSB)								xxxx xxxx	uuuu uuuu
16h	CCPR1H	Capture/Compare/PWM1 (MSB)								xxxx xxxx	uuuu uuuu
17h	CCP1CON	—	—	CCP1X	CCP1Y	CCP1M3	CCP1M2	CCP1M1	CCP1M0	- - 00 0000	- - 00 0000
18h	RCSTA	SPEN	RX9	SREN	CREN	—	FERR	OERR	RX9D	0000 - 00x	0000 - 00x
19h	TXREG	USART Transmit Data Register								0000 0000	0000 0000
1Ah	RCREG	USART Receive Data Register								0000 0000	0000 0000
1Bh	CCPR2L	Capture/Compare/PWM2 (LSB)								xxxx xxxx	uuuu uuuu
1Ch	CCPR2H	Capture/Compare/PWM2 (MSB)								xxxx xxxx	uuuu uuuu
1Dh	CCP2CON	—	—	CCP2X	CCP2Y	CCP2M3	CCP2M2	CCP2M1	CCP2M0	- - 00 0000	- - 00 0000
1Eh-1Fh	—	Unimplemented								—	—

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented location read as '0'.
Shaded locations are unimplemented, read as '0'.

Note 1: These registers can be addressed from either bank.

- The upper byte of the Program Counter (PC) is not directly accessible. PCLATH is a holding register for the PC whose contents are transferred to the upper byte of the program counter. (PC<12:8>)
- Other (non power-up) resets include external reset through \overline{MCLR} and the Watchdog Timer reset.
- The IRP and RP1 bits are reserved on the PIC16C63/R63, always maintain these bits clear.
- PIE1<7:6> and PIR1<7:6> are reserved on the PIC16C63/R63, always maintain these bits clear.

TABLE 4-6: SPECIAL FUNCTION REGISTERS FOR THE PIC16C66/67 (Cont'd)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other resets ⁽³⁾	
Bank 1												
80h ⁽¹⁾	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								0000 0000	0000 0000	
81h	OPTION	RBP \overline{U}	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111	
82h ⁽¹⁾	PCL	Program Counter's (PC) Least Significant Byte								0000 0000	0000 0000	
83h ⁽¹⁾	STATUS	IRP	RP1	RP0	$\overline{T0}$	\overline{PD}	Z	DC	C	0001 1xxx	000q quuu	
84h ⁽¹⁾	FSR	Indirect data memory address pointer								xxxx xxxx	uuuu uuuu	
85h	TRISA	—	—	PORTA Data Direction Register						--11 1111	--11 1111	
86h	TRISB	PORTB Data Direction Register								1111 1111	1111 1111	
87h	TRISC	PORTC Data Direction Register								1111 1111	1111 1111	
88h ⁽⁵⁾	TRISD	PORTD Data Direction Register								1111 1111	1111 1111	
89h ⁽⁵⁾	TRISE	IBF	OBF	IBOV	PSPMODE	—	PORTE Data Direction Bits			0000 -111	0000 -111	
8Ah ^(1,2)	PCLATH	—	—	—	Write Buffer for the upper 5 bits of the Program Counter						---0 0000	---0 0000
8Bh ⁽¹⁾	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000u	
8Ch	PIE1	PSPIE ⁽⁶⁾	(4)	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000	
8Dh	PIE2	—	—	—	—	—	—	—	CCP2IE	---- --0	---- --0	
8Eh	PCON	—	—	—	—	—	—	POR	\overline{BOR}	---- --qq	---- --uu	
8Fh	—	Unimplemented								—	—	
90h	—	Unimplemented								—	—	
91h	—	Unimplemented								—	—	
92h	PR2	Timer2 Period Register								1111 1111	1111 1111	
93h	SSPADD	Synchronous Serial Port (I ² C mode) Address Register								0000 0000	0000 0000	
94h	SSPSTAT	SMP	CKE	D/ \overline{A}	P	S	R/ \overline{W}	UA	BF	0000 0000	0000 0000	
95h	—	Unimplemented								—	—	
96h	—	Unimplemented								—	—	
97h	—	Unimplemented								—	—	
98h	TXSTA	CSRC	TX9	TXEN	SYNC	—	BRGH	TRMT	TX9D	0000 -010	0000 -010	
99h	SPBRG	Baud Rate Generator Register								0000 0000	0000 0000	
9Ah	—	Unimplemented								—	—	
9Bh	—	Unimplemented								—	—	
9Ch	—	Unimplemented								—	—	
9Dh	—	Unimplemented								—	—	
9Eh	—	Unimplemented								—	—	
9Fh	—	Unimplemented								—	—	

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented location read as '0'.

Shaded locations are unimplemented, read as '0'.

Note 1: These registers can be addressed from any bank.

2: The upper byte of the Program Counter (PC) is not directly accessible. PCLATH is a holding register for the PC whose contents are transferred to the upper byte of the program counter. (PC<12:8>)

3: Other (non power-up) resets include external reset through MCLR and the Watchdog Timer reset.

4: PIE1<6> and PIR1<6> are reserved on the PIC16C66/67, always maintain these bits clear.

5: PORTD, PORTE, TRISD, and TRISE are not implemented on the PIC16C66, read as '0'.

6: PSPIF (PIR1<7>) and PSPIE (PIE1<7>) are reserved on the PIC16C66, maintain these bits clear.

PIC16C6X

TABLE 5-6: PORTC FUNCTIONS FOR PIC16C62A/R62/64A/R64

Name	Bit#	Buffer Type	Function
RC0/T1OSO/T1CKI	bit0	ST	Input/output port pin or Timer1 oscillator output or Timer1 clock input
RC1/T1OSI	bit1	ST	Input/output port pin or Timer1 oscillator input
RC2/CCP1	bit2	ST	Input/output port pin or Capture input/Compare output/PWM1 output
RC3/SCK/SCL	bit3	ST	RC3 can also be the synchronous serial clock for both SPI and I ² C modes.
RC4/SDI/SDA	bit4	ST	RC4 can also be the SPI Data In (SPI mode) or data I/O (I ² C mode).
RC5/SDO	bit5	ST	Input/output port pin or synchronous serial port data output
RC6	bit6	ST	Input/output port pin
RC7	bit7	ST	Input/output port pin

Legend: ST = Schmitt Trigger input

TABLE 5-7: PORTC FUNCTIONS FOR PIC16C63/R63/65/65A/R65/66/67

Name	Bit#	Buffer Type	Function
RC0/T1OSO/T1CKI	bit0	ST	Input/output port pin or Timer1 oscillator output or Timer1 clock input
RC1/T1OSI/CCP2	bit1	ST	Input/output port pin or Timer1 oscillator input or Capture2 input/Compare2 output/PWM2 output
RC2/CCP1	bit2	ST	Input/output port pin or Capture1 input/Compare1 output/PWM1 output
RC3/SCK/SCL	bit3	ST	RC3 can also be the synchronous serial clock for both SPI and I ² C modes.
RC4/SDI/SDA	bit4	ST	RC4 can also be the SPI Data In (SPI mode) or data I/O (I ² C mode).
RC5/SDO	bit5	ST	Input/output port pin or synchronous serial port data output
RC6/TX/CK	bit6	ST	Input/output port pin or USART Asynchronous Transmit, or USART Synchronous Clock
RC7/RX/DT	bit7	ST	Input/output port pin or USART Asynchronous Receive, or USART Synchronous Data

Legend: ST = Schmitt Trigger input

TABLE 5-8: SUMMARY OF REGISTERS ASSOCIATED WITH PORTC

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other resets
07h	PORTC	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0	xxxx xxxx	uuuu uuuu
87h	TRISC	PORTC Data Direction Register								1111 1111	1111 1111

Legend: x = unknown, u = unchanged.

6.0 OVERVIEW OF TIMER MODULES

Applicable Devices															
61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67		

All PIC16C6X devices have three timer modules except for the PIC16C61, which has one timer module. Each module can generate an interrupt to indicate that an event has occurred (i.e., timer overflow). Each of these modules are detailed in the following sections. The timer modules are:

- Timer0 module (Section 7.0)
- Timer1 module (Section 8.0)
- Timer2 module (Section 9.0)

6.1 Timer0 Overview

Applicable Devices															
61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67		

The Timer0 module is a simple 8-bit overflow counter. The clock source can be either the internal system clock ($F_{osc}/4$) or an external clock. When the clock source is an external clock, the Timer0 module can be selected to increment on either the rising or falling edge.

The Timer0 module also has a programmable prescaler option. This prescaler can be assigned to either the Timer0 module or the Watchdog Timer. Bit PSA (OPTION<3>) assigns the prescaler, and bits PS2:PS0 (OPTION<2:0>) determine the prescaler value. TMR0 can increment at the following rates: 1:1 when the prescaler is assigned to Watchdog Timer, 1:2, 1:4, 1:8, 1:16, 1:32, 1:64, 1:128, and 1:256.

Synchronization of the external clock occurs after the prescaler. When the prescaler is used, the external clock frequency may be higher than the device's frequency. The maximum frequency is 50 MHz, given the high and low time requirements of the clock.

6.2 Timer1 Overview

Applicable Devices															
61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67		

Timer1 is a 16-bit timer/counter. The clock source can be either the internal system clock ($F_{osc}/4$), an external clock, or an external crystal. Timer1 can operate as either a timer or a counter. When operating as a counter (external clock source), the counter can either operate synchronized to the device or asynchronously to the device. Asynchronous operation allows Timer1 to operate during sleep, which is useful for applications that require a real-time clock as well as the power savings of SLEEP mode.

Timer1 also has a prescaler option which allows TMR1 to increment at the following rates: 1:1, 1:2, 1:4, and 1:8. TMR1 can be used in conjunction with the Capture/Compare/PWM module. When used with a CCP module, Timer1 is the time-base for 16-bit capture or 16-bit compare and must be synchronized to the device.

6.3 Timer2 Overview

Applicable Devices															
61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67		

Timer2 is an 8-bit timer with a programmable prescaler and a programmable postscaler, as well as an 8-bit Period Register (PR2). Timer2 can be used with the CCP module (in PWM mode) as well as the Baud Rate Generator for the Synchronous Serial Port (SSP). The prescaler option allows Timer2 to increment at the following rates: 1:1, 1:4, and 1:16.

The postscaler allows TMR2 register to match the period register (PR2) a programmable number of times before generating an interrupt. The postscaler can be programmed from 1:1 to 1:16 (inclusive).

6.4 CCP Overview

Applicable Devices															
61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67		

The CCP module(s) can operate in one of three modes: 16-bit capture, 16-bit compare, or up to 10-bit Pulse Width Modulation (PWM).

Capture mode captures the 16-bit value of TMR1 into the CCPRxH:CCPRxL register pair. The capture event can be programmed for either the falling edge, rising edge, fourth rising edge, or sixteenth rising edge of the CCPx pin.

Compare mode compares the TMR1H:TMR1L register pair to the CCPRxH:CCPRxL register pair. When a match occurs, an interrupt can be generated and the output pin CCPx can be forced to a given state (High or Low) and Timer1 can be reset. This depends on control bits CCPxM3:CCPxM0.

PWM mode compares the TMR2 register to a 10-bit duty cycle register (CCPRxH:CCPRxL<5:4>) as well as to an 8-bit period register (PR2). When the TMR2 register = Duty Cycle register, the CCPx pin will be forced low. When TMR2 = PR2, TMR2 is cleared to 00h, an interrupt can be generated, and the CCPx pin (if an output) will be forced high.

8.0 TIMER1 MODULE

Applicable Devices

61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67
----	----	-----	-----	----	-----	----	-----	-----	----	-----	-----	----	----

Timer1 is a 16-bit timer/counter consisting of two 8-bit registers (TMR1H and TMR1L) which are readable and writable. Register TMR1 (TMR1H:TMR1L) increments from 0000h to FFFFh and rolls over to 0000h. The TMR1 Interrupt, if enabled, is generated on overflow which is latched in interrupt flag bit TMR1IF (PIR1<0>). This interrupt can be enabled/disabled by setting/clearing the TMR1 interrupt enable bit TMR1IE (PIE1<0>).

Timer1 can operate in one of two modes:

- As a timer
- As a counter

The operating mode is determined by clock select bit, TMR1CS (T1CON<1>) (Figure 8-2).

In timer mode, Timer1 increments every instruction cycle. In counter mode, it increments on every rising edge of the external clock input.

Timer1 can be enabled/disabled by setting/clearing control bit TMR1ON (T1CON<0>).

Timer1 also has an internal "reset input". This reset can be generated by CCP1 or CCP2 (Capture/Compare/PWM) module. See Section 10.0 for details. Figure 8-1 shows the Timer1 control register.

For the PIC16C62A/R62/63/R63/64A/R64/65A/R65/R66/67, when the Timer1 oscillator is enabled (T1OSCEN is set), the RC1 and RC0 pins become inputs. That is, the TRISC<1:0> value is ignored.

For the PIC16C62/64/65, when the Timer1 oscillator is enabled (T1OSCEN is set), RC1 pin becomes an input, however the RC0 pin will have to be configured as an input by setting the TRISC<0> bit.

The Timer1 module also has a software programmable prescaler.

FIGURE 8-1: T1CON: TIMER1 CONTROL REGISTER (ADDRESS 10h)

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	T1CKPS1	T1CKPS0	T1OSCEN	T1SYN \bar{C}	TMR1CS	TMR1ON
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n = Value at POR reset

bit 7-6: **Unimplemented:** Read as '0'

bit 5-4: **T1CKPS1:T1CKPS0:** Timer1 Input Clock Prescale Select bits
11 = 1:8 Prescale value
10 = 1:4 Prescale value
01 = 1:2 Prescale value
00 = 1:1 Prescale value

bit 3: **T1OSCEN:** Timer1 Oscillator Enable Control bit
1 = Oscillator is enabled
0 = Oscillator is shut off
Note: The oscillator inverter and feedback resistor are turned off to eliminate power drain.

bit 2: **T1SYN \bar{C} :** Timer1 External Clock Input Synchronization Control bit
TMR1CS = 1
1 = Do not synchronize external clock input
0 = Synchronize external clock input
TMR1CS = 0
This bit is ignored. Timer1 uses the internal clock when TMR1CS = 0.

bit 1: **TMR1CS:** Timer1 Clock Source Select bit
1 = External clock from T1OSI (on the rising edge) (See pinouts for pin with T1OSI function)
0 = Internal clock (Fosc/4)

bit 0: **TMR1ON:** Timer1 On bit
1 = Enables Timer1
0 = Stops Timer1

14.0 INSTRUCTION SET SUMMARY

Each PIC16CXX instruction is a 14-bit word divided into an OPCODE which specifies the instruction type and one or more operands which further specify the operation of the instruction. The PIC16CXX instruction set summary in Table 14-2 lists **byte-oriented**, **bit-oriented**, and **literal and control** operations. Table 14-1 shows the opcode field descriptions.

For **byte-oriented** instructions, 'f' represents a file register designator and 'd' represents a destination designator. The file register designator specifies which file register is to be used by the instruction.

The destination designator specifies where the result of the operation is to be placed. If 'd' is zero, the result is placed in the W register. If 'd' is one, the result is placed in the file register specified in the instruction.

For **bit-oriented** instructions, 'b' represents a bit field designator which selects the number of the bit affected by the operation, while 'f' represents the number of the file in which the bit is located.

For **literal and control** operations, 'k' represents an eight or eleven bit constant or literal value.

TABLE 14-1: OPCODE FIELD DESCRIPTIONS

Field	Description
f	Register file address (0x00 to 0x7F)
W	Working register (accumulator)
b	Bit address within an 8-bit file register
k	Literal field, constant data or label
x	Don't care location (= 0 or 1) The assembler will generate code with x = 0. It is the recommended form of use for compatibility with all Microchip software tools.
d	Destination select; d = 0: store result in W, d = 1: store result in file register f. Default is d = 1
label	Label name
TOS	Top of Stack
PC	Program Counter
PCLATH	Program Counter High Latch
GIE	Global Interrupt Enable bit
WDT	Watchdog Timer/Counter
TO	Time-out bit
PD	Power-down bit
dest	Destination either the W register or the specified register file location
[]	Options
()	Contents
→	Assigned to
< >	Register bit field
∈	In the set of
<i>italics</i>	User defined term (font is courier)

The instruction set is highly orthogonal and is grouped into three basic categories:

- **Byte-oriented** operations
- **Bit-oriented** operations
- **Literal and control** operations

All instructions are executed within one single instruction cycle, unless a conditional test is true or the program counter is changed as a result of an instruction. In this case, the execution takes two instruction cycles with the second cycle executed as a NOP. One instruction cycle consists of four oscillator periods. Thus, for an oscillator frequency of 4 MHz, the normal instruction execution time is 1 μs. If a conditional test is true or the program counter is changed as a result of an instruction, the instruction execution time is 2 μs.

Table 14-2 lists the instructions recognized by the MPASM assembler.

Figure 14-1 shows the general formats that the instructions can have.

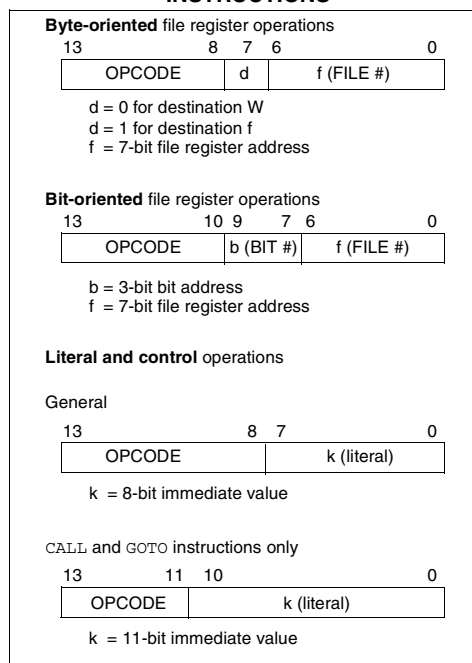
Note: To maintain upward compatibility with future PIC16CXX products, do not use the `OPTION` and `TRIS` instructions.

All examples use the following format to represent a hexadecimal number:

0xhh

where h signifies a hexadecimal digit.

FIGURE 14-1: GENERAL FORMAT FOR INSTRUCTIONS



BTFSS Bit Test f, Skip if Set

Syntax: `[label] BTFSS f,b`

Operands: $0 \leq f \leq 127$
 $0 \leq b < 7$

Operation: skip if $(f < b) = 1$

Status Affected: None

Encoding:

01	11bb	bfff	ffff
----	------	------	------

Description: If bit 'b' in register 'f' is '0' then the next instruction is executed.
 If bit 'b' is '1', then the next instruction is discarded and a NOP is executed instead, making this a 2Tcy instruction.

Words: 1

Cycles: 1(2)

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process data	No-Operation

If Skip: (2nd Cycle)

Q1	Q2	Q3	Q4
No-Operation	No-Operation	No-Operation	No-Operation

Example

```

HERE    BTFSC  FLAG, 1
FALSE   GOTO   PROCESS_CODE
TRUE    •
        •
        •
    
```

Before Instruction

PC = address HERE

After Instruction

```

if FLAG<1> = 0,
PC = address FALSE
if FLAG<1> = 1,
PC = address TRUE
    
```

CALL Call Subroutine

Syntax: `[label] CALL k`

Operands: $0 \leq k \leq 2047$

Operation: $(PC) + 1 \rightarrow TOS$,
 $k \rightarrow PC < 10:0 >$,
 $(PCLATH < 4:3 >) \rightarrow PC < 12:11 >$

Status Affected: None

Encoding:

10	0kkk	kkkk	kkkk
----	------	------	------

Description: Call Subroutine. First, return address $(PC+1)$ is pushed onto the stack. The eleven bit immediate address is loaded into PC bits $<10:0 >$. The upper bits of the PC are loaded from PCLATH. CALL is a two cycle instruction.

Words: 1

Cycles: 2

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read literal 'k', Push PC to Stack	Process data	Write to PC
No-Operation	No-Operation	No-Operation	No-Operation

1st Cycle

2nd Cycle

Example

```

HERE    CALL   THERE
    
```

Before Instruction

PC = Address HERE

After Instruction

PC = Address THERE

TOS = Address HERE+1

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IORWF Inclusive OR W with f

Syntax:	[<i>label</i>] IORWF f,d			
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$			
Operation:	(W) .OR. (f) \rightarrow (destination)			
Status Affected:	Z			
Encoding:	00	0100	dfff	ffff
Description:	Inclusive OR the W register with register 'f'. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'.			
Words:	1			
Cycles:	1			
Q Cycle Activity:	Q1	Q2	Q3	Q4
	Decode	Read register 'f'	Process data	Write to destination

Example IORWF RESULT, 0

Before Instruction

RESULT = 0x13
W = 0x91

After Instruction

RESULT = 0x13
W = 0x93
Z = 1

MOVF Move f

Syntax:	[<i>label</i>] MOVF f,d			
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$			
Operation:	(f) \rightarrow (destination)			
Status Affected:	Z			
Encoding:	00	1000	dfff	ffff
Description:	The contents of register f is moved to a destination dependant upon the status of d. If d = 0, destination is W register. If d = 1, the destination is file register f itself. d = 1 is useful to test a file register since status flag Z is affected.			
Words:	1			
Cycles:	1			
Q Cycle Activity:	Q1	Q2	Q3	Q4
	Decode	Read register 'f'	Process data	Write to destination

Example MOVF FSR, 0

After Instruction

W = value in FSR register
Z = 1

MOVLW Move Literal to W

Syntax:	[<i>label</i>] MOVLW k			
Operands:	0 ≤ k ≤ 255			
Operation:	k → (W)			
Status Affected:	None			
Encoding:	11	00xx	kkkk	kkkk
Description:	The eight bit literal 'k' is loaded into W register. The don't cares will assemble as 0's.			
Words:	1			
Cycles:	1			
Q Cycle Activity:	Q1	Q2	Q3	Q4
	Decode	Read literal 'k'	Process data	Write to W

Example

MOVLW 0x5A

After Instruction

W = 0x5A

MOVWF Move W to f

Syntax:	[<i>label</i>] MOVWF f			
Operands:	$0 \leq f \leq 127$			
Operation:	(W) \rightarrow (f)			
Status Affected:	None			
Encoding:	00	0000	1fff	ffff
Description:	Move data from W register to register 'f'.			
Words:	1			
Cycles:	1			
Q Cycle Activity:	Q1	Q2	Q3	Q4
	Decode	Read register 'f'	Process data	Write register 'f'

Example

MOVWF OPTION_REG

Before Instruction

OPTION = 0xFF
W = 0x4F

After Instruction

OPTION = 0x4F
W = 0x4F

Applicable Devices 61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

DC CHARACTERISTICS		Standard Operating Conditions (unless otherwise stated)					
		Operating temperature -40°C ≤ TA ≤ +125°C for extended, -40°C ≤ TA ≤ +85°C for industrial and 0°C ≤ TA ≤ +70°C for commercial					
		Operating voltage VDD range as described in DC spec Section 15.1 and Section 15.2.					
Param No.	Characteristic	Sym	Min	Typ†	Max	Units	Conditions
D090	Output High Voltage I/O ports (Note 3)	VOH	VDD-0.7	-	-	V	IOH = -3.0 mA, VDD = 4.5V, -40°C to +85°C
D090A			VDD-0.7	-	-	V	IOH = -2.5 mA, VDD = 4.5V, -40°C to +125°C
D092	OSC2/CLKOUT (RC osc config)		VDD-0.7	-	-	V	IOH = -1.3 mA, VDD = 4.5V, -40°C to +85°C
D092A			VDD-0.7	-	-	V	IOH = -1.0 mA, VDD = 4.5V, -40°C to +125°C
D150*	Open-Drain High Voltage	VOD	-	-	14	V	RA4 pin
Capacitive Loading Specs on Output Pins							
D100	OSC2 pin	COSC2			15	pF	In XT, HS and LP modes when external clock is used to drive OSC1.
D101	All I/O pins and OSC2 (in RC mode)	CIO			50	pF	

* The parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C6X be driven with external clock in RC mode.

2: The leakage current on the MCLR/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as current sourced by the pin.

PIC16C6X

Applicable Devices 61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

FIGURE 15-5: TIMER0 EXTERNAL CLOCK TIMINGS

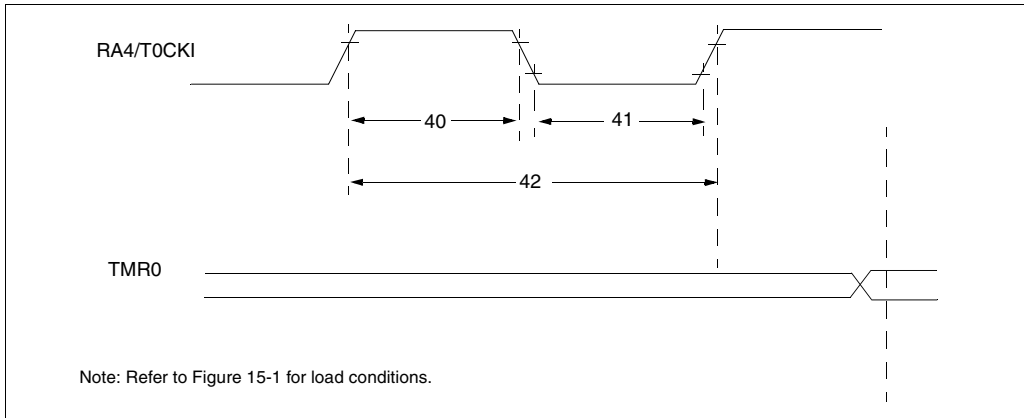


TABLE 15-5: TIMER0 EXTERNAL CLOCK REQUIREMENTS

Parameter No.	Sym	Characteristic		Min	Typ†	Max	Units	Conditions
40*	Tt0H	T0CKI High Pulse Width	No Prescaler	$0.5T_{CY} + 20$	—	—	ns	Must also meet parameter 42
			With Prescaler	10	—	—	ns	
41*	Tt0L	T0CKI Low Pulse Width	No Prescaler	$0.5T_{CY} + 20$	—	—	ns	Must also meet parameter 42
			With Prescaler	10	—	—	ns	
42*	Tt0P	T0CKI Period	No Prescaler	$T_{CY} + 40$	—	—	ns	N = prescale value (2, 4, ..., 256)
			With Prescaler	Greater of: 20 ns or $\frac{T_{CY} + 40}{N}$	—	—	ns	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 16-10: V_{IH} , V_{IL} OF \overline{MCLR} , $T0CKI$ AND $OSC1$ (IN RC MODE) vs. V_{DD}

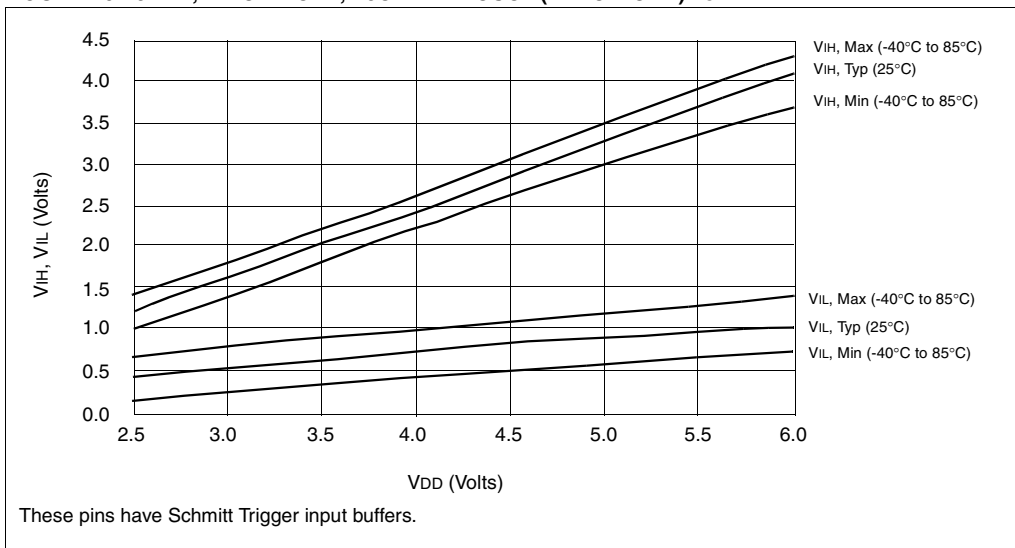
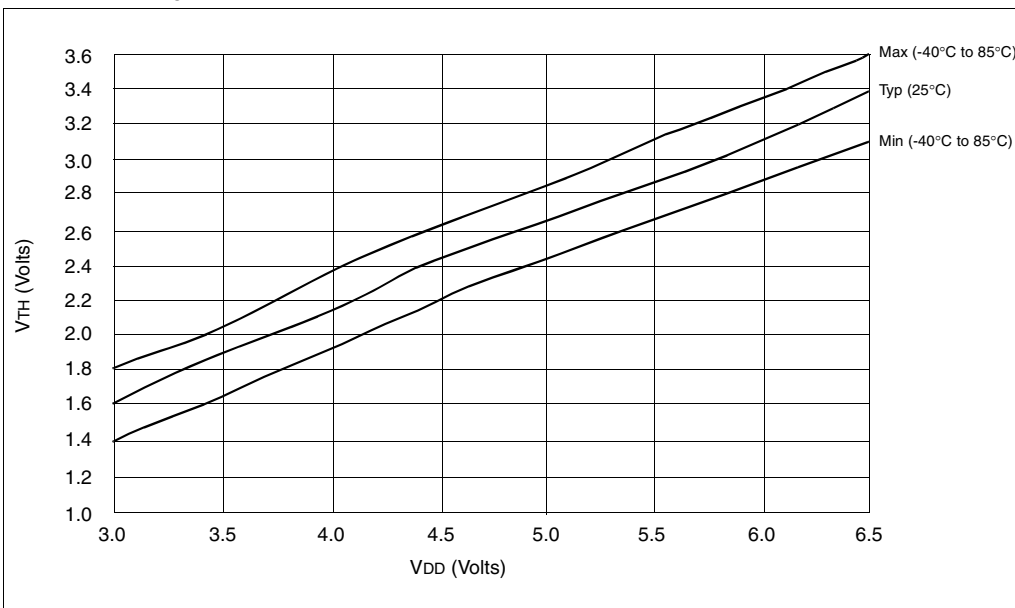


FIGURE 16-11: V_{TH} (INPUT THRESHOLD VOLTAGE) OF $OSC1$ INPUT (IN XT, HS, AND LP MODES) vs. V_{DD}



Data based on matrix samples. See first page of this section for details.

PIC16C6X

Applicable Devices	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67
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NOTES:

PIC16C6X

Applicable Devices 61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

FIGURE 17-9: I²C BUS START/STOP BITS TIMING

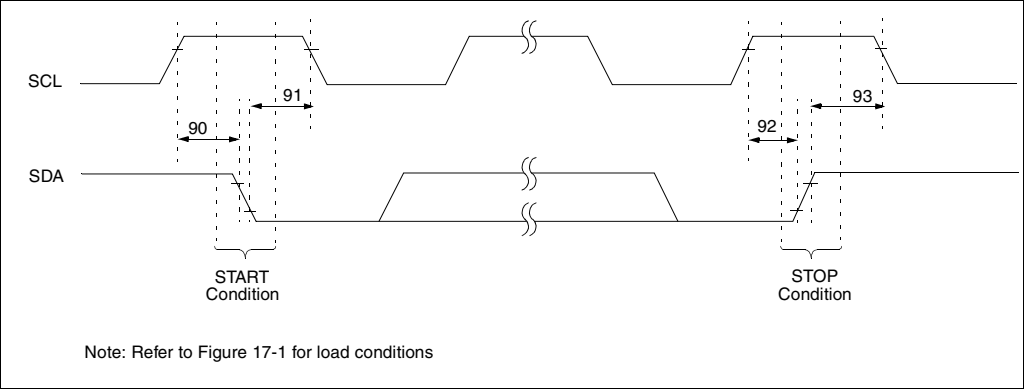


TABLE 17-9: I²C BUS START/STOP BITS REQUIREMENTS

Parameter No.	Sym	Characteristic		Min	Typ	Max	Units	Conditions
90	TSU:STA	START condition	100 kHz mode	4700	—	—	ns	Only relevant for repeated START condition
		Setup time	400 kHz mode	600	—	—		
91	THD:STA	START condition	100 kHz mode	4000	—	—	ns	After this period the first clock pulse is generated
		Hold time	400 kHz mode	600	—	—		
92	TSU:STO	STOP condition	100 kHz mode	4700	—	—	ns	
		Setup time	400 kHz mode	600	—	—		
93	THD:STO	STOP condition	100 kHz mode	4000	—	—	ns	
		Hold time	400 kHz mode	600	—	—		

PIC16C6X

Applicable Devices	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67
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NOTES:

PIC16C6X

Applicable Devices	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67
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NOTES:

19.0 ELECTRICAL CHARACTERISTICS FOR PIC16C65

Absolute Maximum Ratings †

Ambient temperature under bias.....	-55°C to +85°C
Storage temperature	-65°C to +150°C
Voltage on any pin with respect to VSS (except VDD, MCLR, and RA4).....	-0.3V to (VDD + 0.3V)
Voltage on VDD with respect to VSS	-0.3V to +7.5V
Voltage on MCLR with respect to VSS (Note 2).....	0V to +14V
Voltage on RA4 with respect to VSS	0V to +14V
Total power dissipation (Note 1).....	1.0W
Maximum current out of VSS pin	300 mA
Maximum current into VDD pin	250 mA
Input clamp current, I _{IK} (V _I < 0 or V _I > VDD).....	±20 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > VDD)	±20 mA
Maximum output current sunk by any I/O pin.....	25 mA
Maximum output current sourced by any I/O pin	25 mA
Maximum current sunk by PORTA, PORTB, and PORTE (combined).....	200 mA
Maximum current sourced by PORTA, PORTB, and PORTE (combined)	200 mA
Maximum current sunk by PORTC and PORTD (combined)	200 mA
Maximum current sourced by PORTC and PORTD (combined)	200 mA

Note 1: Power dissipation is calculated as follows: $P_{dis} = VDD \times \{I_{DD} - \sum I_{OH}\} + \sum \{(VDD - V_{OH}) \times I_{OH}\} + \sum (V_{OL} \times I_{OL})$

Note 2: Voltage spikes below VSS at the MCLR pin, inducing currents greater than 80 mA, may cause latch-up. Thus, a series resistor of 50-100Ω should be used when applying a “low” level to the MCLR pin rather than pulling this pin directly to VSS.

† NOTICE: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 19-1: CROSS REFERENCE OF DEVICE SPECS FOR OSCILLATOR CONFIGURATIONS AND FREQUENCIES OF OPERATION (COMMERCIAL DEVICES)

OSC	PIC16C65-04	PIC16C65-10	PIC16C65-20	PIC16LC65-04	JW Devices
RC	VDD: 4.0V to 6.0V IDD: 5 mA max. at 5.5V IPD: 21 µA max. at 4V Freq: 4 MHz max.	VDD: 4.5V to 5.5V IDD: 2.7 mA typ. at 5.5V IPD: 1.5 µA typ. at 4V Freq: 4 MHz max.	VDD: 4.5V to 5.5V IDD: 2.7 mA typ. at 5.5V IPD: 1.5 µA typ. at 4V Freq: 4 MHz max.	VDD: 3.0V to 6.0V IDD: 3.8 mA max. at 3V IPD: 800 µA max. at 3V Freq: 4 MHz max.	VDD: 4.0V to 6.0V IDD: 5 mA max. at 5.5V IPD: 21 µA max. at 4V Freq: 4 MHz max.
XT	VDD: 4.0V to 6.0V IDD: 5 mA max. at 5.5V IPD: 21 µA max. at 4V Freq: 4 MHz max.	VDD: 4.5V to 5.5V IDD: 2.7 mA typ. at 5.5V IPD: 1.5 µA typ. at 4V Freq: 4 MHz max.	VDD: 4.5V to 5.5V IDD: 2.7 mA typ. at 5.5V IPD: 1.5 µA typ. at 4V Freq: 4 MHz max.	VDD: 3.0V to 6.0V IDD: 3.8 mA max. at 3V IPD: 800 µA max. at 3V Freq: 4 MHz max.	VDD: 4.0V to 6.0V IDD: 5 mA max. at 5.5V IPD: 21 µA max. at 4V Freq: 4 MHz max.
HS	VDD: 4.5V to 5.5V IDD: 13.5 mA typ. at 5.5V IPD: 1.5 µA typ. at 4.5V Freq: 4 MHz max.	VDD: 4.5V to 5.5V IDD: 15 mA max. at 5.5V IPD: 1.0 µA typ. at 4.5V Freq: 10 MHz max.	VDD: 4.5V to 5.5V IDD: 30 mA max. at 5.5V IPD: 1.5 µA typ. at 4.5V Freq: 20 MHz max.	Not recommended for use in HS mode	VDD: 4.5V to 5.5V IDD: 30 mA max. at 5.5V IPD: 1.5 µA typ. at 4.5V Freq: 20 MHz max.
LP	VDD: 4.0V to 6.0V IDD: 52.5 µA typ. at 32 kHz, 4.0V IPD: 0.9 µA typ. at 4.0V Freq: 200 kHz max.	Not recommended for use in LP mode	Not recommended for use in LP mode	VDD: 3.0V to 6.0V IDD: 105 µA max. at 32 kHz, 3.0V IPD: 800 µA max. at 3.0V Freq: 200 kHz max.	VDD: 3.0V to 6.0V IDD: 105 µA max. at 32 kHz, 3.0V IPD: 800 µA max. at 3.0V Freq: 200 kHz max.

The shaded sections indicate oscillator selections which are tested for functionality, but not for MIN/MAX specifications. It is recommended that the user select the device type that ensures the specifications required.

PIC16C6X

Applicable Devices	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67
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20.4 Timing Parameter Symbology

The timing parameter symbols have been created following one of the following formats:

1. TppS2ppS
2. TppS
3. TCC:ST (I²C specifications only)
4. Ts (I²C specifications only)

T		T	
F	Frequency	T	Time

Lowercase letters (pp) and their meanings:

pp			
cc	CCP1	osc	OSC1
ck	CLKOUT	rd	\overline{RD}
cs	\overline{CS}	rw	\overline{RD} or \overline{WR}
di	SDI	sc	SCK
do	SDO	ss	\overline{SS}
dt	Data in	t0	T0CKI
io	I/O port	t1	T1CKI
mc	\overline{MCLR}	wr	\overline{WR}

Uppercase letters and their meanings:

S			
F	Fall	P	Period
H	High	R	Rise
I	Invalid (Hi-impedance)	V	Valid
L	Low	Z	Hi-impedance
I ² C only			
AA	output access	High	High
BUF	Bus free	Low	Low

TCC:ST (I²C specifications only)

CC			
HD	Hold	SU	Setup
ST			
DAT	DATA input hold	STO	STOP condition
STA	START condition		

FIGURE 20-1: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS

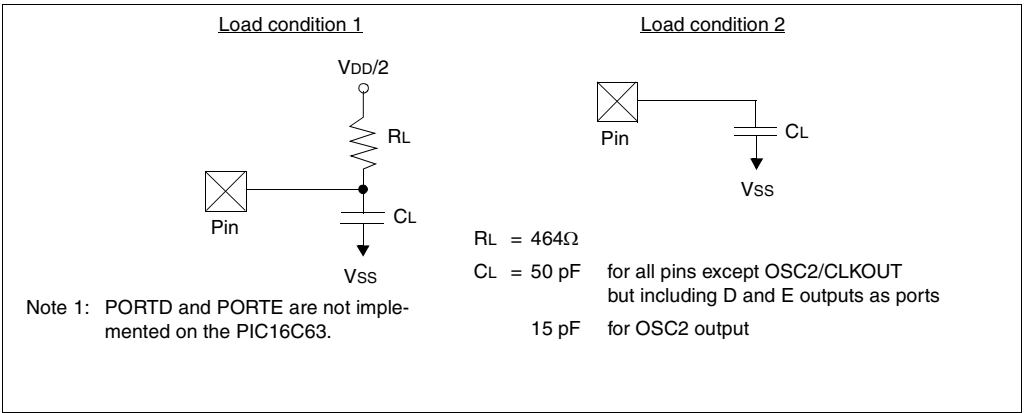


FIGURE 20-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING

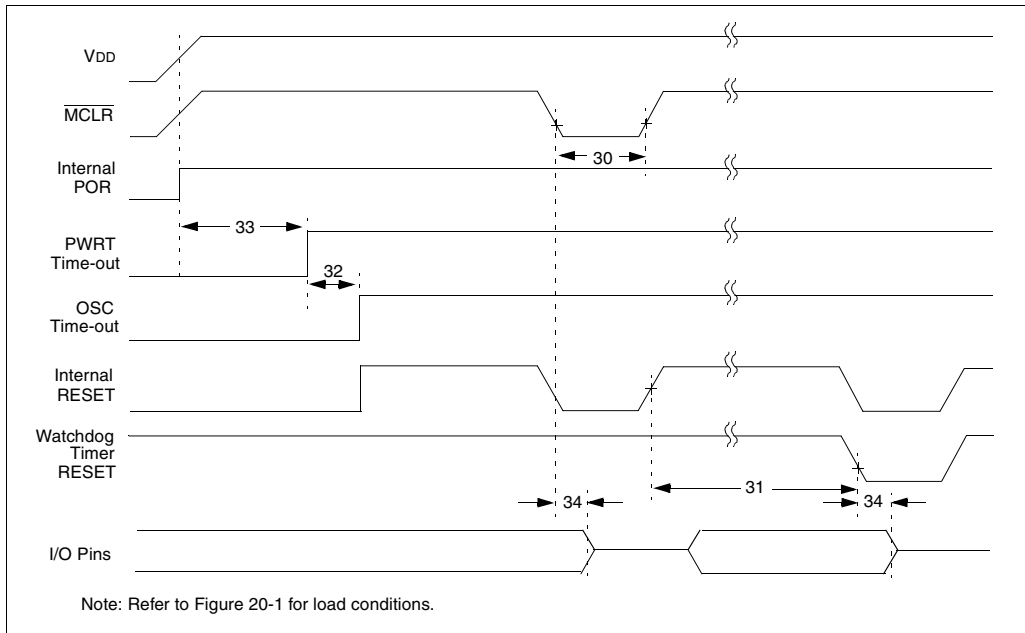


FIGURE 20-5: BROWN-OUT RESET TIMING

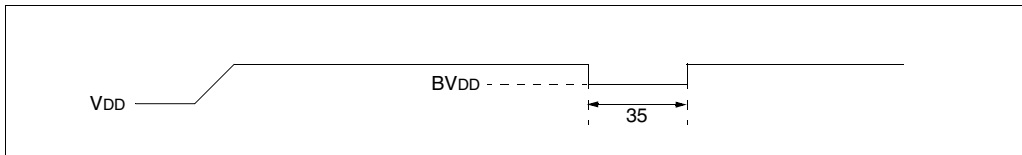


TABLE 20-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, POWER-UP TIMER, AND BROWN-OUT RESET REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
30	Tmcl	MCLR Pulse Width (low)	2	—	—	μs	VDD = 5V, -40°C to +125°C
31*	Twdt	Watchdog Timer Time-out Period (No Prescaler)	7	18	33	ms	VDD = 5V, -40°C to +125°C
32	Tost	Oscillation Start-up Timer Period	—	1024 TOSC	—	—	TOSC = OSC1 period
33*	Tpwrt	Power-up Timer Period	28	72	132	ms	VDD = 5V, -40°C to +125°C
34	Tioz	I/O Hi-impedance from MCLR Low or WDT reset	—	—	2.1	μs	
35	TBOR	Brown-out Reset Pulse Width	100	—	—	μs	VDD ≤ BVDD (D005)

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

PIC16C6X

Applicable Devices 61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

22.3 DC Characteristics: PIC16C66/67-04 (Commercial, Industrial, Extended) PIC16C66/67-10 (Commercial, Industrial, Extended) PIC16C66/67-20 (Commercial, Industrial, Extended) PIC16LC66/67-04 (Commercial, Industrial)

DC CHARACTERISTICS <div> Standard Operating Conditions (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for extended, $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for industrial and $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ for commercial Operating voltage V_{DD} range as described in DC spec Section 22.1 and Section 22.2 </div>							
Param No.	Characteristic	Sym	Min	Typ †	Max	Units	Conditions
D030 D030A D031 D032 D033	Input Low Voltage I/O ports with TTL buffer with Schmitt Trigger buffer MCLR, OSC1 (in RC mode) OSC1 (in XT, HS and LP)	V_{IL}	V_{SS} V_{SS} V_{SS} V_{SS} V_{SS}	- - - - -	$0.15V_{DD}$ $0.8V$ $0.2V_{DD}$ $0.2V_{DD}$ $0.3V_{DD}$	V V V V V	For entire V_{DD} range $4.5V \leq V_{DD} \leq 5.5V$ Note1
D040 D040A D041 D042 D042A D043	Input High Voltage I/O ports with TTL buffer with Schmitt Trigger buffer MCLR OSC1 (XT, HS and LP) OSC1 (in RC mode)	V_{IH}	2.0 $0.25V_{DD} + 0.8V$ $0.8V_{DD}$ $0.8V_{DD}$ $0.7V_{DD}$ $0.9V_{DD}$	- - - - - -	V_{DD} V_{DD} V_{DD} V_{DD} V_{DD} V_{DD}	V V V V V V	$4.5V \leq V_{DD} \leq 5.5V$ For entire V_{DD} range For entire V_{DD} range Note1
D070	PORTB weak pull-up current	IPURB	50	250	400	μA	$V_{DD} = 5V, V_{PIN} = V_{SS}$
D060 D061 D063	Input Leakage Current (Notes 2, 3) I/O ports MCLR, RA4/T0CKI OSC1	I_{IL}	-	-	± 1	μA	$V_{SS} \leq V_{PIN} \leq V_{DD}$, Pin at hi-impedance $V_{SS} \leq V_{PIN} \leq V_{DD}$ $V_{SS} \leq V_{PIN} \leq V_{DD}$, XT, HS and LP osc configuration
D080 D080A D083 D083A	Output Low Voltage I/O ports OSC2/CLKOUT (RC osc config)	V_{OL}	-	-	0.6	V	$I_{OL} = 8.5\text{ mA}$, $V_{DD} = 4.5V$, -40°C to $+85^{\circ}\text{C}$ $I_{OL} = 7.0\text{ mA}$, $V_{DD} = 4.5V$, -40°C to $+125^{\circ}\text{C}$ $I_{OL} = 1.6\text{ mA}$, $V_{DD} = 4.5V$, -40°C to $+85^{\circ}\text{C}$ $I_{OL} = 1.2\text{ mA}$, $V_{DD} = 4.5V$, -40°C to $+125^{\circ}\text{C}$

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C6X be driven with external clock in RC mode.

2: The leakage current on the MCLR/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as current sourced by the pin.

PIC16C6X

Applicable Devices 61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

FIGURE 23-29: TYPICAL I_{DD} vs. FREQUENCY
(HS MODE, 25°C)

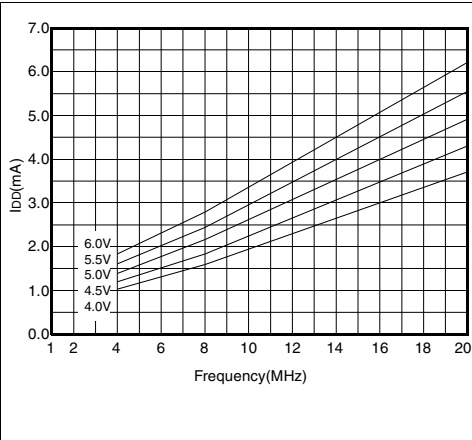
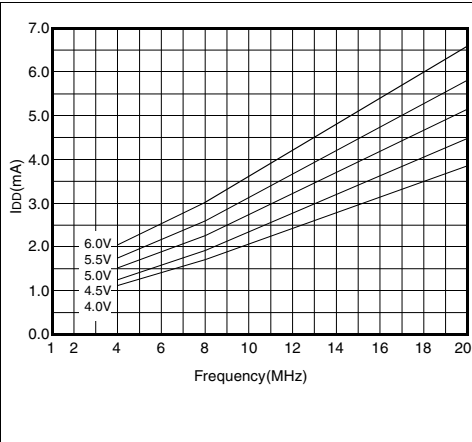


FIGURE 23-30: MAXIMUM I_{DD} vs. FREQUENCY
(HS MODE, -40°C TO 85°C)



Data based on matrix samples. See first page of this section for details.