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Details

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	33
Program Memory Size	14KB (8K x 14)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	368 x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 6V
Data Converters	-
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	44-PLCC (16.59x16.59)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16c67-04-l

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FIGURE 4-6: PIC16C62/62A/R62/64/64A/ R64 REGISTER FILE MAP

1			
File Addre			File Address
00h	INDF ⁽¹⁾	INDF ⁽¹⁾	80h
01h	TMR0	OPTION	81h
02h	PCL	PCL	82h
03h	STATUS	STATUS	83h
04h	FSR	FSR	84h
05h	PORTA	TRISA	85h
06h	PORTB	TRISB	86h
07h	PORTC	TRISC	87h
08h	PORTD ⁽²⁾	TRISD ⁽²⁾	88h
09h	PORTE ⁽²⁾	TRISE ⁽²⁾	89h
0Ah	PCLATH	PCLATH	8Ah
0Bh	INTCON	INTCON	8Bh
0Ch	PIR1	PIE1	8Ch
0Dh			8Dh
0Eh	TMR1L	PCON	8Eh
0Fh	TMR1H		8Fh
10h	T1CON		90h
11h	TMR2		91h
12h	T2CON	PR2	92h
13h	SSPBUF	SSPADD	93h
14h	SSPCON	SSPSTAT	94h
15h	CCPR1L		95h
16h	CCPR1H		96h
17h	CCP1CON		97h
18h			98h
			0.51
1Fh			9Fh
20h		General	A0h
		Purpose	
	General	Register	BFh
	Purpose Register		C0h
	-		
7Fh			FFh
	Bank 0	Bank 1	=
	nplemented data me		ead as '0'.
Note		il register. PORTE are not a	vailable on
	the PIC16C62	2/62A/R62.	

FIGURE 4-7: PIC16C63/R63/65/65A/R65 REGISTER FILE MAP

	REGIST	TER FILE MA	AP
File Addre	ess		File Address
00h	INDF ⁽¹⁾	INDF ⁽¹⁾	80h
01h	TMR0	OPTION	81h
02h	PCL	PCL	82h
03h	STATUS	STATUS	83h
04h	FSR	FSR	84h
05h	PORTA	TRISA	85h
06h	PORTB	TRISB	86h
07h	PORTC	TRISC	87h
08h	PORTD ⁽²⁾ PORTE ⁽²⁾	TRISD ⁽²⁾ TRISE ⁽²⁾	88h
09h	PCLATH	PCLATH	89h 8Ah
0Ah	INTCON	INTCON	8Bh
0Bh 0Ch	PIR1	PIE1	8Ch
	PIR2	PIE2	8Dh
0Dh			
0Eh	TMR1L	PCON	8Eh
0Fh	TMR1H		8Fh
10h	T1CON		90h
11h	TMR2		91h
12h	T2CON	PR2	92h
13h	SSPBUF	SSPADD	93h
14h	SSPCON	SSPSTAT	94h
15h	CCPR1L		95h
16h	CCPR1H		96h
17h	CCP1CON		97h
18h	RCSTA	TXSTA	98h
19h	TXREG	SPBRG	99h
1Ah	RCREG		9Ah
1Bh	CCPR2L		9Bh
1Ch	CCPR2H		9Ch
1Dh	CCP2CON		9Dh
1Eh			9Eh
1Fh			9Fh
20h	General	General	A0h
7Fh	Purpose Register	Purpose Register	FFh
	Bank 0	Bank 1	1
Unin Note		I register PORTE are not a	
L			

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other resets ⁽³⁾
Bank 0											<u> </u>
00h ⁽¹⁾	INDF	Addressing	this location	uses conten	ts of FSR to	address data	a memory (n	ot a physica	l register)	0000 0000	0000 0000
01h	TMR0	Timer0 mod	lule's registe	r						xxxx xxxx	uuuu uuuu
02h ⁽¹⁾	PCL	Program Co	ounter's (PC)	Least Signif	icant Byte					0000 0000	0000 0000
03h ⁽¹⁾	STATUS	IRP ⁽⁵⁾	RP1 ⁽⁵⁾	RP0	TO	PD	Z	DC	С	0001 1xxx	000q quuu
04h ⁽¹⁾	FSR	Indirect data	a memory ad		xxxx xxxx	uuuu uuuu					
05h	PORTA	—	—	xx xxxx	uu uuuu						
06h	PORTB	PORTB Data Latch when written: PORTB pins when read									uuuu uuuu
07h	PORTC	C PORTC Data Latch when written: PORTC pins when read									uuuu uuuu
08h		Unimplemented									_
09h		Unimplemented									_
0Ah ^(1,2)	PCLATH	_	_	_	Write Buffer	for the uppe	r 5 bits of the	e Program C	ounter	0 0000	0 0000
0Bh ⁽¹⁾	INTCON	GIE	PEIE	TOIE	INTE	RBIE	TOIF	INTF	RBIF	0000 000x	0000 000u
0Ch	PIR1	(6)	(6)	_	1	SSPIF	CCP1IF	TMR2IF	TMR1IF	00 0000	00 0000
0Dh		Unimpleme	nted							_	_
0Eh	TMR1L	Holding reg	ister for the L	east Signific	ant Byte of t	he 16-bit TM	R1 register			xxxx xxxx	uuuu uuuu
0Fh	TMR1H	Holding reg	ister for the M	/lost Signific	ant Byte of th	ne 16-bit TMF	R1 register			xxxx xxxx	uuuu uuuu
10h	T1CON	—	—	T1CKPS1	T1CKPS0	T1OSCEN	T1SYNC	TMR1CS	TMR10N	00 0000	uu uuuu
11h	TMR2	Timer2 mod	lule's registe	r						0000 0000	0000 0000
12h	T2CON	—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000 0000	-000 0000
13h	SSPBUF	Synchronou	us Serial Port	Receive Bu	ffer/Transmit	Register				xxxx xxxx	uuuu uuuu
14h	SSPCON	WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0	0000 0000	0000 0000
15h	CCPR1L	Capture/Co	mpare/PWM	1 (LSB)		·	·	•	•	xxxx xxxx	uuuu uuuu
16h	CCPR1H	Capture/Co	mpare/PWM	1 (MSB)						xxxx xxxx	uuuu uuuu
17h	CCP1CON	—	—	CCP1X	CCP1Y	CCP1M3	CCP1M2	CCP1M1	CCP1M0	00 0000	00 0000
18h-1Fh	_	Unimpleme	nted							_	_

TABLE 4-2: SPECIAL FUNCTION REGISTERS FOR THE PIC16C62/62A/R62

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented location read as '0'. Shaded locations are unimplemented, read as '0'.

Note 1: These registers can be addressed from either bank.

2: The upper byte of the Program Counter (PC) is not directly accessible. PCLATH is a holding register for the PC whose contents are transferred to the upper byte of the program counter. (PC<12:8>)

3: Other (non power-up) resets include external reset through MCLR and the Watchdog Timer reset.

4: The BOR bit is reserved on the PIC16C62, always maintain this bit set.

5: The IRP and RP1 bits are reserved on the PIC16C62/62A/R62, always maintain these bits clear.

6: PIE1<7:6> and PIR1<7:6> are reserved on the PIC16C62/62A/R62, always maintain these bits clear.

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other resets ⁽³⁾
Bank 0	1	1	1	1		1	1	1	1	1	<u> </u>
00h ⁽¹⁾	INDF	Addressing	this location	uses conter	its of FSR to	address data	a memory (n	ot a physical	register)	0000 0000	0000 0000
01h	TMR0	Timer0 mod	dule's registe	r						xxxx xxxx	uuuu uuuu
02h ⁽¹⁾	PCL	Program Co	ounter's (PC)	Least Signif	icant Byte					0000 0000	0000 0000
03h ⁽¹⁾	STATUS	IRP ⁽⁴⁾	RP1 ⁽⁴⁾	RP0	TO	PD	Z	DC	С	0001 1xxx	000q quuu
04h ⁽¹⁾	FSR	Indirect dat	a memory ac		xxxx xxxx	uuuu uuuu					
05h	PORTA	—	—	xx xxxx	uu uuuu						
06h	PORTB	PORTB Da	ta Latch whe	xxxx xxxx	uuuu uuuu						
07h	PORTC	PORTC Da	ta Latch whe	xxxx xxxx	uuuu uuuu						
08h	_	Unimpleme	nimplemented								_
09h	—	Unimpleme	nted							—	—
0Ah ^(1,2)	PCLATH	—	—	_	Write Buffer	for the uppe	r 5 bits of the	e Program C	ounter	0 0000	0 0000
0Bh ⁽¹⁾	INTCON	GIE	PEIE	TOIE	INTE	RBIE	TOIF	INTF	RBIF	0000 000x	0000 000u
0Ch	PIR1	(5)	(5)	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
0Dh	PIR2	_	_	—	_	_	_	_	CCP2IF	0	0
0Eh	TMR1L	Holding reg	ister for the I	_east Signific	ant Byte of t	ne 16-bit TM	R1 register		1	xxxx xxxx	uuuu uuuu
0Fh	TMR1H	Holding reg	ister for the I	Most Signific	ant Byte of th	e 16-bit TMF	R1 register			xxxx xxxx	uuuu uuuu
10h	T1CON	—	—	T1CKPS1	T1CKPS0	T1OSCEN	T1SYNC	TMR1CS	TMR10N	00 0000	uu uuuu
11h	TMR2	Timer2 mod	dule's registe	r						0000 0000	0000 0000
12h	T2CON	—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000 0000	-000 0000
13h	SSPBUF	Synchronou	us Serial Por	t Receive Bu	ffer/Transmit	Register				xxxx xxxx	uuuu uuuu
14h	SSPCON	WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0	0000 0000	0000 0000
15h	CCPR1L	Capture/Co	mpare/PWM	1 (LSB)						xxxx xxxx	uuuu uuuu
16h	CCPR1H	Capture/Co	mpare/PWM	1 (MSB)						xxxx xxxx	uuuu uuuu
17h	CCP1CON	—	_	CCP1X	CCP1Y	CCP1M3	CCP1M2	CCP1M1	CCP1M0	00 0000	00 0000
18h	RCSTA	SPEN	RX9	SREN	CREN	—	FERR	OERR	RX9D	0000 -00x	0000 -00x
19h	TXREG	USART Tra	nsmit Data F	legister						0000 0000	0000 0000
1Ah	RCREG	USART Receive Data Register								0000 0000	0000 0000
1Bh	CCPR2L	Capture/Co	mpare/PWM	2 (LSB)						xxxx xxxx	uuuu uuuu
1Ch	CCPR2H	Capture/Co	mpare/PWM	2 (MSB)						xxxx xxxx	uuuu uuuu
1Dh	CCP2CON	—	—	CCP2X	CCP2Y	CCP2M3	CCP2M2	CCP2M1	CCP2M0	00 0000	00 0000
1Eh-1Fh	_	Unimpleme	nted							_	_

TABLE 4-3: SPECIAL FUNCTION REGISTERS FOR THE PIC16C63/R63

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented location read as '0'. Shaded locations are unimplemented, read as '0'.

Note 1: These registers can be addressed from either bank.

2: The upper byte of the Program Counter (PC) is not directly accessible. PCLATH is a holding register for the PC whose contents are transferred to the upper byte of the program counter. (PC<12:8>)

3: Other (non power-up) resets include external reset through MCLR and the Watchdog Timer reset.

4: The IRP and RP1 bits are reserved on the PIC16C63/R63, always maintain these bits clear.

5: PIE1<7:6> and PIR1<7:6> are reserved on the PIC16C63/R63, always maintain these bits clear.

TABLE 5-11: PORTE FUNCTIONS

Name	Bit#	Buffer Type	Function
RE0/RD	bit0	ST/TTL ⁽¹⁾	Input/output port pin or Read control input in parallel slave port mode. RD 1 = Not a read operation 0 = Read operation. The system reads the PORTD register (if chip selected)
RE1/WR	bit1	ST/TTL ⁽¹⁾	Input/output port pin or Write control input in parallel slave port mode. WR 1 = Not a write operation 0 = Write operation. The system writes to the PORTD register (if chip selected)
RE2/CS	bit2	ST/TTL ⁽¹⁾	Input/output port pin or Chip select control input in parallel slave port mode. CS 1 = Device is not selected 0 = Device is selected

Legend: ST = Schmitt Trigger input, TTL = TTL input

Note 1: Buffer is a Schmitt Trigger when in I/O mode, and a TTL buffer when in Parallel Slave Port (PSP) mode.

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other resets
09h	PORTE		—	_	—		RE2	RE1	RE0	xxx	uuu
89h	TRISE	IBF	OBF	IBOV	PSPMODE	_	PORTE Data Direction Bits		Bits	0000 -111	0000 -111

Legend: x = unknown, u = unchanged, - = unimplemented locations read as '0'. Shaded cells not used by PORTE.

TABLE 9-1: REGISTERS ASSOCIATED WITH TIMER2 AS A TIMER/COUNTER

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value PC BC	R,	all o	e on ther ets
0Bh,8Bh 10Bh,18Bh	INTCON	GIE	PEIE	TOIE	INTE	RBIE	T0IF	INTF	RBIF	0000	000x	0000	000u
0Ch	PIR1	PSPIF ⁽²⁾	(3)	RCIF ⁽¹⁾	TXIF ⁽¹⁾	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000	0000	0000	0000
8Ch	PIE1	PSPIE ⁽²⁾	(3)	RCIE ⁽¹⁾	TXIE ⁽¹⁾	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000	0000	0000	0000
11h	TMR2	Timer2 m	odule's reg	ster						0000	0000	0000	0000
12h	T2CON	_	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000	0000	-000	0000
92h	PR2	Timer2 Po	eriod registe	er						1111	1111	1111	1111

Legend: x = unknown, u = unchanged, - = unimplemented locations read as '0'. Shaded cells are not used by Timer2.

Note 1: The USART is implemented on the PIC16C63/R63/65/65A/R65/66/67 only.

2: Bits PSPIE and PSPIF are reserved on the PIC16C62/62A/R62/63/R63/66, always maintain these bits clear.

3: PIR1<6> and PIE1<6> are reserved, always maintain these bits clear.

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets
0Bh,8Bh 10Bh,18Bh	INTCON	GIE	PEIE	TOIE	INTE	RBIE	TOIF	INTF	RBIF	0000 000x	0000 000u
0Ch	PIR1	PSPIF ⁽²⁾	(3)	RCIF ⁽¹⁾	TXIF ⁽¹⁾	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000	0000
0Dh ⁽⁴⁾	PIR2	—	_	_	_	_	_	_	CCP2IF		 0
8Ch	PIE1	PSPIE ⁽²⁾	(3)	RCIE ⁽¹⁾	TXIE ⁽¹⁾	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000	0000
8Dh ⁽⁴⁾	PIE2	—	_	-	_	-	_	-	CCP2IE		 0
87h	TRISC	PORTC I	Data Directio	on register						1111 1111	1111 1111
11h	TMR2	Timer2 m	0000	0000							
92h	PR2	Timer2 m	iodule's Per	iod register						1111 1111	1111 1111
12h	T2CON	—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000 0000	-000 0000
15h	CCPR1L	Capture/0	Compare/P	VM1 (LSB)	1					xxxx xxxx	uuuu uuuu
16h	CCPR1H	Capture/0	Compare/P	VM1 (MSB)					xxxx xxxx	นนนน นนนน
17h	CCP1CON	—	—	CCP1X	CCP1Y	CCP1M3	CCP1M2	CCP1M1	CCP1M0	00 0000	00 0000
1Bh ⁽⁴⁾	CCPR2L	Capture/0	Compare/P\	VM2 (LSB)	1		1			xxxx xxxx	นนนน นนนน
1Ch ⁽⁴⁾	CCPR2H	Capture/0	Compare/P\		xxxx xxxx	นนนน นนนน					
1Dh ⁽⁴⁾	CCP2CON	-	—	CCP2X	CCP2Y	CCP2M3	CCP2M2	CCP2M1	CCP2M0	00 0000	00 0000

TABLE 10-5: REGISTERS ASSOCIATED WITH PWM AND TIMER2

 Legend:
 x = unknown, u = unchanged, - = unimplemented locations read as '0'. Shaded cells are not used in this mode.

 Note
 1:
 These bits are associated with the USART module, which is implemented on the PIC16C63/R63/65/65A/R65/66/67 only.

2: Bits PSPIE and PSPIF are reserved on the PIC16C62/62A/R62/63/R63/66, always maintain these bits clear.

3: The PIR1<6> and PIE1<6> bits are reserved, always maintain these bits clear.

4: These registers are associated with the CCP2 module, which is only implemented on the PIC16C63/R63/65/65A/R65/66/67.

11.2 <u>SPI Mode for PIC16C62/62A/R62/63/</u> R63/64/64A/R64/65/65A/R65

This section contains register definitions and operational characteristics of the SPI module for the PIC16C62, PIC16C62A, PIC16CR62, PIC16C63, PIC16CR63, PIC16C64A, PIC16CR64, PIC16CR64, PIC16C65, PIC16C65A, PIC16CR65.

FIGURE 11-1: SSPSTAT: SYNC SERIAL PORT STATUS REGISTER (ADDRESS 94h)

U-0	U-0	R-0	B-0	B-0	R-0	B-0	B-0	
_	_	D/A	P	S	R/W	UA	BF	R = Readable bit
bit7			1			<u>I</u>	bit0	W = Writable bit U = Unimplemented bit, read as '0' - n =Value at POR reset
bit 7-6:	Unimpl	emented	Read as	'0'				
bit 5:	1 = Indi	cates that	the last b	,) d or transmit d or transmit			
bit 4:	1 = Indi		a stop bi	has been	cleared when detected last			abled, SSPEN is cleared) T)
bit 3:	1 = Indi		a start bi	t has been	cleared wher detected last			abled, SSPEN is cleared) T)
bit 2:	This bit	holds the o the next ad	R/W bit i	ation (I ² C r nformation stop bit, or	following the	e last addre	ess match. T	his bit is valid from the address
bit 1:	1 = Indi	cates that	the user	it I ² C mode needs to up to be upda	odate the add	dress in the	SSPADD re	egister
bit 0:	BF: Buf	fer Full St	atus bit					
	1 = Rec		olete, SSF	es) PBUF is full SSPBUF is				
	1 = Trar		ogress, S	SPBUF is f PBUF is err				

13.5.1 INT INTERRUPT

External interrupt on RB0/INT pin is edge triggered: either rising if edge select bit INTEDG (OPTION<6>) is set, or falling, if bit INTEDG is clear. When a valid edge appears on the RB0/INT pin, flag bit INTF (INTCON<1>) is set. This interrupt can be disabled by clearing enable bit INTE (INTCON<4>). The INTF bit must be cleared in software in the interrupt service routine before re-enabling this interrupt. The INT interrupt can wake the processor from SLEEP, if enable bit INTE was set prior to going into SLEEP. The status of global enable bit GIE decides whether or not the processor branches to the interrupt vector following wake-up. See Section 13.8 for details on SLEEP mode.

13.5.2 TMR0 INTERRUPT

An overflow (FFh \rightarrow 00h) in the TMR0 register will set flag bit T0IF (INTCON<2>). The interrupt can be enabled/disabled by setting/clearing enable bit T0IE (INTCON<5>) (Section 7.0).

13.5.3 PORTB INTERRUPT ON CHANGE

An input change on PORTB<7:4> sets flag bit RBIF (INTCON<0>). The interrupt can be enabled/disabled by setting/clearing enable bit RBIE (INTCON<4>) (Section 5.2).

Note: For the PIC16C61/62/64/65, if a change on the I/O pin should occur when the read operation is being executed (start of the Q2 cycle), then flag bit RBIF may not get set.

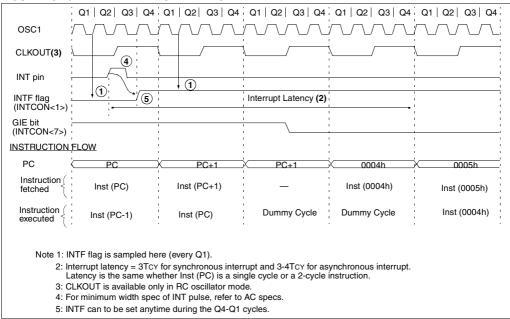
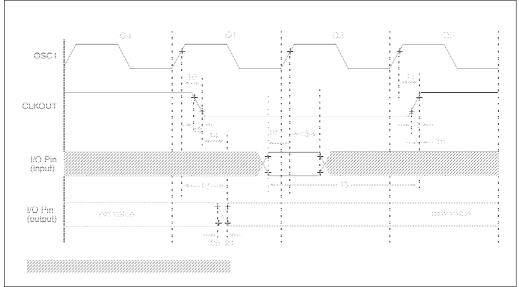


FIGURE 13-19: INT PIN INTERRUPT TIMING

Applicable Devices 61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

FIGURE 15-3: CLKOUT AND I/O TIMING



CLKOUT AND I/O TIMING REQUIREMENTS TABLE 15-3:

Parameter No.	Sym	Characteristic		Min	Тур†	Max	Units	Conditions
10*	TosH2ckL	OSC1↑ to CLKOUT↓		—	15	30	ns	Note 1
11*	TosH2ckH	OSC1↑ to CLKOUT↑		_	15	30	ns	Note 1
12*	TckR	CLKOUT rise time		_	5	15	ns	Note 1
13*	TckF	CLKOUT fall time		_	5	15	ns	Note 1
14*	TckL2ioV	CLKOUT ↓ to Port out va	alid	_		0.5TCY + 20	ns	Note 1
15*	TioV2ckH	Port in valid before CLKC) TUC	0.25Tcy + 25		_	ns	Note 1
16*	TckH2iol	Port in hold after CLKOU	IT ↑	0		_	ns	Note 1
17*	TosH2ioV	OSC1 [↑] (Q1 cycle) to Po	rt out valid	_		80 - 100	ns	
18*	TosH2iol	OSC1 [↑] (Q2 cycle) to Por (I/O in hold time)	rt input invalid	TBD	I	_	ns	
19*	TioV2osH	Port input valid to OSC1 time)	↑ (I/O in setup	TBD		—	ns	
20*	TioR	Port output rise time	PIC16 C 61	_	10	25	ns	
			PIC16LC61	_		60	ns	
21*	TioF	Port output fall time	PIC16 C 61	_	10	25	ns	
			PIC16LC61	_		60	ns	
22††*	Tinp	RB0/INT pin high or low	RB0/INT pin high or low time			—	ns	
23††*	Trbp	RB7:RB4 change int high	n or low time	20		_	ns	

These parameters are characterized but not tested.

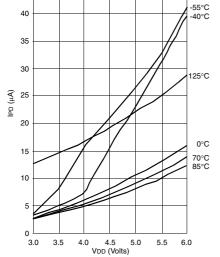
t Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

These parameters are asynchronous events not related to any internal clock edges. ††

Note 1: Measurements are taken in RC Mode where CLKOUT output is 4 x Tosc.

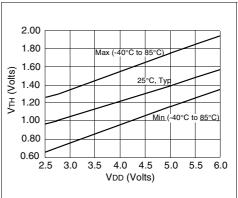
Applicable Devices 61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

FIGURE 16-8: MAXIMUM IPD vs. VDD WATCHDOG ENABLED*



*IPD, with Watchdog Timer enabled, has two components: The leakage current which increases with higher temperature and the operating current of the Watchdog Timer logic which increases with lower temperature. At -40°C, the latter dominates explaining the apparently anomalous behavior.





Applicable Devices 61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

NOTES:

Applicable Devices 61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

17.5 <u>Timing Diagrams and Specifications</u>



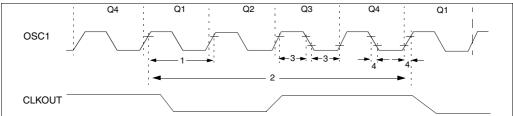


TABLE 17-2:	EXTERNAL CLOCK TIMING REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Тур†	Мах	Units	Conditions
	Fosc	External CLKIN Frequency	DC	I	4	MHz	XT and RC osc mode
		(Note 1)	DC	_	4	MHz	HS osc mode (-04)
			DC	_	10	MHz	HS osc mode (-10)
			DC	_	20	MHz	HS osc mode (-20)
			DC	_	200	kHz	LP osc mode
		Oscillator Frequency	DC	_	4	MHz	RC osc mode
		(Note 1)	0.1	_	4	MHz	XT osc mode
			4	_	20	MHz	HS osc mode
			5	_	200	kHz	LP osc mode
1	Tosc	External CLKIN Period	250		—	ns	XT and RC osc mode
		(Note 1)	250	_	_	ns	HS osc mode (-04)
			100	_	_	ns	HS osc mode (-10)
			50	_	_	ns	HS osc mode (-20)
			5	_	_	μs	LP osc mode
		Oscillator Period	250		_	ns	RC osc mode
		(Note 1)	250	_	10,000	ns	XT osc mode
			250	_	250	ns	HS osc mode (-04)
			100	_	250	ns	HS osc mode (-10)
			50	_	1,000	ns	HS osc mode (-20)
			5	_	_	μs	LP osc mode
2	Тсү	Instruction Cycle Time (Note 1)	200	Тсү	DC	ns	Tcy = 4/Fosc
3	TosL,	External Clock in (OSC1) High	100	_	_	ns	XT oscillator
	TosH	or Low Time	2.5	—	—	μs	LP oscillator
			15	—	—	ns	HS oscillator
4	TosR,	External Clock in (OSC1) Rise	—	-	25	ns	XT oscillator
	TosF	or Fall Time	_	—	50	ns	LP oscillator
			_	—	15	ns	HS oscillator

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Instruction cycle period (TcY) equals four times the input oscillator time-base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min." values with an external clock applied to the OSC1/CLKIN pin. When an external clock input is used, the "Max." cycle time limit is "DC" (no clock) for all devices.

Applicable Devices 61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67



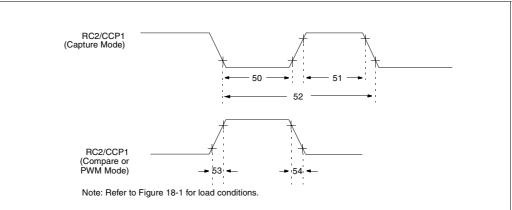


TABLE 18-6: CAPTURE/COMPARE/PWM REQUIREMENTS (CCP1)

Parameter No.	Sym	Characteristic			Min	Тур†	Max	Units	Conditions
50*	TccL	CCP1	No Prescaler		0.5Tcy + 20	—	—	ns	
		input low time	With Prescaler	PIC16 C 62A/R62/ 64A/R64	10	-	—	ns	
			PIC16 LC 62A/R62/ 64A/R64	20	-	—	ns		
51*	TccH	CCP1	No Prescaler		0.5Tcy + 20	_	_	ns	
		input high time	With Prescaler	PIC16 C 62A/R62/ 64A/R64	10	-	—	ns	
			PIC16 LC 62A/R62/ 64A/R64	20	-	—	ns		
52*	TccP	CCP1 input period			<u>3Tcy + 40</u> N	-	—	ns	N = prescale value (1,4 or 16)
53*	TccR	CCP1 output rise ti	ime	PIC16 C 62A/R62/ 64A/R64	_	10	25	ns	
				PIC16 LC 62A/R62/ 64A/R64	_	25	45	ns	
54*	TccF	CCP1 output fall time		PIC16 C 62A/R62/ 64A/R64	_	10	25	ns	
				PIC16 LC 62A/R62/ 64A/R64	_	25	45	ns	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Applicable Devices 61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

19.4 Timing Parameter Symbology

The timing parameter symbols have been created following one of the following formats:

1. TppS2pp	S		3. Tcc:s	 (I²C specifications only)
2. TppS			4. Ts	(I ² C specifications only)
Т				
F	Frequency		Т	Time
Lowercas	e letters (pp) and their me	anings:		
рр				
сс	CCP1		OSC	OSC1
ck	CLKOUT		rd	RD
CS	CS		rw	RD or WR
di	SDI		SC	SCK
do	SDO		SS	SS
dt	Data in		tO	TOCKI
io	I/O port		t1	T1CKI
mc	MCLR		wr	WR
Uppercas	e letters and their meaning	gs:		
S				
F	Fall		P	Period
Н	High		R	Rise
I	Invalid (Hi-impedance)		V	Valid
L	Low		Z	Hi-impedance
I ² C only				
AA	output access		High	High
BUF	Bus free		Low	Low
TCC:ST (l	² C specifications only)			
CC				
HD	Hold		SU	Setup
ST				
DAT	DATA input hold		STO	STOP condition
STA	START condition			
FIGURE 19	-1: LOAD CONDITIO	NS FOR DEVIC		SPECIFICATIONS
	Load condition	<u>n 1</u>		Load condition 2
		Vdd/2		
		ν DD/2 Φ		
		J		
		\geq RL		Pin CL
		\geq		
		-•		Vss
	Pin			
			= 464 Ω	
		Vss CL	= 50 pF	for all pins except OSC2/CLKOUT
				but including D and E outputs as ports
			15 pF	for OSC2 output

Applicable Devices 61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

19.5 <u>Timing Diagrams and Specifications</u>

FIGURE 19-2: EXTERNAL CLOCK TIMING

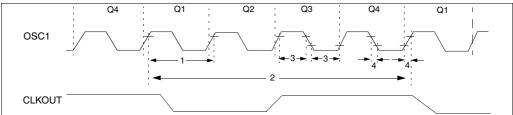


TABLE 19-2: EXTERNAL CLOCK TIMING REQUIREMENTS

arameter No.	Sym	Characteristic	Min	Тур†	Max	Units	Conditions
	Fosc	External CLKIN Frequency	DC	_	4	MHz	XT and RC osc mode
		(Note 1)	DC	_	4	MHz	HS osc mode (-04)
			DC	_	10	MHz	HS osc mode (-10)
			DC	_	20	MHz	HS osc mode (-20)
			DC	_	200	kHz	LP osc mode
		Oscillator Frequency	DC	_	4	MHz	RC osc mode
		(Note 1)	0.1	_	4	MHz	XT osc mode
			4	_	20	MHz	HS osc mode
			5	_	200	kHz	LP osc mode
1	Tosc	External CLKIN Period	250	_	_	ns	XT and RC osc mode
		(Note 1)	250	_	_	ns	HS osc mode (-04)
			100	_	_	ns	HS osc mode (-10)
			50	_	_	ns	HS osc mode (-20)
			5	_	_	μs	LP osc mode
		Oscillator Period	250	_	_	ns	RC osc mode
		(Note 1)	250	_	10,000	ns	XT osc mode
			250	_	250	ns	HS osc mode (-04)
			100	_	250	ns	HS osc mode (-10)
			50	_	250	ns	HS osc mode (-20)
			5	_	_	μs	LP osc mode
2	Тсү	Instruction Cycle Time (Note 1)	200	Тсү	DC	ns	Tcy = 4/Fosc
3	TosL,	External Clock in (OSC1) High or	50	_	_	ns	XT oscillator
	TosH	Low Time	2.5	_	—	μs	LP oscillator
			15	_	—	ns	HS oscillator
4	TosR,	External Clock in (OSC1) Rise or	—	_	25	ns	XT oscillator
	TosF	Fall Time	—	_	50	ns	LP oscillator
			_	_	15	ns	HS oscillator

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Instruction cycle period (TcY) equals four times the input oscillator time-base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min." values with an external clock applied to the OSC1/CLKIN pin. When an external clock input is used, the "Max." cycle time limit is "DC" (no clock) for all devices.

Applicable Devices	61	62	62A	B62	63	B63	64	64A	R64	65	65A	B65	66	67

		Standa	rd Operat	ing C	ondition	s (unle	ss otherwise stated)		
		Operatir	ng temper	ature	-40°	Ć≤T	$A \le +125^{\circ}C$ for extended,		
	RACTERISTICS				-40°	C ≤T	$A \le +85^{\circ}C$ for industrial and		
	RACIERISTICS		$0^{\circ}C \leq TA \leq +70^{\circ}C$ for com						
		Operatir Section	• •	Vdd	range as	describ	ed in DC spec Section 20.1 and		
Param	Characteristic	Sym	Min	Тур	Max	Units	Conditions		
No.				†					
	Output High Voltage								
D090	I/O ports (Note 3)	Vон	VDD-0.7	-	-	V	IOH = -3.0 mA, VDD = 4.5V, -40°С to +85°С		
D090A			VDD-0.7	-	-	V	IOH = -2.5 mA, VDD = 4.5V, -40°С to +125°С		
D092	OSC2/CLKOUT (RC osc config)		VDD-0.7	-	-	V	IOH = -1.3 mA, VDD = 4.5V, -40°С to +85°С		
D092A			VDD-0.7	-	-	V	IOH = -1.0 mA, VDD = 4.5V, -40°С to +125°С		
D150*	Open-Drain High Voltage	Vod	-	-	14	V	RA4 pin		
	Capacitive Loading Specs on Out- put Pins								
D100	OSC2 pin	Cosc ₂	-	-	15	pF	In XT, HS and LP modes when external clock is used to drive OSC1.		
D101	All I/O pins and OSC2 (in RC mode)	Cio	-	-	50	pF			
D102	SCL, SDA in I ² C mode	Cb	-	-	400	pF			

These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C6X be driven with external clock in RC mode.

 The leakage current on the MCLR/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as current sourced by the pin.

Applicable Devices 61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

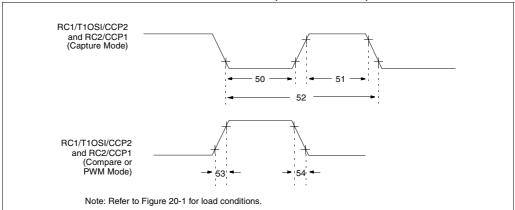


FIGURE 20-7: CAPTURE/COMPARE/PWM TIMINGS (CCP1 AND CCP2)

TABLE 20-6: CAPTURE/COMPARE/PWM REQUIREMENTS (CCP1 AND CCP2)

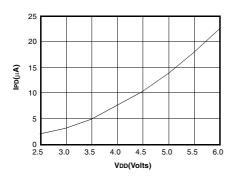
Parameter No.	Sym	Characteristic			Min	Тур†	Max	Units	Conditions
50*	TccL	CCP1 and CCP2	No Prescaler	No Prescaler		_	_	ns	
		input low time	With Prescaler	PIC16 C 63/65A	10	—		ns	
				PIC16LC63/65A	20	—		ns	
51*	TccH CCP1 and CCP2		No Prescaler		0.5TCY + 20	-		ns	
		input high time	With Prescaler	PIC16 C 63/65A	10	—		ns	
				PIC16 LC 63/65A	20	-		ns	
52*	TccP	CCP1 and CCP2 ir	CCP1 and CCP2 input period					ns	N = prescale value (1,4, or 16)
53*	TccR	CCP1 and CCP2 of	utput rise time	PIC16 C 63/65A	_	10	25	ns	
				PIC16 LC 63/65A	_	25	45	ns	
54*	TccF	CCP1 and CCP2 o	utput fall time	PIC16 C 63/65A	—	10	25	ns	
				PIC16 LC 63/65A	_	25	45	ns	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Applicable Devices 61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

FIGURE 23-3: TYPICAL IPD vs. VDD @ 25°C (WDT ENABLED, RC MODE)





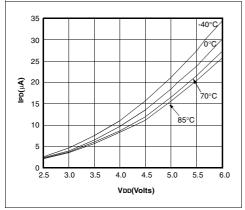
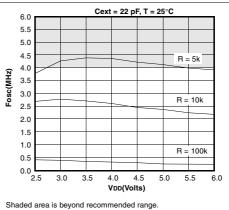
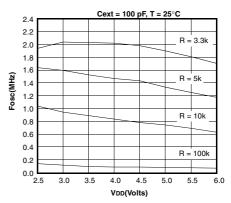


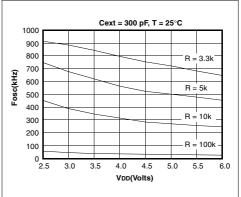
FIGURE 23-5: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD











APPENDIX F: PIC16/17 MICROCONTROLLERS

F.1 PIC12CXXX Family of Devices

		PIC12C508	PIC12C509	PIC12C671	PIC12C672
lock	Maximum Frequency of Operation (MHz)	4	4	4	4
emory	EPROM Program Memory	512 x 12	1024 x 12	1024 x 14	2048 x 14
emory	Data Memory (bytes)	25	41	128	128
	Timer Module(s)	TMR0	TMR0	TMR0	TMR0
eripherals	A/D Converter (8-bit) Channels		_	4	4
	Wake-up from SLEEP on pin change	Yes	Yes	Yes	Yes
	I/O Pins	5	5	5	5
	Input Pins	1	1	1	1
atures	Internal Pull-ups	Yes	Yes	Yes	Yes
	Voltage Range (Volts)	2.5-5.5	2.5-5.5	2.5-5.5	2.5-5.5
	In-Circuit Serial Programming	Yes	Yes	Yes	Yes
	Number of Instructions	33	33	35	35
	Packages	8-pin DIP, SOIC	8-pin DIP, SOIC	8-pin DIP, SOIC	8-pin DIP, SOIC

All PIC12C5XX devices have Power-on Reset, selectable Watchdog Timer, selectable code protect and high I/O current capability. All PIC12C5XX devices use serial programming with data pin GP1 and clock pin GP0.

F.2 PIC14C000 Family of Devices

		PIC14C000
Clock	Maximum Frequency of Operation (MHz)	20
	EPROM Program Memory (x14 words)	4K
Memory	Data Memory (bytes)	192
Memory	Timer Module(s)	TMR0 ADTMR
Peripherals	Serial Port(s) (SPI/I ² C, USART)	I ² C with SMBus Support
	Slope A/D Converter Channels	8 External; 6 Internal
	Interrupt Sources	11
	I/O Pins	22
	Voltage Range (Volts)	2.7-6.0
Features	In-Circuit Serial Programming	Yes
	Additional On-chip Features	Internal 4MHz Oscillator, Bandgap Reference,Temperature Sensor, Calibration Factors, Low Voltage Detector, SLEEP, HIBERNATE, Comparators with Programmable References (2)
	Packages	28-pin DIP (.300 mil), SOIC, SSOP

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Figure 12-2: Figure 12-3:	XMIT_MODE 104 TXSTA: Transmit Status and 105 Control Register (Address 98h) 105 RCSTA: Receive Status and 106 Control Register (Address 18h) 106 RX Pin Sampling Scheme (BRGH = 0) 110 PIC16C63/R63/65/65A/R65) 110 RX Pin Sampling Scheme (BRGH = 1) 110 RX Pin Sampling Scheme (BRGH = 1) 110 RX Pin Sampling Scheme (BRGH = 1) 110
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Figure 12-2: Figure 12-3: Figure 12-4:	XMIT_MODE 104 TXSTA: Transmit Status and 105 Control Register (Address 98h) 105 RCSTA: Receive Status and 106 Control Register (Address 18h) 106 RX Pin Sampling Scheme (BRGH = 0) 101 PIC16C63/R63/65/65A/R65) 110 RX Pin Sampling Scheme (BRGH = 1) 101 (PIC16C63/R63/65/65A/R65) 110 RX Pin Sampling Scheme (BRGH = 1) 101 RX Pin Sampling Scheme (BRGH = 0 or = 1) 110
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