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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

### Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	I <sup>2</sup> C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	33
Program Memory Size	14KB (8K x 14)
Program Memory Type	ОТР
EEPROM Size	-
RAM Size	368 x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 6V
Data Converters	-
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-QFP
Supplier Device Package	44-MQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16c67-20-pq

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

## 2.0 PIC16C6X DEVICE VARIETIES

A variety of frequency ranges and packaging options are available. Depending on application and production requirements, the proper device option can be selected using the information in the PIC16C6X Product Identification System section at the end of this data sheet. When placing orders, please use that page of the data sheet to specify the correct part number.

For the PIC16C6X family of devices, there are four device "types" as indicated in the device number:

- 1. **C**, as in PIC16**C**64. These devices have EPROM type memory and operate over the standard voltage range.
- 2. LC, as in PIC16LC64. These devices have EPROM type memory and operate over an extended voltage range.
- 3. **CR**, as in PIC16**CR**64. These devices have ROM program memory and operate over the standard voltage range.
- 4. LCR, as in PIC16LCR64. These devices have ROM program memory and operate over an extended voltage range.

#### 2.1 UV Erasable Devices

The UV erasable version, offered in CERDIP package is optimal for prototype development and pilot programs. This version can be erased and reprogrammed to any of the oscillator modes.

Microchip's PICSTART<sup>®</sup> Plus and PRO MATE<sup>®</sup> II programmers both support programming of the PIC16C6X.

#### 2.2 <u>One-Time-Programmable (OTP)</u> <u>Devices</u>

The availability of OTP devices is especially useful for customers who need the flexibility for frequent code updates and small volume applications.

The OTP devices, packaged in plastic packages, permit the user to program them once. In addition to the program memory, the configuration bits must also be programmed.

#### 2.3 <u>Quick-Turnaround-Production (QTP)</u> <u>Devices</u>

Microchip offers a QTP Programming Service for factory production orders. This service is made available for users who choose not to program a medium to high quantity of units and whose code patterns have stabilized. The devices are identical to the OTP devices but with all EPROM locations and configuration options already programmed by the factory. Certain code and prototype verification procedures apply before production shipments are available. Please contact your local Microchip Technology sales office for more details.

#### 2.4 <u>Serialized Quick-Turnaround</u> <u>Production (SQTP<sup>SM</sup>) Devices</u>

Microchip offers a unique programming service where a few user-defined locations in each device are programmed with different serial numbers. The serial numbers may be random, pseudo-random, or sequential.

Serial programming allows each device to have a unique number which can serve as an entry-code, password, or ID number.

ROM devices do not allow serialization information in the program memory space. The user may have this information programmed in the data memory space.

For information on submitting ROM code, please contact your regional sales office.

## 2.5 Read Only Memory (ROM) Devices

Microchip offers masked ROM versions of several of the highest volume parts, thus giving customers a low cost option for high volume, mature products.

For information on submitting ROM code, please contact your regional sales office.

Pin Name	DIP Pin#	PLCC Pin#	TQFP MQFP Pin#	Pin Type	Buffer Type	Description
						PORTD can be a bi-directional I/O port or parallel slave port for interfacing to a microprocessor bus.
RD0/PSP0	19	21	38	I/O	ST/TTL <sup>(6)</sup>	
RD1/PSP1	20	22	39	I/O	ST/TTL <sup>(6)</sup>	
RD2/PSP2	21	23	40	I/O	ST/TTL <sup>(6)</sup>	
RD3/PSP3	22	24	41	I/O	ST/TTL(6)	
RD4/PSP4	27	30	2	I/O	ST/TTL <sup>(6)</sup>	
RD5/PSP5	28	31	3	I/O	ST/TTL <sup>(6)</sup>	
RD6/PSP6	29	32	4	I/O	ST/TTL <sup>(6)</sup>	
RD7/PSP7	30	33	5	I/O	ST/TTL(6)	
						PORTE is a bi-directional I/O port.
RE0/RD	8	9	25	I/O	ST/TTL <sup>(6)</sup>	RE0 can also be read control for the parallel slave port.
RE1/WR	9	10	26	I/O	ST/TTL <sup>(6)</sup>	RE1 can also be write control for the parallel slave port.
RE2/CS	10	11	27	I/O	ST/TTL <sup>(6)</sup>	RE2 can also be select control for the parallel slave port.
Vss	12,31	13,34	6,29	Р	—	Ground reference for logic and I/O pins.
VDD	11,32	12,35	7,28	Р	_	Positive supply for logic and I/O pins.
NC	—	1,17,	12,13,	—	—	These pins are not internally connected. These pins should
		28,40	33,34			be left unconnected.
Legend: I = input	O = outp	ut	1/0	) = input/	output	P = power
	— = Not	used	T	TL = TTL	input	ST = Schmitt Trigger input

#### TABLE 3-3: PIC16C64/64A/R64/65/65A/R65/67 PINOUT DESCRIPTION (Cont.'d)

Note 1: Pin functions T1OSO and T1OSI are reversed on the PIC16C64.

2: CCP2 and the USART are not available on the PIC16C64/64A/R64.

3: This buffer is a Schmitt Trigger input when configured in RC oscillator mode and a CMOS input otherwise.

4: This buffer is a Schmitt Trigger input when configured as the external interrupt.

5: This buffer is a Schmitt Trigger input when used in serial programming mode.

6: This buffer is a Schmitt Trigger input when configured as general purpose I/O and a TTL input when used in the Parallel Slave Port mode (for interfacing to a microprocessor bus).

#### 4.2.2 SPECIAL FUNCTION REGISTERS:

The Special Function Registers are registers used by the CPU and peripheral modules for controlling the desired operation of the device. These registers are implemented as static RAM. The special function registers can be classified into two sets (core and peripheral). The registers associated with the "core" functions are described in this section and those related to the operation of the peripheral features are described in the section of that peripheral feature.

TABLE 4-1:	SPECIAL	FUNCTION	REGISTERS	FOR	THE	PIC16C61

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR	Value on all other resets <sup>(3)</sup>
Bank 0											
00h <sup>(1)</sup>	INDF	Addressing	this location	uses conten	ts of FSR to	address data	a memory (n	ot a physical	register)	0000 0000	0000 0000
01h	TMR0	Timer0 mod	lule's registe	r						xxxx xxxx	uuuu uuuu
02h <sup>(1)</sup>	PCL	Program Co	ounter's (PC)	Least Signif	icant Byte					0000 0000	0000 0000
03h <sup>(1)</sup>	STATUS	IRP <sup>(4)</sup>	RP1 <sup>(4)</sup>	RP0	TO	PD	Z	DC	С	0001 1xxx	000q quuu
04h <sup>(1)</sup>	FSR	Indirect data	a memory ad		xxxx xxxx	uuuu uuuu					
05h	PORTA	—	—	en read	x xxxx	u uuuu					
06h	PORTB	PORTB Dat	ta Latch whe	n written: PC	ORTB pins wh	nen read				xxxx xxxx	uuuu uuuu
07h	—	Unimpleme	nted							—	—
08h	-	Unimpleme	Inimplemented								—
09h	—	Unimpleme	nted		—	—					
0Ah <sup>(1,2)</sup>	PCLATH	—	—	—	Write Buffer	for the uppe	er 5 bits of the	e Program C	ounter	0 0000	0 0000
0Bh <sup>(1)</sup>	INTCON	GIE	—	TOIE	INTE	RBIE	TOIF	INTF	RBIF	0-00 000x	0-00 000u
Bank 1											
80h <sup>(1)</sup>	INDF	Addressing	this location	uses conten	ts of FSR to	address data	a memory (n	ot a physical	register)	0000 0000	0000 0000
81h	OPTION	RBPU	INTEDG	TOCS	TOSE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
82h <sup>(1)</sup>	PCL	Program Co	ounter's (PC)	Least Signif	icant Byte					0000 0000	0000 0000
83h <sup>(1)</sup>	STATUS	IRP <sup>(4)</sup>	RP1 <sup>(4)</sup>	RP0	TO	PD	Z	DC	С	0001 1xxx	000q quuu
84h <sup>(1)</sup>	FSR	Indirect data	a memory ad	dress pointe	r					xxxx xxxx	uuuu uuuu
85h	TRISA	—	—	—	PORTA Dat	a Direction F	Register			1 1111	1 1111
86h	TRISB	PORTB Dat	ta Direction C	Control Regis	ster					1111 1111	1111 1111
87h	-	Unimpleme	Unimplemented								—
88h	-	Unimpleme	Unimplemented								—
89h	-	Unimpleme	nted							—	—
8Ah <sup>(1,2)</sup>	PCLATH	—	—	—	Write Buffer	for the uppe	er 5 bits of th	e Program C	ounter	0 0000	0 0000
8Bh <sup>(1)</sup>	INTCON	GIE	_	TOIE	INTE	RBIE	TOIF	INTF	RBIF	0-00 000x	0-00 000u

 $\label{eq:logend: condition} \ensuremath{\mathsf{Legend: }} x = \mathsf{unknown}, u = \mathsf{unchanged}, q = \mathsf{value} \ensuremath{\, depends} \ensuremath{\, on \, condition}, \ensuremath{\, - \, = \, unimplemented \, locations \, read \, as \, '0'.$ 

Shaded locations are unimplemented and read as '0'

Note 1: These registers can be addressed from either bank.

2: The upper byte of the Program Counter (PC) is not directly accessible. PCLATH is a holding register for the PC whose contents are transferred to the upper byte of the program counter. (PC<12:8>)

3: Other (non power-up) resets include external reset through MCLR and the Watchdog Timer Reset.

4: The IRP and RP1 bits are reserved on the PIC16C61, always maintain these bits clear.

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other resets <sup>(3)</sup>
Bank 0											
00h <sup>(1)</sup>	INDF	Addressing	this location	uses conter	nts of FSR to	address data	a memory (n	ot a physical	register)	0000 0000	0000 0000
01h	TMR0	Timer0 mod	lule's registe	r						xxxx xxxx	uuuu uuuu
02h <sup>(1)</sup>	PCL	Program Co	ounter's (PC)	Least Signi	ficant Byte					0000 0000	0000 0000
03h <sup>(1)</sup>	STATUS	IRP <sup>(5)</sup>	RP1 <sup>(5)</sup>	RP0	TO	PD	z	DC	С	0001 1xxx	000q quuu
04h <sup>(1)</sup>	FSR	Indirect data	a memory ac		xxxx xxxx	uuuu uuuu					
05h	PORTA	_	PORTA Data Latch when written: PORTA pins when read								uu uuuu
06h	PORTB	PORTB Dat	ta Latch whe	n written: PC	ORTB pins wi	nen read				xxxx xxxx	uuuu uuuu
07h	PORTC	PORTC Da	TC Data Latch when written: PORTC pins when read								
08h	PORTD	PORTD Da	ta Latch whe	n written: PO	xxxx xxxx	uuuu uuuu					
09h	PORTE	_	_	_	—	_	RE2	RE1	RE0	xxx	uuu
0Ah <sup>(1,2)</sup>	PCLATH	_	— — Write Buffer for the upper 5 bits of the Program Counter								0 0000
0Bh <sup>(1)</sup>	INTCON	GIE	PEIE	TOIE	INTE	RBIE	TOIF	INTF	RBIF	0000 000x	0000 000u
0Ch	PIR1	PSPIF	(6)	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
0Dh	PIR2	_	—	_		—	—	—	CCP2IF	0	0
0Eh	TMR1L	Holding reg	ister for the I	east Signific	cant Byte of t	he 16-bit TM	R1 register			xxxx xxxx	uuuu uuuu
0Fh	TMR1H	Holding reg	ister for the I	Most Signific	ant Byte of th	ne 16-bit TMF	R1 register			xxxx xxxx	uuuu uuuu
10h	T1CON	_	_	T1CKPS1	T1CKPS0	T1OSCEN	T1SYNC	TMR1CS	TMR10N	00 0000	uu uuuu
11h	TMR2	Timer2 mod	lule's registe	r						0000 0000	0000 0000
12h	T2CON	_	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000 0000	-000 0000
13h	SSPBUF	Synchronou	us Serial Por	t Receive Bu	ffer/Transmit	Register				xxxx xxxx	uuuu uuuu
14h	SSPCON	WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0	0000 0000	0000 0000
15h	CCPR1L	Capture/Co	mpare/PWM	1 (LSB)						xxxx xxxx	uuuu uuuu
16h	CCPR1H	Capture/Co	mpare/PWM	1 (MSB)						xxxx xxxx	uuuu uuuu
17h	CCP1CON	-	—	CCP1X	CCP1Y	CCP1M3	CCP1M2	CCP1M1	CCP1M0	00 0000	00 0000
18h	RCSTA	SPEN	RX9	SREN	CREN	-	FERR	OERR	RX9D	0000 -00x	0000 -00x
19h	TXREG	USART Tra	nsmit Data F	legister						0000 0000	0000 0000
1Ah	RCREG	USART Red	USART Receive Data Register								0000 0000
1Bh	CCPR2L	Capture/Co	Capture/Compare/PWM2 (LSB)								uuuu uuuu
1Ch	CCPR2H	Capture/Co	mpare/PWM		xxxx xxxx	uuuu uuuu					
1Dh	CCP2CON	—	_	CCP2X	CCP2Y	CCP2M3	CCP2M2	CCP2M1	CCP2M0	00 0000	00 0000
1Eh-1Fh	—	Unimpleme	nted							—	—

#### TABLE 4-5: SPECIAL FUNCTION REGISTERS FOR THE PIC16C65/65A/R65

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented location read as '0'. Shaded locations are unimplemented, read as '0'.

Note 1: These registers can be addressed from either bank.

2: The upper byte of the Program Counter (PC) is not directly accessible. PCLATH is a holding register for the PC whose contents are transferred to the upper byte of the program counter. (PC<12:8>)

3: Other (non power-up) resets include external reset through MCLR and the Watchdog Timer reset.

4: The BOR bit is reserved on the PIC16C65, always maintain this bit set.

5: The IRP and RP1 bits are reserved on the PIC16C65/65A/R65, always maintain these bits clear.

6: PIE1<6> and PIR1<6> are reserved on the PIC16C65/65A/R65, always maintain these bits clear.

IADLE	4-0:	SPECIA			GISTERS			0000/07	(Cont.a	)	
Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other resets <sup>(3)</sup>
Bank 1											
80h <sup>(1)</sup>	INDF	Addressing	this location	uses conter	nts of FSR to	address data	a memory (n	ot a physical	register)	0000 0000	0000 0000
81h	OPTION	RBPU	INTEDG	TOCS	TOSE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
82h <sup>(1)</sup>	PCL	Program Co	ounter's (PC)	Least Sigr	nificant Byte					0000 0000	0000 0000
83h <sup>(1)</sup>	STATUS	IRP	RP1	RP0	TO	PD	Z	DC	С	0001 1xxx	000q quuu
84h <sup>(1)</sup>	FSR	Indirect data	a memory ac	1	xxxx xxxx	uuuu uuuu					
85h	TRISA	_	—		11 1111	11 1111					
86h	TRISB	PORTB Dat	ta Direction I		1111 1111	1111 1111					
87h	TRISC	PORTC Da	ta Direction I	Register						1111 1111	1111 1111
88h <sup>(5)</sup>	TRISD	PORTD Da	ta Direction I		1111 1111	1111 1111					
89h <sup>(5)</sup>	TRISE	IBF	IBF OBF IBOV PSPMODE — PORTE Data Direction Bits								0000 -111
8Ah <sup>(1,2)</sup>	PCLATH	—	—	—	Write Buffer	for the uppe	r 5 bits of the	e Program C	ounter	0 0000	0 0000
8Bh <sup>(1)</sup>	INTCON	GIE	PEIE	TOIE	INTE	RBIE	TOIF	INTF	RBIF	0000 000x	0000 000u
8Ch	PIE1	PSPIE <sup>(6)</sup>	(4)	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
8Dh	PIE2	—	—	—	_	—	—	—	CCP2IE	0	0
8Eh	PCON	—	—	—	_	—	_	POR	BOR	dd	uu
8Fh	_	Unimpleme	nted				•	•		_	_
90h	-	Unimpleme	nted							—	—
91h	-	Unimpleme	nted							—	—
92h	PR2	Timer2 Peri	od Register							1111 1111	1111 1111
93h	SSPADD	Synchronou	us Serial Por	t (I <sup>2</sup> C mode)	Address Reg	gister				0000 0000	0000 0000
94h	SSPSTAT	SMP	CKE	D/A	Р	S	R/W	UA	BF	0000 0000	0000 0000
95h	—	Unimpleme	nted							—	_
96h	-	Unimpleme	nted							—	—
97h	-	Unimpleme	nted							—	—
98h	TXSTA	CSRC	TX9	TXEN	SYNC	—	BRGH	TRMT	TX9D	0000 -010	0000 -010
99h	SPBRG	Baud Rate	Generator R	egister						0000 0000	0000 0000
9Ah	-	Unimpleme	nted							—	—
9Bh	—	Unimpleme	nted							-	-
9Ch	-	Unimpleme	nted							—	_
9Dh	-	Unimpleme	nted							—	—
9Eh	—	Unimpleme	nted							-	—
9Fh	-	Unimpleme	nted							-	—

TABLE 4-6: SPECIAL FUNCTION REGISTERS FOR THE PIC16C66/67 (Cont.'d)

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented location read as '0'. Shaded locations are unimplemented, read as '0'.

Note 1: These registers can be addressed from any bank.

2: The upper byte of the Program Counter (PC) is not directly accessible. PCLATH is a holding register for the PC whose contents are transferred to the upper byte of the program counter. (PC<12:8>)

3: Other (non power-up) resets include external reset through MCLR and the Watchdog Timer reset.

4: PIE1<6> and PIR1<6> are reserved on the PIC16C66/67, always maintain these bits clear.

5: PORTD, PORTE, TRISD, and TRISE are not implemented on the PIC16C66, read as '0'.

6: PSPIF (PIR1<7>) and PSPIE (PIE1<7>) are reserved on the PIC16C66, maintain these bits clear.

### FIGURE 4-15: PIE1 REGISTER FOR PIC16C65/65A/R65/67 (ADDRESS 8Ch)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0					
PSPIE	_	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	R = Readable bit				
bit7							bitO	W = Writable bit U = Unimplemented bit, read as '0' - n = Value at POR reset				
bit 7:	bit 7: <b>PSPIE:</b> Parallel Slave Port Read/Write Interrupt Enable bit 1 = Enables the PSP read/write interrupt 0 = Disables the PSP read/write interrupt											
bit 6:	Reserved: Always maintain this bit clear.											
bit 5:	<b>RCIE</b> : USART Receive Interrupt Enable bit 1 = Enables the USART receive interrupt 0 = Disables the USART receive interrupt											
bit 4:	TXIE: USART Transmit Interrupt Enable bit      1 = Enables the USART transmit interrupt      0 = Disables the USART transmit interrupt											
bit 3:	SSPIE: Syn 1 = Enable 0 = Disable	nchronous s the SSP es the SSP	Serial Port interrupt interrupt	Interrupt Er	nable bit							
bit 2:	CCP1IE: CCP1 Interrupt Enable bit 1 = Enables the CCP1 interrupt 0 = Disables the CCP1 interrupt											
bit 1:	TMR2IE: T 1 = Enable 0 = Disable	MR2 to PR s the TMR2 es the TMR	2 Match In 2 to PR2 m 2 to PR2 m	terrupt Enat atch interrup atch interru	ole bit pt ipt							
bit 0:	TMR1IE: T 1 = Enable 0 = Disable	MR1 Overf s the TMR es the TMR	low Interru 1 overflow i 1 overflow	ot Enable bi nterrupt interrupt	t							

#### 4.2.2.6 PIE2 REGISTER

Applicable Devices 61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

This register contains the CCP2 interrupt enable bit.

### FIGURE 4-20: PIE2 REGISTER (ADDRESS 8Dh)



## 11.0 SYNCHRONOUS SERIAL PORT (SSP) MODULE

#### 11.1 SSP Module Overview

The Synchronous Serial Port (SSP) module is a serial interface useful for communicating with other peripheral or microcontroller devices. These peripheral devices may be Serial EEPROMs, shift registers, display drivers, A/D converters, etc. The SSP module can operate in one of two modes:

- Serial Peripheral Interface (SPI)
- Inter-Integrated Circuit (I<sup>2</sup>C)

The SSP module in  $l^2$ C mode works the same in all PIC16C6X devices that have an SSP module. However the SSP Module in SPI mode has differences between the PIC16C66/67 and the other PIC16C6X devices.

The register definitions and operational description of SPI mode has been split into two sections because of the differences between the PIC16C66/67 and the other PIC16C6X devices. The default reset values of both the SPI modules is the same regardless of the device:

11.2	SPI Mode for PIC16C62/62A/R62/63/R63/64	1/
	64A/R64/65/65A/R65 8	4
11.3	SPI Mode for PIC16C66/67 8	9
11.4	I <sup>2</sup> C™ Overview9	5
11.5	SSP I <sup>2</sup> C Operation	9

Refer to Application Note AN578, "Use of the SSP Module in the  $I^2C$  Multi-Master Environment."

## 12.0 UNIVERSAL SYNCHRONOUS ASYNCHRONOUS RECEIVER TRANSMITTER (USART) MODULE

#### Applicable Devices

61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

The Universal Synchronous Asynchronous Receiver Transmitter (USART) module is one of the two serial I/O modules. (USART is also known as a Serial Communications Interface or SCI) The USART can be configured as a full duplex asynchronous system that can communicate with peripheral devices such as CRT terminals and personal computers, or it can be configured as a half duplex synchronous system that can communicate with peripheral devices such as A/D or D/A integrated circuits, Serial EEPROMs etc.

The USART can be configured in the following modes:

- Asynchronous (full duplex)
- Synchronous Master (half duplex)
- Synchronous Slave (half duplex)

Bit SPEN (RCSTA<7>) and bits TRISC<7:6> have to be set in order to configure pins RC6/TX/CK and RC7/RX/DT as the Universal Synchronous Asynchronous Receiver Transmitter.

### FIGURE 12-1: TXSTA: TRANSMIT STATUS AND CONTROL REGISTER (ADDRESS 98h)

R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R-1	R/W-0	
CSRC	TX9	TXEN	SYNC	—	BRGH	TRMT	TX9D	R = Readable bit
bit7							bit0	W = Writable bit U = Unimplemented bit, read as '0' - n =Value at POR reset
bit 7:	CSRC: Clo	ck Source	Select bit					<u>,</u>
	Asynchron Don't care	<u>ous mode</u>						
	Synchrono 1 = Master 0 = Slave n	<u>us mode</u> mode (Clo node (Cloo	ock generat k from exte	ed interna rnal sourc	lly from BR æ)	G)		
bit 6:	<b>TX9</b> : 9-bit 1 = Selects 0 = Selects	Transmit Ei 9-bit trans 8-bit trans	nable bit smission smission					
bit 5:	<b>TXEN</b> : Tran 1 = Transm 0 = Transm Note: SRE	nsmit Enab iit enabled iit disabled N/CREN o	le bit verrides Τλ	EN in SYI	NC mode.			
bit 4:	SYNC: US 1 = Synchr 0 = Asynch	ART Mode onous moo ironous mo	Select bit de ode					
bit 3:	Unimplem	ented: Re	ad as '0'					
bit 2:	BRGH: Hig	h Baud Ra	ate Select b	it				
	Asynchron 1 = High sp	<u>ous mode</u> beed						
	Note:	For the P experienc higher ba mation or	IC16C63/F e a high ra ud rate tha use the PI	63/65/65/ te of recein BRGH = C16C66/6	VR65 the a ive errors. I = 0 can sup 7.	synchrond t is recom port, refer	ous high spe mended that to the devic	ed mode (BRGH = 1) may BRGH = 0. If you desire a e errata for additional infor-
	0 = Low sp	eed						
	Synchrono Unused in	<u>us mode</u> this mode						
bit 1:	<b>TRMT</b> : Trai 1 = TSR er 0 = TSR fu	nsmit Shift npty II	Register S	tatus bit				
bit 0:	<b>TX9D</b> : 9th	bit of trans	mit data. C	an be pari	ty bit.			

#### 12.4 USART Synchronous Slave Mode

#### Applicable Devices

#### 61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

Synchronous Slave Mode differs from Master Mode in the fact that the shift clock is supplied externally at the CK pin (instead of being supplied internally in master mode). This allows the device to transfer or receive data while in SLEEP mode. Slave mode is entered by clearing bit CSRC (TXSTA<7>).

#### 12.4.1 USART SYNCHRONOUS SLAVE TRANSMIT

The operation of the synchronous master and slave modes are identical except in the case of the SLEEP mode.

If two words are written to the TXREG and then the SLEEP instruction is executed, the following will occur:

- a) The first word will immediately transfer to the TSR register and transmit.
- b) The second word will remain in TXREG register.
- c) Flag bit TXIF will not be set.
- d) When the first word has been shifted out of TSR, the TXREG register will transfer the second word to the TSR and flag bit TXIF will now be set.
- e) If enable bit TXIE is set, the interrupt will wake the chip from SLEEP and if the global interrupt is enabled, the program will branch to the interrupt vector (0004h).

Steps to follow when setting up Synchronous Slave Transmission:

- 1. Enable the synchronous slave serial port by setting bits SYNC and SPEN, and clearing bit CSRC.
- 2. Clear bits CREN and SREN.
- 3. If interrupts are desired, then set enable bit  $\mathsf{TXIE}.$
- 4. If 9-bit transmission is desired, then set bit TX9.
- 5. Enable the transmission by setting bit TXEN.
- 6. If 9-bit transmission is selected, the ninth bit should be loaded in bit TX9D.
- 7. Start transmission by loading data to the TXREG register.

#### 12.4.2 USART SYNCHRONOUS SLAVE RECEPTION

The operation of the synchronous master and slave modes is identical except in the case of the SLEEP mode. Also, enable bit SREN is a don't care in slave mode.

If receive is enabled by setting bit CREN prior to the SLEEP instruction, then a word may be received during SLEEP. On completely receiving the word, the RSR register will transfer the data to the RCREG register and if enable bit RCIE is set, the interrupt generated will wake the chip from SLEEP. If the global interrupt is enabled, the program will branch to the interrupt vector (0004h).

Steps to follow when setting up a Synchronous Slave Reception:

- Enable the synchronous master serial port by setting bits SYNC and SPEN, and clearing bit CSRC.
- 2. If interrupts are desired, then set enable bit RCIE.
- 3. If 9-bit reception is desired, then set bit RX9.
- 4. To enable reception, set enable bit CREN.
- Flag bit RCIF will be set when reception is complete, and an interrupt will be generated if enable bit RCIE was set.
- Read the RCSTA register to get the ninth bit (if enabled) and determine if any error occurred during reception.
- 7. Read the 8-bit received data by reading the RCREG register.
- 8. If any error occurred, clear the error by clearing enable bit CREN.

#### 13.2.3 EXTERNAL CRYSTAL OSCILLATOR CIRCUIT

Either a prepackaged oscillator can be used or a simple oscillator circuit with TTL gates can be built. Prepackaged oscillators provide a wide operating range and better stability. A well-designed crystal oscillator will provide good performance with TTL gates. Two types of crystal oscillator circuits can be used; one with series resonance, or one with parallel resonance.

Figure 13-6 shows implementation of a parallel resonant oscillator circuit. The circuit is designed to use the fundamental frequency of the crystal. The 74AS04 inverter performs the 180-degree phase shift that a parallel oscillator requires. The 4.7 k $\Omega$  resistor provides the negative feedback for stability. The 10 k $\Omega$  potentiometer biases the 74AS04 in the linear region. This could be used for external oscillator designs.

#### FIGURE 13-6: EXTERNAL PARALLEL RESONANT CRYSTAL OSCILLATOR CIRCUIT



Figure 13-7 shows a series resonant oscillator circuit. This circuit is also designed to use the fundamental frequency of the crystal. The inverter performs a 180-degree phase shift in a series resonant oscillator circuit. The 330 k $\Omega$  resistors provide the negative feedback to bias the inverters in their linear region.

#### FIGURE 13-7: EXTERNAL SERIES RESONANT CRYSTAL OSCILLATOR CIRCUIT



#### 13.2.4 RC OSCILLATOR

For timing insensitive applications the RC device option offers additional cost savings. The RC oscillator frequency is a function of the supply voltage, the resistor (Rext) and capacitor (Cext) values, and the operating temperature. In addition to this, the oscillator frequency will vary from unit to unit due to normal process parameter variation. Furthermore, the difference in lead frame capacitance between package types will also affect the oscillation frequency, especially for low Cext values. The user also needs to take into account variation due to tolerance of external R and C components used. Figure 13-8 shows how the RC combination is connected to the PIC16CXX. For Rext values below 2.2 kΩ, the oscillator operation may become unstable or stop completely. For very high Rext values (e.g. 1 M $\Omega$ ), the oscillator becomes sensitive to noise, humidity and leakage. Thus, we recommend keeping Rext between 3 k $\Omega$  and 100 k $\Omega$ .

Although the oscillator will operate with no external capacitor (Cext = 0 pF), we recommend using values above 20 pF for noise and stability reasons. With no or small external capacitance, the oscillation frequency can vary dramatically due to changes in external capacitances, such as PCB trace capacitance or package lead frame capacitance.

See characterization data for desired device for RC frequency variation from part to part due to normal process variation. The variation is larger for larger R (since leakage current variation will affect RC frequency more for large R) and for smaller C (since variation of input capacitance will affect RC frequency more).

See characterization data for desired device for variation of oscillator frequency due to VDD for given Rext/ Cext values as well as frequency variation due to operating temperature for given R, C, and VDD values.

The oscillator frequency, divided by 4, is available on the OSC2/CLKOUT pin, and can be used for test purposes or to synchronize other logic (see Figure 3-5 for waveform).



#### FIGURE 13-8: RC OSCILLATOR MODE

#### 13.4 Power-on Reset (POR), Power-up Timer (PWRT), Oscillator Start-up Timer (OST) and Brown-out Reset (BOR)

Applicable Devices 61|62|62A|R62|63|R63|64|64A|R64|65|65A|R65|66|67

#### 13.4.1 POWER-ON RESET (POR)

A Power-on Reset pulse is generated on-chip when VDD rise is detected (in the range of 1.5V - 2.1V). To take advantage of the POR, just tie the  $\overline{MCLR}/VPP$  pin directly (or through a resistor) to VDD. This will eliminate external RC components usually needed to create a Power-on Reset. A maximum rise time for VDD is required. See Electrical Specifications for details.

When the device starts normal operation (exits the reset condition), device operating parameters (voltage, frequency, temperature, ...) must be met to ensure operation. If these conditions are not met, the device must be held in reset until the operating conditions are met. Brown-out Reset may be used to meet the startup conditions.

For additional information, refer to Application Note AN607, "*Power-up Trouble Shooting*."

#### 13.4.2 POWER-UP TIMER (PWRT)

The Power-up Timer provides a fixed 72 ms nominal time-out on power-up only, from POR. The Power-up Timer operates on an internal RC oscillator. The chip is kept in reset as long as PWRT is active. The PWRT's time delay allows VDD to rise to an acceptable level. A configuration bit is provided to enable/disable the PWRT.

The power-up time delay will vary from chip to chip due to VDD, temperature, and process variation. See DC parameters for details.

#### 13.4.3 OSCILLATOR START-UP TIMER (OST)

The Oscillator Start-up Timer (OST) provides 1024 oscillator cycle (from OSC1 input) delay after the PWRT delay is over. This ensures the crystal oscillator or resonator has started and stabilized.

The OST time-out is invoked only for XT, LP and HS modes and only on Power-on Reset or wake-up from SLEEP.

#### 13.4.4 BROWN-OUT RESET (BOR)

#### Applicable Devices

61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

A configuration bit, BODEN, can disable (if clear/programmed) or enable (if set) the Brown-out Reset circuitry. If VDD falls below 4.0V (parameter D005 in Electrical Specification section) for greater than parameter #34 (see Electrical Specification section), the brown-out situation will reset the chip. A reset may not occur if VDD falls below 4.0V for less than parameter #34. The chip will remain in Brown-out Reset until VDD rises above BVDD. The Power-up Timer will now be invoked and will keep the chip in RESET an additional 72 ms. If VDD drops below BVDD while the Power-up Timer is running, the chip will go back into a Brown-out Reset and the Power-up Timer will be initialized. Once VDD rises above BVDD, the Power-up Timer will execute a 72 ms time delay. The Power-up Timer should always be enabled when Brown-out Reset is enabled. Figure 13-10 shows typical brown-out situations.



#### FIGURE 13-10: BROWN-OUT SITUATIONS

IORWF	Inclusive	e OR W	with f					
Syntax:	[ label ]	IORWF	f,d					
Operands:	$0 \le f \le 12$ $d \in [0,1]$	27						
Operation:	(W) .OR.	$(f) \rightarrow (d)$	estinatio	on)				
Status Affected:	Z							
Encoding:	00	0100	dfff	ffff				
Description:	Inclusive ( ter 'f'. If 'd' W register back in re	Inclusive OR the W register with regis- ter 'f'. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'.						
Words:	1							
Cycles:	1							
Q Cycle Activity:	Q1	Q2	Q3	Q4				
	Decode	Read register 'f'	Process data	Write to destination				
Example	IORWF		RESULT	, 0				
	Before In	struction	1					
		RESULT	= 0x	13				
	After Instruction							
		RESULT	= 0x	13				
		W	= 0x	93				
		Z	= 1					

MOVLW	Move Literal to W								
Syntax:	[ label ]	MOVLW	/ k						
Operands:	$0 \le k \le 25$	55							
Operation:	$k \to (W)$								
Status Affected:	None								
Encoding:	11	00xx	kkkk	kkkk					
Description:	The eight bit literal 'k' is loaded into W register. The don't cares will assemble as 0's.								
Words:	1								
Cycles:	1								
Q Cycle Activity:	Q1	Q2	Q3	Q4					
	Decode	Read literal 'k'	Process data	Write to W					
Example	MOVLW After Inst	0x5A							
		W =	0x5A						

-

MOVF	Move f							
Syntax:	[ label ]	MOVF	f,d					
Operands:	$\begin{array}{l} 0 \leq f \leq 12 \\ d \in [0,1] \end{array}$	7						
Operation:	$(f) \rightarrow (des$	stination	)					
Status Affected:	Z							
Encoding:	00	1000	dfff	ffff				
Description:	The contents of register f is moved to a destination dependant upon the status of d. If $d = 0$ , destination is W register. If $d = 1$ , the destination is file register f itself. $d = 1$ is useful to test a file register fer since status flag Z is affected.							
Words:	1							
Cycles:	1							
Q Cycle Activity:	Q1	Q2	Q3	Q4				
	Decode	Read register 'f'	Process data	Write to destination				
Example	MOVF	FSR,	0					
	After Instruction W = value in FSR register Z = 1							

MOVWF	Move W	to f				
Syntax:	[ label ]	MOVW	Ff			
Operands:	$0 \leq f \leq 127$					
Operation:	$(W) \rightarrow (f)$					
Status Affected:	None					
Encoding:	00	0000	lfff	ffff		
Description:	Move data 'f'.	from W r	egister to	register		
Words:	1					
Cycles:	1					
Q Cycle Activity:	Q1	Q2	Q3	Q4		
	Decode	Read register 'f'	Process data	Write register 'f'		
Example	MOVWF	OPTIC	DN_REG			
	Before In	struction		-		
		W	= 0xFI = 0x4f	=		
	After Inst	ruction		_		
		OPTION W	= 0x4f = 0x4f	=		
		••	0.411			

Applicable Devices 61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

## FIGURE 15-5: TIMER0 EXTERNAL CLOCK TIMINGS



## TABLE 15-5: TIMER0 EXTERNAL CLOCK REQUIREMENTS

Parameter No.	Sym	Characteristic		Min	Тур†	Max	Units	Conditions	
40*	Tt0H	Tt0H T0CKI High Pulse Width	No Prescaler	0.5Tcy + 20	_	_	ns	Must also meet	
			With Prescaler	10	—		ns	parameter 42	
41*	Tt0L	T0CKI Low Pulse Width	No Prescaler	0.5TCY + 20	—		ns	Must also meet	
			With Prescaler	10	_		ns	parameter 42	
42*	Tt0P T0CKI Period No Prescaler Tcy + 40			ns	N = prescale value				
			With Prescaler	Greater of: 20 ns or <u>Tcy + 40</u> N	_		ns	(2, 4,, 256)	

These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

### Applicable Devices 61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

## FIGURE 17-10: I<sup>2</sup>C BUS DATA TIMING



#### TABLE 17-10: I<sup>2</sup>C BUS DATA REQUIREMENTS

Parameter No.	Sym	Characteristic		Min	Max	Units	Conditions
100	Тнідн	Clock high time	100 kHz mode	4.0	—	μs	Device must operate at a mini- mum of 1.5 MHz
			400 kHz mode	0.6	_	μs	Device must operate at a mini- mum of 10 MHz
			SSP Module	1.5Tcy	_		
101	TLOW	Clock low time	100 kHz mode	4.7	_	μs	Device must operate at a mini- mum of 1.5 MHz
			400 kHz mode	1.3	_	μs	Device must operate at a mini- mum of 10 MHz
			SSP Module	1.5Tcy	_		
102	TR	SDA and SCL rise	100 kHz mode	—	1000	ns	
		time	400 kHz mode	20 + 0.1Cb	300	ns	Cb is specified to be from 10 to 400 pF
103	TF	SDA and SCL fall time	100 kHz mode	_	300	ns	
			400 kHz mode	20 + 0.1Cb	300	ns	Cb is specified to be from 10 to 400 pF
90	TSU:STA	START condition	100 kHz mode	4.7	_	μS	Only relevant for repeated
		setup time	400 kHz mode	0.6	_	μs	START condition
91	THD:STA	START condition hold	100 kHz mode	4.0	_	μS	After this period the first clock
		time	400 kHz mode	0.6	—	μs	pulse is generated
106	THD:DAT	Data input hold time	100 kHz mode	0	—	ns	
			400 kHz mode	0	0.9	μs	
107	TSU:DAT	Data input setup time	100 kHz mode	250	_	ns	Note 2
			400 kHz mode	100	-	ns	
92	Tsu:sto	STOP condition setup	100 kHz mode	4.7	—	μs	
		time	400 kHz mode	0.6	—	μs	
109	ΤΑΑ	Output valid from	100 kHz mode	—	3500	ns	Note 1
		clock	400 kHz mode	—	-	ns	
110	TBUF	Bus free time	100 kHz mode	4.7	—	μS	Time the bus must be free
			400 kHz mode	1.3	_	μs	start
	Cb	Bus capacitive loading		—	400	pF	

Note 1: As a transmitter, the device must provide this internal minimum delay time to bridge the undefined region (min. 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

2: A fast-mode (400 kHz) I<sup>2</sup>C-bus device can be used in a standard-mode (100 kHz) I<sup>2</sup>C-bus system, but the requirement tsu;DAT ≥ 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line TR max. + tsu;DAT = 1000 + 250 = 1250 ns (according to the standard-mode I<sup>2</sup>C bus specification) before the SCL line is released.

## Applicable Devices 61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67





#### TABLE 18-8: SPI MODE REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Тур†	Max	Units	Conditions
70*	TssL2scH, TssL2scL	$\overline{SS}\downarrow$ to SCK $\downarrow$ or SCK $\uparrow$ input	Тсү	_	I	ns	
71*	TscH	SCK input high time (slave mode)	TCY + 20	_	_	ns	
72*	TscL	SCK input low time (slave mode)	TCY + 20	_		ns	
73*	TdiV2scH, TdiV2scL	Setup time of SDI data input to SCK edge	50	—		ns	
74*	TscH2diL, TscL2diL	Hold time of SDI data input to SCK edge	50	_	_	ns	
75*	TdoR	SDO data output rise time	_	10	25	ns	
76*	TdoF	SDO data output fall time	_	10	25	ns	
77*	TssH2doZ	$\overline{\text{SS}}\uparrow$ to SDO output hi-impedance	10	_	50	ns	
78*	TscR	SCK output rise time (master mode)	_	10	25	ns	
79*	TscF	SCK output fall time (master mode)	_	10	25	ns	
80*	TscH2doV, TscL2doV	SDO data output valid after SCK edge	_	_	50	ns	

These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Applicable Devices 61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67



## FIGURE 21-7: CAPTURE/COMPARE/PWM TIMINGS (CCP1 AND CCP2)

#### TABLE 21-6: CAPTURE/COMPARE/PWM REQUIREMENTS (CCP1 AND CCP2)

Param No.	Sym	Characteristic			Min	Тур†	Max	Units	Conditions
50*	TccL	CCP1 and CCP2	No Prescaler		0.5Tcy + 20	_	_	ns	
		input low time	With Prescaler	PIC16CR63/R65	10	—	—	ns	
				PIC16LCR63/R65	20	—	_	ns	
51*	51* TccH CCP1 and CCP2		No Prescaler		0.5TCY + 20	—	_	ns	
	input high time	With Prescaler	PIC16 <b>CR</b> 63/R65	10		_	ns		
				PIC16LCR63/R65	20		_	ns	
52*	TccP	CCP1 and CCP2 input period			<u>3Tcy + 40</u> N		-	ns	N = prescale value (1,4, or 16)
53*	TccR	CCP1 and CCP2 output rise time		PIC16 <b>CR</b> 63/R65	—	10	25	ns	
				PIC16LCR63/R65	—	25	45	ns	
54*	TccF	CCP1 and CCP2 output fall time		PIC16 <b>CR</b> 63/R65	—	10	25	ns	
				PIC16LCR63/R65	_	25	45	ns	

\* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

## 24.0 PACKAGING INFORMATION

## 24.1 <u>18-Lead Plastic Dual In-line (300 mil) (P)</u>

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Package Group: Plastic Dual In-Line (PLA)								
	Millimeters			Inches				
Symbol	Min	Мах	Notes	Min	Мах	Notes		
α	0°	10°		0°	10°			
А	_	4.064		_	0.160			
A1	0.381	_		0.015	_			
A2	3.048	3.810		0.120	0.150			
В	0.355	0.559		0.014	0.022			
B1	1.524	1.524	Reference	0.060	0.060	Reference		
С	0.203	0.381	Typical	0.008	0.015	Typical		
D	22.479	23.495		0.885	0.925			
D1	20.320	20.320	Reference	0.800	0.800	Reference		
E	7.620	8.255		0.300	0.325			
E1	6.096	7.112		0.240	0.280			
e1	2.489	2.591	Typical	0.098	0.102	Typical		
eA	7.620	7.620	Reference	0.300	0.300	Reference		
eB	7.874	9.906		0.310	0.390			
L	3.048	3.556		0.120	0.140			
N	18	18		18	18			
S	0.889	-		0.035	-			
S1	0.127	_		0.005	_			

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- 1. Set your modem to 8-bit, No parity, and One stop (8N1). This is not the normal CompuServe setting which is 7E1.
- 2. Dial your local CompuServe access number.
- 3. Depress the **<Enter>** key and a garbage string will appear because CompuServe is expecting a 7E1 setting.
- Type +, depress the <Enter> key and "Host Name:" will appear.
- 5. Type MCHIPBBS, depress the **<Enter>** key and you will be connected to the Microchip BBS.

In the United States, to find the CompuServe phone number closest to you, set your modem to 7E1 and dial (800) 848-4480 for 300-2400 baud or (800) 331-7166 for 9600-14400 baud connection. After the system responds with "Host Name:", type NETWORK, depress the **<Enter**> key and follow CompuServe's directions.

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