What is "**Embedded - Microcontrollers**"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "**Embedded - Microcontrollers**"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	I²C, SPI
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	22
Program Memory Size	3.5KB (2K x 14)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 6V
Data Converters	-
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lc62a-04-so

PIC16C6X

TABLE 4-5: SPECIAL FUNCTION REGISTERS FOR THE PIC16C65/65A/R65

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other resets[3]
Bank 0											
00h[1]	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								0000 0000	0000 0000
01h	TMR0	Timer0 module's register								xxxx xxxx	uuuu uuuu
02h[1]	PCL	Program Counter's (PC) Least Significant Byte								0000 0000	0000 0000
03h[1]	STATUS	IRP[5]	RP1[5]	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	000q quuu
04h[1]	FSR	Indirect data memory address pointer								xxxx xxxx	uuuu uuuu
05h	PORTA	—	—	PORTA Data Latch when written: PORTA pins when read						--xx xxxx	--uu uuuu
06h	PORTB	PORTB Data Latch when written: PORTB pins when read								xxxx xxxx	uuuu uuuu
07h	PORTC	PORTC Data Latch when written: PORTC pins when read								xxxx xxxx	uuuu uuuu
08h	PORTD	PORTD Data Latch when written: PORTD pins when read								xxxx xxxx	uuuu uuuu
09h	PORTE	—	—	—	—	—	RE2	RE1	RE0	---- -xxx	---- -uuu
0Ah[1,2]	PCLATH	—	—	—	Write Buffer for the upper 5 bits of the Program Counter					---0 0000	---0 0000
0Bh[1]	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000u
0Ch	PIR1	PSPIF	(6)	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
0Dh	PIR2	—	—	—	—	—	—	—	CCP2IF	---- ---0	---- ---0
0Eh	TMR1L	Holding register for the Least Significant Byte of the 16-bit TMR1 register								xxxx xxxx	uuuu uuuu
0Fh	TMR1H	Holding register for the Most Significant Byte of the 16-bit TMR1 register								xxxx xxxx	uuuu uuuu
10h	T1CON	—	—	T1CKPS1	T1CKPS0	T1OSCEN	$\overline{T1SYNC}$	TMR1CS	TMR1ON	--00 0000	--uu uuuu
11h	TMR2	Timer2 module's register								0000 0000	0000 0000
12h	T2CON	—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000 0000	-000 0000
13h	SSPBUF	Synchronous Serial Port Receive Buffer/Transmit Register								xxxx xxxx	uuuu uuuu
14h	SSPCON	WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0	0000 0000	0000 0000
15h	CCPR1L	Capture/Compare/PWM1 (LSB)								xxxx xxxx	uuuu uuuu
16h	CCPR1H	Capture/Compare/PWM1 (MSB)								xxxx xxxx	uuuu uuuu
17h	CCP1CON	—	—	CCP1X	CCP1Y	CCP1M3	CCP1M2	CCP1M1	CCP1M0	--00 0000	--00 0000
18h	RCSTA	SPEN	RX9	SREN	CREN	—	FERR	OERR	RX9D	0000 -00x	0000 -00x
19h	TXREG	USART Transmit Data Register								0000 0000	0000 0000
1Ah	RCREG	USART Receive Data Register								0000 0000	0000 0000
1Bh	CCPR2L	Capture/Compare/PWM2 (LSB)								xxxx xxxx	uuuu uuuu
1Ch	CCPR2H	Capture/Compare/PWM2 (MSB)								xxxx xxxx	uuuu uuuu
1Dh	CCP2CON	—	—	CCP2X	CCP2Y	CCP2M3	CCP2M2	CCP2M1	CCP2M0	--00 0000	--00 0000
1Eh-1Fh	—	Unimplemented								—	—

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented location read as '0'.
Shaded locations are unimplemented, read as '0'.

Note 1: These registers can be addressed from either bank.
2: The upper byte of the Program Counter (PC) is not directly accessible. PCLATH is a holding register for the PC whose contents are transferred to the upper byte of the program counter. (PC<12:8>)
3: Other (non power-up) resets include external reset through $\overline{MCLR}$ and the Watchdog Timer reset.
4: The $\overline{BOR}$ bit is reserved on the PIC16C65, always maintain this bit set.
5: The IRP and RP1 bits are reserved on the PIC16C65/65A/R65, always maintain these bits clear.
6: PIE1<6> and PIR1<6> are reserved on the PIC16C65/65A/R65, always maintain these bits clear.

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TABLE 4-5: **SPECIAL FUNCTION REGISTERS FOR THE PIC16C65/65A/R65 (Cont.'d)**

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other resets[3]
Bank 1											
80h[1]	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								0000 0000	0000 0000
81h	OPTION	$\overline{RBPU}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
82h[1]	PCL	Program Counter's (PC) Least Significant Byte								0000 0000	0000 0000
83h[1]	STATUS	IRP[5]	RP1[5]	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	000q quuu
84h[1]	FSR	Indirect data memory address pointer								xxxx xxxx	uuuu uuuu
85h	TRISA	—	—	PORTA Data Direction Register						--11 1111	--11 1111
86h	TRISB	PORTB Data Direction Register								1111 1111	1111 1111
87h	TRISC	PORTC Data Direction Register								1111 1111	1111 1111
88h	TRISD	PORTD Data Direction Register								1111 1111	1111 1111
89h	TRISE	IBF	OBF	IBOV	PSPMODE	—	PORTE Data Direction Bits			0000 -111	0000 -111
8Ah[1,2]	PCLATH	—	—	—	Write Buffer for the upper 5 bits of the Program Counter					---0 0000	---0 0000
8Bh[1]	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000u
8Ch	PIE1	PSPIE	(6)	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
8Dh	PIE2	—	—	—	—	—	—	—	CCP2IE	---- ---0	---- ---0
8Eh	PCON	—	—	—	—	—	—	$\overline{POR}$	$\overline{BOR}$[4]	---- --qq	---- --uu
8Fh	—	Unimplemented								—	—
90h	—	Unimplemented								—	—
91h	—	Unimplemented								—	—
92h	PR2	Timer2 Period Register								1111 1111	1111 1111
93h	SSPADD	Synchronous Serial Port (I²C mode) Address Register								0000 0000	0000 0000
94h	SSPSTAT	—	—	D/$\overline{A}$	P	S	R/$\overline{W}$	UA	BF	--00 0000	--00 0000
95h	—	Unimplemented								—	—
96h	—	Unimplemented								—	—
97h	—	Unimplemented								—	—
98h	TXSTA	CSRC	TX9	TXEN	SYNC	—	BRGH	TRMT	TX9D	0000 -010	0000 -010
99h	SPBRG	Baud Rate Generator Register								0000 0000	0000 0000
9Ah	—	Unimplemented								—	—
9Bh	—	Unimplemented								—	—
9Ch	—	Unimplemented								—	—
9Dh	—	Unimplemented								—	—
9Eh	—	Unimplemented								—	—
9Fh	—	Unimplemented								—	—

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented location read as '0'.
Shaded locations are unimplemented, read as '0'.

Note 1:   These registers can be addressed from either bank.
2:   The upper byte of the Program Counter (PC) is not directly accessible. PCLATH is a holding register for the PC whose contents are transferred to the upper byte of the program counter. (PC<12:8>)
3:   Other (non power-up) resets include external reset through $\overline{MCLR}$ and the Watchdog Timer reset.
4:   The $\overline{BOR}$ bit is reserved on the PIC16C65, always maintain this bit set.
5:   The IRP and RP1 bits are reserved on the PIC16C65/65A/R65, always maintain these bits clear.
6:   PIE1<6> and PIR1<6> are reserved on the PIC16C65/65A/R65, always maintain these bits clear.

PIC16C6X

5.6   I/O Programming Considerations

Applicable Devices

61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67

5.6.1   BI-DIRECTIONAL I/O PORTS

Any instruction which writes, operates internally as a read followed by a write operation. The `BCF` and `BSF` instructions, for example, read the register into the CPU, execute the bit operation and write the result back to the register. Caution must be used when these instructions are applied to a port with both inputs and outputs defined. For example, a `BSF` operation on bit5 of PORTB will cause all eight bits of PORTB to be read into the CPU. Then the `BSF` operation takes place on bit5 and PORTB is written to the output latches. If another bit of PORTB is used as a bi-directional I/O pin (e.g., bit0) and it is defined as an input at this time, the input signal present on the pin itself would be read into the CPU and rewritten to the data latch of this particular pin, overwriting the previous content. As long as the pin stays in the input mode, no problem occurs. However, if bit0 is switched into output mode later on, the content of the data latch may now be unknown.

Reading the port register, reads the values of the port pins. Writing to the port register writes the value to the port latch. When using read-modify-write instructions (ex. `BCF`, `BSF`, etc.) on a port, the value of the port pins is read, the desired operation is done to this value, and this value is then written to the port latch.

Example 5-4 shows the effect of two sequential read-modify-write instructions on an I/O port.

EXAMPLE 5-4:   READ-MODIFY-WRITE INSTRUCTIONS ON AN I/O PORT
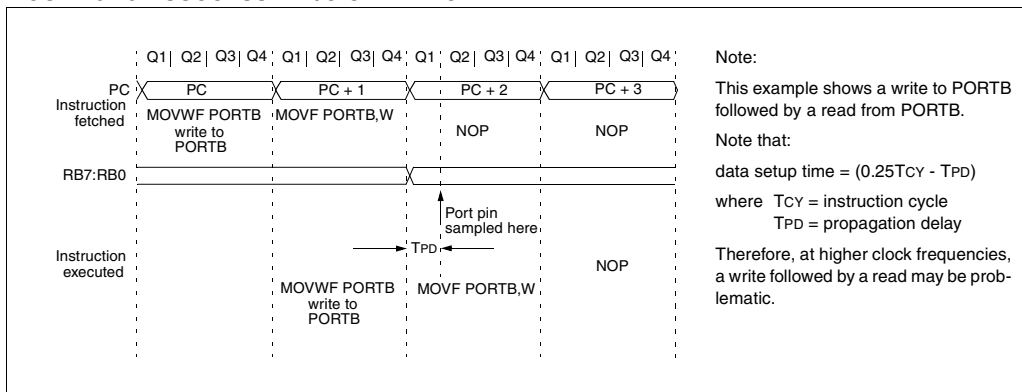
```
;Initial PORT settings: PORTB<7:4> Inputs
;                       PORTB<3:0> Outputs
;PORTB<7:6> have external pull-ups and are
;not connected to other circuitry
;
;                  PORT latch    PORT pins
;                  ----------    ---------
  BCF PORTB, 7    ; 01pp pppp    11pp pppp
  BCF PORTB, 6    ; 10pp pppp    11pp pppp
  BSF STATUS, RP0 ;
  BCF TRISB, 7    ; 10pp pppp    11pp pppp
  BCF TRISB, 6    ; 10pp pppp    10pp pppp
;
;Note that the user may have expected the
;pin values to be 00pp pppp. The 2nd BCF
;caused RB7 to be latched as the pin value
;(high).
```

A pin actively outputting a Low or High should not be driven from external devices at the same time in order to change the level on this pin ("wired-or", "wired-and"). The resulting high output currents may damage the chip.

5.6.2   SUCCESSIVE OPERATIONS ON I/O PORTS

The actual write to an I/O port happens at the end of an instruction cycle, whereas for reading, the data must be valid at the beginning of the instruction cycle (Figure 5-10). Therefore, care must be exercised if a write followed by a read operation is carried out on the same I/O port. The sequence of instructions should be such to allow the pin voltage to stabilize (load dependent) before the next instruction which causes that file to be read into the CPU is executed. Otherwise, the previous state of that pin may be read into the CPU rather than the new state. When in doubt, it is better to separate these instructions with a `NOP` or another instruction not accessing this I/O port.

FIGURE 5-10:   SUCCESSIVE I/O OPERATION

Note:

This example shows a write to PORTB followed by a read from PORTB.

Note that:

data setup time = $(0.25 T_{CY} - T_{PD})$

where T_{CY} = instruction cycle
       T_{PD} = propagation delay

Therefore, at higher clock frequencies, a write followed by a read may be problematic.

7.2   Using Timer0 with External Clock

Applicable Devices

61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67

When an external clock input is used for Timer0, it must meet certain requirements. The requirements ensure the external clock can be synchronized with the internal phase clock (TOSC). Also, there is a delay in the actual incrementing of Timer0 after synchronization.

7.2.1   EXTERNAL CLOCK SYNCHRONIZATION

When no prescaler is used, the external clock input is the same as the prescaler output. The synchronization of T0CKI with the internal phase clocks is accomplished by sampling the prescaler output on the Q2 and Q4 cycles of the internal phase clocks (Figure 7-5). Therefore, it is necessary for T0CKI to be high for at least 2Tosc (and a small RC delay of 20 ns) and low for at least 2Tosc (and a small RC delay of 20 ns). Refer to the electrical specification of the desired device.

When a prescaler is used, the external clock input is divided by the asynchronous ripple-counter type prescaler so that the prescaler output is symmetrical. For the external clock to meet the sampling requirement, the ripple-counter must be taken into account. Therefore, it is necessary for T0CKI to have a period of at least 4Tosc (and a small RC delay of 40 ns) divided by the prescaler value. The only requirement on T0CKI high and low time is that they do not violate the minimum pulse width requirement of 10 ns. Refer to parameters 40, 41 and 42 in the electrical specification of the desired device.

7.2.2   TIMER0 INCREMENT DELAY

Since the prescaler output is synchronized with the internal clocks, there is a small delay from the time the external clock edge occurs to the time the Timer0 module is actually incremented. Figure 7-5 shows the delay from the external clock edge to the timer incrementing.

FIGURE 7-5:   TIMER0 TIMING WITH EXTERNAL CLOCK
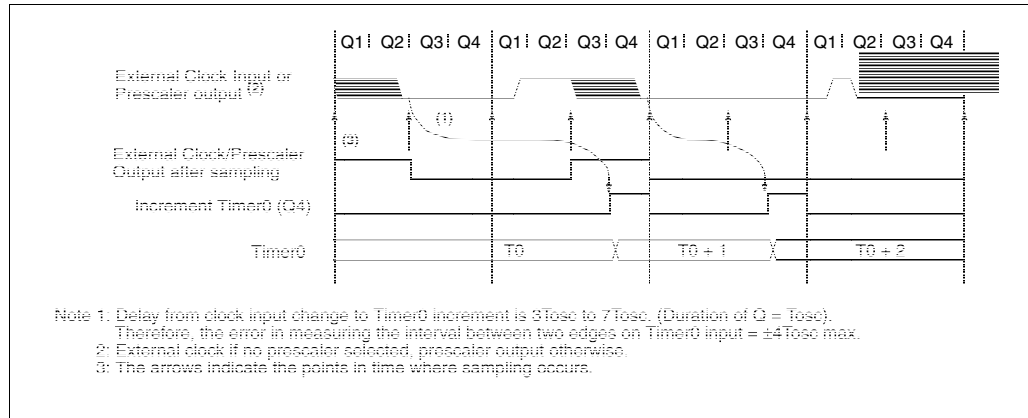
FIGURE 10-1: CCP1CON REGISTER (ADDRESS 17h) / CCP2CON REGISTER (ADDRESS 1Dh)

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	CCPxX	CCPxY	CCPxM3	CCPxM2	CCPxM1	CCPxM0

bit7   bit0

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n = Value at POR reset

bit 7-6: **Unimplemented:** Read as '0'

bit 5-4: **CCPxX:CCPxY**: PWM Least Significant bits
<u>Capture Mode</u>
Unused
<u>Compare Mode</u>
Unused
<u>PWM Mode</u>
These bits are the two LSbs of the PWM duty cycle. The eight MSbs are found in CCPRxL.

bit 3-0: **CCPxM3:CCPxM0**: CCPx Mode Select bits
`0000` = Capture/Compare/PWM off (resets CCPx module)
`0100` = Capture mode, every falling edge
`0101` = Capture mode, every rising edge
`0110` = Capture mode, every 4th rising edge
`0111` = Capture mode, every 16th rising edge
`1000` = Compare mode, set output on match (bit CCPxIF is set)
`1001` = Compare mode, clear output on match (bit CCPxIF is set)
`1010` = Compare mode, generate software interrupt on match (bit CCPxIF is set, CCPx pin is unaffected)
`1011` = Compare mode, trigger special event (CCPxIF bit is set; CCP1 resets TMR1; CCP2 resets TMR1)
`11xx` = PWM mode

10.1 Capture Mode

Applicable Devices

61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67

In Capture mode, CCPR1H:CCPR1L captures the 16-bit value of the TMR1 register when an event occurs on pin RC2/CCP1 (Figure 10-2). An event is defined as:

- Every falling edge
- Every rising edge
- Every 4th rising edge
- Every 16th rising edge

An event is selected by control bits CCP1M3:CCP1M0 (CCP1CON<3:0>). When a capture is made, the interrupt request flag bit CCP1IF (PIR1<2>) is set. It must be cleared in software. If another capture occurs before the value in register CCPR1 is read, the old captured value will be lost.

10.1.1 CCP PIN CONFIGURATION

In Capture mode, the RC2/CCP1 pin should be configured as an input by setting the TRISC<2> bit.

Note:	If the RC2/CCP1 pin is configured as an output, a write to PORTC can cause a capture condition.

FIGURE 10-2: CAPTURE MODE OPERATION BLOCK DIAGRAM
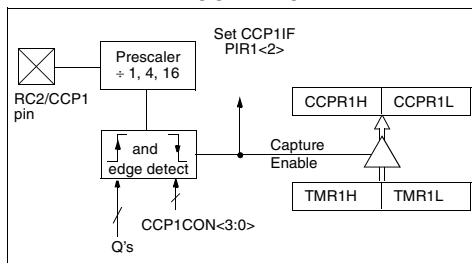
10.1.2 TIMER1 MODE SELECTION

Timer1 must be running in Timer mode or Synchronized Counter mode for the CCP module to use the capture feature. In Asynchronous Counter mode, the capture operation may not work consistently.

10.1.3 SOFTWARE INTERRUPT

When the Capture event is changed, a false capture interrupt may be generated. The user should clear enable bit CCP1IE (PIE1<2>) to avoid false interrupts and should clear flag bit CCP1IF following any such change in operating mode.

Applicable Devices																
61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67

PIC16C6X

11.5 SSP I²C Operation

The SSP module in I²C mode fully implements all slave functions, except general call support, and provides interrupts on start and stop bits in hardware to facilitate firmware implementations of the master functions. The SSP module implements the standard mode specifications as well as 7-bit and 10-bit addressing. Two pins are used for data transfer. These are the RC3/SCK/SCL pin, which is the clock (SCL), and the RC4/SDI/SDA pin, which is the data (SDA). The user must configure these pins as inputs or outputs through the TRISC<4:3> bits. The SSP module functions are enabled by setting SSP Enable bit SSPEN (SSPCON<5>).

FIGURE 11-24: SSP BLOCK DIAGRAM (I²C MODE)
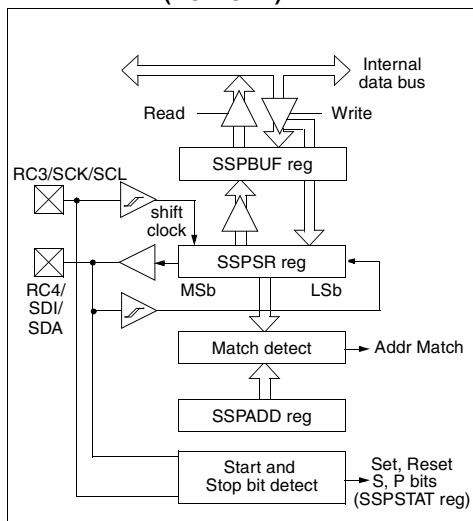
The SSP module has five registers for I²C operation. These are the:

• SSP Control Register (SSPCON)
• SSP Status Register (SSPSTAT)
• Serial Receive/Transmit Buffer (SSPBUF)
• SSP Shift Register (SSPSR) - Not directly accessible
• SSP Address Register (SSPADD)

The SSPCON register allows control of the I²C operation. Four mode selection bits (SSPCON<3:0>) allow one of the following I²C modes to be selected:

• I²C Slave mode (7-bit address)
• I²C Slave mode (10-bit address)
• I²C Slave mode (7-bit address), with start and stop bit interrupts enabled
• I²C Slave mode (10-bit address), with start and stop bit interrupts enabled
• I²C Firmware controlled Master Mode, slave is idle

Selection of any I²C mode, with the SSPEN bit set, forces the SCL and SDA pins to be open drain, provided these pins are programmed to inputs by setting the appropriate TRISC bits.

The SSPSTAT register gives the status of the data transfer. This information includes detection of a START or STOP bit, specifies if the received byte was data or address if the next byte is the completion of 10-bit address, and if this will be a read or write data transfer. The SSPSTAT register is read only.

The SSPBUF is the register to which transfer data is written to or read from. The SSPSR register shifts the data in or out of the device. In receive operations, the SSPBUF and SSPSR create a doubled buffered receiver. This allows reception of the next byte to begin before reading the last byte of received data. When the complete byte is received, it is transferred to the SSPBUF register and flag bit SSPIF is set. If another complete byte is received before the SSPBUF register is read, a receiver overflow has occurred and bit SSPOV (SSPCON<6>) is set and the byte in the SSPSR is lost.

The SSPADD register holds the slave address. In 10-bit mode, the user first needs to write the high byte of the address (`1111 0 A9 A8 0`). Following the high byte address match, the low byte of the address needs to be loaded (A7:A0).

NOTES:

INCFSZ	**Increment f, Skip if 0**
Syntax:	[*label*] INCFSZ f,d
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$
Operation:	(f) + 1 → (destination), skip if result = 0
Status Affected:	None
Encoding:	00 1111 dfff ffff
Description:	The contents of register 'f' are incremented. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'. If the result is 1, the next instruction is executed. If the result is 0, a NOP is executed instead making it a 2T$_{CY}$ instruction.
Words:	1
Cycles:	1(2)

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process data	Write to destination

If Skip: (2nd Cycle)

Q1	Q2	Q3	Q4
No-Operation	No-Operation	No-Operation	No-Operation

Example

```
HERE        INCFSZ    CNT, 1
            GOTO      LOOP
CONTINUE •
            •
            •
```

Before Instruction
    PC   =   address HERE
After Instruction
    CNT   =   CNT + 1
    if CNT=   0,
    PC   =   address CONTINUE
    if CNT≠   0,
    PC   =   address HERE +1

IORLW	**Inclusive OR Literal with W**
Syntax:	[*label*] IORLW k
Operands:	$0 \leq k \leq 255$
Operation:	(W) .OR. k → (W)
Status Affected:	Z
Encoding:	11 1000 kkkk kkkk
Description:	The contents of the W register is OR'ed with the eight bit literal 'k'. The result is placed in the W register.
Words:	1
Cycles:	1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read literal 'k'	Process data	Write to W

Example

```
IORLW    0x35
```

Before Instruction
    W   =   0x9A
After Instruction
    W   =   0xBF
    Z   =   1

SLEEP

Syntax: [*label*] SLEEP

Operands: None

Operation: 00h → WDT,
0 → WDT prescaler,
1 → $\overline{TO}$,
0 → $\overline{PD}$

Status Affected: $\overline{TO}$, $\overline{PD}$

Encoding:

00	0000	0110	0011

Description: The power-down status bit, $\overline{PD}$ is cleared. Time-out status bit, $\overline{TO}$ is set. Watchdog Timer and its prescaler are cleared.
The processor is put into SLEEP mode with the oscillator stopped. See Section 13.8 for more details.

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	No-Operation	No-Operation	Go to Sleep

Example: `SLEEP`

SUBLW   Subtract W from Literal

Syntax: [*label*] SUBLW k

Operands: $0 \leq k \leq 255$

Operation: k - (W) → (W)

Status Affected: C, DC, Z

Encoding:

11	110x	kkkk	kkkk

Description: The W register is subtracted (2's complement method) from the eight bit literal 'k'. The result is placed in the W register.

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read literal 'k'	Process data	Write to W

Example 1:   `SUBLW   0x02`

Before Instruction

W	=	1
C	=	?
Z	=	?

After Instruction

W	=	1
C	=	1; result is positive
Z	=	0

Example 2:   Before Instruction

W	=	2
C	=	?
Z	=	?

After Instruction

W	=	0
C	=	1; result is zero
Z	=	1

Example 3:   Before Instruction

W	=	3
C	=	?
Z	=	?

After Instruction

W	=	0xFF
C	=	0; result is negative
Z	=	0

PIC16C6X

17.4   Timing Parameter Symbology

The timing parameter symbols have been created following one of the following formats:

1. TppS2ppS
2. TppS
3. TCC:ST   (I^2C specifications only)
4. Ts   (I^2C specifications only)

T		
F	Frequency	T	Time

Lowercase letters (pp) and their meanings:

pp				
cc	CCP1	osc	OSC1
ck	CLKOUT	rd	$\overline{RD}$
cs	$\overline{CS}$	rw	$\overline{RD}$ or $\overline{WR}$
di	SDI	sc	SCK
do	SDO	ss	$\overline{SS}$
dt	Data in	t0	T0CKI
io	I/O port	t1	T1CKI
mc	$\overline{MCLR}$	wr	$\overline{WR}$

Uppercase letters and their meanings:

S				
F	Fall	P	Period
H	High	R	Rise
I	Invalid (Hi-impedance)	V	Valid
L	Low	Z	Hi-impedance
I^2C only			
AA	output access	High	High
BUF	Bus free	Low	Low

TCC:ST (I^2C specifications only)

CC				
HD	Hold	SU	Setup
ST			
DAT	DATA input hold	STO	STOP condition
STA	START condition		

FIGURE 17-1:   LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS

$R_L = 464\Omega$

$C_L = 50$ pF   for all pins except OSC2/CLKOUT
but including D and E outputs as ports

15 pF   for OSC2 output

Note 1:   PORTD and PORTE are not implemented on the PIC16C62.
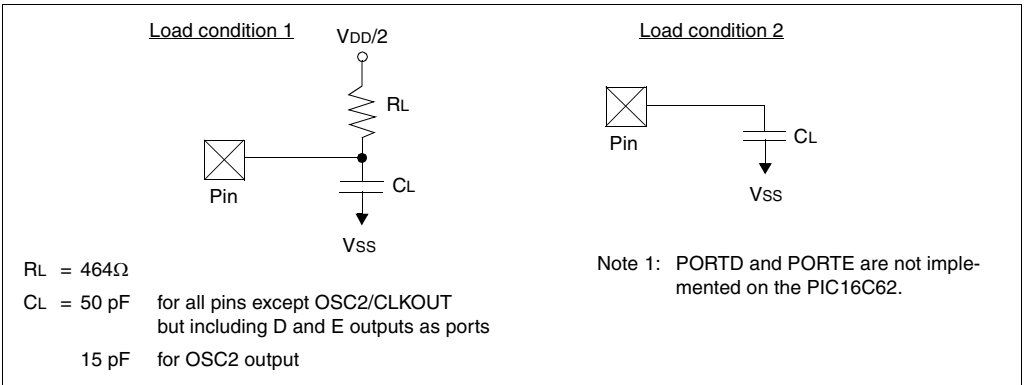
PIC16C6X

FIGURE 17-9: I²C BUS START/STOP BITS TIMING

Note: Refer to Figure 17-1 for load conditions
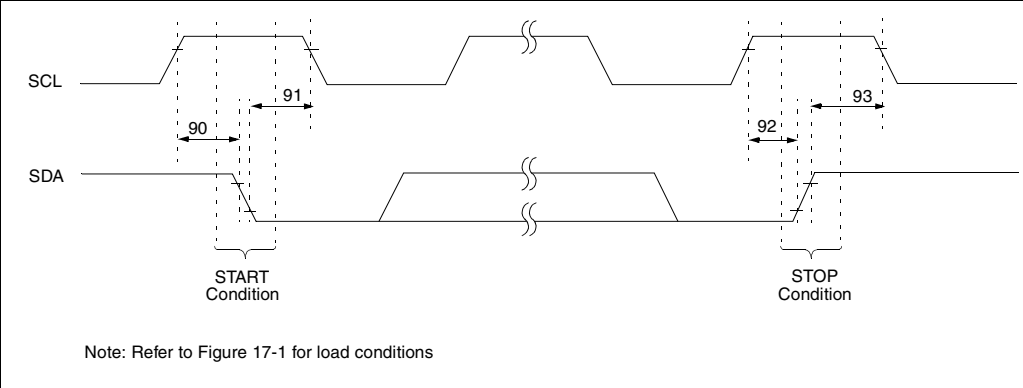
TABLE 17-9: I²C BUS START/STOP BITS REQUIREMENTS

Parameter No.	Sym	Characteristic		Min	Typ	Max	Units	Conditions
90	$T_{SU:STA}$	START condition	100 kHz mode	4700	—	—	ns	Only relevant for repeated START condition
		Setup time	400 kHz mode	600	—	—		
91	$T_{HD:STA}$	START condition	100 kHz mode	4000	—	—	ns	After this period the first clock pulse is generated
		Hold time	400 kHz mode	600	—	—		
92	$T_{SU:STO}$	STOP condition	100 kHz mode	4700	—	—	ns	
		Setup time	400 kHz mode	600	—	—		
93	$T_{HD:STO}$	STOP condition	100 kHz mode	4000	—	—	ns	
		Hold time	400 kHz mode	600	—	—		

FIGURE 19-4: **RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING**

Note: Refer to Figure 19-1 for load conditions.
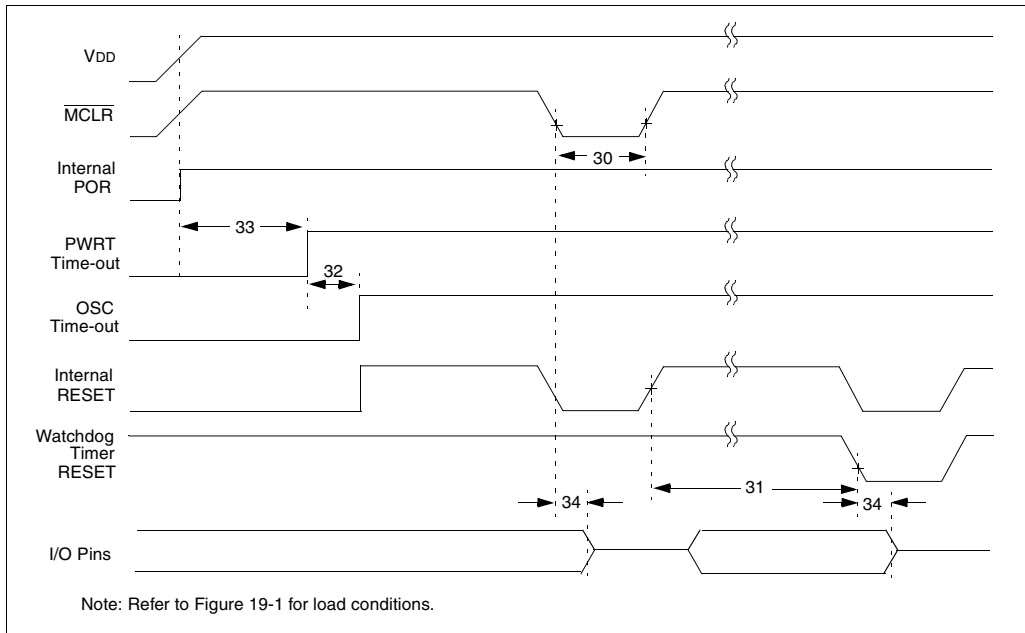
TABLE 19-4: **RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER REQUIREMENTS**

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
30*	TmcL	$\overline{MCLR}$ Pulse Width (low)	100	—	—	ns	V_{DD} = 5V, -40°C to +85°C
31*	Twdt	Watchdog Timer Time-out Period (No Prescaler)	7	18	33	ms	V_{DD} = 5V, -40°C to +85°C
32	Tost	Oscillation Start-up Timer Period	—	1024T_{OSC}	—	—	T_{OSC} = OSC1 period
33*	Tpwrt	Power-up Timer Period or WDT reset	28	72	132	ms	V_{DD} = 5V, -40°C to +85°C
34	T$_{IOZ}$	I/O Hi-impedance from $\overline{MCLR}$ Low	—	—	100	ns	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

PIC16C6X

21.3   DC Characteristics: PIC16CR63/R65-04 (Commercial, Industrial)
PIC16CR63/R65-10 (Commercial, Industrial)
PIC16CR63/R65-20 (Commercial, Industrial)
PIC16LCR63/R65-04 (Commercial, Industrial)

DC CHARACTERISTICS		Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial and 0°C ≤ TA ≤ +70°C for commercial Operating voltage VDD range as described in DC spec Section 21.1 and Section 21.2					
Param No.	Characteristic	Sym	Min	Typ †	Max	Units	Conditions
	Input Low Voltage I/O ports	VIL					
D030	with TTL buffer		Vss	-	0.15VDD	V	For entire VDD range
D030A			Vss	-	0.8V	V	4.5V ≤ VDD ≤ 5.5V
D031	with Schmitt Trigger buffer		Vss	-	0.2VDD	V	
D032	MCLR, OSC1 (in RC mode)		Vss	-	0.2VDD	V	
D033	OSC1 (in XT, HS and LP)		Vss	-	0.3VDD	V	Note1
	Input High Voltage I/O ports	VIH		-			
D040	with TTL buffer		2.0	-	VDD	V	4.5V ≤ VDD ≤ 5.5V
D040A			0.25VDD + 0.8V	-	VDD	V	For entire VDD range
D041	with Schmitt Trigger buffer		0.8VDD	-	VDD	V	For entire VDD range
D042	MCLR		0.8VDD	-	VDD	V	
D042A	OSC1 (XT, HS and LP)		0.7VDD	-	VDD	V	Note1
D043	OSC1 (in RC mode)		0.9VDD	-	VDD	V	
D070	PORTB weak pull-up current	IPURB	50	250	400	µA	VDD = 5V, VPIN = VSS
D060	**Input Leakage Current** (Notes 2, 3) I/O ports	IIL	-	-	±1	µA	Vss ≤ VPIN ≤ VDD, Pin at hi-impedance
D061	MCLR, RA4/T0CKI		-	-	±5	µA	Vss ≤ VPIN ≤ VDD
D063	OSC1		-	-	±5	µA	Vss ≤ VPIN ≤ VDD, XT, HS and LP osc configuration
D080	**Output Low Voltage** I/O ports	VOL	-	-	0.6	V	IOL = 8.5 mA, VDD = 4.5V, -40°C to +85°C
D083	OSC2/CLKOUT (RC osc config)		-	-	0.6	V	IOL = 1.6 mA, VDD = 4.5V, -40°C to +85°C
D090	**Output High Voltage** I/O ports (Note 3)	VOH	VDD-0.7	-	-	V	IOH = -3.0 mA, VDD = 4.5V, -40°C to +85°C
D092	OSC2/CLKOUT (RC osc config)		VDD-0.7	-	-	V	IOH = -1.3 mA, VDD = 4.5V, -40°C to +85°C
D150*	**Open-Drain High Voltage**	VOD	-	-	14	V	RA4 pin

*   These parameters are characterized but not tested.

†   Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C6X be driven with external clock in RC mode.

2: The leakage current on the MCLR/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as current sourced by the pin.

PIC16C6X

21.4   Timing Parameter Symbology

The timing parameter symbols have been created following one of the following formats:

1. TppS2ppS
2. TppS

3. T$_{CC:ST}$ (I^{2}C specifications only)
4. Ts   (I^{2}C specifications only)

T				
F	Frequency		T	Time

Lowercase letters (pp) and their meanings:

pp				
cc	CCP1		osc	OSC1
ck	CLKOUT		rd	$\overline{RD}$
cs	$\overline{CS}$		rw	$\overline{RD}$ or $\overline{WR}$
di	SDI		sc	SCK
do	SDO		ss	$\overline{SS}$
dt	Data in		t0	T0CKI
io	I/O port		t1	T1CKI
mc	$\overline{MCLR}$		wr	$\overline{WR}$

Uppercase letters and their meanings:

S				
F	Fall		P	Period
H	High		R	Rise
I	Invalid (Hi-impedance)		V	Valid
L	Low		Z	Hi-impedance
I^{2}C only				
AA	output access		High	High
BUF	Bus free		Low	Low

T$_{CC:ST}$ (I^{2}C specifications only)

CC				
HD	Hold		SU	Setup
ST				
DAT	DATA input hold		STO	STOP condition
STA	START condition			

FIGURE 21-1:   LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS

Load condition 1

V$_{DD}$/2

R$_L$

Pin

C$_L$

V$_{SS}$

Load condition 2

Pin

C$_L$

V$_{SS}$

R$_L$ = 464Ω

C$_L$ = 50 pF   for all pins except OSC2/CLKOUT
                 but including D and E outputs as ports

     15 pF   for OSC2 output

Note 1: PORTD and PORTE are not imple-
mented on the PIC16CR63.

Applicable Devices	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67
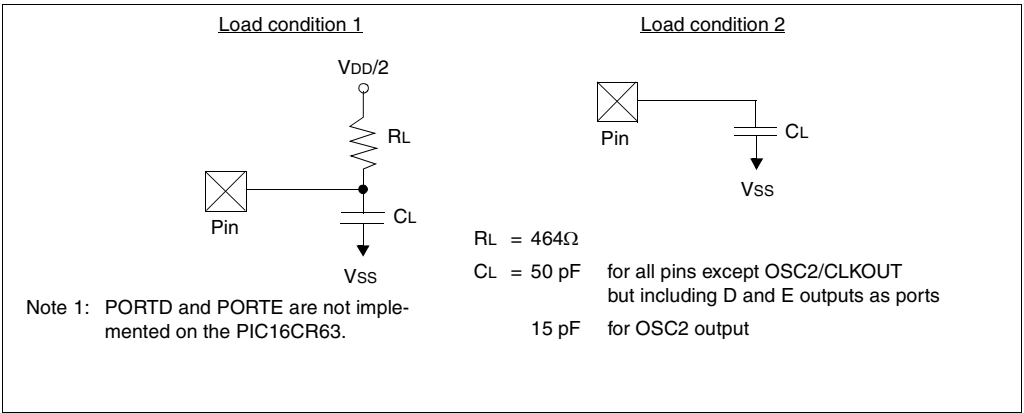
21.5   Timing Diagrams and Specifications

FIGURE 21-2:   EXTERNAL CLOCK TIMING
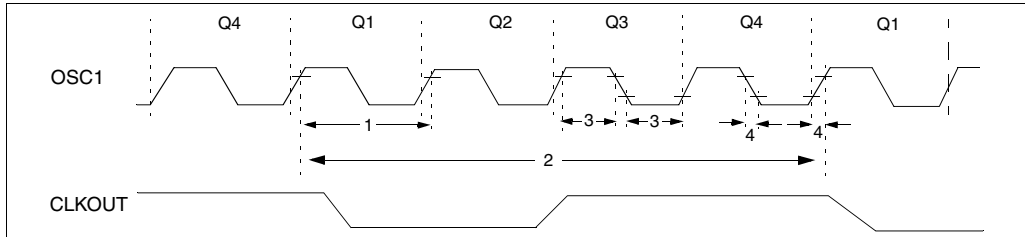
TABLE 21-2:   EXTERNAL CLOCK TIMING REQUIREMENTS

Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
	Fosc	External CLKIN Frequency (Note 1)	DC	—	4	MHz	XT and RC osc mode
			DC	—	4	MHz	HS osc mode (-04)
			DC	—	10	MHz	HS osc mode (-10)
			DC	—	20	MHz	HS osc mode (-20)
			DC	—	200	kHz	LP osc mode
		Oscillator Frequency (Note 1)	DC	—	4	MHz	RC osc mode
			0.1	—	4	MHz	XT osc mode
			4	—	20	MHz	HS osc mode
			5	—	200	kHz	LP osc mode
1	Tosc	External CLKIN Period (Note 1)	250	—	—	ns	XT and RC osc mode
			250	—	—	ns	HS osc mode (-04)
			100	—	—	ns	HS osc mode (-10)
			50	—	—	ns	HS osc mode (-20)
			5	—	—	µs	LP osc mode
		Oscillator Period (Note 1)	250	—	—	ns	RC osc mode
			250	—	10,000	ns	XT osc mode
			250	—	250	ns	HS osc mode (-04)
			100	—	250	ns	HS osc mode (-10)
			50	—	250	ns	HS osc mode (-20)
			5	—	—	µs	LP osc mode
2	TCY	Instruction Cycle Time (Note 1)	200	TCY	DC	ns	TCY = 4/FOSC
3*	TosL, TosH	External Clock in (OSC1) High or Low Time	100	—	—	ns	XT oscillator
			2.5	—	—	µs	LP oscillator
			15	—	—	ns	HS oscillator
4*	TosR, TosF	External Clock in (OSC1) Rise or Fall Time	—	—	25	ns	XT oscillator
			—	—	50	ns	LP oscillator
			—	—	15	ns	HS oscillator

*   These parameters are characterized but not tested.

†   Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1:   Instruction cycle period (TCY) equals four times the input oscillator time-base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min." values with an external clock applied to the OSC1/CLKIN pin. When an external clock input is used, the "Max." cycle time limit is "DC" (no clock) for all devices.

PIC16C6X

Applicable Devices | 61 | 62 | 62A | R62 | 63 | R63 | 64 | 64A | R64 | 65 | 65A | R65 | 66 | 67

FIGURE 22-3: CLKOUT AND I/O TIMING

Note: Refer to Figure 22-1 for load conditions.
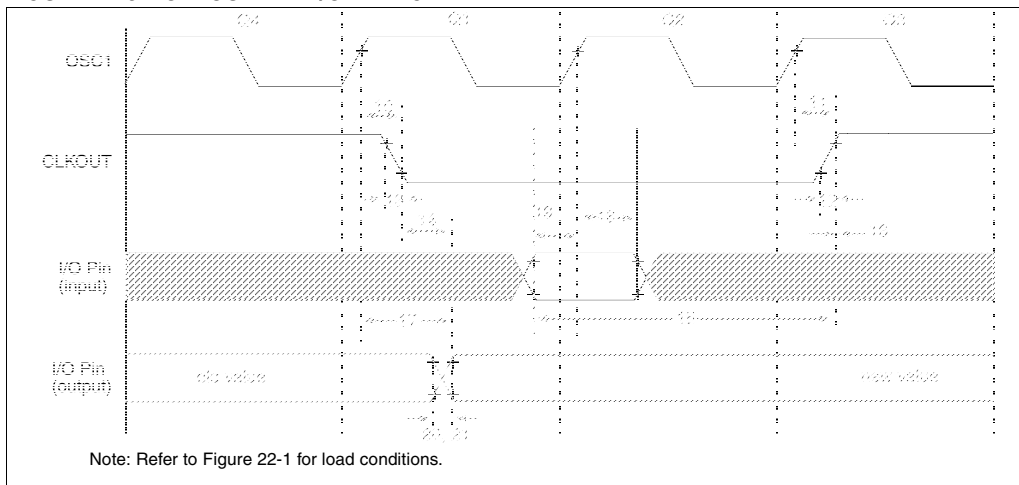
TABLE 22-3: CLKOUT AND I/O TIMING REQUIREMENTS

Parameter No.	Sym	Characteristic		Min	Typ†	Max	Units	Conditions
10*	TosH2ckL	OSC1↑ to CLKOUT↓		—	75	200	ns	Note 1
11*	TosH2ckH	OSC1↑ to CLKOUT↑		—	75	200	ns	Note 1
12*	TckR	CLKOUT rise time		—	35	100	ns	Note 1
13*	TckF	CLKOUT fall time		—	35	100	ns	Note 1
14*	TckL2ioV	CLKOUT ↓ to Port out valid		—	—	0.5TCY + 20	ns	Note 1
15*	TioV2ckH	Port in valid before CLKOUT ↑		Tosc + 200	—	—	ns	Note 1
16*	TckH2ioI	Port in hold after CLKOUT ↑		0	—	—	ns	Note 1
17*	TosH2ioV	OSC1↑ (Q1 cycle) to Port out valid		—	50	150	ns	
18*	TosH2ioI	OSC1↑ (Q2 cycle) to Port input invalid (I/O in hold time)	PIC16**C**66/67	100	—	—	ns	
			PIC16**LC**66/67	200	—	—	ns	
19*	TioV2osH	Port input valid to OSC1↑ (I/O in setup time)		0	—	—	ns	
20*	TioR	Port output rise time	PIC16**C**66/67	—	10	40	ns	
			PIC16**LC**66/67	—	—	80	ns	
21*	TioF	Port output fall time	PIC16**C**66/67	—	10	40	ns	
			PIC16**LC**66/67	—	—	80	ns	
22††*	Tinp	INT pin high or low time		TCY	—	—	ns	
23††*	Trbp	RB7:RB4 change INT high or low time		TCY	—	—	ns	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

†† These parameters are asynchronous events not related to any internal clock edge.

Note 1: Measurements are taken in RC Mode where CLKOUT output is 4 x Tosc.

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Applicable Devices	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67

FIGURE 23-18: TYPICAL I$_{DD}$ vs. CAPACITANCE @ 500 kHz (RC MODE)
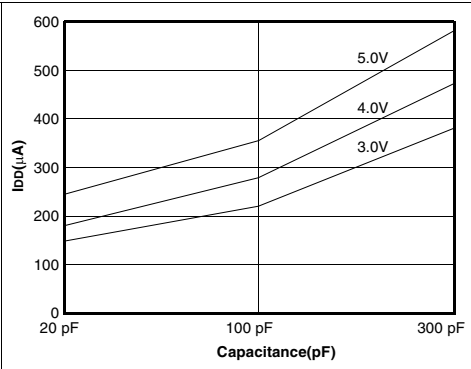
TABLE 23-1: RC OSCILLATOR FREQUENCIES

Cext	Rext	Average	
		Fosc @ 5V, 25°C	
22 pF	5k	4.12 MHz	± 1.4%
	10k	2.35 MHz	± 1.4%
	100k	268 kHz	± 1.1%
100 pF	3.3k	1.80 MHz	± 1.0%
	5k	1.27 MHz	± 1.0%
	10k	688 kHz	± 1.2%
	100k	77.2 kHz	± 1.0%
300 pF	3.3k	707 kHz	± 1.4%
	5k	501 kHz	± 1.2%
	10k	269 kHz	± 1.6%
	100k	28.3 kHz	± 1.1%

The percentage variation indicated here is part to part variation due to normal process distribution. The variation indicated is ±3 standard deviation from average value for V$_{DD}$ = 5V.

FIGURE 23-19: TRANSCONDUCTANCE(gm) OF HS OSCILLATOR vs. V$_{DD}$

Shaded area is beyond recommended range
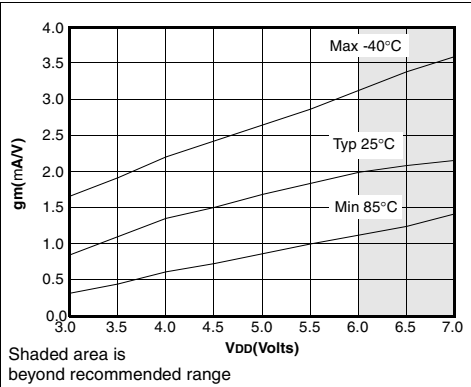
FIGURE 23-20: TRANSCONDUCTANCE(gm) OF LP OSCILLATOR vs. V$_{DD}$

Shaded areas are beyond recommended range
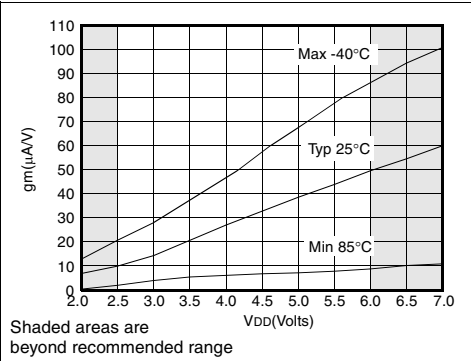
FIGURE 23-21: TRANSCONDUCTANCE(gm) OF XT OSCILLATOR vs. V$_{DD}$

Shaded areas are beyond recommended range
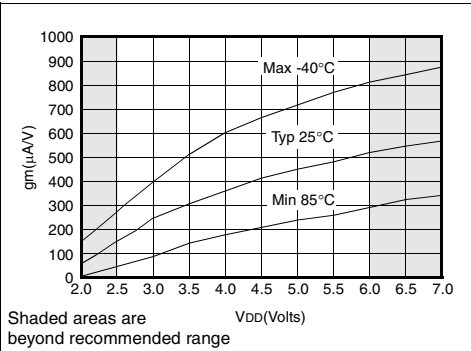
Data based on matrix samples. See first page of this section for details.

PIC16C6X

APPENDIX C: WHAT'S NEW

Added PIC16CR63 and PIC16CR65 devices.

Added PIC16C66 and PIC16C67 devices. The PIC16C66/67 devices have 368 bytes of data memory distributed in 4 banks and 8K of program memory in 4 pages. These two devices have an enhanced SPI that supports both clock phase and polarity. The USART has been enhanced.

When upgrading to the PIC16C66/67 please note that the upper 16 bytes of data memory in banks 1,2, and 3 are mapped into bank 0. This may require relocation of data memory usage in the user application code.

Q-cycles for instruction execution were added to Section 14.0 Instruction Set Summary.

APPENDIX D: WHAT'S CHANGED

Minor changes, spelling and grammatical changes.

Divided SPI section into SPI for the PIC16C66/67 (Section 11.3) and SPI for all other devices (Section 11.2).

Added the following note for the USART. This applies to all devices except the PIC16C66 and PIC16C67.

For the PIC16C63/R63/65/65A/R65 the asynchronous high speed mode (BRGH = 1) may experience a high rate of receive errors. It is recommended that BRGH = 0. If you desire a higher baud rate than BRGH = 0 can support, refer to the device errata for additional information or use the PIC16C66/67.

APPENDIX E: REVISION E

January 2013 - Added a note to each package drawing.

PIC16C6X

F.10   PIC17CXXX Family of Devices

		PIC17C42A	PIC17CR42	PIC17C43	PIC17CR43	PIC17C44
Clock	Maximum Frequency of Operation (MHz)	33	33	33	33	33
Memory	EPROM Program Memory (words)	2K	—	4K	—	8K
	ROM Program Memory (words)	—	2K	—	4K	—
	RAM Data Memory (bytes)	232	232	454	454	454
Peripherals	Timer Module(s)	TMR0, TMR1, TMR2, TMR3	TMR0, TMR1, TMR2, TMR3	TMR0, TMR1, TMR2, TMR3	TMR0, TMR1, TMR2, TMR3	TMR0, TMR1, TMR2, TMR3
	Captures/PWM Module(s)	2	2	2	2	2
	Serial Port(s) (USART)	Yes	Yes	Yes	Yes	Yes
Features	Hardware Multiply	Yes	Yes	Yes	Yes	Yes
	External Interrupts	Yes	Yes	Yes	Yes	Yes
	Interrupt Sources	11	11	11	11	11
	I/O Pins	33	33	33	33	33
	Voltage Range (Volts)	2.5-6.0	2.5-6.0	2.5-6.0	2.5-6.0	2.5-6.0
	Number of Instructions	58	58	58	58	58
	Packages	40-pin DIP; 44-pin PLCC, MQFP, TQFP	40-pin DIP; 44-pin PLCC, MQFP, TQFP	40-pin DIP; 44-pin PLCC, MQFP, TQFP	40-pin DIP; 44-pin PLCC, MQFP, TQFP	40-pin DIP; 44-pin PLCC, MQFP, TQFP

		PIC17C752	PIC17C756
Clock	Maximum Frequency of Operation (MHz)	33	33
Memory	EPROM Program Memory (words)	8K	16K
	ROM Program Memory (words)	—	—
	RAM Data Memory (bytes)	454	902
Peripherals	Timer Module(s)	TMR0, TMR1, TMR2, TMR3	TMR0, TMR1, TMR2, TMR3
	Captures/PWM Module(s)	4/3	4/3
	Serial Port(s) (USART)	2	2
Features	Hardware Multiply	Yes	Yes
	External Interrupts	Yes	Yes
	Interrupt Sources	18	18
	I/O Pins	50	50
	Voltage Range (Volts)	3.0-6.0	3.0-6.0
	Number of Instructions	58	58
	Packages	64-pin DIP; 68-pin LCC, 68-pin TQFP	64-pin DIP; 68-pin LCC, 68-pin TQFP

All PIC16/17 Family devices have Power-on Reset, selectable Watchdog Timer, selectable code protect and high I/O current capability.

PIC16C6X