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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

## Details

Product Status	Obsolete
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	I <sup>2</sup> C, SPI
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	33
Program Memory Size	3.5KB (2K x 14)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 6V
Data Converters	-
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-QFP
Supplier Device Package	44-MQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lc64a-04-pq

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

## 1.0 GENERAL DESCRIPTION

The PIC16CXX is a family of low-cost, high-performance, CMOS, fully-static, 8-bit microcontrollers.

All PIC16/17 microcontrollers employ an advanced RISC architecture. The PIC16CXX microcontroller family has enhanced core features, eight-level deep stack, and multiple internal and external interrupt sources. The separate instruction and data buses of the Harvard architecture allow a 14-bit wide instruction word with separate 8-bit wide data. The two stage instruction pipeline allows all instructions to execute in a single cycle, except for program branches (which require two cycles). A total of 35 instructions (reduced instruction set) are available. Additionally, a large register set gives some of the architectural innovations used to achieve a very high performance.

PIC16CXX microcontrollers typically achieve a 2:1 code compression and a 4:1 speed improvement over other 8-bit microcontrollers in their class.

The **PIC16C61** device has 36 bytes of RAM and 13 I/O pins. In addition a timer/counter is available.

The **PIC16C62/62A/R62** devices have 128 bytes of RAM and 22 I/O pins. In addition, several peripheral features are available, including: three timer/counters, one Capture/Compare/PWM module and one serial port. The Synchronous Serial Port can be configured as either a 3-wire Serial Peripheral Interface (SPI<sup>TM</sup>) or the two-wire Inter-Integrated Circuit (I<sup>2</sup>C) bus.

The **PIC16C63/R63** devices have 192 bytes of RAM, while the **PIC16C66** has 368 bytes. All three devices have 22 I/O pins. In addition, several peripheral features are available, including: three timer/counters, two Capture/Compare/PWM modules and two serial ports. The Synchronous Serial Port can be configured as either a 3-wire Serial Peripheral Interface (SPI) or the two-wire Inter-Integrated Circuit ( $I^2C$ ) bus. The Universal Synchronous Asynchronous Receiver Transmitter (USART) is also know as a Serial Communications Interface or SCI.

The **PIC16C64/64A/R64** devices have 128 bytes of RAM and 33 I/O pins. In addition, several peripheral features are available, including: three timer/counters, one Capture/Compare/PWM module and one serial port. The Synchronous Serial Port can be configured as either a 3-wire Serial Peripheral Interface (SPI) or the two-wire Inter-Integrated Circuit (I<sup>2</sup>C) bus. An 8-bit Parallel Slave Port is also provided.

The **PIC16C65/65A/R65** devices have 192 bytes of RAM, while the **PIC16C67** has 368 bytes. All four devices have 33 I/O pins. In addition, several peripheral features are available, including: three timer/counters, two Capture/Compare/PWM modules and two serial ports. The Synchronous Serial Port can be configured as either a 3-wire Serial Peripheral Interface (SPI) or the two-wire Inter-Integrated Circuit (I<sup>2</sup>C) bus. The Universal Synchronous Asynchronous Receiver Transmit-

ter (USART) is also known as a Serial Communications Interface or SCI. An 8-bit Parallel Slave Port is also provided.

The PIC16C6X device family has special features to reduce external components, thus reducing cost, enhancing system reliability and reducing power consumption. There are four oscillator options, of which the single pin RC oscillator provides a low-cost solution, the LP oscillator minimizes power consumption, XT is a standard crystal, and the HS is for High Speed crystals. The SLEEP (power-down) mode offers a power saving mode. The user can wake the chip from SLEEP through several external and internal interrupts, and resets.

A highly reliable Watchdog Timer with its own on-chip RC oscillator provides protection against software lockup.

A UV erasable CERDIP packaged version is ideal for code development, while the cost-effective One-Time-Programmable (OTP) version is suitable for production in any volume.

The PIC16C6X family fits perfectly in applications ranging from high-speed automotive and appliance control to low-power remote sensors, keyboards and telecom processors. The EPROM technology makes customization of application programs (transmitter codes, motor speeds, receiver frequencies, etc.) extremely fast and convenient. The small footprint packages make this microcontroller series perfect for all applications with space limitations. Low-cost, low-power, high performance, ease-of-use, and I/O flexibility make the PIC16C6X very versatile even in areas where no microcontroller use has been considered before (e.g. timer functions, serial communication, capture and compare, PWM functions, and co-processor applications).

## 1.1 Family and Upward Compatibility

Those users familiar with the PIC16C5X family of microcontrollers will realize that this is an enhanced version of the PIC16C5X architecture. Please refer to Appendix A for a detailed list of enhancements. Code written for PIC16C5X can be easily ported to PIC16CXX family of devices (Appendix B).

## 1.2 Development Support

PIC16C6X devices are supported by the complete line of Microchip Development tools.

Please refer to Section 15.0 for more details about Microchip's development tools.

#### **TABLE 3-3:** PIC16C64/64A/R64/65/65A/R65/67 PINOUT DESCRIPTION

Pin Name	DIP Pin#	PLCC Pin#	TQFP MQFP Pin#	Pin Type	Buffer Type	Description
OSC1/CLKIN	13	14	30	Ι	ST/CMOS(3)	Oscillator crystal input/external clock source input.
OSC2/CLKOUT	14	15	31	0	_	Oscillator crystal output. Connects to crystal or resonator in crystal oscillator mode. In RC mode, the pin outputs CLK- OUT which has 1/4 the frequency of OSC1, and denotes the instruction cycle rate.
MCLR/Vpp	1	2	18	I/P	ST	Master clear reset input or programming voltage input. This pin is an active low reset to the device.
						PORTA is a bi-directional I/O port.
RA0	2	3	19	I/O	TTL	
RA1	3	4	20	I/O	TTL	
RA2	4	5	21	I/O	TTL	
RA3	5	6	22	I/O	TTL	
RA4/T0CKI	6	7	23	I/O	ST	RA4 can also be the clock input to the Timer0 timer/counter. Output is open drain type.
RA5/SS	7	8	24	I/O	TTL	RA5 can also be the slave select for the synchronous serial port.
						PORTB is a bi-directional I/O port. PORTB can be software programmed for internal weak pull-up on all inputs.
RB0/INT	33	36	8	I/O	TTL/ST(4)	RB0 can also be the external interrupt pin.
RB1	34	37	9	I/O	TTL	
RB2	35	38	10	I/O	TTL	
RB3	36	39	11	I/O	TTL	
RB4	37	41	14	I/O	TTL	Interrupt on change pin.
RB5	38	42	15	I/O	TTL	Interrupt on change pin.
RB6	39	43	16	I/O	TTL/ST <sup>(5)</sup>	Interrupt on change pin. Serial programming clock.
RB7	40	44	17	I/O	TTL/ST <sup>(5)</sup>	Interrupt on change pin. Serial programming data.
						PORTC is a bi-directional I/O port.
RC0/T1OSO <sup>(1)</sup> /T1CKI	15	16	32	I/O	ST	RC0 can also be the Timer1 oscillator output <sup>(1)</sup> or Timer1 clock input.
RC1/T1OSI <sup>(1)</sup> /CCP2 <sup>(2)</sup>	16	18	35	I/O	ST	RC1 can also be the Timer1 oscillator input <sup>(1)</sup> or Capture2 input/Compare2 output/PWM2 output <sup>(2)</sup> .
RC2/CCP1	17	19	36	I/O	ST	RC2 can also be the Capture1 input/Compare1 out- put/PWM1 output.
RC3/SCK/SCL	18	20	37	I/O	ST	RC3 can also be the synchronous serial clock input/out- put for both SPI and I <sup>2</sup> C modes.
RC4/SDI/SDA	23	25	42	I/O	ST	RC4 can also be the SPI Data In (SPI mode) or data I/O (I <sup>2</sup> C mode).
RC5/SDO	24	26	43	I/O	ST	RC5 can also be the SPI Data Out (SPI mode).
RC6/TX/CK <sup>(2)</sup>	25	27	44	I/O	ST	RC6 can also be the USART Asynchronous Transmit <sup>(2)</sup> or Synchronous Clock <sup>(2)</sup> .
RC7/RX/DT <sup>(2)</sup>	26	29	1	I/O	ST	RC7 can also be the USART Asynchronous Receive <sup>(2)</sup> or Synchronous Data <sup>(2)</sup> .
Legend: I = input C	) = outp	ut	I/C	) = input/	output	P = power

— = Not used TTL = TTL input

ST = Schmitt Trigger input Note 1: Pin functions T1OSO and T1OSI are reversed on the PIC16C64.

2: CCP2 and the USART are not available on the PIC16C64/64A/R64.

3: This buffer is a Schmitt Trigger input when configured in RC oscillator mode and a CMOS input otherwise.

4: This buffer is a Schmitt Trigger input when configured as the external interrupt.

5: This buffer is a Schmitt Trigger input when used in serial programming mode.

6: This buffer is a Schmitt Trigger input when configured as general purpose I/O and a TTL input when used in the Parallel Slave Port mode (for interfacing to a microprocessor bus).

# 5.0 I/O PORTS

## Applicable Devices

61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

Some pins for these I/O ports are multiplexed with an alternate function(s) for the peripheral features on the device. In general, when a peripheral is enabled, that pin may not be used as a general purpose I/O pin.

## 5.1 PORTA and TRISA Register

### Applicable Devices

61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

All devices have a 6-bit wide PORTA, except for the PIC16C61 which has a 5-bit wide PORTA.

Pin RA4/T0CKI is a Schmitt Trigger input and an open drain output. All other RA port pins have TTL input levels and full CMOS output drivers. All pins have data direction bits (TRIS registers) which can configure these pins as output or input.

Setting a bit in the TRISA register puts the corresponding output driver in a hi-impedance mode. Clearing a bit in the TRISA register puts the contents of the output latch on the selected pin.

Reading PORTA register reads the status of the pins whereas writing to it will write to the port latch. All write operations are read-modify-write operations. Therefore, a write to a port implies that the port pins are read, this value is modified, and then written to the port data latch.

Pin RA4 is multiplexed with Timer0 module clock input to become the RA4/T0CKI pin.

## EXAMPLE 5-1: INITIALIZING PORTA

BCF	STATUS,	RPO ;	;
BCF	STATUS,	RP1 ;	PIC16C66/67 only
CLRF	PORTA	;	Initialize PORTA by
		;	clearing output
		;	data latches
BSF	STATUS,	RP0	: Select Bank 1
MOVLW	0xCF		Value used to
			: initialize data
			direction
MOVWF	TRISA		Set RA<3:0> as inputs
			RA<5:4> as outputs
			TRISA<7:6> are always
			read as '0'.

#### FIGURE 5-1: BLOCK DIAGRAM OF THE RA3:RA0 PINS AND THE RA5 PIN



## FIGURE 5-2: BLOCK DIAGRAM OF THE RA4/T0CKI PIN



## 8.3 <u>Timer1 Operation in Asynchronous</u> <u>Counter Mode</u>

#### Applicable Devices

61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

If control bit  $\overline{T1SYNC}$  (T1CON<2>) is set, the external clock input is not synchronized. The timer continues to increment asynchronous to the internal phase clocks. The timer will continue to run during SLEEP and generate an interrupt on overflow which will wake the processor. However, special precautions in software are needed to read-from or write-to the Timer1 register pair, TMR1L and TMR1H (Section 8.3.2).

In asynchronous counter mode, Timer1 cannot be used as a time-base for capture or compare operations.

# 8.3.1 EXTERNAL CLOCK INPUT TIMING WITH UNSYNCHRONIZED CLOCK

If control bit  $\overline{T1SYNC}$  is set, the timer will increment completely asynchronously. The input clock must meet certain minimum high time and low time requirements, as specified in timing parameters (45 - 47).

#### 8.3.2 READING AND WRITING TMR1 IN ASYNCHRONOUS COUNTER MODE

Reading TMR1H or TMR1L, while the timer is running from an external asynchronous clock, will ensure a valid read (taken care of in hardware). However, the user should keep in mind that reading the 16-bit timer in two 8-bit values itself poses certain problems since the timer may overflow between the reads.

For writes, it is recommended that the user simply stop the timer and write the desired values. A write contention may occur by writing to the timer registers while the register is incrementing. This may produce an unpredictable value in the timer register.

Reading the 16-bit value requires some care. Example 8-1 is an example routine to read the 16-bit timer value. This is useful if the timer cannot be stopped.

## EXAMPLE 8-1: READING A 16-BIT FREE-RUNNING TIMER

;	All Int	errupts	are	disabled
	MOVF	TMR1H,	W	;Read high byte
	MOVWF	TMPH		;
	MOVF	TMR1L,	W	;Read low byte
	MOVWF	TMPL		;
	MOVF	TMR1H,	W	;Read high byte
	SUBWF	TMPH,	W	;Sub 1st read
				;with 2nd read
	BTFSC	STATUS	Z	;is result = 0
	GOTO	CONTINU	JE	;Good 16-bit read
;	TMR1L ma	y have r	olle	d over between the read
;	of the h	igh and	low	bytes. Reading the high
;	and low	bytes no	w w	ill read a good value.
	MOVF	TMR1H,	W	;Read high byte
	MOVWF	TMPH		;
	MOVF	TMR1L,	W	;Read low byte
	MOVWF	TMPL		;
;	Re-ena	ble Inte	rrup	ot (if required)
CC	ONTINUE			;Continue with
	:			;your code

## 8.4 <u>Timer1 Oscillator</u>

#### Applicable Devices 61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

A crystal oscillator circuit is built in-between pins T1OSI (input) and T1OSO (amplifier output). It is enabled by setting control bit T1OSCEN (T1CON<3>). The oscillator is a low power oscillator rated up to 200 kHz. It will continue to run during SLEEP. It is primarily intended for a 32 kHz crystal. Table 8-1 shows the capacitor selection for the Timer1 oscillator.

The Timer1 oscillator is identical to the LP oscillator. The user must allow a software time delay to ensure proper oscillator start-up.

## TABLE 8-1: CAPACITOR SELECTION FOR THE TIMER1 OSCILLATOR

Osc Type	Freq	C2					
LP	32 kHz	33 pF	33 pF				
	100 kHz	15 pF	15 pF				
	200 kHz	15 pF	15 pF				
These v	alues are for o	design guidan	ce only.				
Crystals Tested:							
32.768 kHz	Epson C-001R32.768K-A ± 20 PPM						
100 kHz	Epson C-2 100.00 KC-P ± 20 F						
200 kHz	STD XTL 20	0.000 kHz	$\pm$ 20 PPM				
<ul> <li>Note 1: Higher capacitance increases the stability of oscillator but also increases the stability time.</li> <li>2: Since each resonator/crystal has its own characteristics, the user should consult the resonator/crystal manufacturer for appropriate values of external components.</li> </ul>							

To enable the serial port, SSP enable bit SSPEN (SSPCON<5>) must be set. To reset or reconfigure SPI mode, clear enable bit SSPEN, re-initialize SSPCON register, and then set enable bit SSPEN. This configures the SDI, SDO, SCK, and  $\overline{SS}$  pins as serial port pins. For the pins to behave as the serial port function, they must have their data direction bits (in the TRIS register) appropriately programmed. That is:

- SDI must have TRISC<4> set
- SDO must have TRISC<5> cleared
- SCK (Master mode) must have TRISC<3> cleared
- SCK (Slave mode) must have TRISC<3> set
- SS must have TRISA<5> set (if implemented)

Any serial port function that is not desired may be overridden by programming the corresponding data direction (TRIS) register to the opposite value. An example would be in master mode where you are only sending data (to a display driver), then both SDI and SS could be used as general purpose outputs by clearing their corresponding TRIS register bits.

Figure 11-4 shows a typical connection between two microcontrollers. The master controller (Processor 1) initiates the data transfer by sending the SCK signal. Data is shifted out of both shift registers on their programmed clock edge, and latched on the opposite edge of the clock. Both processors should be programmed to the same Clock Polarity (CKP), then both controllers would send and receive data at the same time. Whether the data is meaningful (or dummy data) depends on the application software. This leads to three scenarios for data transmission:

- Master sends data Slave sends dummy data
- Master sends data Slave sends data
- · Master sends dummy data Slave sends data



## FIGURE 11-4: SPI MASTER/SLAVE CONNECTION

The master can initiate the data transfer at any time because it controls the SCK. The master determines when the slave (Processor 2) is to broadcast data by the software protocol.

In master mode the data is transmitted/received as soon as the SSPBUF register is written to. If the SPI is only going to receive, the SCK output could be disabled (programmed as an input). The SSPSR register will continue to shift in the signal present on the SDI pin at the programmed clock rate. As each byte is received, it will be loaded into the SSPBUF register as if a normal received byte (interrupts and status bits appropriately set). This could be useful in receiver applications as a "line activity monitor" mode.

In slave mode, the data is transmitted and received as the external clock pulses appear on SCK. When the last bit is latched interrupt flag bit SSPIF (PIR1<3>) is set.

The clock polarity is selected by appropriately programming bit CKP (SSPCON<4>). This then would give waveforms for SPI communication as shown in Figure 11-5 and Figure 11-6 where the MSB is transmitted first. In master mode, the SPI clock rate (bit rate) is user programmable to be one of the following:

- Fosc/4 (or TCY)
- Fosc/16 (or 4 TCY)
- Fosc/64 (or 16 TCY)
- Timer2 output/2

This allows a maximum bit clock frequency (at 20 MHz) of 5 MHz. When in slave mode the external clock must meet the minimum high and low times.

In sleep mode, the slave can transmit and receive data and wake the device from sleep.

### 11.5.1.2 RECEPTION

When the R/ $\overline{W}$  bit of the address byte is clear and an address match occurs, the R/ $\overline{W}$  bit of the SSPSTAT register is cleared. The received address is loaded into the SSPBUF register.

When the address byte overflow condition exists, then no acknowledge ( $\overline{ACK}$ ) pulse is given. An overflow condition is defined as either bit BF (SSPSTAT<0>) is set or bit SSPOV (SSPCON<6>) is set. An SSP interrupt is generated for each data transfer byte. Flag bit SSPIF (PIR1<3>) must be cleared in software. The SSPSTAT register is used to determine the status of the byte.

## FIGURE 11-25: I<sup>2</sup>C WAVEFORMS FOR RECEPTION (7-BIT ADDRESS)

Receiving Address         R/W=0         Receiving Data         ACK         Receiving Data         ACK           SDA        /A7_         A6         A5         A4         A3         A2         A1         ACK         D7         D6         D5         D4         D3         D2         D1         D0          D7         D6         D5         D4         D3         D2         D1         D0          D3         D2         D1         D0          S0         A7         A6         A5         A4         A3         A2         A1         D5         D6         D5         D4         D3         D2         D1         D0          D3         D2         D1         D0          C         ACK         ACK         ACK         ACK         ACK         D3         D2         D1         D0          D3         D2         D1         D0          C         ACK         ACK	
SSPIF (PIR1<3>) Cleared in software BF (SSPSTAT<0>) SSPBUF register is read	Bus Master terminates transfer
SSPOV (SSPCON<6>) Bit SSPOV is set because the SSPBUF register is still full.	
ACK is not sent.	

## FIGURE 13-14: EXTERNAL POWER-ON RESET CIRCUIT (FOR SLOW VDD POWER-UP)



- Note 1: External Power-on Reset circuit is required only if VDD power-up slope is too slow. The diode D helps discharge the capacitor quickly when VDD powers down.
  - R < 40 kΩ is recommended to make sure that voltage drop across R does not violate the devices electrical specifications.
  - 3:  $R1 = 100\Omega$  to 1 k $\Omega$  will limit any current flowing into MCLR from external capacitor C in the event of MCLR/VPP pin breakdown due to Electrostatic Discharge (ESD) or Electrostatic Overstress (EOS).

## FIGURE 13-15: EXTERNAL BROWN-OUT PROTECTION CIRCUIT 1



- Note 1: This circuit will activate reset when VDD goes below (Vz + 0.7V) where Vz = Zener voltage.
  - Internal brown-out detection on the PIC16C62A/R62/63/R63/64A/R64/65A/ R65/66/67 should be disabled when using this circuit.
  - 3: Resistors should be adjusted for the characteristics of the transistors.

## FIGURE 13-16: EXTERNAL BROWN-OUT PROTECTION CIRCUIT 2



Note 1: This brown-out circuit is less expensive, albeit less accurate. Transistor Q1 turns off when VDD is below a certain level such that:

$$V_{DD} \bullet \frac{R1}{R1 + R2} = 0.7V$$

- 2: Internal brown-out detection on the PIC16C62A/R62/63/R63/64A/R64/65A/ R65/66/67 should be disabled when using this circuit.
- 3: Resistors should be adjusted for the characteristics of the transistors.

## FIGURE 13-22: WAKE-UP FROM SLEEP THROUGH INTERRUPT

Q1 Q2 Q3 Q4	Q1 Q2 Q3 Q4 Q1	1 : :	Q1 Q2 Q3 Q4	Q1 Q2 Q3 Q4	Q1 Q2 Q3 Q4	Q1 Q2 Q3 Q4
osc1/~_/~_/~_/~_/						
		Tost(2)		\'	\	
INT pin	l I			i i	1	
INTF flag	1			Interrupt Latency		
(11100112)				(Note 2)		
GIE bit (INTCON<7>)	Pro	ocessor in		\		
1 1	. 5	SLEEP			1	1
INSTRUCTION FLOW					1	
РС ( РС )	PC+1 X	PC+2	PC+2	X PC + 2	( <u>0004</u> h	( 0005h
Instruction { Inst(PC) = SLEEP	Inst(PC + 1)	1	Inst(PC + 2)	 	Inst(0004h)	Inst(0005h)
Instruction Inst(PC - 1)	SLEEP	1	Inst(PC + 1)	Dummy cycle	Dummy cycle	Inst(0004h)
Note 1, VT HC or LD coeilleter a	nodo occurrod					

2: TOST = 1024TOSC (drawing not to scale) This delay will not be there for RC osc mode.

3: GIE = '1' assumed. In this case after wake-up, the processor jumps to the interrupt routine.

If GIE = '0', execution will continue in-line.

4: CLKOUT is not available in these osc modes, but shown here for timing reference.

## 13.9 Program Verification/Code Protection

#### Applicable Devices

61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

If the code protection bit(s) have not been programmed, the on-chip program memory can be read out for verification purposes.

Note:	Microchip does not recommend code pro-
	tecting windowed devices.

### 13.10 ID Locations

Applicable Devices 61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

Four memory locations (2000h - 2003h) are designated as ID locations where the user can store checksum or other code-identification numbers. These locations are not accessible during normal execution but are readable and writable during program/verify. It is recommended that only the 4 least significant bits of the ID location are used.

For ROM devices, these values are submitted along with the ROM code.

### 13.11 In-Circuit Serial Programming

#### Applicable Devices

61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

The PIC16CXX microcontrollers can be serially programmed while in the end application circuit. This is simply done with two lines for clock and data, and three other lines for power, ground, and the programming voltage. This allows customers to manufacture boards with unprogrammed devices, and then program the microcontroller just before shipping the product. This also allows the most recent firmware or a custom firmware to be programmed. The device is placed into a program/verify mode by holding pins RB6 and RB7 low while raising the  $\overline{\text{MCLR}}$  (VPP) pin from VIL to VIHH (see programming specification). RB6 becomes the programming clock and RB7 becomes the programming data. Both RB6 and RB7 are Schmitt Trigger inputs in this mode.

After reset, to place the device in program/verify mode, the program counter (PC) is at location 00h. A 6-bit command is then supplied to the device. Depending on the command, 14-bits of program data are then supplied to or from the device, depending if the command was a load or a read. For complete details of serial programming, please refer to the PIC16C6X/7X Programming Specifications (Literature #DS30228).

## FIGURE 13-23: TYPICAL IN-CIRCUIT SERIAL PROGRAMMING CONNECTION



## Applicable Devices 61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

## FIGURE 17-10: I<sup>2</sup>C BUS DATA TIMING



## TABLE 17-10: I<sup>2</sup>C BUS DATA REQUIREMENTS

Parameter No.	Sym	Characteristic		Min	Max	Units	Conditions
100	Тнідн	Clock high time	100 kHz mode	4.0	-	μs	Device must operate at a mini- mum of 1.5 MHz
			400 kHz mode	0.6	—	μs	Device must operate at a mini- mum of 10 MHz
			SSP Module	1.5Tcy	-		
101	TLOW	Clock low time	100 kHz mode	4.7	-	μs	Device must operate at a mini- mum of 1.5 MHz
			400 kHz mode	1.3	_	μs	Device must operate at a mini- mum of 10 MHz
			SSP Module	1.5Tcy	-		
102	TR	SDA and SCL rise	100 kHz mode	_	1000	ns	
		time	400 kHz mode	20 + 0.1Cb	300	ns	Cb is specified to be from 10 to 400 pF
103	TF	SDA and SCL fall time	100 kHz mode	_	300	ns	
			400 kHz mode	20 + 0.1Cb	300	ns	Cb is specified to be from 10 to 400 pF
90	TSU:STA	START condition	100 kHz mode	4.7	_	μS	Only relevant for repeated
		setup time	400 kHz mode	0.6	_	μs	START condition
91	THD:STA	START condition hold	100 kHz mode	4.0	-	μS	After this period the first clock
		time	400 kHz mode	0.6	—	μs	pulse is generated
106	THD:DAT	Data input hold time	100 kHz mode	0	—	ns	
			400 kHz mode	0	0.9	μs	
107	TSU:DAT	Data input setup time	100 kHz mode	250	_	ns	Note 2
			400 kHz mode	100	—	ns	
92	Tsu:sto	STOP condition setup	100 kHz mode	4.7	_	μs	
		time	400 kHz mode	0.6	_	μs	
109	ΤΑΑ	Output valid from	100 kHz mode	—	3500	ns	Note 1
		clock	400 kHz mode	—	—	ns	
110	TBUF	Bus free time	100 kHz mode	4.7	_	μS	Time the bus must be free
			400 kHz mode	1.3	_	μs	start
	Cb	Bus capacitive loading		—	400	pF	

Note 1: As a transmitter, the device must provide this internal minimum delay time to bridge the undefined region (min. 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

2: A fast-mode (400 kHz) I<sup>2</sup>C-bus device can be used in a standard-mode (100 kHz) I<sup>2</sup>C-bus system, but the requirement tsu;DAT ≥ 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line TR max. + tsu;DAT = 1000 + 250 = 1250 ns (according to the standard-mode I<sup>2</sup>C bus specification) before the SCL line is released.

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NOTES:

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# FIGURE 18-10: I<sup>2</sup>C BUS START/STOP BITS TIMING



## TABLE 18-9: I<sup>2</sup>C BUS START/STOP BITS REQUIREMENTS

Parameter No.	Sym	Characteristic		Min	Тур	Мах	Units	Conditions
			I					
90*	TSU:STA	START condition	100 kHz mode	4700	—	—	ne	Only relevant for repeated START
		Setup time	400 kHz mode	600	—	—	115	condition
91*	THD:STA	START condition	100 kHz mode	4000	—	—	ne	After this period the first clock
		Hold time	400 kHz mode	600	—	_	115	pulse is generated
92*	TSU:STO	STOP condition	100 kHz mode	4700	—	—	ne	
		Setup time	400 kHz mode	600	—	-	113	
93*	THD:STO	STOP condition	100 kHz mode	4000	—	—	ne	
		Hold time	400 kHz mode	600	—	—	115	

\*These parameters are characterized but not tested.

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## FIGURE 20-8: PARALLEL SLAVE PORT TIMING (PIC16C65A)



## TABLE 20-7: PARALLEL SLAVE PORT REQUIREMENTS (PIC16C65A)

Parameter No.	Sym	Characteristic		Min	Тур†	Max	Units	Conditions
62*	TdtV2wrH	Data in valid before $\overline{WR}^{\uparrow}$ or $\overline{CS}^{\uparrow}$ (set	up time)	20	_	_	ns	
				25	—	—	ns	Extended Range Only
63*	TwrH2dtl	$\overline{\text{WR}}$ or $\overline{\text{CS}}$ to data–in invalid (hold	PIC16 <b>C</b> 65A	20	—	_	ns	
		time)	PIC16 <b>LC</b> 65A	35	—	_	ns	
64	TrdL2dtV	$\overline{\text{RD}}\downarrow$ and $\overline{\text{CS}}\downarrow$ to data–out valid		_	_	80	ns	
				_	_	90	ns	Extended Range Only
65*	TrdH2dtl	RD↑ or CS↑ to data–out invalid		10	—	30	ns	
* The	a naramata	ra are abaractorized but not tested		1	1	1	1	1

These parameters are characterized but not tested.

Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not t tested.

		Standard Operating Conditions (unless otherwise stated)							
		Operating temperature $-40^{\circ}C \leq TA \leq +85^{\circ}C$ for industrial and							
DC CHA	RACTERISTICS				0°C	≤ T.	$A \le +70^{\circ}C$ for commercial		
		Operatir	ng voltage	Vdd	range as o	describ	ed in DC spec Section 21.1 and		
		Section	21.2						
Param	Characteristic	Sym	Min	Тур	Max	Units	Conditions		
No.				†					
	Capacitive Loading Specs on Out-								
	put Pins								
D100	OSC2 pin	Cosc2	-	-	15	pF	In XT, HS and LP modes when		
							external clock is used to drive		
							OSC1.		
D101	All I/O pins and OSC2 (in RC mode)	Cio	-	-	50	pF			
D102	SCL, SDA in I <sup>2</sup> C mode	Cb	-	-	400	pF			
* т	le a calendar de la compaña		امما						

Applicable Devices 61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

These parameters are characterized but not tested.

t Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C6X be driven with external clock in RC mode.

2: The leakage current on the MCLR/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as current sourced by the pin.

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## FIGURE 22-6: TIMER0 AND TIMER1 EXTERNAL CLOCK TIMINGS



## TABLE 22-5: TIMER0 AND TIMER1 EXTERNAL CLOCK REQUIREMENTS

Param	Sym	Characteristic			Min	Тур†	Max	Units	Conditions
NO.									
40*	Tt0H	T0CKI High Pulse V	Vidth	No Prescaler	0.5TCY + 20	—	—	ns	Must also meet
				With Prescaler	10	_	—	ns	parameter 42
41*	Tt0L	T0CKI Low Pulse W	/idth	No Prescaler	0.5TCY + 20	—	—	ns	Must also meet
				With Prescaler	10	—	—	ns	parameter 42
42*	Tt0P	T0CKI Period		No Prescaler	TCY + 40	_	—	ns	
				With Prescaler	Greater of:	_	—	ns	N = prescale value
					20 or <u>TCY + 40</u>				(2, 4,, 256)
					N				
45*	Tt1H	T1CKI High Time	Synchronous, P	rescaler = 1	0.5TCY + 20		—	ns	Must also meet
			Synchronous,	PIC16 <b>C</b> 6X	15	—	—	ns	parameter 47
			Prescaler =	PIC16 <b>LC</b> 6X	25	_	—	ns	
			2,4,8						
			Asynchronous	PIC16 <b>C</b> 6X	30		—	ns	
				PIC16 <b>LC</b> 6X	50	-	—	ns	
46*	Tt1L	T1CKI Low Time	Synchronous, P	rescaler = 1	0.5TCY + 20		—	ns	Must also meet
			Synchronous,	PIC16 <b>C</b> 6X	15		—	ns	parameter 47
			Prescaler =	PIC16 <b>LC</b> 6X	25	-	—	ns	
			2,4,8						
			Asynchronous	PIC16 <b>C</b> 6X	30	—	—	ns	
				PIC16 <b>LC</b> 6X	50		—	ns	
47*	Tt1P	T1CKI input period	Synchronous	PIC16 <b>C</b> 6X	Greater of:	_	—	ns	N = prescale value
					30 OR <u>TCY + 40</u>				(1, 2, 4, 8)
					N				
				PIC16 <b>LC</b> 6X	Greater of:				N = prescale value
					50 OR <u>ICY + 40</u>				(1, 2, 4, 8)
				<b>B</b> 10.100001	N				
			Asynchronous	PIC16 <b>C</b> 6X	60	-	-	ns	
				PIC16 <b>LC</b> 6X	100	<u> </u>		ns	
	Ft1	Timer1 oscillator inp	out frequency rar	ige	DC	-	200	kHz	
		(oscillator enabled b	by setting bit T1C	SCEN)					
48	ICKEZtmr1	Delay from external	clock edge to tin	ner increment	2Tosc	-	/Tosc	—	

\* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

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Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
70*	TssL2scH, TssL2scL	$\overline{SS}\downarrow$ to $SCK\downarrow$ or $SCK\uparrow$ input	Тсү		—	ns	
71*	TscH	SCK input high time (slave mode)	TCY + 20	_	_	ns	
72*	TscL	SCK input low time (slave mode)	TCY + 20	_	_	ns	
73*	TdiV2scH, TdiV2scL	Setup time of SDI data input to SCK edge	100	_	—	ns	
74*	TscH2diL, TscL2diL	Hold time of SDI data input to SCK edge	100	_	—	ns	
75*	TdoR	SDO data output rise time	_	10	25	ns	
76*	TdoF	SDO data output fall time	—	10	25	ns	
77*	TssH2doZ	SS↑ to SDO output hi-impedance	10	_	50	ns	
78*	TscR	SCK output rise time (master mode)	—	10	25	ns	
79*	TscF	SCK output fall time (master mode)	_	10	25	ns	
80*	TscH2doV, TscL2doV	SDO data output valid after SCK edge	_	_	50	ns	
81*	TdoV2scH, TdoV2scL	SDO data output setup to SCK edge	Тсү	_	—	ns	
82*	TssL2doV	SDO data output valid after $\overline{SS}\downarrow$ edge	_	—	50	ns	
83*	TscH2ssH, TscL2ssH	SS ↑ after SCK edge	1.5TCY + 40	_	—	ns	

# TABLE 22-8: SPI MODE REQUIREMENTS

\* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested. Applicable Devices 61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

## FIGURE 22-15: USART SYNCHRONOUS TRANSMISSION (MASTER/SLAVE) TIMING



## TABLE 22-11: USART SYNCHRONOUS TRANSMISSION REQUIREMENTS

Parameter No.	Sym	Characteristic		Min	Тур†	Max	Units	Conditions
120*	TckH2dtV	SYNC XMIT (MASTER & SLAVE)	PIC16 <b>C</b> 66/67	-	_	80	ns	
		Clock high to data out valid	PIC16LC66/67	-	_	100	ns	
121*	Tckrf	Clock out rise time and fall time	PIC16 <b>C</b> 66/67	-		45	ns	
		(Master Mode)	PIC16LC66/67	-	_	50	ns	
122*	Tdtrf	Data out rise time and fall time	PIC16 <b>C</b> 66/67	Ι	—	45	ns	
			PIC16LC66/67	_		50	ns	

\* These parameters are characterized but not tested.

†: Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

### FIGURE 22-16: USART SYNCHRONOUS RECEIVE (MASTER/SLAVE) TIMING



## TABLE 22-12: USART SYNCHRONOUS RECEIVE REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
125*	TdtV2ckL	SYNC RCV (MASTER & SLAVE) Data setup before CK $\downarrow$ (DT setup time)	15	_	_	ns	
126*	TckL2dtl	Data hold after CK $\downarrow$ (DT hold time)	15	_	—	ns	

These parameters are characterized but not tested.

†: Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.



Data based on matrix samples. See first page of this section for details.

# 24.0 PACKAGING INFORMATION

## 24.1 <u>18-Lead Plastic Dual In-line (300 mil) (P)</u>

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



		Package Grou	p: Plastic Dual	In-Line (PLA)		
		Millimeters			Inches	
Symbol	Min	Мах	Notes	Min	Мах	Notes
α	0°	10°		0°	10°	
А	_	4.064		_	0.160	
A1	0.381	_		0.015	_	
A2	3.048	3.810		0.120	0.150	
В	0.355	0.559		0.014	0.022	
B1	1.524	1.524	Reference	0.060	0.060	Reference
С	0.203	0.381	Typical	0.008	0.015	Typical
D	22.479	23.495		0.885	0.925	
D1	20.320	20.320	Reference	0.800	0.800	Reference
E	7.620	8.255		0.300	0.325	
E1	6.096	7.112		0.240	0.280	
e1	2.489	2.591	Typical	0.098	0.102	Typical
eA	7.620	7.620	Reference	0.300	0.300	Reference
eB	7.874	9.906		0.310	0.390	
L	3.048	3.556		0.120	0.140	
N	18	18		18	18	
S	0.889	-		0.035	-	
S1	0.127	_		0.005	_	

## F.5 PIC16C55X Family of Devices

		PIC16C554	PIC16C556 <sup>(1)</sup>	PIC16C558
Clock	Maximum Frequency of Operation (MHz)	20	20	20
Memory	EPROM Program Memory (x14 words)	512	1K	2K
wentory	Data Memory (bytes)	80	80	128
	Timer Module(s)	TMR0	TMR0	TMR0
Peripherals	Comparators(s)	—	—	—
	Internal Reference Voltage	—	—	—
	Interrupt Sources	3	3	3
	I/O Pins	13	13	13
	Voltage Range (Volts)	2.5-6.0	2.5-6.0	2.5-6.0
Features	Brown-out Reset	—	—	—
	Packages	18-pin DIP, SOIC; 20-pin SSOP	18-pin DIP, SOIC; 20-pin SSOP	18-pin DIP, SOIC; 20-pin SSOP

All PIC16/17 Family devices have Power-on Reset, selectable Watchdog Timer, selectable code protect and high I/O current capability. All PIC16C5XX Family devices use serial programming with clock pin RB6 and data pin RB7. Note 1: Please contact your local Microchip sales office for availability of these devices.

## F.6 PIC16C62X and PIC16C64X Family of Devices

		PIC16C620	PIC16C621	PIC16C622	PIC16C642	PIC16C662
Clock	Maximum Frequency of Operation (MHz)	20	20	20	20	20
Memory	EPROM Program Memory (x14 words)	512	1K	2К	4K	4K
	Data Memory (bytes)	80	80	128	176	176
	Timer Module(s)	TMR0	TMR0	TMR0	TMR0	TMR0
Peripherals	Comparators(s)	2	2	2	2	2
	Internal Reference Voltage	Yes	Yes	Yes	Yes	Yes
	Interrupt Sources	4	4	4	4	5
	I/O Pins	13	13	13	22	33
	Voltage Range (Volts)	2.5-6.0	2.5-6.0	2.5-6.0	3.0-6.0	3.0-6.0
Footuroo	Brown-out Reset	Yes	Yes	Yes	Yes	Yes
Teatules	Packages	18-pin DIP, SOIC; 20-pin SSOP	18-pin DIP, SOIC; 20-pin SSOP	18-pin DIP, SOIC; 20-pin SSOP	28-pin PDIP, SOIC, Windowed CDIP	40-pin PDIP, Windowed CDIP; 44-pin PLCC, MQFP

All PIC16/17 Family devices have Power-on Reset, selectable Watchdog Timer, selectable code protect and high

I/O current capability. All PIC16C62X and PIC16C64X Family devices use serial programming with clock pin RB6 and data pin RB7.

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