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# Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

# Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	I <sup>2</sup> C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	33
Program Memory Size	7KB (4K × 14)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	192 x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 6V
Data Converters	-
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-QFP
Supplier Device Package	44-MQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lc65a-04-pq

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# FIGURE 4-6: PIC16C62/62A/R62/64/64A/ R64 REGISTER FILE MAP

File Addre	ess	F	ile Address
00h	INDF <sup>(1)</sup>	INDF <sup>(1)</sup>	80h
01h	TMR0	OPTION	81h
02h	PCL	PCL	82h
03h	STATUS	STATUS	83h
04h	FSR	FSR	84h
05h	PORTA	TRISA	85h
06h	PORTB	TRISB	86h
07h	PORTC	TRISC	87h
08h	PORTD <sup>(2)</sup>	TRISD <sup>(2)</sup>	88h
09h	PORIE <sup>(2)</sup>		89h
0Ah	PCLAIH	PCLAIH	8Ah
0Bh	INTCON	INTCON	8Bh
0Ch	PIR1	PIE1	8Ch
0Dh			8Dh
0Eh	TMR1L	PCON	8Eh
0Fh	TMR1H		8Fh
10h	T1CON		90h
11h	TMR2		91h
12h	T2CON	PR2	92h
13h	SSPBUF	SSPADD	93h
14h	SSPCON	SSPSTAT	94h
15h	CCPR1L		95h
16h	CCPR1H		96h
17h	CCP1CON		97h
18h			98h
1Fh			9Fh
20h		Gaparal	A0h
		Purpose	
	General	Register	BFh
	Purpose Register		C0h
	0		
7Fh			FFh
	Bank 0	Bank 1	
Unin Note	e 1: Not a physica	emory location; rea Il register.	u as 0°.
	2: PORTD and	PORTE are not ava	ilable on
	the PIC16C6	2/62A/R62.	

### FIGURE 4-7: PIC16C63/R63/65/65A/R65 REGISTER FILE MAP

	i i Edio		
File Addre	ess		File Address
00h	INDF <sup>(1)</sup>	INDF <sup>(1)</sup>	80h
01h	TMR0	OPTION	81h
02h	PCL	PCL	82h
03h	STATUS	STATUS	83h
04h	FSR	FSR	84h
05h	PORTA	TRISA	85h
06h	PORTB	TRISB	86h
07h	PORTC	TRISC	87h
08h	PORTD <sup>(2)</sup>	TRISD <sup>(2)</sup>	88h
09h	PCLATH	PCLATH	89h
	INTCON	INTCON	8Bh
0Ch	PIR1	PIE1	8Ch
0Dh	PIR2	PIE2	8Dh
0Eh	TMR1L	PCON	8Eh
0Fh	TMR1H		8Fh
10h	TICON		
11h	TMB2		91h
12h	T2CON	PB2	
106	SSPRIJE	SERVED	
14h		SSPSTAT	
15h	CCPP1		95h
166			96h
176			97h
1711	CCP1CON		0.0%h
18N	RCSTA	TXSTA	9011
19h	TXREG	SPBRG	99h
1Ah	RCREG		9Ah
1Bh	CCPR2L		9Bh
1Ch	CCPR2H		9Ch
1Dh	CCP2CON		9Dh
1Eh			9Eh
1Fh			9Fh
20h	General	General	A0h
ZEb	Purpose Begister	Purpose Register	
/Fn	Bank 0	Bank 1	FFh
🗌 Unir	nplemented data me	emory location; re	ad as '0'.
Note	e 1: Not a physica	I register	voilable or
	the PIC16C6	- On i E are not av 3/R63.	valiable on

#### 4.2.2.6 PIE2 REGISTER

Applicable Devices 61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

This register contains the CCP2 interrupt enable bit.

# FIGURE 4-20: PIE2 REGISTER (ADDRESS 8Dh)



#### FIGURE 5-4: BLOCK DIAGRAM OF THE RB7:RB4 PINS FOR PIC16C62A/63/R63/64A/65A/ R65/66/67



# TABLE 5-3: PORTB FUNCTIONS

#### FIGURE 5-5: BLOCK DIAGRAM OF THE RB3:RB0 PINS



Name	Bit#	Buffer Type	Function
RB0/INT	bit0	TTL/ST <sup>(1)</sup>	Input/output pin or external interrupt input. Internal software programmable weak pull-up.
RB1	bit1	TTL	Input/output pin. Internal software programmable weak pull-up.
RB2	bit2	TTL	Input/output pin. Internal software programmable weak pull-up.
RB3	bit3	TTL	Input/output pin. Internal software programmable weak pull-up.
RB4	bit4	TTL	Input/output pin (with interrupt on change). Internal software programmable weak pull-up.
RB5	bit5	TTL	Input/output pin (with interrupt on change). Internal software programmable weak pull-up.
RB6	bit6	TTL/ST <sup>(2)</sup>	Input/output pin (with interrupt on change). Internal software programmable weak pull-up. Serial programming clock.
RB7	bit7	TTL/ST <sup>(2)</sup>	Input/output pin (with interrupt on change). Internal software programmable weak pull-up. Serial programming data.

Legend: TTL = TTL input, ST = Schmitt Trigger input

Note 1: This buffer is a Schmitt Trigger input when configured as the external interrupt.

2: This buffer is a Schmitt Trigger input when used in serial programming mode.

#### TABLE 5-4: SUMMARY OF REGISTERS ASSOCIATED WITH PORTB

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other resets
06h, 106h	PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx xxxx	uuuu uuuuu
86h, 186h	TRISB	TRISB PORTB Data Direction Register								1111 1111	1111 1111
81h, 181h	OPTION	RBPU	INTEDG	TOCS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111

Legend: x = unknown, u = unchanged. Shaded cells are not used by PORTB.

# 5.3 PORTC and TRISC Register

#### Applicable Devices

#### 61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

PORTC is an 8-bit wide bi-directional port. Each pin is individually configurable as an input or output through the TRISC register. PORTC is multiplexed with several peripheral functions (Table 5-5). PORTC pins have Schmitt Trigger input buffers.

When enabling peripheral functions, care should be taken in defining TRIS bits for each PORTC pin. Some peripherals override the TRIS bit to make a pin an output, while other peripherals override the TRIS bit to make a pin an input. Since the TRIS bit override is in effect while the peripheral is enabled, read-modifywrite instructions (BSF, BCF, XORWF) with TRISC as destination should be avoided. The user should refer to the corresponding peripheral section for the correct TRIS bit settings.

#### EXAMPLE 5-3: INITIALIZING PORTC



# FIGURE 5-6: PORTC BLOCK DIAGRAM



3: Peripheral OE (output enable) is only activated if peripheral select is active.

# TABLE 5-5: PORTC FUNCTIONS FOR PIC16C62/64

Name	Bit#	Buffer Type	Function
RC0/T1OSI/T1CKI	bit0	ST	Input/output port pin or Timer1 oscillator input or Timer1 clock input
RC1/T1OSO	bit1	ST	Input/output port pin or Timer1 oscillator output
RC2/CCP1	bit2	ST	Input/output port pin or Capture1 input/Compare1 output/PWM1 output
RC3/SCK/SCL	bit3	ST	RC3 can also be the synchronous serial clock for both SPI and $I^2C$ modes.
RC4/SDI/SDA	bit4	ST	RC4 can also be the SPI Data In (SPI mode) or data I/O (I <sup>2</sup> C mode).
RC5/SDO	bit5	ST	Input/output port pin or synchronous serial port data output
RC6	bit6	ST	Input/output port pin
RC7	bit7	ST	Input/output port pin

Legend: ST = Schmitt Trigger input

# 6.0 OVERVIEW OF TIMER MODULES

#### Applicable Devices

61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

All PIC16C6X devices have three timer modules except for the PIC16C61, which has one timer module. Each module can generate an interrupt to indicate that an event has occurred (i.e., timer overflow). Each of these modules are detailed in the following sections. The timer modules are:

- Timer0 module (Section 7.0)
- Timer1 module (Section 8.0)
- Timer2 module (Section 9.0)

#### 6.1 <u>Timer0 Overview</u>

#### Applicable Devices

#### 61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

The Timer0 module is a simple 8-bit overflow counter. The clock source can be either the internal system clock (Fosc/4) or an external clock. When the clock source is an external clock, the Timer0 module can be selected to increment on either the rising or falling edge.

The Timer0 module also has a programmable prescaler option. This prescaler can be assigned to either the Timer0 module or the Watchdog Timer. Bit PSA (OPTION<3>) assigns the prescaler, and bits PS2:PS0 (OPTION<2:0>) determine the prescaler value. TMR0 can increment at the following rates: 1:1 when the prescaler is assigned to Watchdog Timer, 1:2, 1:4, 1:8, 1:16, 1:32, 1:64, 1:128, and 1:256.

Synchronization of the external clock occurs after the prescaler. When the prescaler is used, the external clock frequency may be higher then the device's frequency. The maximum frequency is 50 MHz, given the high and low time requirements of the clock.

# 6.2 <u>Timer1 Overview</u>

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#### 61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

Timer1 is a 16-bit timer/counter. The clock source can be either the internal system clock (Fosc/4), an external clock, or an external crystal. Timer1 can operate as either a timer or a counter. When operating as a counter (external clock source), the counter can either operate synchronized to the device or asynchronously to the device. Asynchronous operation allows Timer1 to operate during sleep, which is useful for applications that require a real-time clock as well as the power savings of SLEEP mode.

TImer1 also has a prescaler option which allows TMR1 to increment at the following rates: 1:1, 1:2, 1:4, and 1:8. TMR1 can be used in conjunction with the Capture/Compare/PWM module. When used with a CCP module, Timer1 is the time-base for 16-bit capture or 16-bit compare and must be synchronized to the device.

#### 6.3 <u>Timer2 Overview</u>

#### Applicable Devices

#### 61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

Timer2 is an 8-bit timer with a programmable prescaler and a programmable postscaler, as well as an 8-bit Period Register (PR2). Timer2 can be used with the CCP module (in PWM mode) as well as the Baud Rate Generator for the Synchronous Serial Port (SSP). The prescaler option allows Timer2 to increment at the following rates: 1:1, 1:4, and 1:16.

The postscaler allows TMR2 register to match the period register (PR2) a programmable number of times before generating an interrupt. The postscaler can be programmed from 1:1 to 1:16 (inclusive).

### 6.4 <u>CCP Overview</u>

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61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

The CCP module(s) can operate in one of three modes: 16-bit capture, 16-bit compare, or up to 10-bit Pulse Width Modulation (PWM).

Capture mode captures the 16-bit value of TMR1 into the CCPRxH:CCPRxL register pair. The capture event can be programmed for either the falling edge, rising edge, fourth rising edge, or sixteenth rising edge of the CCPx pin.

Compare mode compares the TMR1H:TMR1L register pair to the CCPRxH:CCPRxL register pair. When a match occurs, an interrupt can be generated and the output pin CCPx can be forced to a given state (High or Low) and Timer1 can be reset. This depends on control bits CCPxM3:CCPxM0.

PWM mode compares the TMR2 register to a 10-bit duty cycle register (CCPRxH:CCPRxL<5:4>) as well as to an 8-bit period register (PR2). When the TMR2 register = Duty Cycle register, the CCPx pin will be forced low. When TMR2 = PR2, TMR2 is cleared to 00h, an interrupt can be generated, and the CCPx pin (if an output) will be forced high.



#### TIMER0 TIMING: INTERNAL CLOCK/PRESCALE 1:2 FIGURE 7-3:

#### FIGURE 7-4: **TMR0 INTERRUPT TIMING**



#### 8.5 <u>Resetting Timer1 using a CCP Trigger</u> Output

#### Applicable Devices

61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

CCP2 is implemented on the PIC16C63/R63/65/65A/ R65/66/67 only.

If CCP1 or CCP2 module is configured in Compare mode to generate a "special event trigger" (CCPxM3:CCPxM0 = 1011), this signal will reset Timer1.

Note: The "special event trigger" from the CCP1 and CCP2 modules will not set interrupt flag bit TMR1IF(PIR1<0>).

Timer1 must be configured for either timer or synchronized counter mode to take advantage of this feature. If the Timer1 is running in asynchronous counter mode, this reset operation may not work.

In the event that a write to Timer1 coincides with a special event trigger from CCP1 or CCP2, the write will take precedence.

In this mode of operation, the CCPRxH:CCPRxL registers pair effectively becomes the period register for the Timer1 module.

### 8.6 <u>Resetting of TMR1 Register Pair</u> (TMR1H:TMR1L)

#### Applicable Devices

61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

The TMR1H and TMR1L registers are not reset to 00h on a POR or any other reset except by the CCP1 or CCP2 special event trigger.

The T1CON register is reset to 00h on a Power-on Reset or a Brown-out Reset, which shuts off the timer and leaves a 1:1 prescaler. In all other resets, the register is unaffected.

# 8.7 <u>Timer1 Prescaler</u>

Applicable Devices

61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

The prescaler counter is cleared on writes to the TMR1H or TMR1L registers.

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR		Valu all c res	e on other sets
0Bh,8Bh 10Bh,18Bh	INTCON	GIE	PEIE	TOIE	INTE	RBIE	TOIF	INTF	RBIF	0000	000x	0000	000u
0Ch	PIR1	PSPIF <sup>(2)</sup>	(3)	RCIF <sup>(1)</sup>	TXIF <sup>(1)</sup>	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000	0000	0000	0000
8Ch	PIE1	PSPIE <sup>(2)</sup>	(3)	RCIE <sup>(1)</sup>	TXIE <sup>(1)</sup>	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000	0000	0000	0000
0Eh	TMR1L	Holding register for the Least Significant Byte of the 16-bit TMR1 register									xxxx	uuuu	uuuu
0Fh	TMR1H	Holding r	Holding register for the Most Significant Byte of the 16-bit TMR1 register								xxxx	uuuu	uuuu
10h	T1CON	_	_	T1CKPS1	T1CKPS0	T1OSCEN	T1SYNC	TMR1CS	TMR10N	00	0000	uu	uuuu

# TABLE 8-2: REGISTERS ASSOCIATED WITH TIMER1 AS A TIMER/COUNTER

Legend: x = unknown, u = unchanged, - = unimplemented read as '0'. Shaded cells are not used by the Timer1 module.

Note 1: The USART is implemented on the PIC16C63/R63/65/65A/R65/66/67 only.

2: Bits PSPIE and PSPIF are reserved on the PIC16C62/62A/R62/63/R63/66, always maintain these bits clear.

3: PIR1<6> and PIE1<6> are reserved, always maintain these bits clear.

# TABLE 9-1: REGISTERS ASSOCIATED WITH TIMER2 AS A TIMER/COUNTER

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR		Valu all o res	e on ther ets
0Bh,8Bh 10Bh,18Bh	INTCON	GIE	PEIE	TOIE	INTE	RBIE	TOIF	INTF	RBIF	0000	000x	0000	000u
0Ch	PIR1	PSPIF <sup>(2)</sup>	(3)	RCIF <sup>(1)</sup>	TXIF <sup>(1)</sup>	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000	0000	0000	0000
8Ch	PIE1	PSPIE <sup>(2)</sup>	(3)	RCIE <sup>(1)</sup>	TXIE <sup>(1)</sup>	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000	0000	0000	0000
11h	TMR2	Timer2 m	Timer2 module's register								0000	0000	0000
12h	T2CON		TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000	0000	-000	0000
92h	PR2	Timer2 P	Timer2 Period register								1111	1111	1111

Legend: x = unknown, u = unchanged, - = unimplemented locations read as '0'. Shaded cells are not used by Timer2.

Note 1: The USART is implemented on the PIC16C63/R63/65/65A/R65/66/67 only.

2: Bits PSPIE and PSPIF are reserved on the PIC16C62/62A/R62/63/R63/66, always maintain these bits clear.

3: PIR1<6> and PIE1<6> are reserved, always maintain these bits clear.

### 11.3 SPI Mode for PIC16C66/67

This section contains register definitions and operational characterisitics of the SPI module on the PIC16C66 and PIC16C67 only.

# FIGURE 11-7: SSPSTAT: SYNC SERIAL PORT STATUS REGISTER (ADDRESS 94h)(PIC16C66/67)

R/W-0	R/W-0	R-0	R-0	R-0	R-0	R-0	R-0					
SMP	CKE	D/A	Р	S	R/W	UA	BF	R = Readable bit				
bit7							bit0	W = Writable bit U = Unimplemented bit, read as '0' - n =Value at POR reset				
bit 7:	SMP: S SPI Mas 1 = Inpu 0 = Inpu SPI Slav SMP mu	PI data in <u>ster Mod</u> it data sa it data sa <u>ve Mode</u> ust be cle	nput samp <u>e</u> ampled at e ampled at r eared whe	le phase and of data niddle of da n SPI is use	output time ata output tir ed in slave m	ne node						
bit 6:	<b>CKE</b> : SI CKP = 0 $1 = Data$ $0 = Data$ $CKP = 1$ $1 = Data$ $0 = Data$	PI Clock <u>)</u> a transm a transm <u>1</u> a transm a transm	Edge Sele itted on ris itted on fal itted on fal itted on ris	ct (Figure <sup>-</sup> ing edge of ling edge o ing edge o ing edge of	11-11, Figure SCK f SCK f SCK SCK	e 11-12, an	d Figure 11-	13)				
bit 5:	<ul> <li>D/A: Data/Address bit (I<sup>2</sup>C mode only)</li> <li>1 = Indicates that the last byte received or transmitted was data</li> <li>0 = Indicates that the last byte received or transmitted was address</li> </ul>											
bit 4:	<b>P</b> : Stop bit ( $l^2C$ mode only. This bit is cleared when the SSP module is disabled, or when the Start bit is detected last, SSPEN is cleared) 1 = Indicates that a stop bit has been detected last (this bit is '0' on RESET) 0 = Stop bit was not detected last											
bit 3:	<b>S</b> : Start detected 1 = India 0 = Star	bit (I <sup>2</sup> C d last, SS cates tha t bit was	mode only SPEN is cle at a start bi not detect	. This bit is eared) t has been ed last	cleared whe	en the SSP t (this bit is	module is d	lisabled, or when the Stop bit is				
bit 2:	<b>R/W</b> : Re This bit address 1 = Rea 0 = Writ	ead/Write holds th match to d e	e bit inform ne R/W bit o the next	ation (I <sup>2</sup> C r information start bit, sto	mode only) n following t op bit, or ACI	he last ado K bit.	Iress match	. This bit is only valid from the				
bit 1:	<b>UA</b> : Upo 1 = Indio 0 = Add	date Add cates tha ress doe	lress (10-b at the user es not neec	it I <sup>2</sup> C mode needs to up I to be upda	e only) odate the ad ated	dress in the	e SSPADD r	egister				
bit 0:	BF: Buff	fer Full S	status bit									
	<u>Receive</u> 1 = Rec 0 = Rec	e (SPI an eive com eive not	d I <sup>2</sup> C moden plete, SSF complete,	es) PBUF is full SSPBUF is	sempty							
	<u>Transmi</u> 1 = Tran 0 = Tran	<u>t</u> (I <sup>2</sup> C mo Ismit in p Ismit con	ode only) progress, S nplete, SS	SPBUF is f PBUF is en	full npty							

The  $\overline{SS}$  pin allows a synchronous slave mode. The SPI must be in slave mode (SSPCON<3:0> = 04h) and the TRISA<5> bit must be set for the synchronous slave mode to be enabled. When the  $\overline{SS}$  pin is low, transmission and reception are enabled and the SDO pin is driven. When the  $\overline{SS}$  pin goes high, the SDO pin is no longer driven, even if in the middle of a transmitted byte, and becomes a floating output. If the  $\overline{SS}$  pin is taken low without resetting SPI mode, the transmission will continue from the point at which it was taken high. External pull-up/ pull-down resistors may be desirable, depending on the application.

- Note: When the SPI is in Slave Mode with SS pin control enabled, (SSPCON<3:0> = 0100) the SPI module will reset if the SS pin is set to VDD.
- Note: If the SPI is used in Slave Mode with CKE = '1', then the SS pin control must be enabled.

To emulate two-wire communication, the SDO pin can be connected to the SDI pin. When the SPI needs to operate as a receiver the SDO pin can be configured as an input. This disables transmissions from the SDO. The SDI can always be left as an input (SDI function) since it cannot create a bus conflict.



# FIGURE 11-11: SPI MODE TIMING, MASTER MODE (PIC16C66/67)

# FIGURE 11-12: SPI MODE TIMING (SLAVE MODE WITH CKE = 0) (PIC16C66/67)



# FIGURE 11-13: SPI MODE TIMING (SLAVE MODE WITH CKE = 1) (PIC16C66/67)



TABLE 11-2:	<b>REGISTERS ASSOCIATED WITH SPI OPERATION (</b>	PIC16C66/67)	,

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Valu Pow Re	ie on er-on set	Value other	on all resets
0Bh,8Bh, 10Bh,18Bh	INTCON	GIE	PEIE	TOIE	INTE	RBIE	T0IF	INTF	RBIF	0000	000x	0000	000u
0Ch	PIR1	PSPIF <sup>(1)</sup>	(2)	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000	0000	0000	0000
8Ch	PIE1	PSPIE <sup>(1)</sup>	(2)	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000	0000	0000	0000
13h	SSPBUF	Synchron	ous Serial	Port Rec	eive Buffe	r/Transmit	Register			xxxx	xxxx	uuuu	uuuu
14h	SSPCON	WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0	0000	0000	0000	0000
85h	TRISA	_		PORTA D	Data Direc	tion regist	er			11	1111	11	1111
87h	TRISC	PORTC D	ata Direct	ion registe	ər					1111	1111	1111	1111
94h	SSPSTAT	SMP	CKE	D/A	Р	S	R/W	UA	BF	0000	0000	0000	0000

Legend: x = unknown, u = unchanged, - = unimplemented locations read as '0'.

Shaded cells are not used by SSP module in SPI mode.

Note 1: PSPIF and PSPIE are reserved on the PIC16C66, always maintain these bits clear.

2: PIR1<6> and PIE1<6> are reserved, always maintain these bits clear.

#### 11.5.1 SLAVE MODE

PIC16C6X

In slave mode, the SCL and SDA pins must be configured as inputs (TRISC<4:3> set). The SSP module will override the input state with the output data when required (slave-transmitter).

When an address is matched or the data transfer after an address match is received, the hardware automatically will generate the acknowledge ( $\overline{ACK}$ ) pulse, and then load the SSPBUF register with the received value currently in the SSPSR register.

There are certain conditions that will cause the SSP module not to give this ACK pulse. These are if either (or both):

- a) The buffer full bit BF (SSPSTAT<0>) was set before the transfer was received.
- b) The overflow bit SSPOV (SSPCON<6>) was set before the transfer was received.

In this case, the SSPSR register value is not loaded into the SSPBUF, but bit SSPIF (PIR1<3>) is set. Table 11-4 shows what happens when a data transfer byte is received, given the status of bits BF and SSPOV. The shaded cells show the condition where user software did not properly clear the overflow condition. Flag bit BF is cleared by reading the SSPBUF register while bit SSPOV is cleared through software.

The SCL clock input must have a minimum high and low for proper operation. The high and low times of the  $I^2C$  specification as well as the requirement of the SSP module is shown in timing parameter #100 and parameter #101.

#### 11.5.1.1 ADDRESSING

Once the SSP module has been enabled, it waits for a START condition to occur. Following the START condition, the 8-bits are shifted into the SSPSR register. All incoming bits are sampled with the rising edge of the clock (SCL) line. The value of register SSPSR<7:1> is compared to the value of the SSPADD register. The

address is compared on the falling edge of the eighth clock (SCL) pulse. If the addresses match, and the BF and SSPOV bits are clear, the following events occur:

- a) The SSPSR register value is loaded into the SSPBUF register.
- b) The buffer full bit, BF is set.
- c) An ACK pulse is generated.
- d) SSP interrupt flag bit, SSPIF (PIR1<3>) is set (interrupt is generated if enabled) - on the falling edge of the ninth SCL pulse.

In 10-bit address mode, two address bytes need to be received by the slave (Figure 11-16). The five Most Significant bits (MSbs) of the first address byte specify if this is a 10-bit address. Bit  $R/\overline{W}$  (SSPSTAT-<2>) must specify a write so the slave device will receive the second address byte. For a 10-bit address the first byte would equal '1111 0 A9 A8 0', where A9 and A8 are the two MSbs of the address. The sequence of events for 10-bit address is as follows, with steps 7-9 for slave-transmitter:

- 1. Receive first (high) byte of Address (bits SSPIF, BF, and bit UA (SSPSTAT<1>) are set).
- Update the SSPADD register with second (low) byte of Address (clears bit UA and releases the SCL line).
- 3. Read the SSPBUF register (clears bit BF) and clear flag bit SSPIF.
- 4. Receive second (low) byte of Address (bits SSPIF, BF, and UA are set).
- Update the SSPADD register with the first (high) byte of Address, if match releases SCL line, this will clear bit UA.
- 6. Read the SSPBUF register (clears bit BF) and clear flag bit SSPIF.
- 7. Receive repeated START condition.
- 8. Receive first (high) byte of Address (bits SSPIF and BF are set).
- 9. Read the SSPBUF register (clears bit BF) and clear flag bit SSPIF.

### TABLE 11-4: DATA TRANSFER RECEIVED BYTE ACTIONS

Status Bit Transfer is	ts as Data s Received			Set bit SSPIF
BF	SSPOV	$SSPSR \to SSPBUF$	Generate ACK Pulse	(SSP Interrupt occurs if enabled)
0	0	Yes	Yes	Yes
1	0	No	No	Yes
1	1	No	No	Yes
0	1	No	No	Yes

#### 11.5.2 MASTER MODE

Master mode of operation is supported in firmware using interrupt generation on the detection of the START and STOP conditions. The STOP (P) and START (S) bits are cleared from a reset or when the SSP module is disabled. The STOP (P) and START (S) bits will toggle based on the START and STOP conditions. Control of the  $l^2C$  bus may be taken when the P bit is set, or the bus is idle and both the S and P bits are clear.

In master mode the SCL and SDA lines are manipulated by clearing the corresponding TRISC<4:3> bit(s). The output level is always low, irrespective of the value(s) in PORTC<4:3>. So when transmitting data, a '1' data bit must have the TRISC<4> bit set (input) and a '0' data bit must have the TRISC<4> bit cleared (output). The same scenario is true for the SCL line with the TRISC<3> bit.

The following events will cause SSP Interrupt Flag bit, SSPIF, to be set (SSP Interrupt if enabled):

- START condition
- STOP condition
- Data transfer byte transmitted/received

Master mode of operation can be done with either the slave mode idle (SSPM3:SSPM0 = 1011) or with the slave active. When both master and slave modes are enabled, the software needs to differentiate the source(s) of the interrupt.

#### 11.5.3 MULTI-MASTER MODE

In multi-master mode, the interrupt generation on the detection of the START and STOP conditions allows the determination of when the bus is free. The STOP (P) and START (S) bits are cleared from a reset or when the SSP module is disabled. The STOP (P) and START (S) bits will toggle based on the START and STOP conditions. Control of the  $I^2C$  bus may be taken when bit P (SSPSTAT<4>) is set, or the bus is idle and both the S and P bits clear. When the bus is busy, enabling the SSP Interrupt will generate the interrupt when the STOP condition occurs.

In multi-master operation, the SDA line must be monitored to see if the signal level is the expected output level. This check only needs to be done when a high level is output. If a high level is expected and a low level is present, the device needs to release the SDA and SCL lines (set TRISC<4:3>). There are two stages where this arbitration can be lost, these are:

- · Address Transfer
- Data Transfer

When the slave logic is enabled, the slave continues to receive. If arbitration was lost during the address transfer stage, communication to the device may be in progress. If addressed an ACK pulse will be generated. If arbitration was lost during the data transfer stage, the device will need to re-transfer the data at a later time.

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR		Value on all other resets	
0Bh, 8Bh, 10Bh, 18Bh	INTCON	GIE	PEIE	TOIE	INTE	RBIE	T0IF	INTF	RBIF	0000	000x	0000	000u
0Ch	PIR1	PSPIF <sup>(1)</sup>	(2)	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000	0000	0000	0000
8Ch	PIE1	PSPIE <sup>(1)</sup>	(2)	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000	0000	0000	0000
13h	SSPBUF	Synchrono	ynchronous Serial Port Receive Buffer/Transmit Register							xxxx	xxxx	uuuu	uuuu
93h	SSPADD	Synchrono	us Serial	Port (I <sup>2</sup> C	mode) Ad	ldress Re	gister			0000	0000	0000	0000
14h	SSPCON	WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0	0000	0000	0000	0000
94h	SSPSTAT	SMP <sup>(3)</sup>	CKE <sup>(3)</sup>	D/A	Р	S	R/W	UA	BF	0000	0000	0000	0000
87h	TRISC	PORTC Da	ta Directi	on registe	er		-			1111	1111	1111	1111

#### TABLE 11-5: REGISTERS ASSOCIATED WITH I<sup>2</sup>C OPERATION

Legend: x = unknown, u = unchanged, - = unimplemented locations read as '0'.

Shaded cells are not used by SSP module in SPI mode.

Note 1: PSPIF and PSPIE are reserved on the PIC16C66, always maintain these bits clear.

2: PIR1<6> and PIE1<6> are reserved, always maintain these bits clear.

3: The SMP and CKE bits are implemented on the PIC16C66/67 only. All other PIC16C6X devices have these two bits unimplemented, read as '0'.

# 12.1 USART Baud Rate Generator (BRG)

#### Applicable Devices

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The BRG supports both the Asynchronous and Synchronous modes of the USART. It is a dedicated 8-bit baud rate generator. The SPBRG register controls the period of a free running 8-bit timer. In asynchronous mode bit BRGH (TXSTA<2>) also controls the baud rate. In synchronous mode bit BRGH is ignored. Table 12-1 shows the formula for computation of the baud rate for different USART modes which only apply in master mode (internal clock).

Given the desired baud rate and Fosc, the nearest integer value for the SPBRG register can be calculated using the formula in Table 12-1. From this, the error in baud rate can be determined.

Example 12-1 shows the calculation of the baud rate error for the following conditions:

Fosc = 16 MHz Desired Baud Rate = 9600 BRGH = 0 SYNC = 0

#### EXAMPLE 12-1: CALCULATING BAUD RATE ERROR

Desired Baud rate = Fosc / (64 (X + 1))

9600 = 16000000 / (64 (X + 1))

 $X = \lfloor 25.042 \rfloor = 25$ 

Calculated Baud Rate=16000000 / (64 (25 + 1))

= 9615

- Error = <u>(Calculated Baud Rate Desired Baud Rate)</u> Desired Baud Rate
  - = (9615 9600) / 9600

= 0.16%

It may be advantageous to use the high baud rate (BRGH = 1) even for slower baud clocks. This is because the FOSC/(16(X + 1)) equation can reduce the baud rate error in some cases.

Note:	For the PIC16C63/R63/65/65A/R65 the
	asynchronous high speed mode
	(BRGH = 1) may experience a high rate of
	receive errors. It is recommended that
	BRGH = 0. If you desire a higher baud rate
	than BRGH = 0 can support, refer to the
	device errata for additional information or
	use the PIC16C66/67.

Writing a new value to the SPBRG register, causes the BRG timer to be reset (or cleared), this ensures that the BRG does not wait for a timer overflow before outputting the new baud rate.

# TABLE 12-1: BAUD RATE FORMULA

SYNC	BRGH = 0 (Low Speed)	BRGH = 1 (High Speed)
0	(Asynchronous) Baud Rate = Fosc/(64(X+1))	Baud Rate = Fosc/(16(X+1))
1	(Synchronous) Baud Rate = FOSC/(4(X+1))	N/A

X = value in SPBRG (0 to 255)

# TABLE 12-2: REGISTERS ASSOCIATED WITH BAUD RATE GENERATOR

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value POF BO	e on R, R	Valu all o Res	e on other sets
98h	TXSTA	CSRC	TX9	TXEN	SYNC		BRGH	TRMT	TX9D	0000	-010	0000	-010
18h	RCSTA	SPEN	RX9	SREN	CREN		FERR	OERR	RX9D	0000 ·	-00x	0000	-00x
99h	SPBRG	Baud Rat	te Genera	tor Registe	ər					0000	0000	0000	0000

Legend: x = unknown, - = unimplemented read as '0'. Shaded cells are not used by the BRG.

### 13.5 Interrupts

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The PIC16C6X family has up to 11 sources of interrupt. The interrupt control register (INTCON) records individual interrupt requests in flag bits. It also has individual and global interrupt enable bits.

Note:	Individual interrupt flag bits are set regard-
	less of the status of their corresponding
	mask bit or global enable bit, GIE.

Global interrupt enable bit, GIE (INTCON<7>) enables (if set) all un-masked interrupts or disables (if cleared) all interrupts. When bit GIE is enabled, and an interrupt flag bit and mask bit are set, the interrupt will vector immediately. Individual interrupts can be disabled through their corresponding enable bits in the INTCON register. GIE is cleared on reset.

The "return from interrupt" instruction, RETFIE, exits the interrupt routine as well as sets the GIE bit, which re-enable interrupts.

The RB0/INT pin interrupt, the RB port change interrupt and the TMR0 overflow interrupt flag bits are contained in the INTCON register.

The peripheral interrupt flag bits are contained in special function registers PIR1 and PIR2. The corresponding interrupt enable bits are contained in special function registers PIE1 and PIE2 and the peripheral interrupt enable bit is contained in special function register INTCON.

When an interrupt is responded to, bit GIE is cleared to disable any further interrupts, the return address is pushed onto the stack and the PC is loaded with 0004h. Once in the interrupt service routine the source(s) of the interrupt can be determined by polling the interrupt flag bits. The interrupt flag bit(s) must be cleared in software before re-enabling interrupts to avoid recursive interrupts.

For external interrupt events, such as the RB0/INT pin or RB port change interrupt, the interrupt latency will be three or four instruction cycles. The exact latency depends when the interrupt event occurs (Figure 13-19). The latency is the same for one or two cycle instructions. Once in the interrupt service routine the source(s) of the interrupt can be determined by polling the interrupt flag bits. The interrupt flag bit(s) must be cleared in software before re-enabling interrupts to avoid infinite interrupt requests. Individual interrupt flag bits are set regardless of the status of their corresponding mask bit or the GIE bit.

- Note: For the PIC16C61/62/64/65, if an interrupt occurs while the Global Interrupt Enable bit, GIE is being cleared, bit GIE may unintentionally be re-enabled by the user's Interrupt Service Routine (the RETFIE instruction). The events that would cause this to occur are:
  - 1. An instruction clears the GIE bit while an interrupt is acknowledged
  - 2. The program branches to the Interrupt vector and executes the Interrupt Service Routine.
  - The Interrupt Service Routine completes with the execution of the RET-FIE instruction. This causes the GIE bit to be set (enables interrupts), and the program returns to the instruction after the one which was meant to disable interrupts.
  - 4. Perform the following to ensure that interrupts are globally disabled.

LOOP	BCF IN	NTCON,GIE	;Disable Global
			;Interrupt bit
	BTFSC	INTCON,GIE	;Global Interrupt
			;Disabled?
	GOTO	LOOP	;NO, try again
	:		;Yes, continue
			;with program flow

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#### 20.1 DC Characteristics: PIC16C63/65A-04 (Commercial, Industrial, Extended) PIC16C63/65A-10 (Commercial, Industrial, Extended) PIC16C63/65A-20 (Commercial, Industrial, Extended)

DC CH	ARACTERISTICS	<b>Standaı</b> Operatir	r <b>d Ope</b> i ng temp	r <b>ating</b> berature	Condi e -40 -40 0°0	tions (ι )°C ≤ )°C ≤ C ≤	unless otherwise stated) $\leq TA \leq +125^{\circ}C$ for extended, $\leq TA \leq +85^{\circ}C$ for industrial and $\leq TA \leq +70^{\circ}C$ for commercial
Param No.	Characteristic	Sym	Min	Тур†	Max	Units	Conditions
D001 D001A	Supply Voltage	Vdd	4.0 4.5	-	6.0 5.5	V V	XT, RC and LP osc configuration HS osc configuration
D002*	RAM Data Retention Voltage (Note 1)	Vdr	-	1.5	-	V	
D003	VDD start voltage to ensure internal Power-on Reset signal	VPOR	-	Vss	-	V	See section on Power-on Reset for details
D004*	VDD rise rate to ensure internal Power-on Reset signal	Svdd	0.05	-	-	V/ms	See section on Power-on Reset for details
D005	Brown-out Reset Voltage	BVDD	3.7	4.0	4.3	V	BODEN configuration bit is enabled
			3.7	4.0	4.4	V	Extended Range Only
D010	Supply Current (Note 2, 5)	IDD	-	2.7	5	mA	XT, RC, osc config Fosc = 4 MHz, VDD = 5.5V (Note 4)
D013			-	10	20	mA	HS osc config FOSC = 20 MHz, VDD = 5.5V
D015*	Brown-out Reset Current (Note 6)	$\Delta$ IBOR	-	350	425	μA	BOR enabled, VDD = 5.0V
D020 D021 D021A D021B	Power-down Current (Note 3, 5)	IPD	- - -	10.5 1.5 1.5 2.5	42 16 19 19	μΑ μΑ μΑ μΑ	VDD = 4.0V, WDT enabled,-40°C to +85°C VDD = 4.0V, WDT disabled,-0°C to +70°C VDD = 4.0V, WDT disabled,-40°C to +85°C VDD = 4.0V, WDT disabled,-40°C to +125°C
D023*	Brown-out Reset Current (Note 6)	AIBOR	-	350	425	μA	BOR enabled, VDD = 5.0V

These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.

The test conditions for all IDD measurements in active operation mode are:

OSC1 = external square wave, from rail to rail; all I/O pins tristated, pulled to VDD,

 $\overline{MCLR} = VDD$ ; WDT enabled/disabled as specified.

3: The power down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and Vss.

4: For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula Ir = VDD/2Rext (mA) with Rext in kOhm.

5: Timer1 oscillator (when enabled) adds approximately 20 μA to the specification. This value is from characterization and is for design guidance only. This is not tested.

6: The ∆ current is the additional current consumed when this peripheral is enabled. This current should be added to the base IDD or IPD measurement.

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### 20.3 DC Characteristics: PIC16C63/65A-04 (Commercial, Industrial, Extended) PIC16C63/65A-10 (Commercial, Industrial, Extended) PIC16C63/65A-20 (Commercial, Industrial, Extended) PIC16LC63/65A-04 (Commercial, Industrial)

		Standa	rd Operat	ing C	Condition	s (unle	ss otherwise stated)
		Operatir	ng tempera	ature	-40°0	C ≤ T	$A \le +125^{\circ}C$ for extended,
	RACTERISTICS				-40°0	C ≤T	$A \le +85^{\circ}C$ for industrial and
20 0114					0°C	≤T	$A \le +70^{\circ}C$ for commercial
		Operatir	ng voltage	Vdd	range as o	describ	ed in DC spec Section 20.1 and
		Section	20.2				
Param	Characteristic	Sym	Min	Тур	Max	Units	Conditions
NO.				T			
	Input Low Voltage						
	I/O ports	VIL					
D030	with TTL buffer		Vss	-	0.15Vdd	V	For entire VDD range
D030A			Vss	-	0.8V	V	$4.5V \le VDD \le 5.5V$
D031	with Schmitt Trigger buffer		Vss	-	0.2Vdd	V	
D032	MCLR, OSC1 (in RC mode)		Vss	-	0.2Vdd	V	
D033	OSC1 (in XT, HS and LP)		Vss	-	0.3Vdd	V	Note1
	Input High Voltage						
	I/O ports	VIH		-			
D040	with TTL buffer		2.0	-	VDD	V	$4.5V \le VDD \le 5.5V$
D040A			0.25VDD	-	Vdd	V	For entire VDD range
			+ 0.8V				-
D041	with Schmitt Trigger buffer		0.8VDD	-	Vdd	V	For entire VDD range
D042	MCLR		0.8VDD	-	Vdd	V	
D042A	OSC1 (XT, HS and LP)		0.7Vdd	-	Vdd	V	Note1
D043	OSC1 (in RC mode)		0.9Vdd	-	Vdd	V	
D070	PORTB weak pull-up current	IPURB	50	250	400	μΑ	VDD = 5V, VPIN = VSS
	Input Leakage Current (Notes 2, 3)						
D060	I/O ports	lı∟	-	-	±1	μA	Vss $\leq$ VPIN $\leq$ VDD, Pin at hi-
						•	impedance
D061	MCLR, RA4/T0CKI		-	-	±5	μA	$Vss \le VPIN \le VDD$
D063	OSC1		-	-	±5	μA	Vss $\leq$ VPIN $\leq$ VDD, XT, HS and
						•	LP osc configuration
	Output Low Voltage						-
D080	I/O ports	VOL	-	-	0.6	v	IOL = 8.5 mA, VDD = 4.5V,
							-40°C to +85°C
D080A			-	-	0.6	v	IOL = 7.0 mA, VDD = 4.5V,
							-40°C to +125°C
D083	OSC2/CLKOUT (RC osc config)		-	-	0.6	V	IOL = 1.6 mA, VDD = 4.5V,
							-40°C to +85°C
D083A			-	-	0.6	V	IOL = 1.2 mA, VDD = 4.5V,
							-40°C to +125°C

These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C6X be driven with external clock in RC mode.

 The leakage current on the MCLR/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as current sourced by the pin.

\*

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# TABLE 20-8: SPI MODE REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Тур†	Max	Units	Conditions
70*	TssL2scH, TssL2scL	$\overline{SS}\downarrow$ to SCK $\downarrow$ or SCK $\uparrow$ input	Тсү	_	—	ns	
71*	TscH	SCK input high time (slave mode)	TCY + 20	_	_	ns	
72*	TscL	SCK input low time (slave mode)	TCY + 20	_	_	ns	
73*	TdiV2scH, TdiV2scL	Setup time of SDI data input to SCK edge	50	_	—	ns	
74*	TscH2diL, TscL2diL	Hold time of SDI data input to SCK edge	50	_	_	ns	
75*	TdoR	SDO data output rise time	_	10	25	ns	
76*	TdoF	SDO data output fall time	—	10	25	ns	
77*	TssH2doZ	SS↑ to SDO output hi-impedance	10	_	50	ns	
78*	TscR	SCK output rise time (master mode)	—	10	25	ns	
79*	TscF	SCK output fall time (master mode)	—	10	25	ns	
80*	TscH2doV, TscL2doV	SDO data output valid after SCK edge	_	_	50	ns	

\* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

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