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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

### Details

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Product Status	Obsolete
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	I <sup>2</sup> C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	33
Program Memory Size	7KB (4K x 14)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	192 x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 6V
Data Converters	-
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lc65at-04-pt

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#### FIGURE 4-15: PIE1 REGISTER FOR PIC16C65/65A/R65/67 (ADDRESS 8Ch)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
PSPIE	—	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	R = Readable bit
bit7							bit0	W = Writable bit
								U = Unimplemented bit,
								read as '0'
								- n = Value at POR reset
bit 7:	1 = Enable				upt Enable b	bit		
	0 = Disable							
1.1.0				•				
bit 6:	Reserved:	Always ma	aintain this	oit clear.				
bit 5:	RCIE: USA							
	1 = Enable							
	0 = Disable			•				
bit 4:	TXIE: USA							
	1 = Enable							
	0 = Disable			•				
bit 3:	SSPIE: Syr			Interrupt Er	nable bit			
	1 = Enable							
	0 = Disable		•					
bit 2:	CCP1IE: C			bit				
	1 = Enable							
	0 = Disable		•					
bit 1:	TMR2IE: T							
	1 = Enable							
	0 = Disable				•			
bit 0:	TMR1IE: T				it			
	1 = Enable							
	0 = Disable	s the TMR	I OVERTION	nterrupt				

NOTES:

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#### 11.2.1 OPERATION OF SSP MODULE IN SPI MODE

Applicable Devices 61 62 624 R62 63 R63 64 644 R64 65 654 R65 66 67

The SPI mode allows 8-bits of data to be synchronously transmitted and received simultaneously. To accomplish communication, typically three pins are used:

Serial Data Out (SDO)

PIC16C6X

- Serial Data In (SDI)
- Serial Clock (SCK)

Additionally a fourth pin may be used when in a slave mode of operation:

Slave Select (SS)

When initializing the SPI, several options need to be specified. This is done by programming the appropriate control bits in the SSPCON register (SSPCON<5:0>). These control bits allow the following to be specified:

- Master Mode (SCK is the clock output)
- · Slave Mode (SCK is the clock input)
- Clock Polarity (Output/Input data on the Rising/ Falling edge of SCK)
- · Clock Rate (Master mode only)
- Slave Select Mode (Slave mode only)

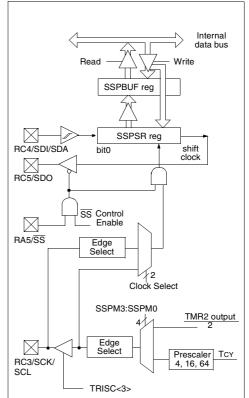
The SSP consists of a transmit/receive Shift Register (SSPSR) and a Buffer register (SSPBUF). The SSPSR shifts the data in and out of the device, MSb first. The SSPBUF holds the data that was written to the SSPSR, until the received data is ready. Once the 8-bits of data have been received, that byte is moved to the SSPBUF register. Then the Buffer Full bit, BF (SSPSTAT<0>) and flag bit SSPIF are set. This double buffering of the received data (SSPBUF) allows the next byte to start reception before reading the data that was just received. Any write to the SSPBUF register during transmission/reception of data will be ignored, and the write collision detect bit, WCOL (SSPCON<7>) will be set. User software must clear bit WCOL so that it can be determined if the following write(s) to the SSPBUF completed successfully. When the application software is expecting to receive valid data, the SSPBUF register should be read before the next byte of data to transfer is written to the SSPBUF register. The Buffer Full bit BF (SSPSTAT<0>) indicates when the SSPBUF register has been loaded with the received data (transmission is complete). When the SSPBUF is read, bit BF is cleared. This data may be irrelevant if the SPI is only a transmitter. Generally the SSP Interrupt is used to determine when the transmission/reception has completed. The SSPBUF register must be read and/or written. If the interrupt method is not going to be used, then software polling can be done to ensure that a write collision does not occur. Example 11-1 shows the loading of the SSPBUF (SSPSR) register for data transmission. The shaded instruction is only required if the received data is meaningful.

#### EXAMPLE 11-1: LOADING THE SSPBUF (SSPSR) REGISTER

		•	,	
	BSF	STATUS,	RP0	;Specify Bank 1
LOOP	BTFSS	SSPSTAT	, BF	;Has data been
				;received
				;(transmit
				;complete)?
	GOTO	LOOP		;No
	BCF	STATUS,	RP0	;Specify Bank 0
	MOVF	SSPBUF,	W	;W reg = contents
				; of SSPBUF
	MOVWF	RXDATA		;Save in user RAM
	MOVF	TXDATA,	W	;W reg = contents
				; of TXDATA
	MOVWF	SSPBUF		;New data to xmit

The block diagram of the SSP module, when in SPI mode (Figure 11-3), shows that the SSPSR register is not directly readable or writable, and can only be accessed from addressing the SSPBUF register. Additionally, the SSP status register (SSPSTAT) indicates the various status conditions.

#### FIGURE 11-3: SSP BLOCK DIAGRAM (SPI MODE)



#### 11.5.1.2 RECEPTION

When the  $R/\overline{W}$  bit of the address byte is clear and an address match occurs, the  $R/\overline{W}$  bit of the SSPSTAT register is cleared. The received address is loaded into the SSPBUF register.

When the address byte overflow condition exists, then no acknowledge ( $\overline{ACK}$ ) pulse is given. An overflow condition is defined as either bit BF (SSPSTAT<0>) is set or bit SSPOV (SSPCON<6>) is set. An SSP interrupt is generated for each data transfer byte. Flag bit SSPIF (PIR1<3>) must be cleared in software. The SSPSTAT register is used to determine the status of the byte.

### FIGURE 11-25: I<sup>2</sup>C WAVEFORMS FOR RECEPTION (7-BIT ADDRESS)

Receiving Address         R/W=0         Receiving Data         ACK         Receiving Data         ACK           SDA         -	F 7 I I I I / I PI - A
SSPIF (PIR1<3>) Cleared in software BF (SSPSTAT<0>) SSPBUF register is read	Bus Master terminates transfer
SSPOV (SSPCON<6>) Bit SSPOV is set because the SSPBUF register is still full.	
ACK is not sent.	

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### FIGURE 12-2: RCSTA: RECEIVE STATUS AND CONTROL REGISTER (ADDRESS 18h)

R/W-0	R/W-0	R/W-0	R/W-0	U-0	R-0	R-0	R-x		
SPEN	RX9	SREN	CREN	—	FERR	OERR	RX9D	R	= Readable bit
bit7							bitO	W U - n x	<ul> <li>Writable bit</li> <li>Unimplemented</li> <li>bit, read as '0'</li> <li>Value at POR rese</li> <li>unknown</li> </ul>
bit 7:	SPEN: Ser (Configures 1 = Serial p 0 = Serial p	s RC7/RX/l	DT and RC d	6/TX/CK	pins as seri	al port pins	s when bits	TRIS	C<7:6> are set)
bit 6:	<b>RX9</b> : 9-bit I 1 = Selects 0 = Selects	9-bit rece	otion						
bit 5:	SREN: Sing	gle Receiv	e Enable bi	t					
	Asynchrone Don't care	ous mode							
	$\frac{Synchronof}{1 = Enables}$ $0 = Disables$ This bit is c	s single ree s single re	ceive ceive	is comple	ete.				
	Synchrono Unused in t		<u>slave</u>						
bit 4:	CREN: Cor	ntinuous R	eceive Ena	ble bit					
	$\frac{\text{Asynchrono}}{1 = \text{Enable}}$ $0 = \text{Disable}$	s continuo							
	$\frac{\text{Synchronor}}{1 = \text{Enables}}$ $0 = \text{Disables}$	s continuo		until enabl	le bit CREN	l is cleared	(CREN ov	erride	s SREN)
bit 3:	Unimplem	ented: Rea	ad as '0'						
bit 2:	FERR: Fran 1 = Framing 0 = No fran	g error (Ca		ed by rea	ding RCRE	G register	and receive	e next	valid byte)
bit 1:	<b>OERR</b> : Ove 1 = Overrun 0 = No ove	n error (Ca		d by clea	ring bit CRI	EN)			
bit 0:	<b>RX9D</b> : 9th								

NOTES:

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COMF	Complement f	DECFSZ	Decrement f, Skip if 0
Syntax:	[ <i>label</i> ] COMF f,d	Syntax:	[label] DECFSZ f,d
Operands:	$\begin{array}{l} 0\leq f\leq 127\\ d\in [0,1] \end{array}$	Operands:	$\begin{array}{l} 0 \leq f \leq 127 \\ d \in [0,1] \end{array}$
Operation:	$(\bar{f}) \rightarrow (destination)$	Operation:	(f) - 1 $\rightarrow$ (destination);
Status Affected:	Z		skip if result = 0
Encoding:	00 1001 dfff ffff	Status Affected:	None
Description:	The contents of register 'f' are comple- mented. If 'd' is 0 the result is stored in	Encoding:	00 1011 dfff ffff
Words: Cycles:	W. If 'd' is 1 the result is stored back in register 'f'. 1	Description:	The contents of register 'f' are decre- mented. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'. If the result is 1, the next instruction, is executed. If the result is 0, then a NOP is
Q Cycle Activity:	Q1 Q2 Q3 Q4		executed instead making it a 2TCY instruc- tion.
, ,	Decode Read Process Write to	Words:	1
	register data destination	Cycles:	1(2)
		Q Cycle Activity:	Q1 Q2 Q3 Q4
Example	COMF REG1, 0 Before Instruction	, ,	Decode Read Process Write to register 'f' data destination
	$\begin{array}{rcl} REG1 &=& 0x13\\ After Instruction & \\ REG1 &=& 0x13\\ W &=& 0xEC \end{array}$	lf Skip:	Q1         Q2         Q3         Q4           No- Operation         Operation         Operation         Operation
DECF	Decrement f		
Syntax:	[ <i>label</i> ] DECF f,d	Example	HERE DECFSZ CNT, 1 GOTO LOOP
Operands:	$0 \le f \le 127$		CONTINUE •
	d ∈ [0,1]		•
Operation:	$d \in [0,1]$ (f) - 1 $\rightarrow$ (destination)		• Before Instruction
Operation: Status Affected:			• Before Instruction PC = address HERE
•	(f) - 1 $\rightarrow$ (destination)		PC = address HERE After Instruction
Status Affected:	(f) - 1 → (destination) Z 00 0011 dfff ffff Decrement register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is		PC = address HERE After Instruction CNT = CNT - 1 if CNT = 0, PC = address CONTINUE
Status Affected: Encoding:	(f) - 1 → (destination) Z 00 0011 dfff ffff		$\begin{array}{rcl} PC &=& address {}_{HERE}\\ \textbf{After Instruction}\\ & CNT &=& CNT-1\\ & & & & \\ & & & & \\ & & & & \\ & & & &$
Status Affected: Encoding: Description: Words:	(f) - 1 $\rightarrow$ (destination) Z Decrement register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'.		PC = address HERE After Instruction CNT = CNT - 1 if CNT = 0, PC = address CONTINUE
Status Affected: Encoding: Description: Words: Cycles:	(f) - 1 $\rightarrow$ (destination) Z Decrement register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'.		PC = address HERE After Instruction CNT = CNT - 1 if CNT = 0, PC = address CONTINUE if CNT ≠ 0,
Status Affected: Encoding: Description: Words:	(f) - 1 $\rightarrow$ (destination) Z 00 0011 dfff ffff Decrement register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'. 1 1		$\begin{array}{rcl} PC &=& address \mbox{ HERE} \\ \mbox{After Instruction} \\ CNT &=& CNT - 1 \\ \mbox{if CNT} &=& 0, \\ PC &=& address \mbox{ continue} \\ \mbox{if CNT} &\neq& 0, \\ \end{array}$
Status Affected: Encoding: Description: Words: Cycles:	(f) - 1 $\rightarrow$ (destination) Z 00 0011 dfff ffff Decrement register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'. 1 1 Q1 Q2 Q3 Q4 Decode Read Process Write to data destination		PC = address HERE After Instruction CNT = CNT - 1 if CNT = 0, PC = address CONTINUE if CNT ≠ 0,
Status Affected: Encoding: Description: Words: Cycles: Q Cycle Activity:	$ \begin{array}{c c} (f) - 1 \rightarrow (destination) \\ \hline Z \\ \hline 00 & 0011 & dfff & ffff \\ \hline Decrement register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'. \\ 1 & & \\ 1 & & \\ Q1 & Q2 & Q3 & Q4 \\ \hline \hline Decode & Read & Process & Write to destination \\ \hline & & \\ f'' & & \\ \end{array} $		$\begin{array}{rcl} PC &=& address {}_{HERE}\\ \textbf{After Instruction}\\ & CNT &=& CNT-1\\ & & & & \\ & & & & \\ & & & & \\ & & & &$
Status Affected: Encoding: Description: Words: Cycles: Q Cycle Activity:	(f) - 1 $\rightarrow$ (destination) Z 00  0011  dfff  ffff Decrement register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'. 1 2 Q1 Q2 Q3 Q4 Decode Read Process Write to data destination DECF CNT, 1 Before Instruction CNT = 0x01		PC = address HERE After Instruction CNT = CNT - 1 if CNT = 0, PC = address CONTINUE if CNT ≠ 0,
Status Affected: Encoding: Description: Words: Cycles: Q Cycle Activity:	(f) - 1 → (destination) Z 00 0011 dfff fff Decrement register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'. 1 1 Q1 Q2 Q3 Q4 Decode Read Process Write to register data destination DECF CNT, 1 Before Instruction CNT = 0x01 Z = 0		$\begin{array}{rcl} PC &=& address \mbox{ HERE} \\ \mbox{After Instruction} \\ CNT &=& CNT - 1 \\ \mbox{if CNT} &=& 0, \\ PC &=& address \mbox{ CONTINUE} \\ \mbox{if CNT} &\neq& 0, \\ \end{array}$
Status Affected: Encoding: Description: Words: Cycles: Q Cycle Activity:	(f) - 1 $\rightarrow$ (destination) Z 00  0011  dfff  ffff Decrement register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'. 1 2 Q1 Q2 Q3 Q4 Decode Read Process Write to data destination DECF CNT, 1 Before Instruction CNT = 0x01		$\begin{array}{rcl} PC &=& address \mbox{ HERE} \\ \mbox{After Instruction} \\ CNT &=& CNT - 1 \\ \mbox{if CNT} &=& 0, \\ PC &=& address \mbox{ continue} \\ \mbox{if CNT} &\neq& 0, \\ \end{array}$

SUBWF	Subtract	W from f					
Syntax:	[ label ]	SUBWF	f,d				
Operands:	$\begin{array}{l} 0 \leq f \leq 127 \\ d \in \left[0,1\right] \end{array}$	,					
Operation:	(f) - (W) $\rightarrow$	(destina	tion)				
Status Affected:	C, DC, Z						
Encoding:	00	0010	dfff	ffff			
Description:	ister from re stored in the	Subtract (2's complement method) W reg- ister from register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'.					
Words:	1						
Cycles:	1						
Q Cycle Activity:	Q1	Q2	Q3	Q4			
	Decode	Read register 'f'	Process data	Write to destination			
Example 1:	SUBWF	reg1,1					
	Before Ins	truction					
	REG1	=	3				
	W C	=	2 ?				
	Z	=	?				
	After Instru	uction					
	REG1	=	1				
	W C	=	2 1; result is	nositive			
	z	=	0	poolavo			
Example 2:	Before Ins	truction					
	REG1	=	2				
	W C	=	2 ?				
	Z	=	?				
	After Instru	uction					
	REG1	=	0				
	W C	=	2 1; result is	7010			
	z	=	1	2010			
Example 3:	Before Ins	truction					
	REG1	=	1				
	W C	=	2 ?				
	z	=	?				
	After Instru	uction					
	REG1	=	0xFF				
	W C	=	2 0; result is	negative			
	z	=	0	guivo			

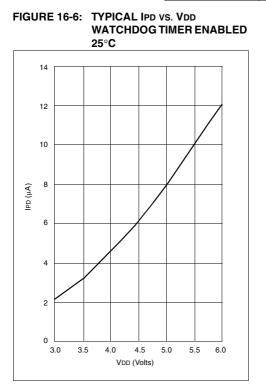
SWAPF	Swap Ni	bbles in	f					
Syntax:	[label]	SWAPF 1	,d					
Operands:	$0 \le f \le 12$ $d \in [0,1]$	$\begin{array}{l} 0 \leq f \leq 127 \\ d \in [0,1] \end{array}$						
Operation:	· · ·	$(f<3:0>) \rightarrow (destination<7:4>),$ $(f<7:4>) \rightarrow (destination<3:0>)$						
Status Affected:	None	None						
Encoding:	0 0	1110	dfff	ffff				
Description:	The upper and lower nibbles of register 'f' are exchanged. If 'd' is 0 the result is placed in W register. If 'd' is 1 the result is placed in register 'f'.							
Words:	1							
Cycles:	1							
Q Cycle Activity:	Q1	Q2	Q3	Q4				
	Decode	Read register 'f'	Process data	Write to destination				
Example	SWAPF	REG,	0					
	Before In	struction						
		REG1	= 0x/	A5				
	After Inst	truction						
		REG1 W	= 0x/ = 0x5	.0				

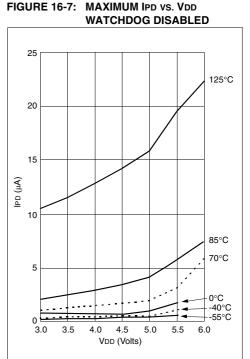
TRIS	Load TR	IS Regis	ster		
Syntax:	[label]	TRIS	f		
Operands:	$5 \leq f \leq 7$				
Operation:	$(W) \rightarrow TI$	RIS regis	ster f;		
Status Affected:	None				
Encoding:	00	0000	0110	Offf	
Description:	The instruction is supported for code compatibility with the PIC16C5X prod- ucts. Since TRIS registers are read- able and writable, the user can directly address them.				
Words:	1				
Cycles:	1				
Example					
	To maintain upward compatibility with future PIC16CXX products, do not use this instruction.				

XORLW	Exclusive OR Literal with W								
Syntax:	[ <i>label</i> ]	XORLV	Vk						
Operands:	$0 \le k \le 2$	$0 \le k \le 255$							
Operation:	(W) .XO	$R. k \to (N$	N)						
Status Affected:	Z								
Encoding:	11	1010	kkkk	kkkk					
Description:	The contents of the W register are XOR'ed with the eight bit literal 'k'. The result is placed in the W regis- ter.								
Words:	1								
Cycles:	1								
Q Cycle Activity:	Q1	Q2	Q3	Q4					
	Decode	Read literal 'k'	Process data	Write to W					
Example:	XORLW	0xAF							
	Before Ir	nstruction	n						
		W =	0xB5						
	After Ins	truction							
		W =	0x1A						

XORWF	Exclusiv	e OR W	with f				
Syntax:	[label]	XORWF	f,d				
Operands:	$\begin{array}{l} 0 \leq f \leq 12 \\ d \in [0,1] \end{array}$	27					
Operation:	(W) .XOR. (f) $\rightarrow$ (destination)						
Status Affected:	Z						
Encoding:	00	0110	dfff	ffff			
Description:	Exclusive OR the contents of the W register with register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'.						
Words:	1						
Cycles:	1						
Q Cycle Activity:	Q1	Q2	Q3	Q4			
	Decode	Read register 'f'	Process data	Write to destination			
Example	XORWF	REG	1				
	Before In	struction	I				
		REG W	0/1	AF B5			
	After Inst	ruction					
		REG W	0/1	1A B5			

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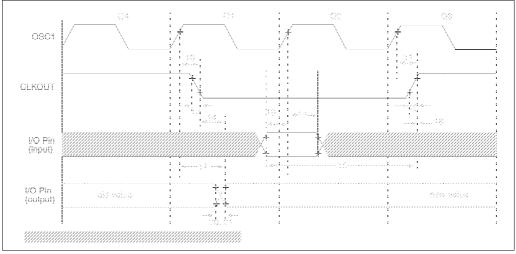




Data based on matrix samples. See first page of this section for details.

Applicable Devices 61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

### FIGURE 17-3: CLKOUT AND I/O TIMING



### TABLE 17-3: CLKOUT AND I/O TIMING REQUIREMENTS

Parameters	Sym	Characteristic		Min	Typ†	Max	Units	Conditions
10*	TosH2ckL	OSC1↑ to CLKOUT↓		-	75	200	ns	Note 1
11*	TosH2ckH	OSC1 <sup>↑</sup> to CLKOUT <sup>↑</sup>		_	75	200	ns	Note 1
12*	TckR	CLKOUT rise time		—	35	100	ns	Note 1
13*	TckF	CLKOUT fall time	—	35	100	ns	Note 1	
14*	TckL2ioV	CLKOUT $\downarrow$ to Port out valid	—		0.5TCY + 20	ns	Note 1	
15*	TioV2ckH	Port in valid before CLKOUT	Tosc + 200		_	ns	Note 1	
16*	TckH2ioI	Port in hold after CLKOUT 1	0		_	ns	Note 1	
17*	TosH2ioV	OSC1↑ (Q1 cycle) to Port out valid		—	50	150	ns	
18*	18* TosH2iol OSC1↑ (Q2 cycle) to Port	PIC16 <b>C</b> 62/64	100		_	ns		
		input invalid (I/O in hold time)	PIC16LC62/64	200		_	ns	
19*	TioV2osH	Port input valid to OSC1↑ (I/O in setup time)		0		—	ns	
20*	TioR	Port output rise time	PIC16 <b>C</b> 62/64	—	10	40	ns	
			PIC16LC62/64	—		80	ns	
21*	TioF	Port output fall time	PIC16 <b>C</b> 62/64	—	10	40	ns	
			PIC16LC62/64	—		80	ns	
22††*	Tinp	INT pin high or low time	•	Тсү	_	—	ns	
23††*	Trbp	RB7:RB4 change INT high or	low time	Тсү	_	—	ns	

\* These parameters are characterized but not tested.

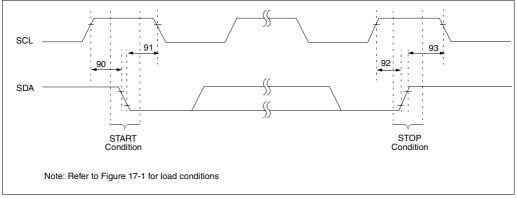
† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

these parameters are asynchronous events not related to any internal clock edge.

Note 1: Measurements are taken in RC Mode where CLKOUT output is 4 x Tosc.

Applicable Devices 61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

## FIGURE 17-9: I<sup>2</sup>C BUS START/STOP BITS TIMING

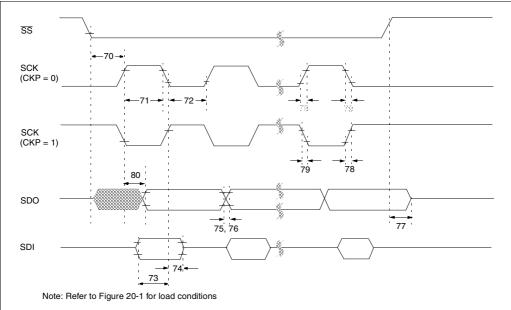


## TABLE 17-9: I<sup>2</sup>C BUS START/STOP BITS REQUIREMENTS

Parameter No.	Sym	Characteristic		Min	Тур	Max	Units	Conditions
90	TSU:STA	START condition	100 kHz mode	4700	—	—	-	Only relevant for repeated START
		Setup time	400 kHz mode	600	_	_	ns	condition
91	THD:STA	START condition	100 kHz mode	4000	_	_		After this period the first clock
		Hold time	400 kHz mode	600	_	—	ns	pulse is generated
92	TSU:STO	STOP condition	100 kHz mode	4700	_	_		
		Setup time	400 kHz mode	600		_	ns	
93	THD:STO	STOP condition	100 kHz mode	4000	_	_		
		Hold time	400 kHz mode	600	—	—	ns	

### Applicable Devices 61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67





#### TABLE 20-8: SPI MODE REQUIREMENTS

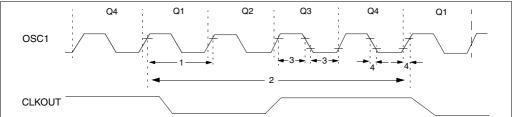
Parameter No.	Sym	Characteristic	Min	Тур†	Max	Units	Conditions
70*	TssL2scH, TssL2scL	$\overline{SS}\downarrow$ to SCK $\downarrow$ or SCK $\uparrow$ input	Тсү	—	—	ns	
71*	TscH	SCK input high time (slave mode)	Tcy + 20	_	_	ns	
72*	TscL	SCK input low time (slave mode)	Tcy + 20	_	_	ns	
73*	TdiV2scH, TdiV2scL	Setup time of SDI data input to SCK edge	50	—	—	ns	
74*	TscH2diL, TscL2diL	Hold time of SDI data input to SCK edge	50	_	—	ns	
75*	TdoR	SDO data output rise time	_	10	25	ns	
76*	TdoF	SDO data output fall time		10	25	ns	
77*	TssH2doZ	SS↑ to SDO output hi-impedance	10	_	50	ns	
78*	TscR	SCK output rise time (master mode)		10	25	ns	
79*	TscF	SCK output fall time (master mode)	_	10	25	ns	
80*	TscH2doV, TscL2doV	SDO data output valid after SCK edge	_	_	50	ns	

\* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

#### 21.5 <u>Timing Diagrams and Specifications</u>

#### FIGURE 21-2: EXTERNAL CLOCK TIMING



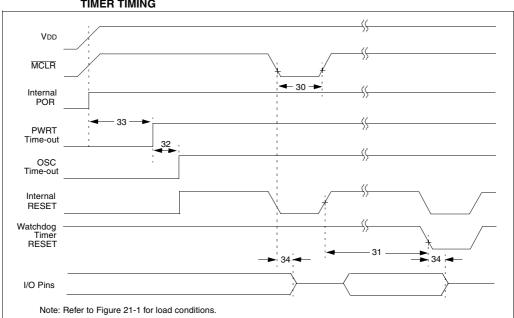
#### TABLE 21-2: EXTERNAL CLOCK TIMING REQUIREMENTS

Param No.	Sym	Characteristic	Min	Тур†	Max	Units	Conditions
	Fosc	External CLKIN Frequency	DC	-	4	MHz	XT and RC osc mode
		(Note 1)	DC	_	4	MHz	HS osc mode (-04)
			DC	_	10	MHz	HS osc mode (-10)
			DC	_	20	MHz	HS osc mode (-20)
			DC	_	200	kHz	LP osc mode
		Oscillator Frequency	DC	-	4	MHz	RC osc mode
		(Note 1)	0.1	_	4	MHz	XT osc mode
			4	_	20	MHz	HS osc mode
			5	_	200	kHz	LP osc mode
1	Tosc	External CLKIN Period	250	-	_	ns	XT and RC osc mode
		(Note 1)	250	_	_	ns	HS osc mode (-04)
			100	_	_	ns	HS osc mode (-10)
			50	_	_	ns	HS osc mode (-20)
			5	_	_	μs	LP osc mode
		Oscillator Period	250		—	ns	RC osc mode
		(Note 1)	250	_	10,000	ns	XT osc mode
			250	_	250	ns	HS osc mode (-04)
			100	_	250	ns	HS osc mode (-10)
			50	_	250	ns	HS osc mode (-20)
			5	_	_	μs	LP osc mode
2	Тсү	Instruction Cycle Time (Note 1)	200	Тсү	DC	ns	Tcy = 4/Fosc
3*	TosL,	External Clock in (OSC1) High or	100		—	ns	XT oscillator
	TosH	Low Time	2.5	—	—	μs	LP oscillator
			15	—	—	ns	HS oscillator
4*	TosR,	External Clock in (OSC1) Rise or	_	I	25	ns	XT oscillator
	TosF	Fall Time	—	—	50	ns	LP oscillator
			_	_	15	ns	HS oscillator

These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Instruction cycle period (TcY) equals four times the input oscillator time-base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min." values with an external clock applied to the OSC1/CLKIN pin. When an external clock input is used, the "Max." cycle time limit is "DC" (no clock) for all devices.



## FIGURE 21-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING

#### FIGURE 21-5: BROWN-OUT RESET TIMING

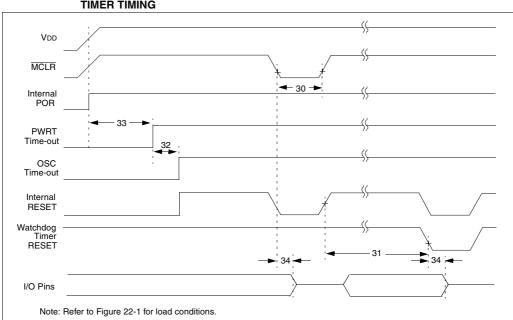


# TABLE 21-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, POWER-UP TIMER, AND BROWN-OUT RESET REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Тур†	Max	Units	Conditions
30	TmcL	MCLR Pulse Width (low)	2	-	—	μs	VDD = 5V, -40°C to +125°C
31*	Twdt	Watchdog Timer Time-out Period (No Prescaler)	7	18	33	ms	VDD = 5V, -40°C to +125°C
32	Tost	Oscillation Start-up Timer Period	—	1024 Tosc	_	_	TOSC = OSC1 period
33*	Tpwrt	Power-up Timer Period	28	72	132	ms	VDD = 5V, -40°C to +125°C
34	Tioz	I/O Hi-impedance from MCLR Low or WDT reset	—	_	2.1	μs	
35	TBOR	Brown-out Reset Pulse Width	100	_	_	μs	$V$ DD $\leq$ BVDD (D005)

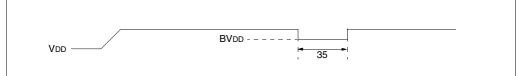
\* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.



## FIGURE 22-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING

#### FIGURE 22-5: BROWN-OUT RESET TIMING

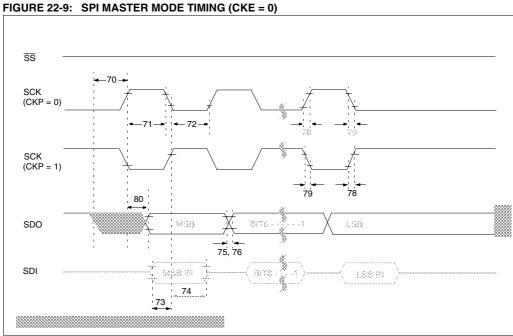


# TABLE 22-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, POWER-UP TIMER, AND BROWN-OUT RESET REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Тур†	Max	Units	Conditions
30	TmcL	MCLR Pulse Width (low)	2	—		μs	VDD = 5V, -40°C to +125°C
31*	Twdt	Watchdog Timer Time-out Period (No Prescaler)	7	18	33	ms	VDD = 5V, -40°C to +125°C
32	Tost	Oscillation Start-up Timer Period	-	1024 Tosc		_	TOSC = OSC1 period
33*	Tpwrt	Power-up Timer Period	28	72	132	ms	VDD = 5V, -40°C to +125°C
34	Tioz	I/O Hi-impedance from MCLR Low or WDT reset		_	2.1	μs	
35	TBOR	Brown-out Reset Pulse Width	100	_	l	μs	$V$ DD $\leq$ BVDD (D005)

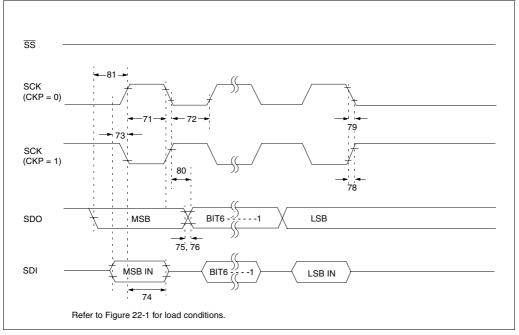
\* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.



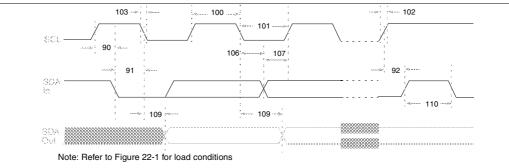
## Applicable Devices 61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67





#### Applicable Devices 61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

### FIGURE 22-14: I<sup>2</sup>C BUS DATA TIMING



#### TABLE 22-10: I<sup>2</sup>C BUS DATA REQUIREMENTS

Parameter No.	Sym	Characteristic		Min	Max	Units	Conditions
100*	Тнідн	Clock high time	100 kHz mode	4.0	-	μs	Device must operate at a mini- mum of 1.5 MHz
			400 kHz mode	0.6	_	μs	Device must operate at a mini- mum of 10 MHz
			SSP Module	1.5TCY	—		
101*	TLOW	Clock low time	100 kHz mode	4.7	_	μs	Device must operate at a mini- mum of 1.5 MHz
			400 kHz mode	1.3	_	μs	Device must operate at a mini- mum of 10 MHz
			SSP Module	1.5TCY	—		
102*	TR	SDA and SCL rise	100 kHz mode	—	1000	ns	
		time	400 kHz mode	20 + 0.1Cb	300	ns	Cb is specified to be from 10-400 pF
103*	TF	SDA and SCL fall time	100 kHz mode	—	300	ns	
			400 kHz mode	20 + 0.1Cb	300	ns	Cb is specified to be from 10-400 pF
90*	TSU:STA	START condition	100 kHz mode	4.7	—	μs	Only relevant for repeated
		setup time	400 kHz mode	0.6	—	μs	START condition
91*	THD:STA	START condition hold	100 kHz mode	4.0	—	μs	After this period the first clock
		time	400 kHz mode	0.6	—	μs	pulse is generated
106*	THD:DAT	Data input hold time	100 kHz mode	0	—	ns	
			400 kHz mode	0	0.9	μS	
107*	TSU:DAT	Data input setup time	100 kHz mode	250	—	ns	Note 2
			400 kHz mode	100	—	ns	
92*	TSU:STO	STOP condition setup	100 kHz mode	4.7	—	μs	
		time	400 kHz mode	0.6	—	μs	
109*	TAA	Output valid from	100 kHz mode	—	3500	ns	Note 1
		clock	400 kHz mode	—	—	ns	
110*	TBUF	Bus free time	100 kHz mode	4.7	—	μS	Time the bus must be free
			400 kHz mode	1.3	_	μs	before a new transmission can start
	Cb	Bus capacitive loading		—	400	pF	

These parameters are characterized but not tested.

Note 1: As a transmitter, the device must provide this internal minimum delay time to bridge the undefined region (min. 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

2: A fast-mode (400 kHz) I<sup>2</sup>C-bus device can be used in a standard-mode (100 kHz) I<sup>2</sup>C-bus system, but the requirement Tsu:DAT ≥ 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line TR max.+tsu;DAT = 1000 + 250 = 1250 ns (according to the standard-mode I<sup>2</sup>C bus specification) before the SCL line is released.

### **PIN COMPATIBILITY**

Devices that have the same package type and VDD, VSs and  $\overline{\text{MCLR}}$  pin locations are said to be pin compatible. This allows these different devices to operate in the same socket. Compatible devices may only requires minor software modification to allow proper operation in the application socket (ex., PIC16C56 and PIC16C61 devices). Not all devices in the same package size are pin compatible; for example, the PIC16C62 is compatible with the PIC16C63, but not the PIC16C55.

Pin compatibility does not mean that the devices offer the same features. As an example, the PIC16C54 is pin compatible with the PIC16C71, but does not have an A/D converter, weak pull-ups on PORTB, or interrupts.

Pin Compatible Devices	Package
PIC12C508, PIC12C509, PIC12C671, PIC12C672	8-pin
PIC16C154, PIC16CR154, PIC16C156, PIC16CR156, PIC16C158, PIC16CR158, PIC16C52, PIC16C54, PIC16C54A, PIC16C56, PIC16C58A, PIC16CR58A, PIC16C554, PIC16CR58A, PIC16C554, PIC16C556, PIC16C558 PIC16C620, PIC16C621, PIC16C622 PIC16C641, PIC16C642, PIC16C661, PIC16C662 PIC16C710, PIC16C71, PIC16C711, PIC16C715 PIC16F83, PIC16CR83, PIC16F84A, PIC16CR84	18-pin, 20-pin
PIC16C55, PIC16C57, PIC16CR57B	28-pin
PIC16CR62, PIC16C62A, PIC16C63, PIC16CR63, PIC16C66, PIC16C72, PIC16C73A, PIC16C76	28-pin
PIC16CR64, PIC16C64A, PIC16C65A, PIC16CR65, PIC16C67, PIC16C74A, PIC16C77	40-pin
PIC17CR42, PIC17C42A, PIC17C43, PIC17CR43, PIC17C44	40-pin
PIC16C923, PIC16C924	64/68-pin
PIC17C756, PIC17C752	64/68-pin

#### TABLE F-1: PIN COMPATIBLE DEVICES

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