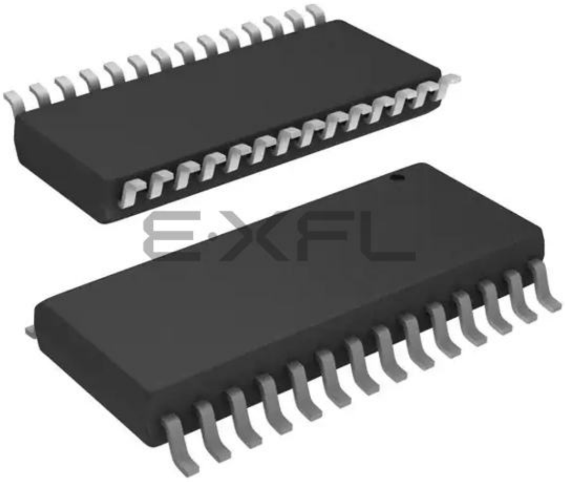
# Microchip Technology - PIC16LC66-04/SO Datasheet



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### Applications of "Embedded - Microcontrollers"

| **Details** | |
|---|---|
| Product Status | Obsolete |
| Core Processor | PIC |
| Core Size | 8-Bit |
| Speed | 4MHz |
| Connectivity | I²C, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, POR, PWM, WDT |
| Number of I/O | 22 |
| Program Memory Size | 14KB (8K x 14) |
| Program Memory Type | OTP |
| EEPROM Size | - |
| RAM Size | 368 x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.5V ~ 6V |
| Data Converters | - |
| Oscillator Type | External |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 28-SOIC (0.295", 7.50mm Width) |
| Supplier Device Package | 28-SOIC |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic16lc66-04-so |

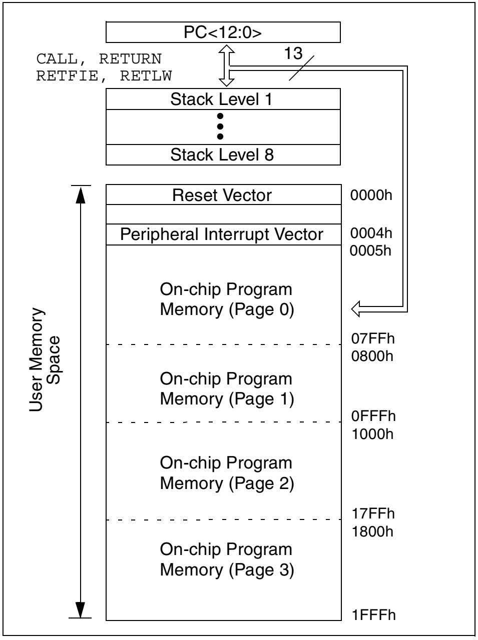
### TABLE 3-1: PIC16C61 PINOUT DESCRIPTION

| Pin Name | DIP Pin# | SOIC Pin# | Pin Type | Buffer Type | Description |
|---|---|---|---|---|---|
| OSC1/CLKIN | 16 | 16 | I | ST/CMOS(1) | Oscillator crystal input/external clock source input. |
| OSC2/CLKOUT | 15 | 15 | O | — | Oscillator crystal output. Connects to crystal or resonator in crystal oscillator mode. In RC mode, the pin outputs CLKOUT which has 1/4 the frequency of OSC1, and denotes the instruction cycle rate. |
| $\overline{\text{MCLR}}$/VPP | 4 | 4 | I/P | ST | Master clear reset input or programming voltage input. This pin is an active low reset to the device. |
| | | | | | PORTA is a bi-directional I/O port. |
| RA0 | 17 | 17 | I/O | TTL | |
| RA1 | 18 | 18 | I/O | TTL | |
| RA2 | 1 | 1 | I/O | TTL | |
| RA3 | 2 | 2 | I/O | TTL | |
| RA4/T0CKI | 3 | 3 | I/O | ST | RA4 can also be the clock input to the Timer0 timer/counter. Output is open drain type. |
| | | | | | PORTB is a bi-directional I/O port. PORTB can be software programmed for internal weak pull-up on all inputs. |
| RB0/INT | 6 | 6 | I/O | TTL/ST(2) | RB0 can also be the external interrupt pin. |
| RB1 | 7 | 7 | I/O | TTL | |
| RB2 | 8 | 8 | I/O | TTL | |
| RB3 | 9 | 9 | I/O | TTL | |
| RB4 | 10 | 10 | I/O | TTL | Interrupt on change pin. |
| RB5 | 11 | 11 | I/O | TTL | Interrupt on change pin. |
| RB6 | 12 | 12 | I/O | TTL/ST(3) | Interrupt on change pin. Serial programming clock. |
| RB7 | 13 | 13 | I/O | TTL/ST(3) | Interrupt on change pin. Serial programming data. |
| VSS | 5 | 5 | P | — | Ground reference for logic and I/O pins. |
| VDD | 14 | 14 | P | — | Positive supply for logic and I/O pins. |

Legend: I = input O = output I/O = input/output P = power
— = Not used TTL = TTL input ST = Schmitt Trigger input

Note 1: This buffer is a Schmitt Trigger input when configured in RC oscillator mode and a CMOS input otherwise.
2: This buffer is a Schmitt Trigger input when configured as the external interrupt.
3: This buffer is a Schmitt Trigger input when used in serial programming mode.

**FIGURE 4-4: PIC16C66/67 PROGRAM MEMORY MAP AND STACK**



## 4.2 Data Memory Organization

| Applicable Devices | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 61 | 62 | 62A | R62 | 63 | R63 | 64 | 64A | R64 | 65 | 65A | R65 | 66 | 67 |

The data memory is partitioned into multiple banks which contain the General Purpose Registers and the Special Function Registers. Bits RP1 and RP0 are the bank select bits.

RP1:RP0 (STATUS<6:5>)
= 00 → Bank0
= 01 → Bank1
= 10 → Bank2
= 11 → Bank3

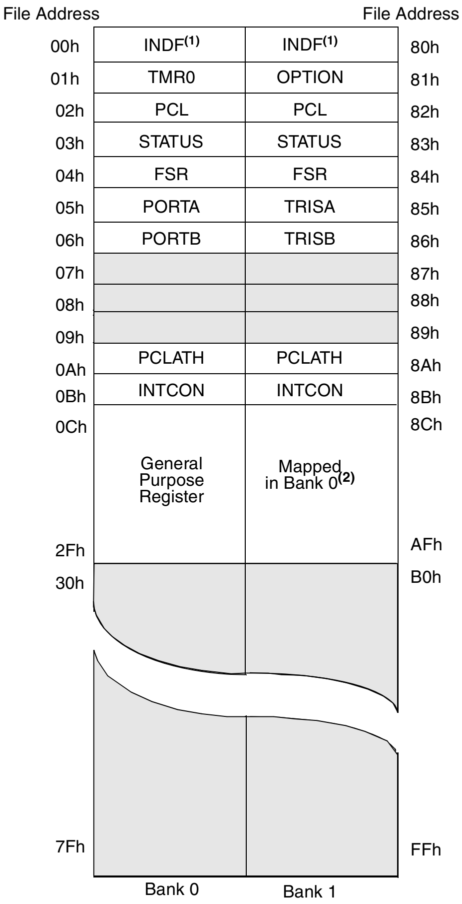
Each bank extends up to 7Fh (128 bytes). The lower locations of each bank are reserved for the Special Function Registers. Above the Special Function Registers are General Purpose Registers, implemented as static RAM. All implemented banks contain special function registers. Some “high use” special function registers from one bank may be mirrored in another bank for code reduction and quicker access.

### 4.2.1 GENERAL PURPOSE REGISTERS

These registers are accessed either directly or indirectly through the File Select Register (FSR) (Section 4.5).

For the PIC16C61, general purpose register locations 8Ch-AFh of Bank 1 are not physically implemented. These locations are mapped into 0Ch-2Fh of Bank 0.

**FIGURE 4-5: PIC16C61 REGISTER FILE MAP**



| File Address | | | File Address |
|---|---|---|---|
| 00h | INDF[1] | INDF[1] | 80h |
| 01h | TMR0 | OPTION | 81h |
| 02h | PCL | PCL | 82h |
| 03h | STATUS | STATUS | 83h |
| 04h | FSR | FSR | 84h |
| 05h | PORTA | TRISA | 85h |
| 06h | PORTB | TRISB | 86h |
| 07h | ▨ | ▨ | 87h |
| 08h | ▨ | ▨ | 88h |
| 09h | ▨ | ▨ | 89h |
| 0Ah | PCLATH | PCLATH | 8Ah |
| 0Bh | INTCON | INTCON | 8Bh |
| 0Ch<br>2Fh | General Purpose Register | Mapped in Bank 0[2] | 8Ch<br>AFh |
| 30h<br>7Fh | ▨ | ▨ | B0h<br>FFh |
| | Bank 0 | Bank 1 | |

▨ Unimplemented data memory location; read as '0'.

Note 1: Not a physical register.

2: These locations are unimplemented in Bank 1. Any access to these locations will access the corresponding Bank 0 register.

**FIGURE 4-8: PIC16C66/67 DATA MEMORY MAP**

| | | | | | | | File Address |
|---|---|---|---|---|---|---|---|
| Indirect addr.(*) | 00h | Indirect addr.(*) | 80h | Indirect addr.(*) | 100h | Indirect addr.(*) | 180h |
| TMR0 | 01h | OPTION | 81h | TMR0 | 101h | OPTION | 181h |
| PCL | 02h | PCL | 82h | PCL | 102h | PCL | 182h |
| STATUS | 03h | STATUS | 83h | STATUS | 103h | STATUS | 183h |
| FSR | 04h | FSR | 84h | FSR | 104h | FSR | 184h |
| PORTA | 05h | TRISA | 85h | ▨ | 105h | ▨ | 185h |
| PORTB | 06h | TRISB | 86h | PORTB | 106h | TRISB | 186h |
| PORTC | 07h | TRISC | 87h | ▨ | 107h | ▨ | 187h |
| PORTD (1) | 08h | TRISD (1) | 88h | ▨ | 108h | ▨ | 188h |
| PORTE (1) | 09h | TRISE (1) | 89h | ▨ | 109h | ▨ | 189h |
| PCLATH | 0Ah | PCLATH | 8Ah | PCLATH | 10Ah | PCLATH | 18Ah |
| INTCON | 0Bh | INTCON | 8Bh | INTCON | 10Bh | INTCON | 18Bh |
| PIR1 | 0Ch | PIE1 | 8Ch | ▨ | 10Ch | ▨ | 18Ch |
| PIR2 | 0Dh | PIE2 | 8Dh | ▨ | 10Dh | ▨ | 18Dh |
| TMR1L | 0Eh | PCON | 8Eh | ▨ | 10Eh | ▨ | 18Eh |
| TMR1H | 0Fh | ▨ | 8Fh | ▨ | 10Fh | ▨ | 18Fh |
| T1CON | 10h | ▨ | 90h | General Purpose Register 16 Bytes | 110h | General Purpose Register 16 Bytes | 190h |
| TMR2 | 11h | ▨ | 91h | | 111h | | 191h |
| T2CON | 12h | PR2 | 92h | | 112h | | 192h |
| SSPBUF | 13h | SSPADD | 93h | | 113h | | 193h |
| SSPCON | 14h | SSPSTAT | 94h | | 114h | | 194h |
| CCPR1L | 15h | ▨ | 95h | | 115h | | 195h |
| CCPR1H | 16h | ▨ | 96h | | 116h | | 196h |
| CCP1CON | 17h | ▨ | 97h | | 117h | | 197h |
| RCSTA | 18h | TXSTA | 98h | | 118h | | 198h |
| TXREG | 19h | SPBRG | 99h | | 119h | | 199h |
| RCREG | 1Ah | ▨ | 9Ah | | 11Ah | | 19Ah |
| CCPR2L | 1Bh | ▨ | 9Bh | | 11Bh | | 19Bh |
| CCPR2H | 1Ch | ▨ | 9Ch | | 11Ch | | 19Ch |
| CCP2CON | 1Dh | ▨ | 9Dh | | 11Dh | | 19Dh |
| ▨ | 1Eh | ▨ | 9Eh | | 11Eh | | 19Eh |
| ▨ | 1Fh | ▨ | 9Fh | | 11Fh | | 19Fh |
| General Purpose Register 96 Bytes | 20h | General Purpose Register 80 Bytes | A0h | General Purpose Register 80 Bytes | 120h | General Purpose Register 80 Bytes | 1A0h |
| | | | EFh | | 16Fh | | 1EFh |
| | | accesses 70h-7Fh in Bank 0 | F0h | accesses 70h-7Fh in Bank 0 | 170h | accesses 70h-7Fh in Bank 0 | 1F0h |
| | 7Fh | | FFh | | 17Fh | | 1FFh |
| Bank 0 | | Bank 1 | | Bank 2 | | Bank 3 | |

▨ Unimplemented data memory locations, read as '0'.

* Not a physical register.

These registers are not implemented on the PIC16C66.

| | |
|---|---|
| **Note:** | The upper 16 bytes of data memory in banks 1, 2, and 3 are mapped in Bank 0. This may require relocation of data memory usage in the user application code if upgrading to the PIC16C66/67. |

## 8.1 Timer1 Operation in Timer Mode

| Applicable Devices | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 61 | 62 | 62A | R62 | 63 | R63 | 64 | 64A | R64 | 65 | 65A | R65 | 66 | 67 |

Timer mode is selected by clearing bit TMR1CS (T1CON<1>). In this mode, the input clock to the timer is Fosc/4. The synchronize control bit $\overline{\text{T1SYNC}}$ (T1CON<2>) has no effect since the internal clock is always in sync.

## 8.2 Timer1 Operation in Synchronized Counter Mode

| Applicable Devices | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 61 | 62 | 62A | R62 | 63 | R63 | 64 | 64A | R64 | 65 | 65A | R65 | 66 | 67 |

Counter mode is selected by setting bit TMR1CS. In this mode the timer increments on every rising edge of clock input on T1OSI when enable bit T1OSCEN is set or pin with T1CKI when bit T1OSCEN is cleared.

> **Note:** The T1OSI function is multiplexed to different pins, depending on the device. See the pinout descriptions to see which pin has the T1OSI function.

If $\overline{\text{T1SYNC}}$ is cleared, then the external clock input is synchronized with internal phase clocks. The synchronization is done after the prescaler stage. The prescaler stage is an asynchronous ripple counter.

In this configuration, during SLEEP mode, Timer1 will not increment even if an external clock is present, since the synchronization circuit is shut off. The prescaler, however, will continue to increment.

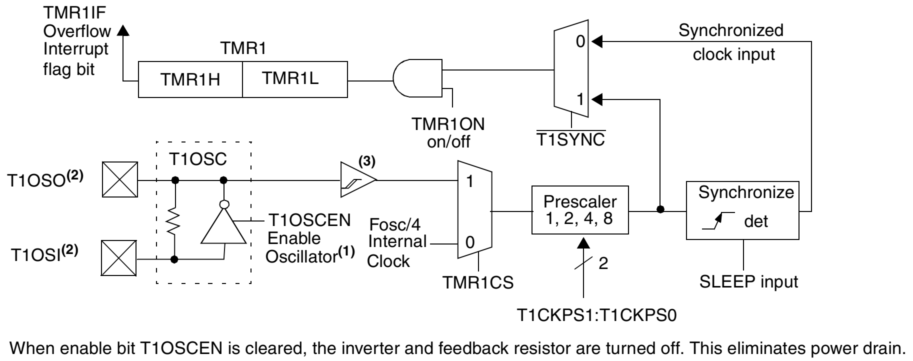
### 8.2.1 EXTERNAL CLOCK INPUT TIMING FOR SYNCHRONIZED COUNTER MODE

When an external clock input is used for Timer1 in synchronized counter mode, it must meet certain requirements. The external clock requirement is due to internal phase clock (Tosc) synchronization. Also, there is a delay in the actual incrementing of TMR1 after synchronization.

When the prescaler is 1:1, the external clock input is the same as the prescaler output. The synchronization of T1CKI with the internal phase clocks is accomplished by sampling the prescaler output on the Q2 and Q4 cycles of the internal phase clocks. Therefore, it is necessary for T1CKI to be high for at least 2Tosc (and a small RC delay of 20 ns) and low for at least 2Tosc (and a small RC delay of 20 ns). Refer to appropriate electrical specification section, parameters 45, 46, and 47.

When a prescaler other than 1:1 is used, the external clock input is divided by the asynchronous ripple-counter type prescaler so that the prescaler output is symmetrical. In order for the external clock to meet the sampling requirement, the ripple counter must be taken into account. Therefore, it is necessary for T1CKI to have a period of at least 4Tosc (and a small RC delay of 40 ns) divided by the prescaler value. The only requirement on T1CKI high and low time is that they do not violate the minimum pulse width requirements of 10 ns). Refer to applicable electrical specification section, parameters 40, 42, 45, 46, and 47.

FIGURE 8-2: TIMER1 BLOCK DIAGRAM



Note 1: When enable bit T1OSCEN is cleared, the inverter and feedback resistor are turned off. This eliminates power drain.
2: See pinouts for pins with T1OSO and T1OSI functions.
3: For the PIC16C62/64/65, the Schmitt Trigger is not implemented in external clock mode.

## 10.3 PWM Mode

| Applicable Devices | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 61 | 62 | 62A | R62 | 63 | R63 | 64 | 64A | R64 | 65 | 65A | R65 | 66 | 67 | | |

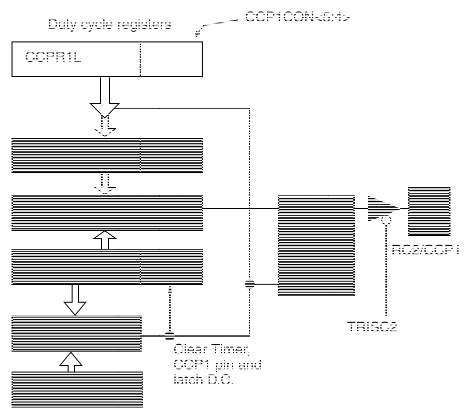
In Pulse Width Modulation (PWM) mode, the CCP1 pin produces up to a 10-bit resolution PWM output. Since the CCP1 pin is multiplexed with the PORTC data latch, the TRISC<2> bit must be cleared to make the CCP1 pin an output.

**Note:** Clearing the CCP1CON register will force the CCP1 PWM output latch to the default low level. This is not the PORTC I/O data latch.

Figure 10-4 shows a simplified block diagram of the CCP module in PWM mode.

For a step by step procedure on how to set up the CCP module for PWM operation, see Section 10.3.3.

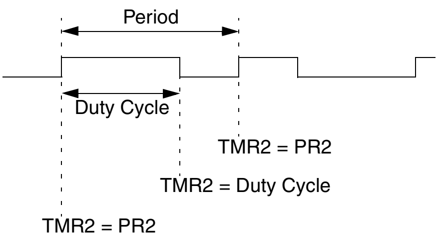
**FIGURE 10-4: SIMPLIFIED PWM BLOCK DIAGRAM**



Note 1: 8-bit timer is concatenated with 2-bit internal Q clock or 2 bits of the prescaler to create 10-bit time-base.

A PWM output (Figure 10-5) has a time base (period) and a time that the output stays high (duty cycle). The frequency of the PWM is the inverse of the period (1/period).

**FIGURE 10-5: PWM OUTPUT**



### 10.3.1 PWM PERIOD

The PWM period is specified by writing to the PR2 register. The PWM period can be calculated using the following formula:

$$\textbf{PWM period} = [(\text{PR2}) + 1] \cdot 4 \cdot T_{OSC} \cdot (\text{TMR2 prescale value})$$

PWM frequency is defined as 1 / [PWM period].

When TMR2 is equal to PR2, the following three events occur on the next increment cycle:

- TMR2 is cleared
- The PWM duty cycle is latched from CCPR1L into CCPR1H
- The CCP1 pin is set (exception: if PWM duty cycle = 0%, the CCP1 pin will not be set)

**Note:** The Timer2 postscaler (see Section 9.1) is not used in the determination of the PWM frequency. The postscaler could be used to have a servo update rate at a different frequency than the PWM output.

### 10.3.2 PWM DUTY CYCLE

The PWM duty cycle is specified by writing to the CCPR1L register and to the CCP1CON<5:4> bits. Up to 10-bit resolution is available: the CCPR1L contains the eight MSbs and the CCP1CON<5:4> contains the two LSbs. This 10-bit value is represented by CCPR1L:CCP1CON<5:4>. The following equation is used to calculate the PWM duty cycle in time:

$$\textbf{PWM duty cycle} = (\text{CCPR1L:CCP1CON<5:4>}) \cdot T_{osc} \cdot (\text{TMR2 prescale value})$$

CCPR1L and CCP1CON<5:4> can be written to at any time, but the duty cycle value is not latched into CCPR1H until after a match between PR2 and TMR2 occurs (i.e., the period is complete). In PWM mode, CCPR1H is a read-only register.

The CCPR1H register and a 2-bit internal latch are used to double buffer the PWM duty cycle. This double buffering is essential for glitchless PWM operation.

When the CCPR1H and 2-bit latch match TMR2 concatenated with an internal 2-bit Q clock or 2 bits of the TMR2 prescaler, the CCP1 pin is cleared.

Maximum PWM resolution (bits) for a given PWM frequency:

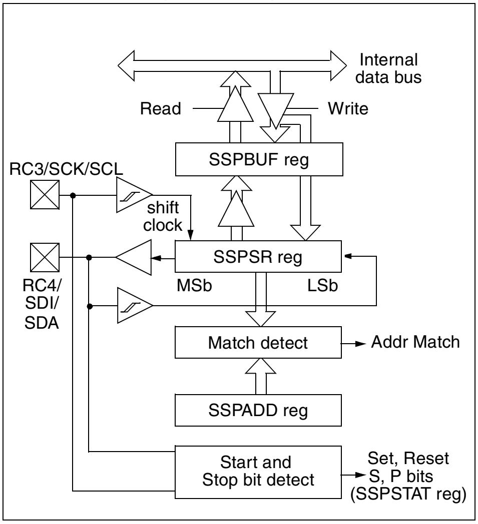
$$= \frac{\log\left(\frac{F_{OSC}}{F_{PWM}}\right)}{\log(2)} \text{ bits}$$

**Note:** If the PWM duty cycle value is longer than the PWM period the CCP1 pin will not be forced to the low level.

## 11.5 SSP $I^2C$ Operation

The SSP module in $I^2C$ mode fully implements all slave functions, except general call support, and provides interrupts on start and stop bits in hardware to facilitate firmware implementations of the master functions. The SSP module implements the standard mode specifications as well as 7-bit and 10-bit addressing. Two pins are used for data transfer. These are the RC3/SCK/SCL pin, which is the clock (SCL), and the RC4/SDI/SDA pin, which is the data (SDA). The user must configure these pins as inputs or outputs through the TRISC<4:3> bits. The SSP module functions are enabled by setting SSP Enable bit SSPEN (SSPCON<5>).

**FIGURE 11-24: SSP BLOCK DIAGRAM ($I^2C$ MODE)**



The SSP module has five registers for $I^2C$ operation. These are the:

- SSP Control Register (SSPCON)
- SSP Status Register (SSPSTAT)
- Serial Receive/Transmit Buffer (SSPBUF)
- SSP Shift Register (SSPSR) - Not directly accessible
- SSP Address Register (SSPADD)

The SSPCON register allows control of the $I^2C$ operation. Four mode selection bits (SSPCON<3:0>) allow one of the following $I^2C$ modes to be selected:

- $I^2C$ Slave mode (7-bit address)
- $I^2C$ Slave mode (10-bit address)
- $I^2C$ Slave mode (7-bit address), with start and stop bit interrupts enabled
- $I^2C$ Slave mode (10-bit address), with start and stop bit interrupts enabled
- $I^2C$ Firmware controlled Master Mode, slave is idle

Selection of any $I^2C$ mode, with the SSPEN bit set, forces the SCL and SDA pins to be open drain, provided these pins are programmed to inputs by setting the appropriate TRISC bits.

The SSPSTAT register gives the status of the data transfer. This information includes detection of a START or STOP bit, specifies if the received byte was data or address if the next byte is the completion of 10-bit address, and if this will be a read or write data transfer. The SSPSTAT register is read only.

The SSPBUF is the register to which transfer data is written to or read from. The SSPSR register shifts the data in or out of the device. In receive operations, the SSPBUF and SSPSR create a doubled buffered receiver. This allows reception of the next byte to begin before reading the last byte of received data. When the complete byte is received, it is transferred to the SSPBUF register and flag bit SSPIF is set. If another complete byte is received before the SSPBUF register is read, a receiver overflow has occurred and bit SSPOV (SSPCON<6>) is set and the byte in the SSPSR is lost.

The SSPADD register holds the slave address. In 10-bit mode, the user first needs to write the high byte of the address (`1111 0 A9 A8 0`). Following the high byte address match, the low byte of the address needs to be loaded (A7:A0).

## 12.1 USART Baud Rate Generator (BRG)

| Applicable Devices | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 61 | 62 | 62A | R62 | 63 | R63 | 64 | 64A | R64 | 65 | 65A | R65 | 66 | 67 | |

The BRG supports both the Asynchronous and Synchronous modes of the USART. It is a dedicated 8-bit baud rate generator. The SPBRG register controls the period of a free running 8-bit timer. In asynchronous mode bit BRGH (TXSTA<2>) also controls the baud rate. In synchronous mode bit BRGH is ignored. Table 12-1 shows the formula for computation of the baud rate for different USART modes which only apply in master mode (internal clock).

Given the desired baud rate and Fosc, the nearest integer value for the SPBRG register can be calculated using the formula in Table 12-1. From this, the error in baud rate can be determined.

Example 12-1 shows the calculation of the baud rate error for the following conditions:

FOSC = 16 MHz
Desired Baud Rate = 9600
BRGH = 0
SYNC = 0

### EXAMPLE 12-1: CALCULATING BAUD RATE ERROR

Desired Baud rate = Fosc / (64 (X + 1))

$$9600 = 16000000 / (64 (X + 1))$$

$$X = \lfloor 25.042 \rfloor = 25$$

Calculated Baud Rate=16000000 / (64 (25 + 1))

$$= 9615$$

$$\text{Error} = \frac{\text{(Calculated Baud Rate - Desired Baud Rate)}}{\text{Desired Baud Rate}}$$

$$= (9615 - 9600) / 9600$$

$$= 0.16\%$$

It may be advantageous to use the high baud rate (BRGH = 1) even for slower baud clocks. This is because the FOSC/(16(X + 1)) equation can reduce the baud rate error in some cases.

**Note:** For the PIC16C63/R63/65/65A/R65 the asynchronous high speed mode (BRGH = 1) may experience a high rate of receive errors. It is recommended that BRGH = 0. If you desire a higher baud rate than BRGH = 0 can support, refer to the device errata for additional information or use the PIC16C66/67.

Writing a new value to the SPBRG register, causes the BRG timer to be reset (or cleared), this ensures that the BRG does not wait for a timer overflow before outputting the new baud rate.

### TABLE 12-1: BAUD RATE FORMULA

| SYNC | BRGH = 0 (Low Speed) | BRGH = 1 (High Speed) |
|---|---|---|
| 0 | (Asynchronous) Baud Rate = FOSC/(64(X+1)) | Baud Rate = FOSC/(16(X+1)) |
| 1 | (Synchronous) Baud Rate = FOSC/(4(X+1)) | N/A |

X = value in SPBRG (0 to 255)

### TABLE 12-2: REGISTERS ASSOCIATED WITH BAUD RATE GENERATOR

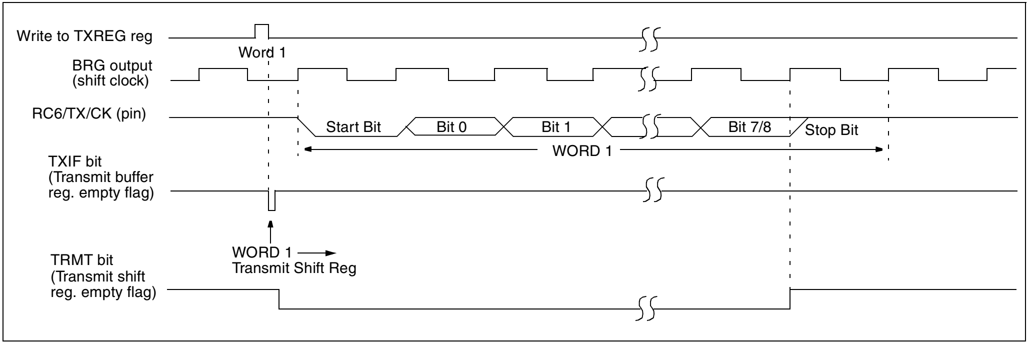
| Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Value on POR, BOR | Value on all other Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 98h | TXSTA | CSRC | TX9 | TXEN | SYNC | — | BRGH | TRMT | TX9D | 0000 -010 | 0000 -010 |
| 18h | RCSTA | SPEN | RX9 | SREN | CREN | — | FERR | OERR | RX9D | 0000 -00x | 0000 -00x |
| 99h | SPBRG | Baud Rate Generator Register | | | | | | | | 0000 0000 | 0000 0000 |

Legend: `x` = unknown, `-` = unimplemented read as '0'. Shaded cells are not used by the BRG.

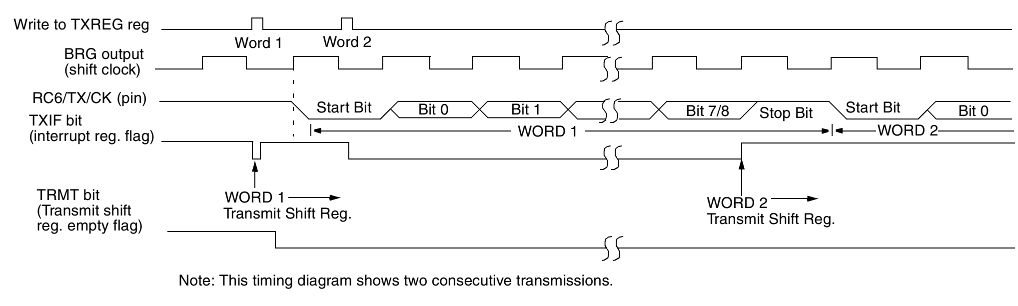
Steps to follow when setting up an Asynchronous Transmission:

1. Initialize the SPBRG register for the appropriate baud rate. If a high speed baud rate is desired, then set bit BRGH. (Section 12.1).
2. Enable the asynchronous serial port by clearing bit SYNC and setting bit SPEN.
3. If interrupts are desired, then set enable bit TXIE.
4. If 9-bit transmission is desired, then set transmit bit TX9.
5. Enable the transmission by setting bit TXEN, which will also set bit TXIF.
6. If 9-bit transmission is selected, the ninth bit should be loaded in bit TX9D.
7. Load data to the TXREG register (starts transmission).

### FIGURE 12-8: ASYNCHRONOUS MASTER TRANSMISSION



### FIGURE 12-9: ASYNCHRONOUS MASTER TRANSMISSION (BACK TO BACK)



Note: This timing diagram shows two consecutive transmissions.

### TABLE 12-6: REGISTERS ASSOCIATED WITH ASYNCHRONOUS TRANSMISSION

| Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Value on POR, BOR | Value on all other Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0Ch | PIR1 | PSPIF(1) | (2) | RCIF | TXIF | SSPIF | CCP1IF | TMR2IF | TMR1IF | `0000 0000` | `0000 0000` |
| 18h | RCSTA | SPEN | RX9 | SREN | CREN | — | FERR | OERR | RX9D | `0000 -00x` | `0000 -00x` |
| 19h | TXREG | USART Transmit Register | | | | | | | | `0000 0000` | `0000 0000` |
| 8Ch | PIE1 | PSPIE(1) | (2) | RCIE | TXIE | SSPIE | CCP1IE | TMR2IE | TMR1IE | `0000 0000` | `0000 0000` |
| 98h | TXSTA | CSRC | TX9 | TXEN | SYNC | — | BRGH | TRMT | TX9D | `0000 -010` | `0000 -010` |
| 99h | SPBRG | Baud Rate Generator Register | | | | | | | | `0000 0000` | `0000 0000` |

Legend: `x` = unknown, `-` = unimplemented locations read as '0'. Shaded cells are not used for Asynchronous Transmission.
Note 1: PSPIF and PSPIE are reserved on the PIC16C63/R63/66, always maintain these bits clear.
2: PIR1<6> and PIE1<6> are reserved, always maintain these bits clear.

## 12.3 USART Synchronous Master Mode

| Applicable Devices | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 61 | 62 | 62A | R62 | 63 | R63 | 64 | 64A | R64 | 65 | 65A | R65 | 66 | 67 |

In Synchronous Master mode the data is transmitted in a half-duplex manner i.e., transmission and reception do not occur at the same time. When transmitting data the reception is inhibited and vice versa. Synchronous mode is entered by setting bit SYNC (TXSTA<4>). In addition enable bit SPEN (RCSTA<7>) is set in order to configure the RC6 and RC7 I/O pins to CK (clock) and DT (data) lines respectively. The Master mode indicates that the processor transmits the master clock on the CK line. The Master mode is entered by setting bit CSRC (TXSTA<7>).

### 12.3.1 USART SYNCHRONOUS MASTER TRANSMISSION

The USART transmitter block diagram is shown in Figure 12-7. The heart of the transmitter is the transmit (serial) shift register (TSR). The shift register obtains its data from the read/write transmit buffer register, TXREG. The TXREG register is loaded with data in software. The TSR register is not loaded until the last bit has been transmitted from the previous load. As soon as the last bit is transmitted, the TSR register is loaded with new data from the TXREG register (if available). Once the TXREG register transfers the data to the TSR register (occurs in one Tcycle), the TXREG register is empty and interrupt flag bit TXIF (PIR1<4>) is set. This interrupt can be enabled/disabled by setting/clearing enable bit TXIE (PIE1<4>). Flag bit TXIF will be set regardless of the status of enable bit TXIE and cannot be cleared in software. It will clear only when new data is loaded into the TXREG register. While flag bit TXIF indicates the status of the TXREG register, another bit, TRMT (TXSTA<1>), shows the status of the TSR register. Status bit TRMT is a read only bit which is set when the TSR register is empty. No interrupt logic is tied to this bit, so the user has to poll this bit in order to determine if the TSR register is empty. The TSR register is not mapped in data memory so it is not available to the user.

Transmission is enabled by setting enable bit TXEN (TXSTA<5>). The actual transmission will not occur until the TXREG register has been loaded with data. The first data bit will be shifted out on the next available rising edge of the clock on the CK line. Data out is stable around the falling edge of the synchronous clock (Figure 12-12). The transmission can also be started by first loading the TXREG register and then setting enable bit TXEN (Figure 12-13). This is advantageous when slow baud rates are selected, since the BRG is kept in reset when bits TXEN, CREN, and SREN are clear. Setting enable bit TXEN will start the BRG, creating a shift clock immediately. Normally when transmission is first started, the TSR register is empty, so a transfer to the TXREG register will result in an immediate transfer to TSR resulting in an empty TXREG register. Back-to-back transfers are possible.

Clearing enable bit TXEN, during a transmission, will cause the transmission to be aborted and will reset the transmitter. The DT and CK pins will revert to hi-impedance. If, during a transmission, either bit CREN or bit SREN is set the transmission is aborted and the DT pin reverts to a hi-impedance state (for a reception). The CK pin will remain an output if bit CSRC is set (internal clock). The transmitter logic however, is not reset although it is disconnected from the pins. In order to reset the transmitter, the user has to clear enable bit TXEN. If enable bit SREN is set (to interrupt an on going transmission and receive a single word), then after the single word is received, enable bit SREN will be cleared, and the serial port will revert back to transmitting since enable bit TXEN is still set. The DT line will immediately switch from hi-impedance receive mode to transmit and start driving. To avoid this, enable bit TXEN should be cleared.

In order to select 9-bit transmission, bit TX9 (TXSTA<6>) should be set and the ninth bit should be written to bit TX9D (TXSTA<0>). The ninth bit must be written before writing the 8-bit data to the TXREG register. This is because a data write to the TXREG register can result in an immediate transfer of the data to the TSR register (if the TSR is empty). If the TSR register was empty and the TXREG register was written before writing the “new” TX9D, the “present” value of bit TX9D is loaded.

Steps to follow when setting up a Synchronous Master Transmission:

1. Initialize the SPBRG register for the appropriate baud rate (Section 12.1).
2. Enable the synchronous master serial port by setting bits SYNC, SPEN, and CSRC.
3. If interrupts are desired, then set enable bit TXIE.
4. If 9-bit transmission is desired, then set bit TX9.
5. Enable the transmission by setting enable bit TXEN.
6. If 9-bit transmission is selected, the ninth bit should be loaded in bit TX9D.
7. Start transmission by loading data to the TXREG register.

| Applicable Devices | 61 | 62 | 62A | R62 | 63 | R63 | 64 | 64A | R64 | 65 | 65A | R65 | 66 | 67 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|

## 17.2 DC Characteristics: PIC16LC62/64-04 (Commercial, Industrial)

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| **DC CHARACTERISTICS** | **Standard Operating Conditions (unless otherwise stated)**<br>Operating temperature -40°C ≤ TA ≤ +85°C for industrial and<br>0°C ≤ TA ≤ +70°C for commercial | | | | | | |
| **Param No.** | **Characteristic** | **Sym** | **Min** | **Typ†** | **Max** | **Units** | **Conditions** |
| D001 | Supply Voltage | VDD | 3.0 | - | 6.0 | V | LP, XT, RC osc configuration (DC - 4 MHz) |
| D002* | RAM Data Retention Voltage (Note 1) | VDR | - | 1.5 | - | V | |
| D003 | VDD start voltage to ensure internal Power-on Reset signal | VPOR | - | VSS | - | V | See section on Power-on Reset for details |
| D004* | VDD rise rate to ensure internal Power-on Reset signal | SVDD | 0.05 | - | - | V/ms | See section on Power-on Reset for details |
| D010 | Supply Current (Note 2, 5) | IDD | - | 2.0 | 3.8 | mA | XT, RC osc configuration<br>FOSC = 4 MHz, VDD = 3.0V (Note 4) |
| D010A | | | - | 22.5 | 48 | µA | LP osc configuration<br>FOSC = 32 kHz, VDD = 3.0V, WDT disabled |
| D020 | Power-down Current (Note 3, 5) | IPD | - | 7.5 | 30 | µA | VDD = 3.0V, WDT enabled, -40°C to +85°C |
| D021 | | | - | 0.9 | 13.5 | µA | VDD = 3.0V, WDT disabled, 0°C to +70°C |
| D021A | | | - | 0.9 | 18 | µA | VDD = 3.0V, WDT disabled, -40°C to +85°C |

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.
The test conditions for all IDD measurements in active operation mode are:
OSC1 = external square wave, from rail to rail; all I/O pins tristated, pulled to VDD
$\overline{\text{MCLR}}$ = VDD; WDT enabled/disabled as specified.

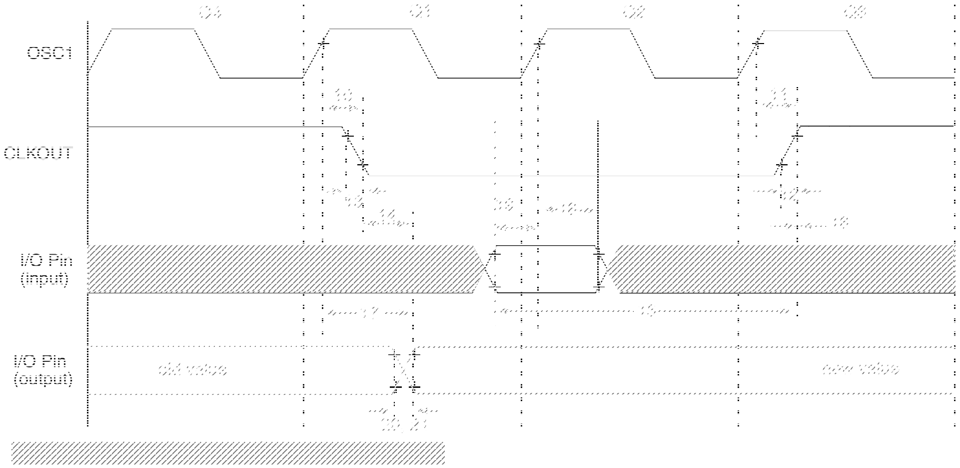
3: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

4: For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula Ir = VDD/2Rext (mA) with Rext in kOhm.

5: Timer1 oscillator (when enabled) adds approximately 20 µA to the specification. This value is from characterization and is for design guidance only. This is not tested.

| | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Applicable Devices** | 61 | 62 | 62A | R62 | 63 | R63 | 64 | 64A | R64 | 65 | 65A | R65 | 66 | 67 |

### FIGURE 17-3: CLKOUT AND I/O TIMING



### TABLE 17-3: CLKOUT AND I/O TIMING REQUIREMENTS

| Parameters | Sym | Characteristic | | Min | Typ† | Max | Units | Conditions |
|---|---|---|---|---|---|---|---|---|
| 10* | TosH2ckL | OSC1↑ to CLKOUT↓ | | — | 75 | 200 | ns | Note 1 |
| 11* | TosH2ckH | OSC1↑ to CLKOUT↑ | | — | 75 | 200 | ns | Note 1 |
| 12* | TckR | CLKOUT rise time | | — | 35 | 100 | ns | Note 1 |
| 13* | TckF | CLKOUT fall time | | — | 35 | 100 | ns | Note 1 |
| 14* | TckL2ioV | CLKOUT ↓ to Port out valid | | — | — | 0.5TCY + 20 | ns | Note 1 |
| 15* | TioV2ckH | Port in valid before CLKOUT ↑ | | TOSC + 200 | — | — | ns | Note 1 |
| 16* | TckH2ioI | Port in hold after CLKOUT ↑ | | 0 | — | — | ns | Note 1 |
| 17* | TosH2ioV | OSC1↑ (Q1 cycle) to Port out valid | | — | 50 | 150 | ns | |
| 18* | TosH2ioI | OSC1↑ (Q2 cycle) to Port input invalid (I/O in hold time) | PIC16**C**62/64 | 100 | — | — | ns | |
| | | | PIC16**LC**62/64 | 200 | — | — | ns | |
| 19* | TioV2osH | Port input valid to OSC1↑ (I/O in setup time) | | 0 | — | — | ns | |
| 20* | TioR | Port output rise time | PIC16**C**62/64 | — | 10 | 40 | ns | |
| | | | PIC16**LC**62/64 | — | — | 80 | ns | |
| 21* | TioF | Port output fall time | PIC16**C**62/64 | — | 10 | 40 | ns | |
| | | | PIC16**LC**62/64 | — | — | 80 | ns | |
| 22††* | Tinp | INT pin high or low time | | TCY | — | — | ns | |
| 23††* | Trbp | RB7:RB4 change INT high or low time | | TCY | — | — | ns | |

* These parameters are characterized but not tested.

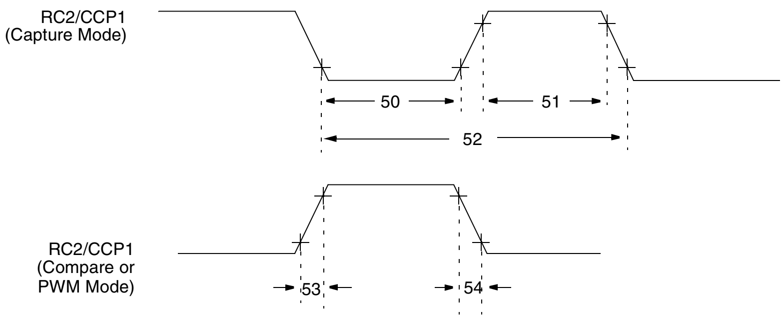
† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

†† These parameters are asynchronous events not related to any internal clock edge.

Note 1: Measurements are taken in RC Mode where CLKOUT output is 4 x TOSC.

| **Applicable Devices** | 61 | 62 | 62A | R62 | 63 | R63 | 64 | 64A | R64 | 65 | 65A | R65 | 66 | 67 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|

### FIGURE 17-6: CAPTURE/COMPARE/PWM TIMINGS (CCP1)



Note: Refer to Figure 17-1 for load conditions.

### TABLE 17-6: CAPTURE/COMPARE/PWM REQUIREMENTS (CCP1)

| Parameter No. | Sym | Characteristic | | | Min | Typ† | Max | Units | Conditions |
|---|---|---|---|---|---|---|---|---|---|
| 50* | TccL | CCP1<br>input low time | No Prescaler | | $0.5T_{CY} + 20$ | — | — | ns | |
| | | | With Prescaler | PIC16**C**62/64 | 10 | — | — | ns | |
| | | | | PIC16**LC**62/64 | 20 | — | — | ns | |
| 51* | TccH | CCP1<br>input high time | No Prescaler | | $0.5T_{CY} + 20$ | — | — | ns | |
| | | | With Prescaler | PIC16**C**62/64 | 10 | — | — | ns | |
| | | | | PIC16**LC**62/64 | 20 | — | — | ns | |
| 52* | TccP | CCP1 input period | | | $\frac{3T_{CY} + 40}{N}$ | — | — | ns | N = prescale value (1,4 or 16) |
| 53 | TccR | CCP1 output rise time | | PIC16**C**62/64 | — | 10 | 25 | ns | |
| | | | | PIC16**LC**62/64 | — | 25 | 45 | ns | |
| 54 | TccF | CCP1 output fall time | | PIC16**C**62/64 | — | 10 | 25 | ns | |
| | | | | PIC16**LC**62/64 | — | 25 | 45 | ns | |

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

| Applicable Devices | 61 | 62 | 62A | R62 | 63 | R63 | 64 | 64A | R64 | 65 | 65A | R65 | 66 | 67 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|

**DC CHARACTERISTICS**

**Standard Operating Conditions (unless otherwise stated)**
Operating temperature -40°C ≤ TA ≤ +125°C for extended,
-40°C ≤ TA ≤ +85°C for industrial and
0°C ≤ TA ≤ +70°C for commercial
Operating voltage VDD range as described in DC spec Section 18.1 and Section 18.2

| Param No. | Characteristic | Sym | Min | Typ † | Max | Units | Conditions |
|---|---|---|---|---|---|---|---|
| | **Output High Voltage** | | | | | | |
| D090 | I/O ports (Note 3) | VOH | VDD-0.7 | - | - | V | IOH = -3.0 mA, VDD = 4.5V, -40°C to +85°C |
| D090A | | | VDD-0.7 | - | - | V | IOH = -2.5 mA, VDD = 4.5V, -40°C to +125°C |
| D092 | OSC2/CLKOUT (RC osc config) | | VDD-0.7 | - | - | V | IOH = -1.3 mA, VDD = 4.5V, -40°C to +85°C |
| D092A | | | VDD-0.7 | - | - | V | IOH = -1.0 mA, VDD = 4.5V, -40°C to +125°C |
| D150* | **Open-Drain High Voltage** | VOD | - | - | 14 | V | RA4 pin |
| | **Capacitive Loading Specs on Output Pins** | | | | | | |
| D100 | OSC2 pin | COSC2 | - | - | 15 | pF | In XT, HS and LP modes when external clock is used to drive OSC1. |
| D101 | All I/O pins and OSC2 (in RC mode) | CIO | - | - | 50 | pF | |
| D102 | SCL, SDA in $I^2C$ mode | Cb | - | - | 400 | pF | |

* These parameters are characterized but not tested.

† Data in “Typ” column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

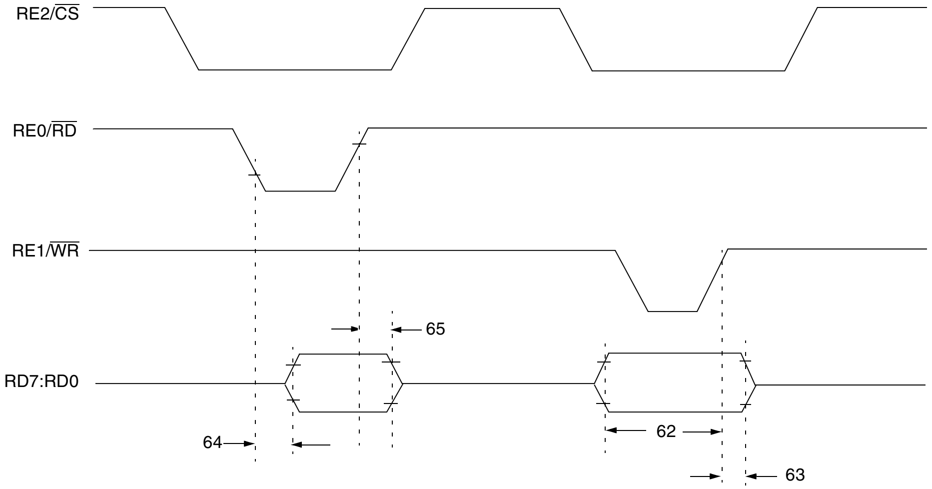
Note 1: In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C6X be driven with external clock in RC mode.

2: The leakage current on the $\overline{\text{MCLR}}$/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as current sourced by the pin.

| **Applicable Devices** | 61 | 62 | 62A | R62 | 63 | R63 | 64 | 64A | R64 | 65 | 65A | R65 | 66 | 67 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|

### FIGURE 18-8: PARALLEL SLAVE PORT TIMING (PIC16C64A/R64)



Note: Refer to Figure 18-1 for load conditions

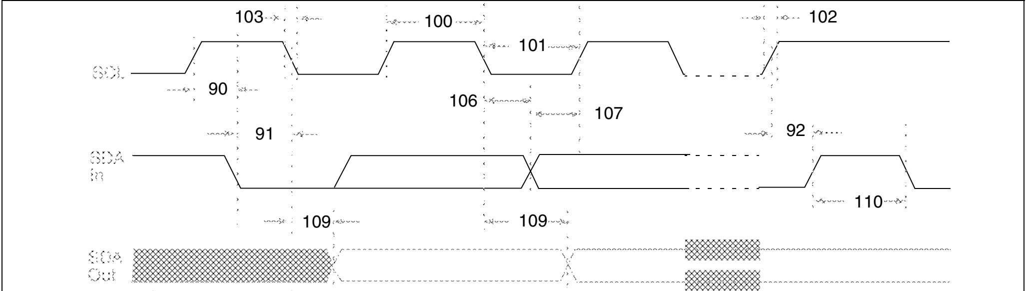
### TABLE 18-7: PARALLEL SLAVE PORT REQUIREMENTS (PIC16C64A/R64)

| Parameter No. | Sym | Characteristic | | Min | Typ† | Max | Units | Conditions |
|---|---|---|---|---|---|---|---|---|
| 62 | TdtV2wrH | Data in valid before $\overline{\mathrm{WR}}$↑ or $\overline{\mathrm{CS}}$↑ (setup time) | | 20 | — | — | ns | |
| | | | | 25 | — | — | ns | Extended Range Only |
| 63* | TwrH2dtI | $\overline{\mathrm{WR}}$↑ or $\overline{\mathrm{CS}}$↑ to data–in invalid (hold time) | PIC16**C**64A/R64 | 20 | — | — | ns | |
| | | | PIC16**LC**64A.R64 | 35 | — | — | ns | |
| 64 | TrdL2dtV | $\overline{\mathrm{RD}}$↓ and $\overline{\mathrm{CS}}$↓ to data–out valid | | — | — | 80 | ns | |
| | | | | — | — | 90 | ns | Extended Range Only |
| 65* | TrdH2dtI | $\overline{\mathrm{RD}}$↑ or $\overline{\mathrm{CS}}$↑ to data–out invalid | | 10 | — | 30 | ns | |

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

## FIGURE 18-11: I$^2$C BUS DATA TIMING



Note: Refer to Figure 18-1 for load conditions

## TABLE 18-10: I$^2$C BUS DATA REQUIREMENTS

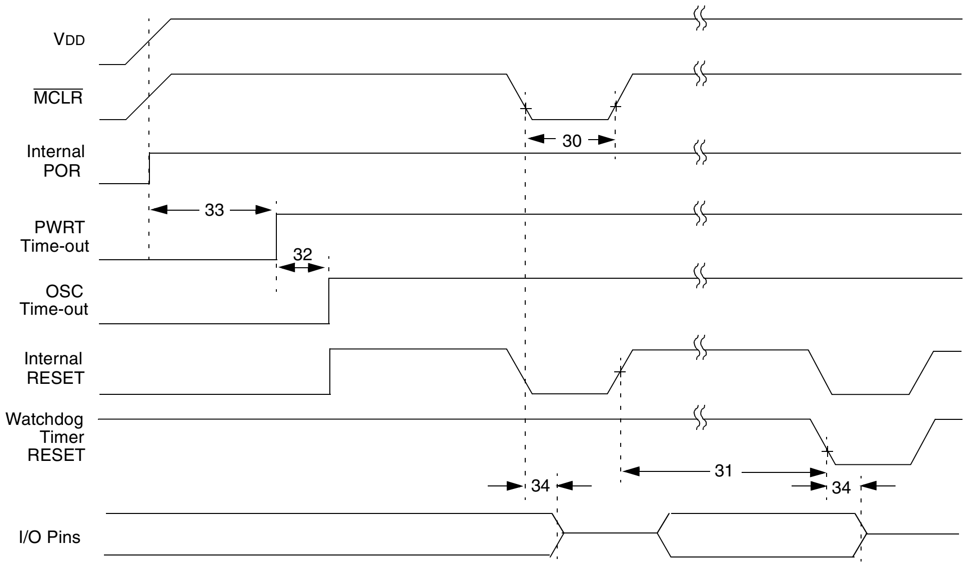
| Parameter No. | Sym | Characteristic | | Min | Max | Units | Conditions |
|---|---|---|---|---|---|---|---|
| 100* | THIGH | Clock high time | 100 kHz mode | 4.0 | — | μs | Device must operate at a minimum of 1.5 MHz |
| | | | 400 kHz mode | 0.6 | — | μs | Device must operate at a minimum of 10 MHz |
| | | | SSP Module | 1.5TCY | — | | |
| 101* | TLOW | Clock low time | 100 kHz mode | 4.7 | — | μs | Device must operate at a minimum of 1.5 MHz |
| | | | 400 kHz mode | 1.3 | — | μs | Device must operate at a minimum of 10 MHz |
| | | | SSP Module | 1.5TCY | — | | |
| 102* | TR | SDA and SCL rise time | 100 kHz mode | — | 1000 | ns | |
| | | | 400 kHz mode | 20 + 0.1Cb | 300 | ns | Cb is specified to be from 10-400 pF |
| 103* | TF | SDA and SCL fall time | 100 kHz mode | — | 300 | ns | |
| | | | 400 kHz mode | 20 + 0.1Cb | 300 | ns | Cb is specified to be from 10-400 pF |
| 90* | TSU:STA | START condition setup time | 100 kHz mode | 4.7 | — | μs | Only relevant for repeated START condition |
| | | | 400 kHz mode | 0.6 | — | μs | |
| 91* | THD:STA | START condition hold time | 100 kHz mode | 4.0 | — | μs | After this period the first clock pulse is generated |
| | | | 400 kHz mode | 0.6 | — | μs | |
| 106* | THD:DAT | Data input hold time | 100 kHz mode | 0 | — | ns | |
| | | | 400 kHz mode | 0 | 0.9 | μs | |
| 107* | TSU:DAT | Data input setup time | 100 kHz mode | 250 | — | ns | Note 2 |
| | | | 400 kHz mode | 100 | — | ns | |
| 92* | TSU:STO | STOP condition setup time | 100 kHz mode | 4.7 | — | μs | |
| | | | 400 kHz mode | 0.6 | — | μs | |
| 109* | TAA | Output valid from clock | 100 kHz mode | — | 3500 | ns | Note 1 |
| | | | 400 kHz mode | — | — | ns | |
| 110* | TBUF | Bus free time | 100 kHz mode | 4.7 | — | μs | Time the bus must be free before a new transmission can start |
| | | | 400 kHz mode | 1.3 | — | μs | |
| | Cb | Bus capacitive loading | | — | 400 | pF | |

* These parameters are characterized but not tested.

Note 1: As a transmitter, the device must provide this internal minimum delay time to bridge the undefined region (min. 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

2: A fast-mode (400 kHz) I$^2$C-bus device can be used in a standard-mode (100 kHz) I$^2$C-bus system, but the requirement tsu;DAT ≥ 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line TR max.+tsu;DAT = 1000 + 250 = 1250 ns (according to the standard-mode I$^2$C bus specification) before the SCL line is released.

## FIGURE 19-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING



Note: Refer to Figure 19-1 for load conditions.

## TABLE 19-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER REQUIREMENTS

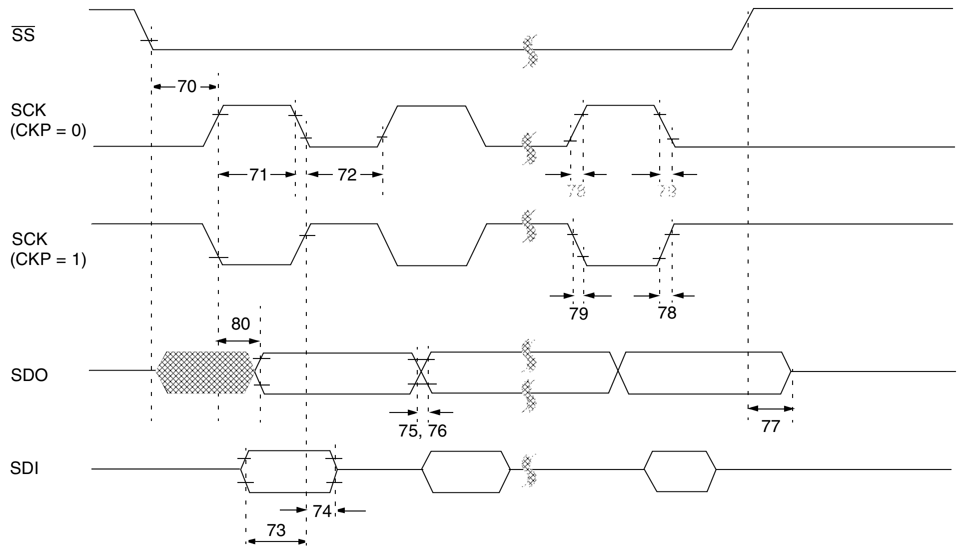
| Parameter No. | Sym | Characteristic | Min | Typ† | Max | Units | Conditions |
|---|---|---|---|---|---|---|---|
| 30* | TmcL | $\overline{\text{MCLR}}$ Pulse Width (low) | 100 | — | — | ns | VDD = 5V, -40°C to +85°C |
| 31* | Twdt | Watchdog Timer Time-out Period (No Prescaler) | 7 | 18 | 33 | ms | VDD = 5V, -40°C to +85°C |
| 32 | Tost | Oscillation Start-up Timer Period | — | 1024TOSC | — | — | TOSC = OSC1 period |
| 33* | Tpwrt | Power-up Timer Period or WDT reset | 28 | 72 | 132 | ms | VDD = 5V, -40°C to +85°C |
| 34 | TIOZ | I/O Hi-impedance from $\overline{\text{MCLR}}$ Low | — | — | 100 | ns | |

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

| Applicable Devices | 61 | 62 | 62A | R62 | 63 | R63 | 64 | 64A | R64 | 65 | 65A | R65 | 66 | 67 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|

## FIGURE 19-8: SPI MODE TIMING



Note: Refer to Figure 19-1 for load conditions

## TABLE 19-8: SPI MODE REQUIREMENTS

| Parameter No. | Sym | Characteristic | Min | Typ† | Max | Units | Conditions |
|---|---|---|---|---|---|---|---|
| 70 | TssL2scH,<br>TssL2scL | $\overline{\mathrm{SS}}$↓ to SCK↓ or SCK↑ input | TCY | — | — | ns | |
| 71 | TscH | SCK input high time (slave mode) | TCY + 20 | — | — | ns | |
| 72 | TscL | SCK input low time (slave mode) | TCY + 20 | — | — | ns | |
| 73 | TdiV2scH,<br>TdiV2scL | Setup time of SDI data input to SCK edge | 50 | — | — | ns | |
| 74 | TscH2diL,<br>TscL2diL | Hold time of SDI data input to SCK edge | 50 | — | — | ns | |
| 75 | TdoR | SDO data output rise time | — | 10 | 25 | ns | |
| 76 | TdoF | SDO data output fall time | — | 10 | 25 | ns | |
| 77 | TssH2doZ | $\overline{\mathrm{SS}}$↑ to SDO output hi-impedance | 10 | — | 50 | ns | |
| 78 | TscR | SCK output rise time (master mode) | — | 10 | 25 | ns | |
| 79 | TscF | SCK output fall time (master mode) | — | 10 | 25 | ns | |
| 80 | TscH2doV,<br>TscL2doV | SDO data output valid after SCK edge | — | — | 50 | ns | |

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

| | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Applicable Devices** | 61 | 62 | 62A | R62 | 63 | R63 | 64 | 64A | R64 | 65 | 65A | R65 | 66 | 67 |

## 22.3 DC Characteristics: PIC16C66/67-04 (Commercial, Industrial, Extended) PIC16C66/67-10 (Commercial, Industrial, Extended) PIC16C66/67-20 (Commercial, Industrial, Extended) PIC16LC66/67-04 (Commercial, Industrial)

| **DC CHARACTERISTICS** | | **Standard Operating Conditions (unless otherwise stated)**<br>Operating temperature -40°C ≤ TA ≤ +125°C for extended,<br>-40°C ≤ TA ≤ +85°C for industrial and<br>0°C ≤ TA ≤ +70°C for commercial<br>Operating voltage VDD range as described in DC spec Section 22.1 and Section 22.2 | | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Characteristic** | **Sym** | **Min** | **Typ †** | **Max** | **Units** | **Conditions** |
| | **Input Low Voltage** | | | | | | |
| | I/O ports | VIL | | | | | |
| D030 | with TTL buffer | | VSS | - | 0.15VDD | V | For entire VDD range |
| D030A | | | VSS | - | 0.8V | V | 4.5V ≤ VDD ≤ 5.5V |
| D031 | with Schmitt Trigger buffer | | VSS | - | 0.2VDD | V | |
| D032 | $\overline{\text{MCLR}}$, OSC1 (in RC mode) | | Vss | - | 0.2VDD | V | |
| D033 | OSC1 (in XT, HS and LP) | | Vss | - | 0.3VDD | V | Note1 |
| | **Input High Voltage** | | | | | | |
| | I/O ports | VIH | | - | | | |
| D040 | with TTL buffer | | 2.0 | - | VDD | V | 4.5V ≤ VDD ≤ 5.5V |
| D040A | | | 0.25VDD + 0.8V | - | VDD | V | For entire VDD range |
| D041 | with Schmitt Trigger buffer | | 0.8VDD | - | VDD | V | For entire VDD range |
| D042 | $\overline{\text{MCLR}}$ | | 0.8VDD | - | VDD | V | |
| D042A | OSC1 (XT, HS and LP) | | 0.7VDD | - | VDD | V | Note1 |
| D043 | OSC1 (in RC mode) | | 0.9VDD | - | VDD | V | |
| D070 | PORTB weak pull-up current | IPURB | 50 | 250 | 400 | μA | VDD = 5V, VPIN = VSS |
| | **Input Leakage Current** (Notes 2, 3) | | | | | | |
| D060 | I/O ports | IIL | - | - | ±1 | μA | Vss ≤ VPIN ≤ VDD, Pin at hi-impedance |
| D061 | $\overline{\text{MCLR}}$, RA4/T0CKI | | - | - | ±5 | μA | Vss ≤ VPIN ≤ VDD |
| D063 | OSC1 | | - | - | ±5 | μA | Vss ≤ VPIN ≤ VDD, XT, HS and LP osc configuration |
| | **Output Low Voltage** | | | | | | |
| D080 | I/O ports | VOL | - | - | 0.6 | V | IOL = 8.5 mA, VDD = 4.5V, -40°C to +85°C |
| D080A | | | - | - | 0.6 | V | IOL = 7.0 mA, VDD = 4.5V, -40°C to +125°C |
| D083 | OSC2/CLKOUT (RC osc config) | | - | - | 0.6 | V | IOL = 1.6 mA, VDD = 4.5V, -40°C to +85°C |
| D083A | | | - | - | 0.6 | V | IOL = 1.2 mA, VDD = 4.5V, -40°C to +125°C |

* These parameters are characterized but not tested.

† Data in “Typ” column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C6X be driven with external clock in RC mode.

2: The leakage current on the $\overline{\text{MCLR}}$/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as current sourced by the pin.

| Applicable Devices | 61 | 62 | 62A | R62 | 63 | R63 | 64 | 64A | R64 | 65 | 65A | R65 | 66 | 67 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|

**FIGURE 23-16: TYPICAL IDD vs. FREQUENCY (RC MODE @ 300 pF, 25°C)**

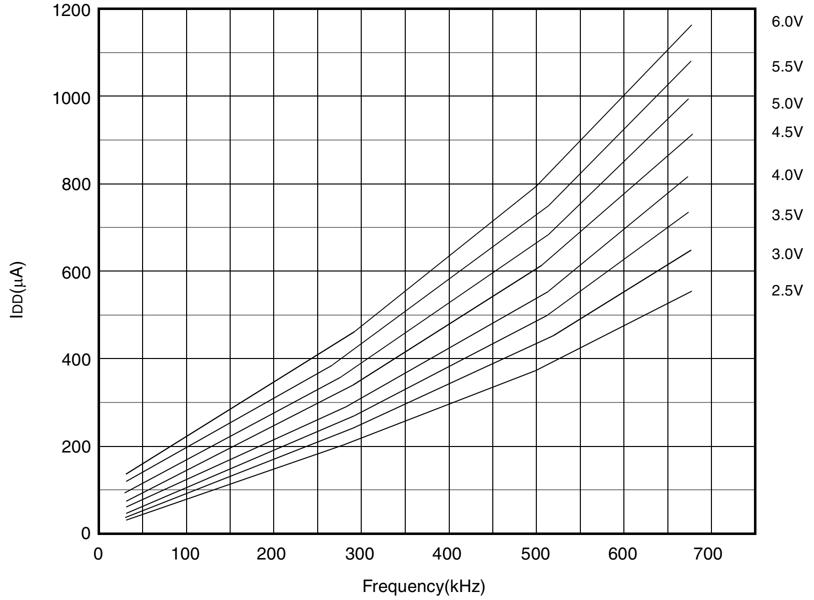
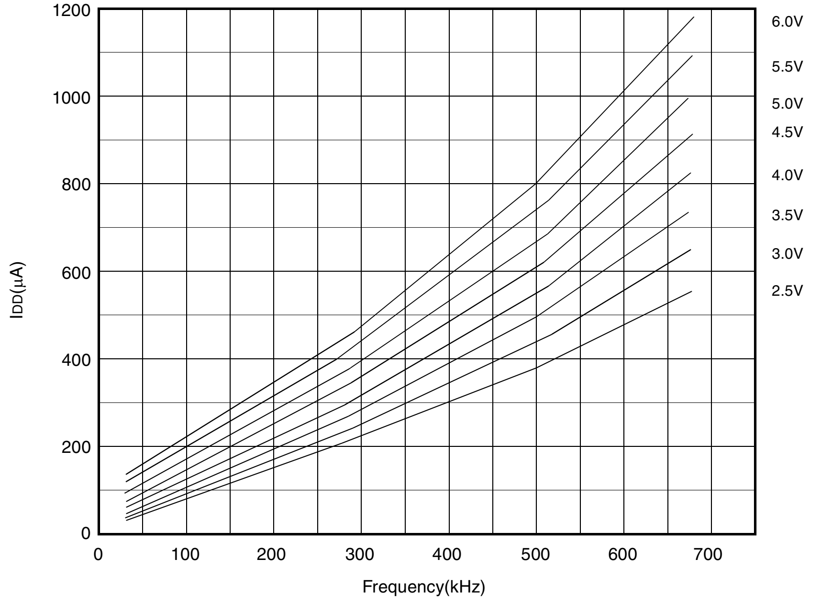


**FIGURE 23-17: MAXIMUM IDD vs. FREQUENCY (RC MODE @ 300 pF, -40°C TO 85°C)**



Data based on matrix samples. See first page of this section for details.

## F.5 PIC16C55X Family of Devices

| | | PIC16C554 | PIC16C556[1] | PIC16C558 |
|---|---|---|---|---|
| **Clock** | Maximum Frequency of Operation (MHz) | 20 | 20 | 20 |
| **Memory** | EPROM Program Memory (x14 words) | 512 | 1K | 2K |
| | Data Memory (bytes) | 80 | 80 | 128 |
| **Peripherals** | Timer Module(s) | TMR0 | TMR0 | TMR0 |
| | Comparators(s) | — | — | — |
| | Internal Reference Voltage | — | — | — |
| **Features** | Interrupt Sources | 3 | 3 | 3 |
| | I/O Pins | 13 | 13 | 13 |
| | Voltage Range (Volts) | 2.5-6.0 | 2.5-6.0 | 2.5-6.0 |
| | Brown-out Reset | — | — | — |
| | Packages | 18-pin DIP,<br>SOIC;<br>20-pin SSOP | 18-pin DIP,<br>SOIC;<br>20-pin SSOP | 18-pin DIP,<br>SOIC;<br>20-pin SSOP |

All PIC16/17 Family devices have Power-on Reset, selectable Watchdog Timer, selectable code protect and high I/O current capability. All PIC16C5XX Family devices use serial programming with clock pin RB6 and data pin RB7.

Note 1: Please contact your local Microchip sales office for availability of these devices.

## F.6 PIC16C62X and PIC16C64X Family of Devices

| | | PIC16C620 | PIC16C621 | PIC16C622 | PIC16C642 | PIC16C662 |
|---|---|---|---|---|---|---|
| **Clock** | Maximum Frequency of Operation (MHz) | 20 | 20 | 20 | 20 | 20 |
| **Memory** | EPROM Program Memory (x14 words) | 512 | 1K | 2K | 4K | 4K |
| | Data Memory (bytes) | 80 | 80 | 128 | 176 | 176 |
| **Peripherals** | Timer Module(s) | TMR0 | TMR0 | TMR0 | TMR0 | TMR0 |
| | Comparators(s) | 2 | 2 | 2 | 2 | 2 |
| | Internal Reference Voltage | Yes | Yes | Yes | Yes | Yes |
| **Features** | Interrupt Sources | 4 | 4 | 4 | 4 | 5 |
| | I/O Pins | 13 | 13 | 13 | 22 | 33 |
| | Voltage Range (Volts) | 2.5-6.0 | 2.5-6.0 | 2.5-6.0 | 3.0-6.0 | 3.0-6.0 |
| | Brown-out Reset | Yes | Yes | Yes | Yes | Yes |
| | Packages | 18-pin DIP,<br>SOIC;<br>20-pin SSOP | 18-pin DIP,<br>SOIC;<br>20-pin SSOP | 18-pin DIP,<br>SOIC;<br>20-pin SSOP | 28-pin PDIP,<br>SOIC,<br>Windowed CDIP | 40-pin PDIP,<br>Windowed CDIP;<br>44-pin PLCC, MQFP |

All PIC16/17 Family devices have Power-on Reset, selectable Watchdog Timer, selectable code protect and high I/O current capability. All PIC16C62X and PIC16C64X Family devices use serial programming with clock pin RB6 and data pin RB7.