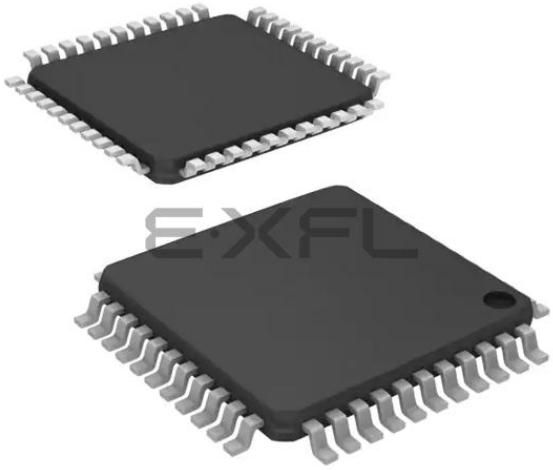

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | PIC |
| Core Size | 8-Bit |
| Speed | 4MHz |
| Connectivity | I²C, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, POR, PWM, WDT |
| Number of I/O | 33 |
| Program Memory Size | 14KB (8K x 14) |
| Program Memory Type | OTP |
| EEPROM Size | - |
| RAM Size | 368 x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.5V ~ 6V |
| Data Converters | - |
| Oscillator Type | External |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 44-TQFP |
| Supplier Device Package | 44-TQFP (10x10) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic16lc67-04-pt |

#### 4.2.2.1 STATUS REGISTER

| Applicable Devices | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 61 | 62 | 62A | R62 | 63 | R63 | 64 | 64A | R64 | 65 | 65A | R65 | 66 | 67 |

The STATUS register, shown in Figure 4-9, contains the arithmetic status of the ALU, the RESET status and the bank select bits for data memory.

The STATUS register can be the destination for any instruction, as with any other register. If the STATUS register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Furthermore, the $\overline{TO}$ and $\overline{PD}$ bits are not writable. Therefore, the result of an instruction with the STATUS register as destination may be different than intended.

For example, `CLRF STATUS` will clear the upper-three bits and set the Z bit. This leaves the STATUS register as `000u u1uu` (where `u` = unchanged).

It is recommended, therefore, that only `BCF`, `BSF`, `SWAPF` and `MOVWF` instructions are used to alter the STATUS register because these instructions do not affect the Z, C or DC bits from the STATUS register. For other instructions, not affecting any status bits, see the "Instruction Set Summary."

**Note 1:** For those devices that do not use bits IRP and RP1 (STATUS<7:6>), maintain these bits clear to ensure upward compatibility with future products.

**Note 2:** The C and DC bits operate as a $\overline{borrow}$ and $\overline{digit\ borrow}$ bit, respectively, in subtraction. See the `SUBLW` and `SUBWF` instructions for examples.

**FIGURE 4-9: STATUS REGISTER (ADDRESS 03h, 83h, 103h, 183h)**

| R/W-0 | R/W-0 | R/W-0 | R-1 | R-1 | R/W-x | R/W-x | R/W-x |
|---|---|---|---|---|---|---|---|
| IRP | RP1 | RP0 | $\overline{TO}$ | $\overline{PD}$ | Z | DC | C |
| bit7 | | | | | | | bit0 |

R = Readable bit
W = Writable bit
- n = Value at POR reset
x = unknown

bit 7: **IRP**: RegIster Bank Select bit (used for indirect addressing)
1 = Bank 2, 3 (100h - 1FFh)
0 = Bank 0, 1 (00h - FFh)

bit 6-5: **RP1:RP0**: Register Bank Select bits (used for direct addressing)
11 = Bank 3 (180h - 1FFh)
10 = Bank 2 (100h - 17Fh)
01 = Bank 1 (80h - FFh)
00 = Bank 0 (00h - 7Fh)
Each bank is 128 bytes.

bit 4: **$\overline{TO}$**: Time-out bit
1 = After power-up, `CLRWDT` instruction, or `SLEEP` instruction
0 = A WDT time-out occurred

bit 3: **$\overline{PD}$**: Power-down bit
1 = After power-up or by the `CLRWDT` instruction
0 = By execution of the `SLEEP` instruction

bit 2: **Z**: Zero bit
1 = The result of an arithmetic or logic operation is zero
0 = The result of an arithmetic or logic operation is not zero

bit 1: **DC**: Digit carry/$\overline{borrow}$ bit (for `ADDWF`, `ADDLW`, `SUBLW`, and `SUBWF` instructions) (For $\overline{borrow}$ the polarity is reversed).
1 = A carry-out from the 4th low order bit of the result occurred
0 = No carry-out from the 4th low order bit of the result

bit 0: **C**: Carry/$\overline{borrow}$ bit (for `ADDWF`, `ADDLW`, `SUBLW`, and `SUBWF` instructions)( For $\overline{borrow}$ the polarity is reversed).
1 = A carry-out from the most significant bit of the result occurred
0 = No carry-out from the most significant bit of the result
Note: a subtraction is executed by adding the two's complement of the second operand.
For rotate (`RRF`, `RLF`) instructions, this bit is loaded with either the high or low order bit of the source register.

**NOTES:**

### 5.3 PORTC and TRISC Register

| Applicable Devices | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 61 | 62 | 62A | R62 | 63 | R63 | 64 | 64A | R64 | 65 | 65A | R65 | 66 | 67 |

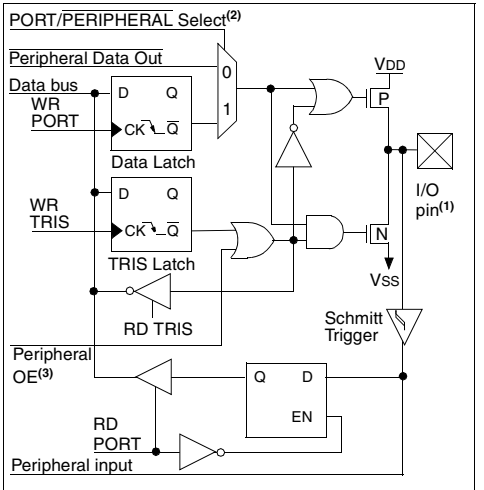
PORTC is an 8-bit wide bi-directional port. Each pin is individually configurable as an input or output through the TRISC register. PORTC is multiplexed with several peripheral functions (Table 5-5). PORTC pins have Schmitt Trigger input buffers.

When enabling peripheral functions, care should be taken in defining TRIS bits for each PORTC pin. Some peripherals override the TRIS bit to make a pin an output, while other peripherals override the TRIS bit to make a pin an input. Since the TRIS bit override is in effect while the peripheral is enabled, read-modify-write instructions (`BSF, BCF, XORWF`) with TRISC as destination should be avoided. The user should refer to the corresponding peripheral section for the correct TRIS bit settings.

**EXAMPLE 5-3: INITIALIZING PORTC**

```
BCF     STATUS, RP0   ;
BCF     STATUS, RP1   ; PIC16C66/67 only
CLRF    PORTC         ; Initialize PORTC by
                      ; clearing output
                      ; data latches
BSF     STATUS, RP0   ; Select Bank 1
MOVLW   0xCF          ; Value used to
                      ; initialize data
                      ; direction
MOVWF   TRISC         ; Set RC<3:0> as inputs
                      ; RC<5:4> as outputs
                      ; RC<7:6> as inputs
```

**FIGURE 5-6: PORTC BLOCK DIAGRAM**




Note 1: I/O pins have diode protection to VDD and VSS.
2: Port/Peripheral select signal selects between port data and peripheral output.
3: Peripheral OE (output enable) is only activated if peripheral select is active.

**TABLE 5-5: PORTC FUNCTIONS FOR PIC16C62/64**

| Name | Bit# | Buffer Type | Function |
|---|---|---|---|
| RC0/T1OSI/T1CKI | bit0 | ST | Input/output port pin or Timer1 oscillator input or Timer1 clock input |
| RC1/T1OSO | bit1 | ST | Input/output port pin or Timer1 oscillator output |
| RC2/CCP1 | bit2 | ST | Input/output port pin or Capture1 input/Compare1 output/PWM1 output |
| RC3/SCK/SCL | bit3 | ST | RC3 can also be the synchronous serial clock for both SPI and $I^2C$ modes. |
| RC4/SDI/SDA | bit4 | ST | RC4 can also be the SPI Data In (SPI mode) or data I/O ($I^2C$ mode). |
| RC5/SDO | bit5 | ST | Input/output port pin or synchronous serial port data output |
| RC6 | bit6 | ST | Input/output port pin |
| RC7 | bit7 | ST | Input/output port pin |

Legend: ST = Schmitt Trigger input

### 11.3.1 SSP MODULE IN SPI MODE FOR PIC16C66/67

The SPI mode allows 8-bits of data to be synchronously transmitted and received simultaneously. To accomplish communication, typically three pins are used:

- Serial Data Out (SDO) RC5/SDO
- Serial Data In (SDI) RC4/SDI/SDA
- Serial Clock (SCK) RC3/SCK/SCL

Additionally a fourth pin may be used when in a slave mode of operation:

- Slave Select ($\overline{SS}$) RA5/$\overline{SS}$

When initializing the SPI, several options need to be specified. This is done by programming the appropriate control bits in the SSPCON register (SSPCON<5:0>) and SSPSTAT<7:6>. These control bits allow the following to be specified:

- Master Mode (SCK is the clock output)
- Slave Mode (SCK is the clock input)
- Clock Polarity (Idle state of SCK)
- Clock edge (output data on rising/falling edge of SCK)
- Clock Rate (Master mode only)
- Slave Select Mode (Slave mode only)

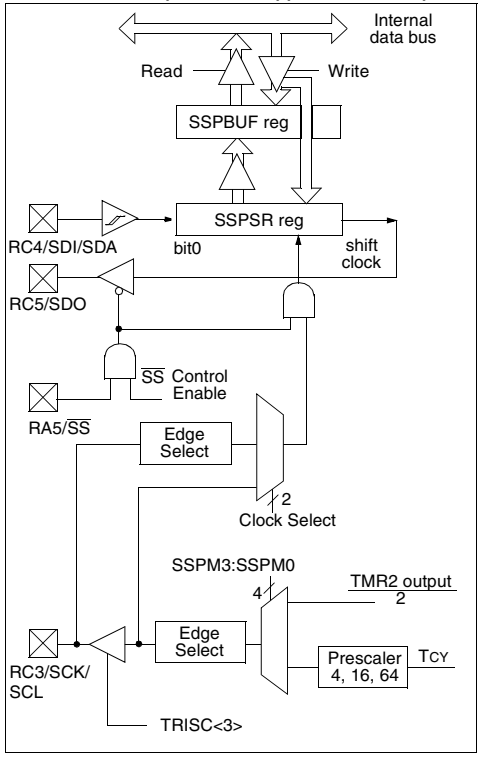
The SSP consists of a transmit/receive Shift Register (SSPSR) and a buffer register (SSPBUF). The SSPSR shifts the data in and out of the device, MSb first. The SSPBUF holds the data that was written to the SSPSR until the received data is ready. Once the 8-bits of data have been received, that byte is moved to the SSPBUF register. Then the buffer full detect bit BF (SSPSTAT<0>) and interrupt flag bit SSPIF (PIR1<3>) are set. This double buffering of the received data (SSPBUF) allows the next byte to start reception before reading the data that was just received. Any write to the SSPBUF register during transmission/reception of data will be ignored, and the write collision detect bit WCOL (SSPCON<7>) will be set. User software must clear the WCOL bit so that it can be determined if the following write(s) to the SSPBUF register completed successfully. When the application software is expecting to receive valid data, the SSPBUF should be read before the next byte of data to transfer is written to the SSPBUF. Buffer full bit BF (SSPSTAT<0>) indicates when SSPBUF has been loaded with the received data (transmission is complete). When the SSPBUF is read, bit BF is cleared. This data may be irrelevant if the SPI is only a transmitter. Generally the SSP Interrupt is used to determine when the transmission/reception has completed. The SSPBUF must be read and/or written. If the interrupt method is not going to be used, then software polling can be done to ensure that a write collision does not occur. Example 11-2 shows the loading of the SSPBUF (SSPSR) for data transmission. The shaded instruction is only required if the received data is meaningful.

**EXAMPLE 11-2: LOADING THE SSPBUF (SSPSR) REGISTER (PIC16C66/67)**

```
     BCF   STATUS, RP1    ;Specify Bank 1
     BSF   STATUS, RP0    ;
LOOP BTFSS SSPSTAT, BF    ;Has data been
                          ;received
                          ;(transmit
                          ;complete)?
     GOTO  LOOP           ;No
     BCF   STATUS, RP0    ;Specify Bank 0
     MOVF  SSPBUF, W      ;W reg = contents
                          ; of SSPBUF
     MOVWF RXDATA         ;Save in user RAM
     MOVF  TXDATA, W      ;W reg = contents
                          ; of TXDATA
     MOVWF SSPBUF         ;New data to xmit
```

The block diagram of the SSP module, when in SPI mode (Figure 11-9), shows that the SSPSR is not directly readable or writable, and can only be accessed from addressing the SSPBUF register. Additionally, the SSP status register (SSPSTAT) indicates the various status conditions.

**FIGURE 11-9: SSP BLOCK DIAGRAM (SPI MODE)(PIC16C66/67)**



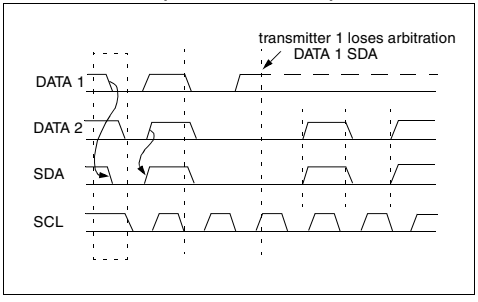
11.4.4 MULTI-MASTER

The $I^2C$ protocol allows a system to have more than one master. This is called multi-master. When two or more masters try to transfer data at the same time, arbitration and synchronization occur.

11.4.4.1 ARBITRATION

Arbitration takes place on the SDA line, while the SCL line is high. The master which transmits a high when the other master transmits a low loses arbitration (Figure 11-22), and turns off its data output stage. A master which lost arbitration can generate clock pulses until the end of the data byte where it lost arbitration. When the master devices are addressing the same device, arbitration continues into the data.

**FIGURE 11-22: MULTI-MASTER ARBITRATION (TWO MASTERS)**




Masters that also incorporate the slave function, and have lost arbitration must immediately switch over to slave-receiver mode. This is because the winning master-transmitter may be addressing it.

Arbitration is not allowed between:

- A repeated START condition
- A STOP condition and a data bit
- A repeated START condition and a STOP condition

Care needs to be taken to ensure that these conditions do not occur.

11.2.4.2 Clock Synchronization

Clock synchronization occurs after the devices have started arbitration. This is performed using a wired-AND connection to the SCL line. A high to low transition on the SCL line causes the concerned devices to start counting off their low period. Once a device clock has gone low, it will hold the SCL line low until its SCL high state is reached. The low to high transition of this clock may not change the state of the SCL line, if another device clock is still within its low period. The SCL line is held low by the device with the longest low period. Devices with shorter low periods enter a high wait-state, until the SCL line comes high. When the SCL line comes high, all devices start counting off their high periods. The first device to complete its high period will pull the SCL line low. The SCL line high time is determined by the device with the shortest high period, Figure 11-23.

**FIGURE 11-23: CLOCK SYNCHRONIZATION**

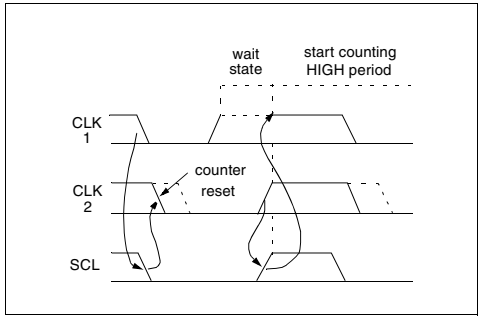


**TABLE 13-12: INITIALIZATION CONDITIONS FOR ALL REGISTERS (Cont.'d)**

| Register | Applicable Devices | | | | | | | | | | | | | | Power-on Reset Brown-out Reset | $\overline{\text{MCLR}}$ Reset during: – normal operation – SLEEP WDT Reset | Wake-up via interrupt or WDT Wake-up |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TRISD | 61 | 62 | 62A | R62 | 63 | R63 | 64 | 64A | R64 | 65 | 65A | R65 | 66 | 67 | 1111 1111 | 1111 1111 | uuuu uuuu |
| TRISE | 61 | 62 | 62A | R62 | 63 | R63 | 64 | 64A | R64 | 65 | 65A | R65 | 66 | 67 | 0000 -111 | 0000 -111 | uuuu -uuu |
| PIE1 | 61 | 62 | 62A | R62 | 63 | R63 | 64 | 64A | R64 | 65 | 65A | R65 | 66 | 67 | 00-- 0000 | 00-- 0000 | uu-- uuuu |
| | 61 | 62 | 62A | R62 | 63 | R63 | 64 | 64A | R64 | 65 | 65A | R65 | 66 | 67 | 0000 0000 | 0000 0000 | uuuu uuuu |
| PIE2 | 61 | 62 | 62A | R62 | 63 | R63 | 64 | 64A | R64 | 65 | 65A | R65 | 66 | 67 | ---- ---0 | ---- ---0 | ---- ---u |
| PCON | 61 | 62 | 62A | R62 | 63 | R63 | 64 | 64A | R64 | 65 | 65A | R65 | 66 | 67 | ---- --0u | ---- --uu | ---- --uu |
| | 61 | 62 | 62A | R62 | 63 | R63 | 64 | 64A | R64 | 65 | 65A | R65 | 66 | 67 | ---- --0- | ---- --u- | ---- --u- |
| PR2 | 61 | 62 | 62A | R62 | 63 | R63 | 64 | 64A | R64 | 65 | 65A | R65 | 66 | 67 | 1111 1111 | 1111 1111 | 1111 1111 |
| SSPADD | 61 | 62 | 62A | R62 | 63 | R63 | 64 | 64A | R64 | 65 | 65A | R65 | 66 | 67 | 0000 0000 | 0000 0000 | uuuu uuuu |
| SSPSTAT | 61 | 62 | 62A | R62 | 63 | R63 | 64 | 64A | R64 | 65 | 65A | R65 | 66 | 67 | --00 0000 | --00 0000 | --uu uuuu |
| TXSTA | 61 | 62 | 62A | R62 | 63 | R63 | 64 | 64A | R64 | 65 | 65A | R65 | 66 | 67 | 0000 -010 | 0000 -010 | uuuu -uuu |
| SPBRG | 61 | 62 | 62A | R62 | 63 | R63 | 64 | 64A | R64 | 65 | 65A | R65 | 66 | 67 | 0000 0000 | 0000 0000 | uuuu uuuu |

Legend: u = unchanged, x = unknown, - = unimplemented bit read as '0', q = value depends on condition.

Note 1: One or more bits in INTCON, PIR1 and/or PIR2 will be affected (to cause wake-up).

2: When the wake-up is due to an interrupt and the global enable bit, GIE is set, the PC is loaded with the interrupt vector (0004h) after execution of PC + 1.

3: See Table 13-10 and Table 13-11 for reset value for specific conditions.

**GOTO** **Unconditional Branch**

Syntax: [ *label* ] GOTO k

Operands: $0 \le k \le 2047$

Operation: $k \rightarrow PC<10:0>$
$PCLATH<4:3> \rightarrow PC<12:11>$

Status Affected: None

Encoding:

| | | | |
|---|---|---|---|
| 10 | 1kkk | kkkk | kkkk |

Description: GOTO is an unconditional branch. The eleven bit immediate value is loaded into PC bits <10:0>. The upper bits of PC are loaded from PCLATH<4:3>. GOTO is a two cycle instruction.

Words: 1

Cycles: 2

Q Cycle Activity:

| | Q1 | Q2 | Q3 | Q4 |
|---|---|---|---|---|
| 1st Cycle | Decode | Read literal 'k' | Process data | Write to PC |
| 2nd Cycle | No-Operation | No-Operation | No-Operation | No-Operation |

Example GOTO THERE

After Instruction
PC = Address THERE

**INCF** **Increment f**

Syntax: [ *label* ] INCF f,d

Operands: $0 \le f \le 127$
$d \in [0,1]$

Operation: (f) + 1 → (destination)

Status Affected: Z

Encoding:

| | | | |
|---|---|---|---|
| 00 | 1010 | dfff | ffff |

Description: The contents of register 'f' are incremented. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'.

Words: 1

Cycles: 1

Q Cycle Activity:

| Q1 | Q2 | Q3 | Q4 |
|---|---|---|---|
| Decode | Read register 'f' | Process data | Write to destination |

Example INCF CNT, 1

Before Instruction
CNT = 0xFF
Z = 0
After Instruction
CNT = 0x00
Z = 1

| Applicable Devices | 61 | 62 | 62A | R62 | 63 | R63 | 64 | 64A | R64 | 65 | 65A | R65 | 66 | 67 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|

## 16.0 DC AND AC CHARACTERISTICS GRAPHS AND TABLES FOR PIC16C61

The graphs and tables provided in this section are for design guidance and are not tested or guaranteed.

**In some graphs or tables the data presented are outside specified operating range (i.e., outside specified VDD range). This is for information only and devices are guaranteed to operate properly only within the specified range.**

**Note:** The data presented in this section is a statistical summary of data collected on units from different lots over a period of time and matrix samples. 'Typical' represents the mean of the distribution while 'max' or 'min' represents (mean +3σ) and (mean -3σ) respectively where σ is standard deviation.

**FIGURE 16-1: TYPICAL RC OSCILLATOR FREQUENCY vs. TEMPERATURE**

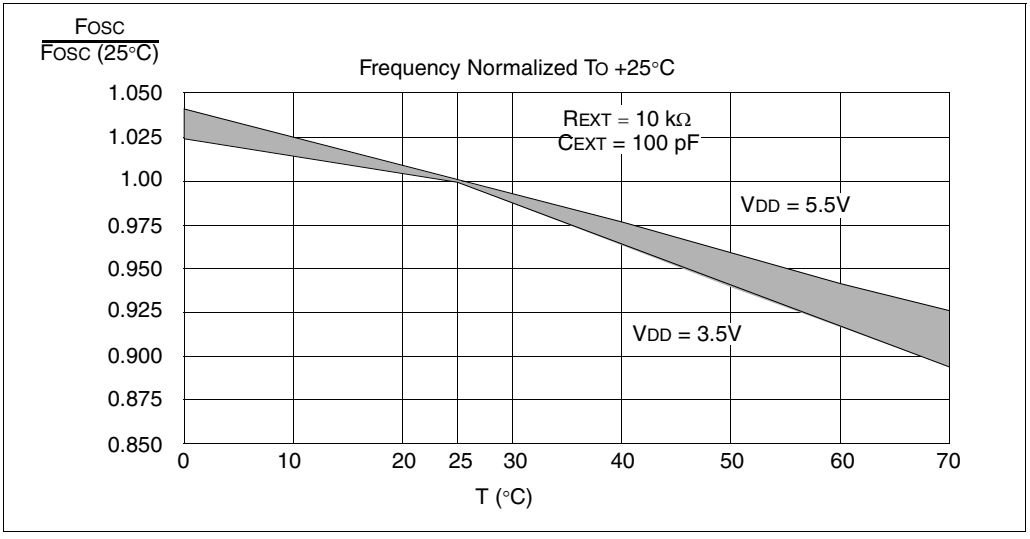



**TABLE 16-1: RC OSCILLATOR FREQUENCIES**

| Cext | Rext | Average Fosc @ 5V, 25°C | |
|---|---|---|---|
| 20 pF | 4.7k | 4.52 MHz | ± 17.35% |
| | 10k | 2.47 MHz | ± 10.10% |
| | 100k | 290.86 kHz | ± 11.90% |
| 100 pF | 3.3k | 1.92 MHz | ± 9.43% |
| | 4.7k | 1.48 MHz | ± 9.83% |
| | 10k | 788.77 kHz | ± 10.92% |
| | 100k | 88.11 kHz | ± 16.03% |
| 300 pF | 3.3k | 726.89 kHz | ± 10.97% |
| | 4.7k | 573.95 kHz | ± 10.14% |
| | 10k | 307.31 kHz | ± 10.43% |
| | 100k | 33.82 kHz | ± 11.24% |

The percentage variation indicated here is part to part variation due to normal process distribution. The variation indicated is ±3 standard deviation from average value for VDD = 5V.

| Applicable Devices | 61 | 62 | 62A | R62 | 63 | R63 | 64 | 64A | R64 | 65 | 65A | R65 | 66 | 67 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|

**FIGURE 16-17: TRANSCONDUCTANCE (gm) OF LP OSCILLATOR vs. VDD**

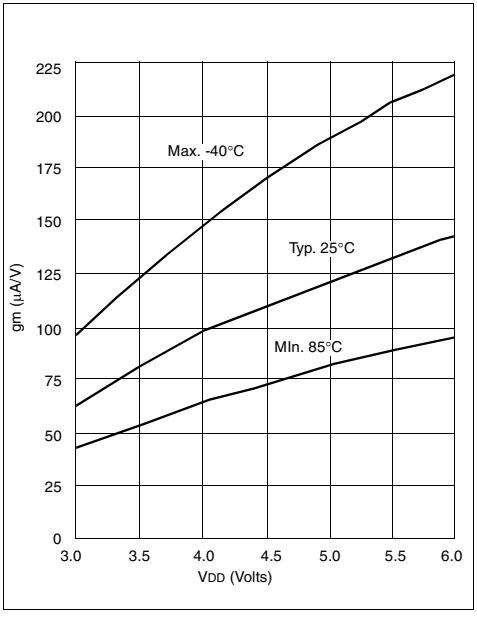



**FIGURE 16-18: TRANSCONDUCTANCE (gm) OF XT OSCILLATOR vs. VDD**

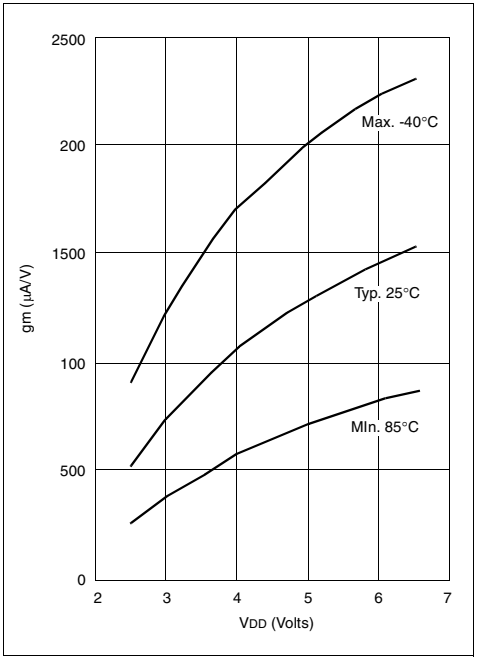



**FIGURE 16-19: IOH vs. VOH, VDD = 3V**

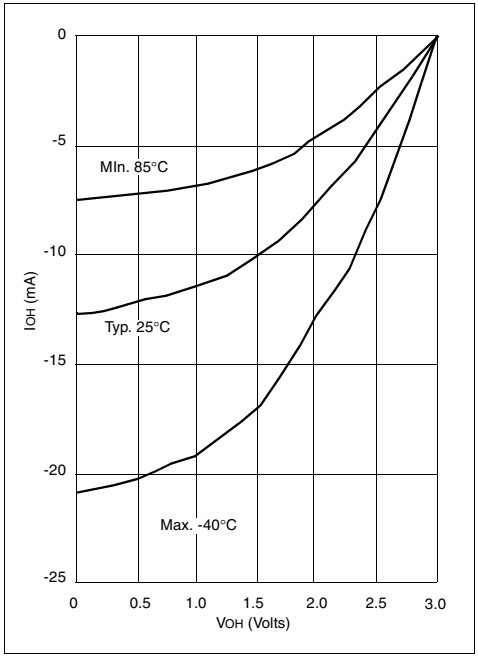
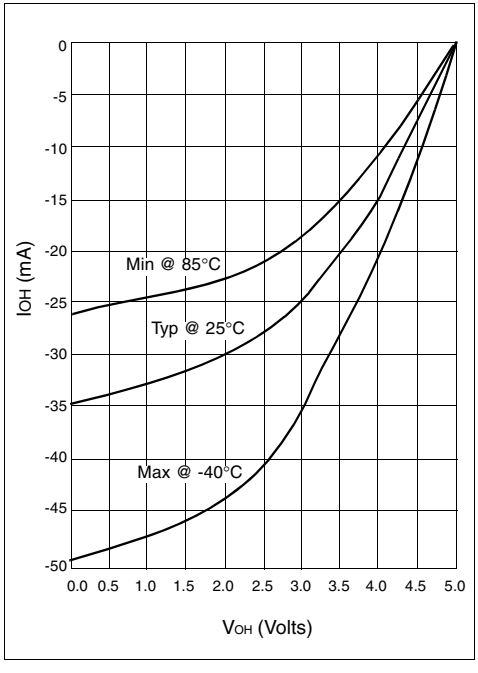


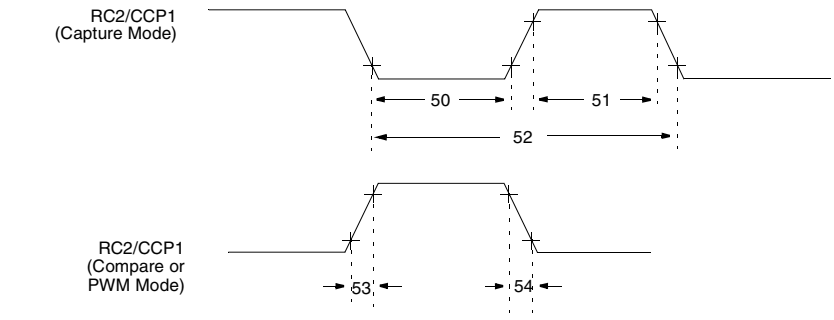

**FIGURE 16-20: IOH vs. VOH, VDD = 5V**




Data based on matrix samples. See first page of this section for details.

| Applicable Devices | 61 | 62 | 62A | R62 | 63 | R63 | 64 | 64A | R64 | 65 | 65A | R65 | 66 | 67 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|

**FIGURE 17-6: CAPTURE/COMPARE/PWM TIMINGS (CCP1)**




Note: Refer to Figure 17-1 for load conditions.

**TABLE 17-6: CAPTURE/COMPARE/PWM REQUIREMENTS (CCP1)**

| Parameter No. | Sym | Characteristic | | | Min | Typ† | Max | Units | Conditions |
|---|---|---|---|---|---|---|---|---|---|
| 50* | TccL | CCP1 input low time | No Prescaler | | 0.5TCY + 20 | — | — | ns | |
| | | | With Prescaler | PIC16**C**62/64 | 10 | — | — | ns | |
| | | | | PIC16**LC**62/64 | 20 | — | — | ns | |
| 51* | TccH | CCP1 input high time | No Prescaler | | 0.5TCY + 20 | — | — | ns | |
| | | | With Prescaler | PIC16**C**62/64 | 10 | — | — | ns | |
| | | | | PIC16**LC**62/64 | 20 | — | — | ns | |
| 52* | TccP | CCP1 input period | | | $\frac{3T_{CY} + 40}{N}$ | — | — | ns | N = prescale value (1,4 or 16) |
| 53 | TccR | CCP1 output rise time | | PIC16**C**62/64 | — | 10 | 25 | ns | |
| | | | | PIC16**LC**62/64 | — | 25 | 45 | ns | |
| 54 | TccF | CCP1 output fall time | | PIC16**C**62/64 | — | 10 | 25 | ns | |
| | | | | PIC16**LC**62/64 | — | 25 | 45 | ns | |

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

| Applicable Devices | 61 | 62 | 62A | R62 | 63 | R63 | 64 | 64A | R64 | 65 | 65A | R65 | 66 | 67 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|

**DC CHARACTERISTICS**

**Standard Operating Conditions (unless otherwise stated)**
Operating temperature -40°C ≤ TA ≤ +125°C for extended,
-40°C ≤ TA ≤ +85°C for industrial and
0°C ≤ TA ≤ +70°C for commercial
Operating voltage VDD range as described in DC spec Section 18.1 and Section 18.2

| Param No. | Characteristic | Sym | Min | Typ † | Max | Units | Conditions |
|---|---|---|---|---|---|---|---|
| | **Output High Voltage** | | | | | | |
| D090 | I/O ports (Note 3) | VOH | VDD-0.7 | - | - | V | IOH = -3.0 mA, VDD = 4.5V, -40°C to +85°C |
| D090A | | | VDD-0.7 | - | - | V | IOH = -2.5 mA, VDD = 4.5V, -40°C to +125°C |
| D092 | OSC2/CLKOUT (RC osc config) | | VDD-0.7 | - | - | V | IOH = -1.3 mA, VDD = 4.5V, -40°C to +85°C |
| D092A | | | VDD-0.7 | - | - | V | IOH = -1.0 mA, VDD = 4.5V, -40°C to +125°C |
| D150* | **Open-Drain High Voltage** | VOD | - | - | 14 | V | RA4 pin |
| | **Capacitive Loading Specs on Output Pins** | | | | | | |
| D100 | OSC2 pin | COSC2 | - | - | 15 | pF | In XT, HS and LP modes when external clock is used to drive OSC1. |
| D101 | All I/O pins and OSC2 (in RC mode) | CIO | - | - | 50 | pF | |
| D102 | SCL, SDA in $I^2C$ mode | Cb | - | - | 400 | pF | |

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

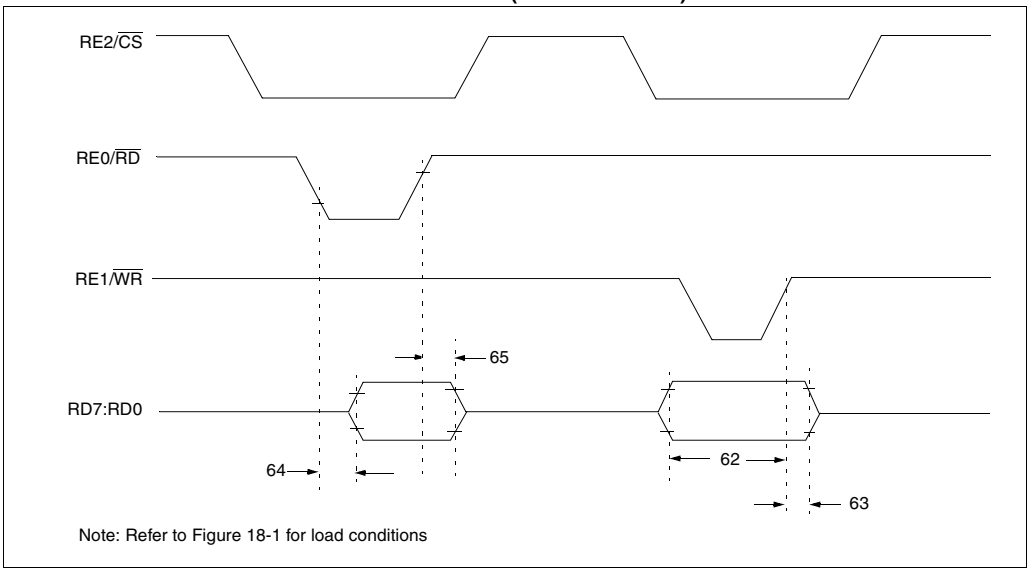
Note 1: In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C6X be driven with external clock in RC mode.

2: The leakage current on the $\overline{MCLR}$/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as current sourced by the pin.

| Applicable Devices | 61 | 62 | 62A | R62 | 63 | R63 | 64 | 64A | R64 | 65 | 65A | R65 | 66 | 67 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|

**FIGURE 18-8: PARALLEL SLAVE PORT TIMING (PIC16C64A/R64)**




Note: Refer to Figure 18-1 for load conditions

**TABLE 18-7: PARALLEL SLAVE PORT REQUIREMENTS (PIC16C64A/R64)**

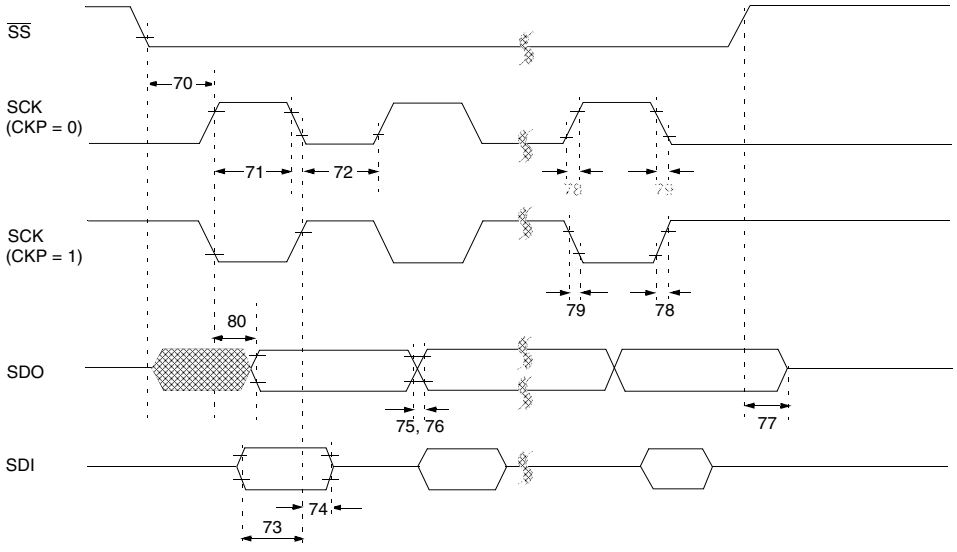
| Parameter No. | Sym | Characteristic | | Min | Typ† | Max | Units | Conditions |
|---|---|---|---|---|---|---|---|---|
| 62 | TdtV2wrH | Data in valid before $\overline{WR}\uparrow$ or $\overline{CS}\uparrow$ (setup time) | | 20 | — | — | ns | |
| | | | | 25 | — | — | ns | Extended Range Only |
| 63* | TwrH2dtI | $\overline{WR}\uparrow$ or $\overline{CS}\uparrow$ to data–in invalid (hold time) | PIC16**C**64A/R64 | 20 | — | — | ns | |
| | | | PIC16**LC**64A.R64 | 35 | — | — | ns | |
| 64 | TrdL2dtV | $\overline{RD}\downarrow$ and $\overline{CS}\downarrow$ to data–out valid | | — | — | 80 | ns | |
| | | | | — | — | 90 | ns | Extended Range Only |
| 65* | TrdH2dtI | $\overline{RD}\uparrow$ or $\overline{CS}\uparrow$ to data–out invalid | | 10 | — | 30 | ns | |

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

| Applicable Devices | 61 | 62 | 62A | R62 | 63 | R63 | 64 | 64A | R64 | 65 | 65A | R65 | 66 | 67 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|

**FIGURE 18-9: SPI MODE TIMING**




Note: Refer to Figure 18-1 for load conditions

**TABLE 18-8: SPI MODE REQUIREMENTS**

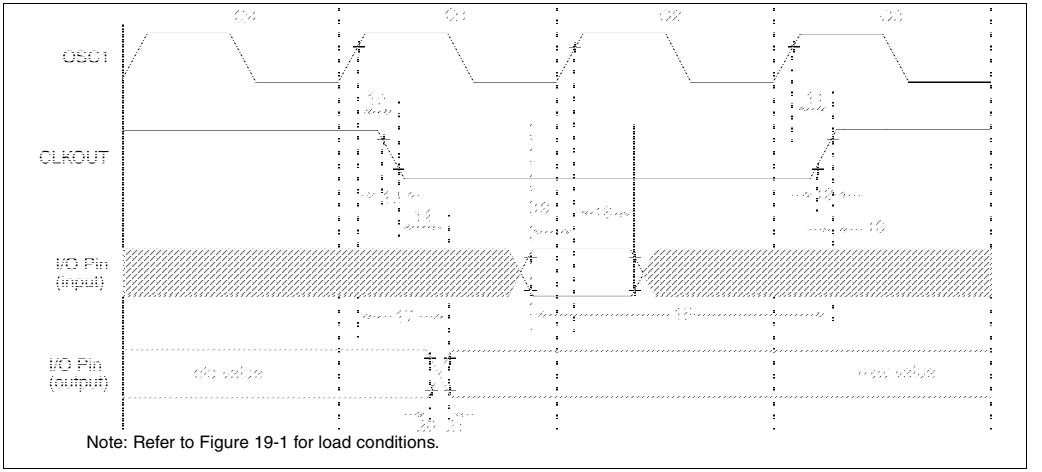
| Parameter No. | Sym | Characteristic | Min | Typ† | Max | Units | Conditions |
|---|---|---|---|---|---|---|---|
| 70* | TssL2scH, TssL2scL | $\overline{SS}\downarrow$ to SCK↓ or SCK↑ input | TCY | — | — | ns | |
| 71* | TscH | SCK input high time (slave mode) | TCY + 20 | — | — | ns | |
| 72* | TscL | SCK input low time (slave mode) | TCY + 20 | — | — | ns | |
| 73* | TdiV2scH, TdiV2scL | Setup time of SDI data input to SCK edge | 50 | — | — | ns | |
| 74* | TscH2diL, TscL2diL | Hold time of SDI data input to SCK edge | 50 | — | — | ns | |
| 75* | TdoR | SDO data output rise time | — | 10 | 25 | ns | |
| 76* | TdoF | SDO data output fall time | — | 10 | 25 | ns | |
| 77* | TssH2doZ | $\overline{SS}\uparrow$ to SDO output hi-impedance | 10 | — | 50 | ns | |
| 78* | TscR | SCK output rise time (master mode) | — | 10 | 25 | ns | |
| 79* | TscF | SCK output fall time (master mode) | — | 10 | 25 | ns | |
| 80* | TscH2doV, TscL2doV | SDO data output valid after SCK edge | — | — | 50 | ns | |

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

| Applicable Devices | 61 | 62 | 62A | R62 | 63 | R63 | 64 | 64A | R64 | 65 | 65A | R65 | 66 | 67 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|

**FIGURE 19-3: CLKOUT AND I/O TIMING**




Note: Refer to Figure 19-1 for load conditions.

**TABLE 19-3: CLKOUT AND I/O TIMING REQUIREMENTS**

| Parameter No. | Sym | Characteristic | | Min | Typ† | Max | Units | Conditions |
|---|---|---|---|---|---|---|---|---|
| 10* | TosH2ckL | OSC1↑ to CLKOUT↓ | | — | 75 | 200 | ns | Note 1 |
| 11* | TosH2ckH | OSC1↑ to CLKOUT↑ | | — | 75 | 200 | ns | Note 1 |
| 12* | TckR | CLKOUT rise time | | — | 35 | 100 | ns | Note 1 |
| 13* | TckF | CLKOUT fall time | | — | 35 | 100 | ns | Note 1 |
| 14* | TckL2ioV | CLKOUT ↓ to Port out valid | | — | — | 0.5TCY + 20 | ns | Note 1 |
| 15* | TioV2ckH | Port in valid before CLKOUT ↑ | | 0.25TCY + 25 | — | — | ns | Note 1 |
| 16* | TckH2ioI | Port in hold after CLKOUT ↑ | | 0 | — | — | ns | Note 1 |
| 17* | TosH2ioV | OSC1↑ (Q1 cycle) to Port out valid | | — | 50 | 150 | ns | |
| 18* | TosH2ioI | OSC1↑ (Q2 cycle) to Port input invalid (I/O in hold time) | PIC16**C**65 | 100 | — | — | ns | |
| | | | PIC16**LC**65 | 200 | — | — | ns | |
| 19* | TioV2osH | Port input valid to OSC1↑ (I/O in setup time) | | 0 | — | — | ns | |
| 20* | TioR | Port output rise time | PIC16**C**65 | — | 10 | 25 | ns | |
| | | | PIC16**LC**65 | — | — | 60 | ns | |
| 21* | TioF | Port output fall time | PIC16**C**65 | — | 10 | 25 | ns | |
| | | | PIC16**LC**65 | — | — | 60 | ns | |
| 22††* | Tinp | RB0/INT pin high or low time | | TCY | — | — | ns | |
| 23††* | Trbp | RB7:RB4 change int high or low time | | TCY | — | — | ns | |

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

†† These parameters are asynchronous events not related to any internal clock edge.

Note 1: Measurements are taken in RC Mode where CLKOUT output is 4 x TOSC.

| Applicable Devices | 61 | 62 | 62A | R62 | 63 | R63 | 64 | 64A | R64 | 65 | 65A | R65 | 66 | 67 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|

## 20.1 DC Characteristics: PIC16C63/65A-04 (Commercial, Industrial, Extended) PIC16C63/65A-10 (Commercial, Industrial, Extended) PIC16C63/65A-20 (Commercial, Industrial, Extended)

| DC CHARACTERISTICS | | | Standard Operating Conditions (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +125°C for extended,<br>-40°C ≤ TA ≤ +85°C for industrial and<br>0°C ≤ TA ≤ +70°C for commercial | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Characteristic** | **Sym** | **Min** | **Typ†** | **Max** | **Units** | **Conditions** |
| D001 | Supply Voltage | VDD | 4.0 | - | 6.0 | V | XT, RC and LP osc configuration |
| D001A | | | 4.5 | - | 5.5 | V | HS osc configuration |
| D002* | RAM Data Retention Voltage (Note 1) | VDR | - | 1.5 | - | V | |
| D003 | VDD start voltage to ensure internal Power-on Reset signal | VPOR | - | VSS | - | V | See section on Power-on Reset for details |
| D004* | VDD rise rate to ensure internal Power-on Reset signal | SVDD | 0.05 | - | - | V/ms | See section on Power-on Reset for details |
| D005 | Brown-out Reset Voltage | BVDD | 3.7 | 4.0 | 4.3 | V | BODEN configuration bit is enabled |
| | | | 3.7 | 4.0 | 4.4 | V | Extended Range Only |
| D010 | Supply Current (Note 2, 5) | IDD | - | 2.7 | 5 | mA | XT, RC, osc config FOSC = 4 MHz, VDD = 5.5V (Note 4) |
| D013 | | | - | 10 | 20 | mA | HS osc config FOSC = 20 MHz, VDD = 5.5V |
| D015* | Brown-out Reset Current (Note 6) | ΔIBOR | - | 350 | 425 | µA | BOR enabled, VDD = 5.0V |
| D020 | Power-down Current (Note 3, 5) | IPD | - | 10.5 | 42 | µA | VDD = 4.0V, WDT enabled,-40°C to +85°C |
| D021 | | | - | 1.5 | 16 | µA | VDD = 4.0V, WDT disabled,-0°C to +70°C |
| D021A | | | - | 1.5 | 19 | µA | VDD = 4.0V, WDT disabled,-40°C to +85°C |
| D021B | | | - | 2.5 | 19 | µA | VDD = 4.0V, WDT disabled,-40°C to +125°C |
| D023* | Brown-out Reset Current (Note 6) | ΔIBOR | - | 350 | 425 | µA | BOR enabled, VDD = 5.0V |

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.
The test conditions for all IDD measurements in active operation mode are:
OSC1 = external square wave, from rail to rail; all I/O pins tristated, pulled to VDD,
$\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

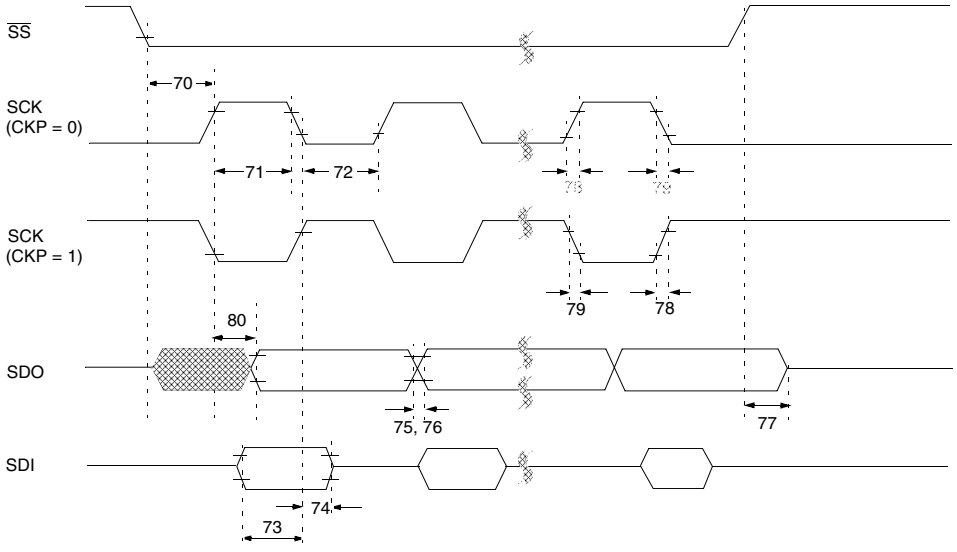
3: The power down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

4: For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula Ir = VDD/2Rext (mA) with Rext in kOhm.

5: Timer1 oscillator (when enabled) adds approximately 20 µA to the specification. This value is from characterization and is for design guidance only. This is not tested.

6: The Δ current is the additional current consumed when this peripheral is enabled. This current should be added to the base IDD or IPD measurement.

**FIGURE 21-9: SPI MODE TIMING**




Note: Refer to Figure 21-1 for load conditions

**TABLE 21-8: SPI MODE REQUIREMENTS**

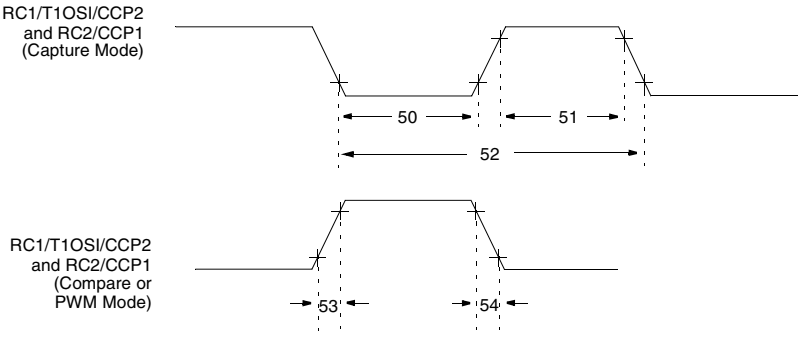
| Parameter No. | Sym | Characteristic | Min | Typ† | Max | Units | Conditions |
|---|---|---|---|---|---|---|---|
| 70* | TssL2scH, TssL2scL | $\overline{SS}$↓ to SCK↓ or SCK↑ input | TCY | — | — | ns | |
| 71* | TscH | SCK input high time (slave mode) | TCY + 20 | — | — | ns | |
| 72* | TscL | SCK input low time (slave mode) | TCY + 20 | — | — | ns | |
| 73* | TdiV2scH, TdiV2scL | Setup time of SDI data input to SCK edge | 50 | — | — | ns | |
| 74* | TscH2diL, TscL2diL | Hold time of SDI data input to SCK edge | 50 | — | — | ns | |
| 75* | TdoR | SDO data output rise time | — | 10 | 25 | ns | |
| 76* | TdoF | SDO data output fall time | — | 10 | 25 | ns | |
| 77* | TssH2doZ | $\overline{SS}$↑ to SDO output hi-impedance | 10 | — | 50 | ns | |
| 78* | TscR | SCK output rise time (master mode) | — | 10 | 25 | ns | |
| 79* | TscF | SCK output fall time (master mode) | — | 10 | 25 | ns | |
| 80* | TscH2doV, TscL2doV | SDO data output valid after SCK edge | — | — | 50 | ns | |

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

| Applicable Devices | 61 | 62 | 62A | R62 | 63 | R63 | 64 | 64A | R64 | 65 | 65A | R65 | 66 | 67 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|

**FIGURE 22-7: CAPTURE/COMPARE/PWM TIMINGS (CCP1 AND CCP2)**




Note: Refer to Figure 22-1 for load conditions.

**TABLE 22-6: CAPTURE/COMPARE/PWM REQUIREMENTS (CCP1 AND CCP2)**

| Parameter No. | Sym | Characteristic | | | Min | Typ† | Max | Units | Conditions |
|---|---|---|---|---|---|---|---|---|---|
| 50* | TccL | CCP1 and CCP2 input low time | No Prescaler | | 0.5TCY + 20 | — | — | ns | |
| | | | With Prescaler | PIC16**C**66/67 | 10 | — | — | ns | |
| | | | | PIC16**LC**66/67 | 20 | — | — | ns | |
| 51* | TccH | CCP1 and CCP2 input high time | No Prescaler | | 0.5TCY + 20 | — | — | ns | |
| | | | With Prescaler | PIC16**C**66/67 | 10 | — | — | ns | |
| | | | | PIC16**LC**66/67 | 20 | — | — | ns | |
| 52* | TccP | CCP1 and CCP2 input period | | | $\frac{3T_{CY} + 40}{N}$ | — | — | ns | N = prescale value (1,4, or 16) |
| 53* | TccR | CCP1 and CCP2 output rise time | | PIC16**C**66/67 | — | 10 | 25 | ns | |
| | | | | PIC16**LC**66/67 | — | 25 | 45 | ns | |
| 54* | TccF | CCP1 and CCP2 output fall time | | PIC16**C**66/67 | — | 10 | 25 | ns | |
| | | | | PIC16**LC**66/67 | — | 25 | 45 | ns | |

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

| Applicable Devices | 61 | 62 | 62A | R62 | 63 | R63 | 64 | 64A | R64 | 65 | 65A | R65 | 66 | 67 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|

**FIGURE 23-29: TYPICAL IDD vs. FREQUENCY (HS MODE, 25°C)**

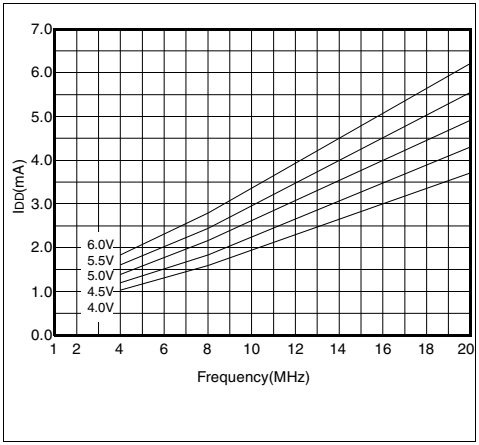
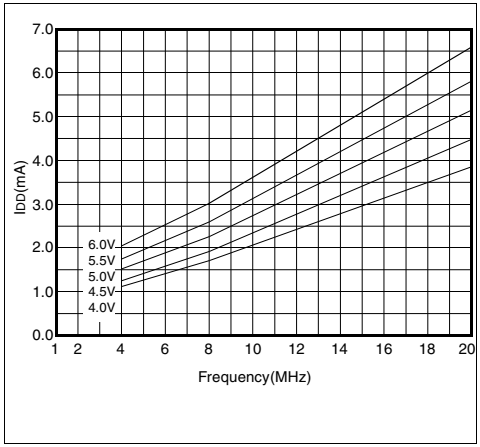


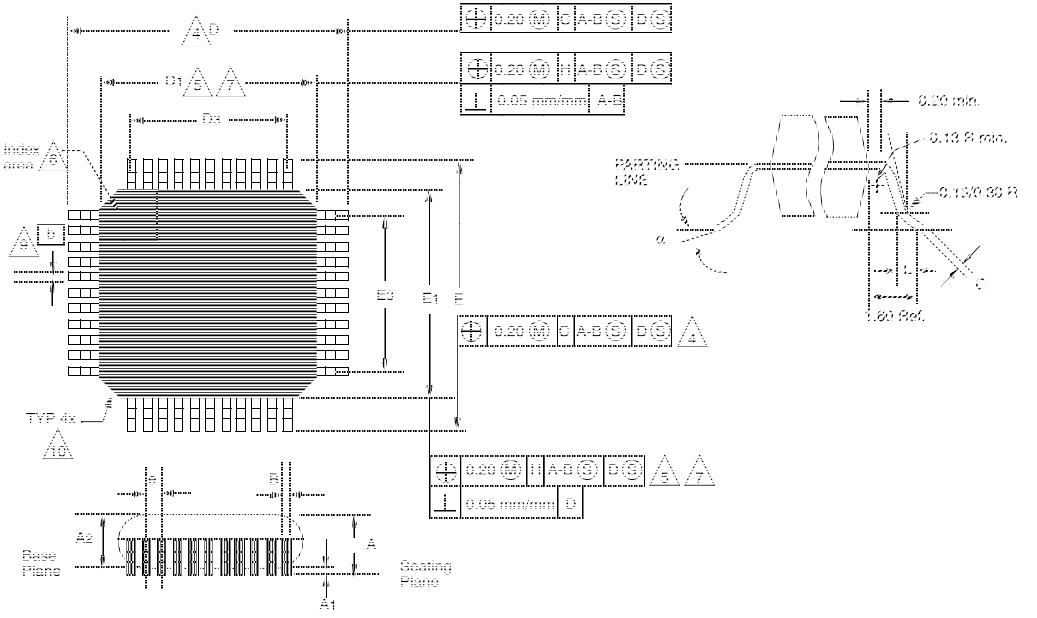

**FIGURE 23-30: MAXIMUM IDD vs. FREQUENCY (HS MODE, -40°C TO 85°C)**




Data based on matrix samples. See first page of this section for details.

### 24.12 44-Lead Plastic Surface Mount (MQFP 10x10 mm Body 1.6/0.15 mm Lead Form) (PQ)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




| Package Group: Plastic MQFP | | | | | | |
|---|---|---|---|---|---|---|
| | Millimeters | | | Inches | | |
| Symbol | Min | Max | Notes | Min | Max | Notes |
| α | 0° | 7° | | 0° | 7° | |
| A | 2.000 | 2.350 | | 0.078 | 0.093 | |
| A1 | 0.050 | 0.250 | | 0.002 | 0.010 | |
| A2 | 1.950 | 2.100 | | 0.768 | 0.083 | |
| b | 0.300 | 0.450 | **Typical** | 0.011 | 0.018 | **Typical** |
| C | 0.150 | 0.180 | | 0.006 | 0.007 | |
| D | 12.950 | 13.450 | | 0.510 | 0.530 | |
| D1 | 9.900 | 10.100 | | 0.390 | 0.398 | |
| D3 | 8.000 | 8.000 | **Reference** | 0.315 | 0.315 | **Reference** |
| E | 12.950 | 13.450 | | 0.510 | 0.530 | |
| E1 | 9.900 | 10.100 | | 0.390 | 0.398 | |
| E3 | 8.000 | 8.000 | **Reference** | 0.315 | 0.315 | **Reference** |
| e | 0.800 | 0.800 | | 0.031 | 0.032 | |
| L | 0.730 | 1.030 | | 0.028 | 0.041 | |
| N | 44 | 44 | | 44 | 44 | |
| CP | 0.102 | – | | 0.004 | – | |