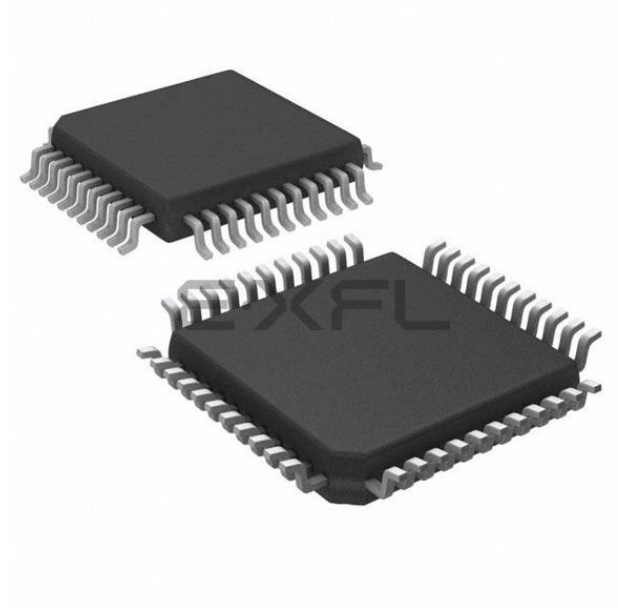
# Microchip Technology - PIC16LC67-04I/PQ Datasheet



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## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | PIC |
| Core Size | 8-Bit |
| Speed | 4MHz |
| Connectivity | I²C, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, POR, PWM, WDT |
| Number of I/O | 33 |
| Program Memory Size | 14KB (8K x 14) |
| Program Memory Type | OTP |
| EEPROM Size | - |
| RAM Size | 368 x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.5V ~ 6V |
| Data Converters | - |
| Oscillator Type | External |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 44-QFP |
| Supplier Device Package | 44-MQFP (10x10) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic16lc67-04i-pq |

**TABLE 3-1: PIC16C61 PINOUT DESCRIPTION**

| Pin Name | DIP Pin# | SOIC Pin# | Pin Type | Buffer Type | Description |
|---|---|---|---|---|---|
| OSC1/CLKIN | 16 | 16 | I | ST/CMOS(1) | Oscillator crystal input/external clock source input. |
| OSC2/CLKOUT | 15 | 15 | O | — | Oscillator crystal output. Connects to crystal or resonator in crystal oscillator mode. In RC mode, the pin outputs CLKOUT which has 1/4 the frequency of OSC1, and denotes the instruction cycle rate. |
| $\overline{MCLR}$/VPP | 4 | 4 | I/P | ST | Master clear reset input or programming voltage input. This pin is an active low reset to the device. |
| | | | | | PORTA is a bi-directional I/O port. |
| RA0 | 17 | 17 | I/O | TTL | |
| RA1 | 18 | 18 | I/O | TTL | |
| RA2 | 1 | 1 | I/O | TTL | |
| RA3 | 2 | 2 | I/O | TTL | |
| RA4/T0CKI | 3 | 3 | I/O | ST | RA4 can also be the clock input to the Timer0 timer/counter. Output is open drain type. |
| | | | | | PORTB is a bi-directional I/O port. PORTB can be software programmed for internal weak pull-up on all inputs. |
| RB0/INT | 6 | 6 | I/O | TTL/ST(2) | RB0 can also be the external interrupt pin. |
| RB1 | 7 | 7 | I/O | TTL | |
| RB2 | 8 | 8 | I/O | TTL | |
| RB3 | 9 | 9 | I/O | TTL | |
| RB4 | 10 | 10 | I/O | TTL | Interrupt on change pin. |
| RB5 | 11 | 11 | I/O | TTL | Interrupt on change pin. |
| RB6 | 12 | 12 | I/O | TTL/ST(3) | Interrupt on change pin. Serial programming clock. |
| RB7 | 13 | 13 | I/O | TTL/ST(3) | Interrupt on change pin. Serial programming data. |
| VSS | 5 | 5 | P | — | Ground reference for logic and I/O pins. |
| VDD | 14 | 14 | P | — | Positive supply for logic and I/O pins. |

Legend: I = input O = output I/O = input/output P = power
— = Not used TTL = TTL input ST = Schmitt Trigger input

Note 1: This buffer is a Schmitt Trigger input when configured in RC oscillator mode and a CMOS input otherwise.
2: This buffer is a Schmitt Trigger input when configured as the external interrupt.
3: This buffer is a Schmitt Trigger input when used in serial programming mode.

4.2.2 SPECIAL FUNCTION REGISTERS:

The Special Function Registers are registers used by the CPU and peripheral modules for controlling the desired operation of the device. These registers are implemented as static RAM.

The special function registers can be classified into two sets (core and peripheral). The registers associated with the “core” functions are described in this section and those related to the operation of the peripheral features are described in the section of that peripheral feature.

**TABLE 4-1: SPECIAL FUNCTION REGISTERS FOR THE PIC16C61**

| Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Value on: POR | Value on all other resets(3) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Bank 0** | | | | | | | | | | | |
| 00h(1) | INDF | Addressing this location uses contents of FSR to address data memory (not a physical register) | | | | | | | | 0000 0000 | 0000 0000 |
| 01h | TMR0 | Timer0 module’s register | | | | | | | | xxxx xxxx | uuuu uuuu |
| 02h(1) | PCL | Program Counter's (PC) Least Significant Byte | | | | | | | | 0000 0000 | 0000 0000 |
| 03h(1) | STATUS | IRP(4) | RP1(4) | RP0 | $\overline{TO}$ | $\overline{PD}$ | Z | DC | C | 0001 1xxx | 000q quuu |
| 04h(1) | FSR | Indirect data memory address pointer | | | | | | | | xxxx xxxx | uuuu uuuu |
| 05h | PORTA | — | — | — | PORTA Data Latch when written: PORTA pins when read | | | | | ---x xxxx | ---u uuuu |
| 06h | PORTB | PORTB Data Latch when written: PORTB pins when read | | | | | | | | xxxx xxxx | uuuu uuuu |
| 07h | — | Unimplemented | | | | | | | | — | — |
| 08h | — | Unimplemented | | | | | | | | — | — |
| 09h | — | Unimplemented | | | | | | | | — | — |
| 0Ah(1,2) | PCLATH | — | — | — | Write Buffer for the upper 5 bits of the Program Counter | | | | | ---0 0000 | ---0 0000 |
| 0Bh(1) | INTCON | GIE | — | T0IE | INTE | RBIE | T0IF | INTF | RBIF | 0-00 000x | 0-00 000u |
| **Bank 1** | | | | | | | | | | | |
| 80h(1) | INDF | Addressing this location uses contents of FSR to address data memory (not a physical register) | | | | | | | | 0000 0000 | 0000 0000 |
| 81h | OPTION | $\overline{RBPU}$ | INTEDG | T0CS | T0SE | PSA | PS2 | PS1 | PS0 | 1111 1111 | 1111 1111 |
| 82h(1) | PCL | Program Counter's (PC) Least Significant Byte | | | | | | | | 0000 0000 | 0000 0000 |
| 83h(1) | STATUS | IRP(4) | RP1(4) | RP0 | $\overline{TO}$ | $\overline{PD}$ | Z | DC | C | 0001 1xxx | 000q quuu |
| 84h(1) | FSR | Indirect data memory address pointer | | | | | | | | xxxx xxxx | uuuu uuuu |
| 85h | TRISA | — | — | — | PORTA Data Direction Register | | | | | ---1 1111 | ---1 1111 |
| 86h | TRISB | PORTB Data Direction Control Register | | | | | | | | 1111 1111 | 1111 1111 |
| 87h | – | Unimplemented | | | | | | | | — | — |
| 88h | – | Unimplemented | | | | | | | | — | — |
| 89h | — | Unimplemented | | | | | | | | — | — |
| 8Ah(1,2) | PCLATH | — | — | — | Write Buffer for the upper 5 bits of the Program Counter | | | | | ---0 0000 | ---0 0000 |
| 8Bh(1) | INTCON | GIE | — | T0IE | INTE | RBIE | T0IF | INTF | RBIF | 0-00 000x | 0-00 000u |

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented locations read as '0'. Shaded locations are unimplemented and read as ‘0’

Note 1: These registers can be addressed from either bank.

2: The upper byte of the Program Counter (PC) is not directly accessible. PCLATH is a holding register for the PC whose contents are transferred to the upper byte of the program counter. (PC<12:8>)

3: Other (non power-up) resets include external reset through $\overline{MCLR}$ and the Watchdog Timer Reset.

4: The IRP and RP1 bits are reserved on the PIC16C61, always maintain these bits clear.

### 5.3 PORTC and TRISC Register

| Applicable Devices | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 61 | 62 | 62A | R62 | 63 | R63 | 64 | 64A | R64 | 65 | 65A | R65 | 66 | 67 |

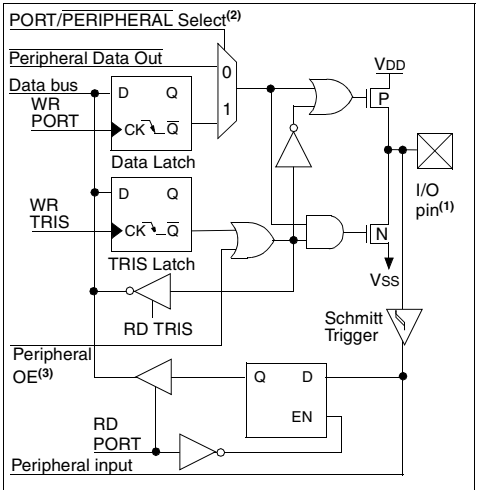
PORTC is an 8-bit wide bi-directional port. Each pin is individually configurable as an input or output through the TRISC register. PORTC is multiplexed with several peripheral functions (Table 5-5). PORTC pins have Schmitt Trigger input buffers.

When enabling peripheral functions, care should be taken in defining TRIS bits for each PORTC pin. Some peripherals override the TRIS bit to make a pin an output, while other peripherals override the TRIS bit to make a pin an input. Since the TRIS bit override is in effect while the peripheral is enabled, read-modify-write instructions (`BSF, BCF, XORWF`) with TRISC as destination should be avoided. The user should refer to the corresponding peripheral section for the correct TRIS bit settings.

**EXAMPLE 5-3: INITIALIZING PORTC**

```
BCF     STATUS, RP0   ;
BCF     STATUS, RP1   ; PIC16C66/67 only
CLRF    PORTC         ; Initialize PORTC by
                      ; clearing output
                      ; data latches
BSF     STATUS, RP0   ; Select Bank 1
MOVLW   0xCF          ; Value used to
                      ; initialize data
                      ; direction
MOVWF   TRISC         ; Set RC<3:0> as inputs
                      ; RC<5:4> as outputs
                      ; RC<7:6> as inputs
```

**FIGURE 5-6: PORTC BLOCK DIAGRAM**




Note 1: I/O pins have diode protection to VDD and VSS.
2: Port/Peripheral select signal selects between port data and peripheral output.
3: Peripheral OE (output enable) is only activated if peripheral select is active.

**TABLE 5-5: PORTC FUNCTIONS FOR PIC16C62/64**

| Name | Bit# | Buffer Type | Function |
|---|---|---|---|
| RC0/T1OSI/T1CKI | bit0 | ST | Input/output port pin or Timer1 oscillator input or Timer1 clock input |
| RC1/T1OSO | bit1 | ST | Input/output port pin or Timer1 oscillator output |
| RC2/CCP1 | bit2 | ST | Input/output port pin or Capture1 input/Compare1 output/PWM1 output |
| RC3/SCK/SCL | bit3 | ST | RC3 can also be the synchronous serial clock for both SPI and $I^2C$ modes. |
| RC4/SDI/SDA | bit4 | ST | RC4 can also be the SPI Data In (SPI mode) or data I/O ($I^2C$ mode). |
| RC5/SDO | bit5 | ST | Input/output port pin or synchronous serial port data output |
| RC6 | bit6 | ST | Input/output port pin |
| RC7 | bit7 | ST | Input/output port pin |

Legend: ST = Schmitt Trigger input

**FIGURE 5-12: PARALLEL SLAVE PORT WRITE WAVEFORMS**

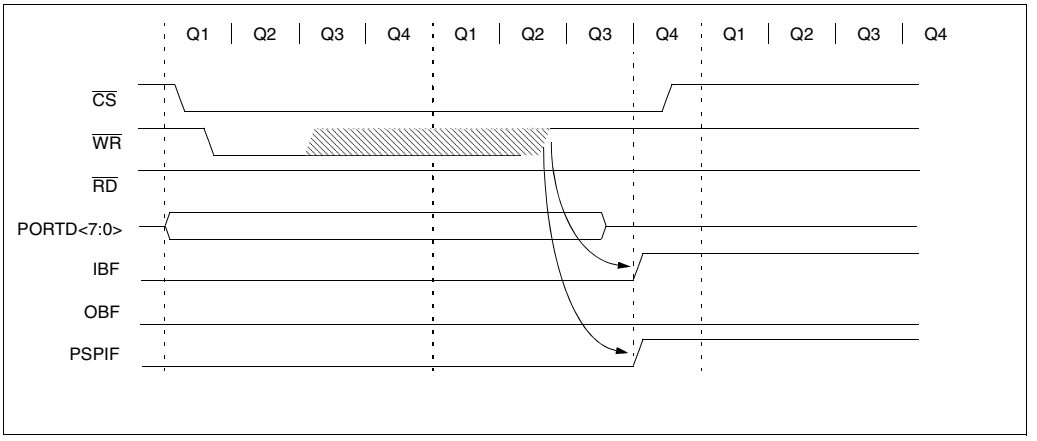



**FIGURE 5-13: PARALLEL SLAVE PORT READ WAVEFORMS**

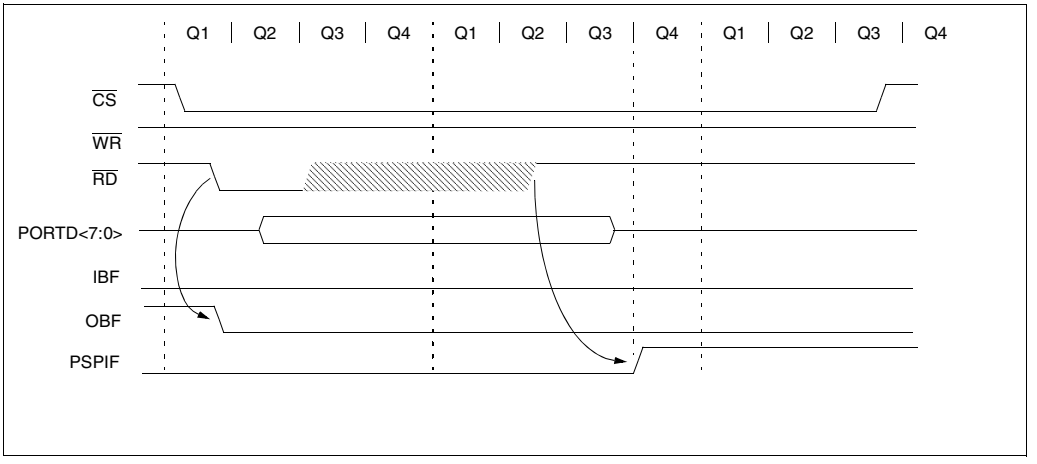



**TABLE 5-13: REGISTERS ASSOCIATED WITH PARALLEL SLAVE PORT**

| Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Value on: POR, BOR | Value on all other resets |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 08h | PORTD | PSP7 | PSP6 | PSP5 | PSP4 | PSP3 | PSP2 | PSP1 | PSP0 | xxxx xxxx | uuuu uuuu |
| 09h | PORTE | — | — | — | — | — | RE2 | RE1 | RE0 | ---- -xxx | ---- -uuu |
| 89h | TRISE | IBF | OBF | IBOV | PSPMODE | — | PORTE Data Direction Bits | | | 0000 -111 | 0000 -111 |
| 0Ch | PIR1 | PSPIF | (1) | RCIF(2) | TXIF(2) | SSPIF | CCP1IF | TMR2IF | TRM1IF | 0000 0000 | 0000 0000 |
| 8Ch | PIE1 | PSPIE | (1) | RCIE(2) | TXIE(2) | SSPIE | CCP1IE | TMR2IE | TMR1IE | 0000 0000 | 0000 0000 |

Legend: x = unknown, u = unchanged, - = unimplemented locations read as '0'. Shaded cells are not used by the PSP.
Note 1: These bits are reserved, always maintain these bits clear.
2: These bits are implemented on the PIC16C65/65A/R65/67 only.

## 6.0 OVERVIEW OF TIMER MODULES

| Applicable Devices | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 61 | 62 | 62A | R62 | 63 | R63 | 64 | 64A | R64 | 65 | 65A | R65 | 66 | 67 |

All PIC16C6X devices have three timer modules except for the PIC16C61, which has one timer module. Each module can generate an interrupt to indicate that an event has occurred (i.e., timer overflow). Each of these modules are detailed in the following sections. The timer modules are:

- Timer0 module (Section 7.0)
- Timer1 module (Section 8.0)
- Timer2 module (Section 9.0)

### 6.1 Timer0 Overview

| Applicable Devices | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 61 | 62 | 62A | R62 | 63 | R63 | 64 | 64A | R64 | 65 | 65A | R65 | 66 | 67 |

The Timer0 module is a simple 8-bit overflow counter. The clock source can be either the internal system clock (Fosc/4) or an external clock. When the clock source is an external clock, the Timer0 module can be selected to increment on either the rising or falling edge.

The Timer0 module also has a programmable prescaler option. This prescaler can be assigned to either the Timer0 module or the Watchdog Timer. Bit PSA (OPTION<3>) assigns the prescaler, and bits PS2:PS0 (OPTION<2:0>) determine the prescaler value. TMR0 can increment at the following rates: 1:1 when the prescaler is assigned to Watchdog Timer, 1:2, 1:4, 1:8, 1:16, 1:32, 1:64, 1:128, and 1:256.

Synchronization of the external clock occurs after the prescaler. When the prescaler is used, the external clock frequency may be higher then the device's frequency. The maximum frequency is 50 MHz, given the high and low time requirements of the clock.

### 6.2 Timer1 Overview

| Applicable Devices | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 61 | 62 | 62A | R62 | 63 | R63 | 64 | 64A | R64 | 65 | 65A | R65 | 66 | 67 |

Timer1 is a 16-bit timer/counter. The clock source can be either the internal system clock (Fosc/4), an external clock, or an external crystal. Timer1 can operate as either a timer or a counter. When operating as a counter (external clock source), the counter can either operate synchronized to the device or asynchronously to the device. Asynchronous operation allows Timer1 to operate during sleep, which is useful for applications that require a real-time clock as well as the power savings of SLEEP mode.

TImer1 also has a prescaler option which allows TMR1 to increment at the following rates: 1:1, 1:2, 1:4, and 1:8. TMR1 can be used in conjunction with the Capture/Compare/PWM module. When used with a CCP module, Timer1 is the time-base for 16-bit capture or 16-bit compare and must be synchronized to the device.

### 6.3 Timer2 Overview

| Applicable Devices | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 61 | 62 | 62A | R62 | 63 | R63 | 64 | 64A | R64 | 65 | 65A | R65 | 66 | 67 |

Timer2 is an 8-bit timer with a programmable prescaler and a programmable postscaler, as well as an 8-bit Period Register (PR2). Timer2 can be used with the CCP module (in PWM mode) as well as the Baud Rate Generator for the Synchronous Serial Port (SSP). The prescaler option allows Timer2 to increment at the following rates: 1:1, 1:4, and 1:16.

The postscaler allows TMR2 register to match the period register (PR2) a programmable number of times before generating an interrupt. The postscaler can be programmed from 1:1 to 1:16 (inclusive).

### 6.4 CCP Overview

| Applicable Devices | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 61 | 62 | 62A | R62 | 63 | R63 | 64 | 64A | R64 | 65 | 65A | R65 | 66 | 67 |

The CCP module(s) can operate in one of three modes: 16-bit capture, 16-bit compare, or up to 10-bit Pulse Width Modulation (PWM).

Capture mode captures the 16-bit value of TMR1 into the CCPRxH:CCPRxL register pair. The capture event can be programmed for either the falling edge, rising edge, fourth rising edge, or sixteenth rising edge of the CCPx pin.

Compare mode compares the TMR1H:TMR1L register pair to the CCPRxH:CCPRxL register pair. When a match occurs, an interrupt can be generated and the output pin CCPx can be forced to a given state (High or Low) and Timer1 can be reset. This depends on control bits CCPxM3:CCPxM0.

PWM mode compares the TMR2 register to a 10-bit duty cycle register (CCPRxH:CCPRxL<5:4>) as well as to an 8-bit period register (PR2). When the TMR2 register = Duty Cycle register, the CCPx pin will be forced low. When TMR2 = PR2, TMR2 is cleared to 00h, an interrupt can be generated, and the CCPx pin (if an output) will be forced high.

**TABLE 10-5: REGISTERS ASSOCIATED WITH PWM AND TIMER2**

| Addr | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Value on: POR, BOR | Value on all other Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0Bh,8Bh 10Bh,18Bh | INTCON | GIE | PEIE | T0IE | INTE | RBIE | T0IF | INTF | RBIF | 0000 000x | 0000 000u |
| 0Ch | PIR1 | PSPIF(2) | (3) | RCIF(1) | TXIF(1) | SSPIF | CCP1IF | TMR2IF | TMR1IF | 0000 0000 | 0000 0000 |
| 0Dh(4) | PIR2 | — | — | — | — | — | — | — | CCP2IF | ---- --- 0 | ---- --- 0 |
| 8Ch | PIE1 | PSPIE(2) | (3) | RCIE(1) | TXIE(1) | SSPIE | CCP1IE | TMR2IE | TMR1IE | 0000 0000 | 0000 0000 |
| 8Dh(4) | PIE2 | — | — | — | — | — | — | — | CCP2IE | ---- --- 0 | ---- --- 0 |
| 87h | TRISC | PORTC Data Direction register | | | | | | | | 1111 1111 | 1111 1111 |
| 11h | TMR2 | Timer2 module's register | | | | | | | | 0000 0000 | 0000 0000 |
| 92h | PR2 | Timer2 module's Period register | | | | | | | | 1111 1111 | 1111 1111 |
| 12h | T2CON | — | TOUTPS3 | TOUTPS2 | TOUTPS1 | TOUTPS0 | TMR2ON | T2CKPS1 | T2CKPS0 | -000 0000 | -000 0000 |
| 15h | CCPR1L | Capture/Compare/PWM1 (LSB) | | | | | | | | xxxx xxxx | uuuu uuuu |
| 16h | CCPR1H | Capture/Compare/PWM1 (MSB) | | | | | | | | xxxx xxxx | uuuu uuuu |
| 17h | CCP1CON | — | — | CCP1X | CCP1Y | CCP1M3 | CCP1M2 | CCP1M1 | CCP1M0 | --00 0000 | --00 0000 |
| 1Bh(4) | CCPR2L | Capture/Compare/PWM2 (LSB) | | | | | | | | xxxx xxxx | uuuu uuuu |
| 1Ch(4) | CCPR2H | Capture/Compare/PWM2 (MSB) | | | | | | | | xxxx xxxx | uuuu uuuu |
| 1Dh(4) | CCP2CON | — | — | CCP2X | CCP2Y | CCP2M3 | CCP2M2 | CCP2M1 | CCP2M0 | --00 0000 | --00 0000 |

Legend: x = unknown, u = unchanged, - = unimplemented locations read as '0'. Shaded cells are not used in this mode.

Note 1: These bits are associated with the USART module, which is implemented on the PIC16C63/R63/65/65A/R65/66/67 only.

2: Bits PSPIE and PSPIF are reserved on the PIC16C62/62A/R62/63/R63/66, always maintain these bits clear.

3: The PIR1<6> and PIE1<6> bits are reserved, always maintain these bits clear.

4: These registers are associated with the CCP2 module, which is only implemented on the PIC16C63/R63/65/65A/R65/66/67.

**TABLE 12-3: BAUD RATES FOR SYNCHRONOUS MODE**

| BAUD RATE (K) | FOSC = 20 MHz KBAUD | % ERROR | SPBRG value (decimal) | 16 MHz KBAUD | % ERROR | SPBRG value (decimal) | 10 MHz KBAUD | % ERROR | SPBRG value (decimal) | 7.15909 MHz KBAUD | % ERROR | SPBRG value (decimal) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0.3 | NA | - | - | NA | - | - | NA | - | - | NA | - | - |
| 1.2 | NA | - | - | NA | - | - | NA | - | - | NA | - | - |
| 2.4 | NA | - | - | NA | - | - | NA | - | - | NA | - | - |
| 9.6 | NA | - | - | NA | - | - | 9.766 | +1.73 | 255 | 9.622 | +0.23 | 185 |
| 19.2 | 19.53 | +1.73 | 255 | 19.23 | +0.16 | 207 | 19.23 | +0.16 | 129 | 19.24 | +0.23 | 92 |
| 76.8 | 76.92 | +0.16 | 64 | 76.92 | +0.16 | 51 | 75.76 | -1.36 | 32 | 77.82 | +1.32 | 22 |
| 96 | 96.15 | +0.16 | 51 | 95.24 | -0.79 | 41 | 96.15 | +0.16 | 25 | 94.20 | -1.88 | 18 |
| 300 | 294.1 | -1.96 | 16 | 307.69 | +2.56 | 12 | 312.5 | +4.17 | 7 | 298.3 | -0.57 | 5 |
| 500 | 500 | 0 | 9 | 500 | 0 | 7 | 500 | 0 | 4 | NA | - | - |
| HIGH | 5000 | - | 0 | 4000 | - | 0 | 2500 | - | 0 | 1789.8 | - | 0 |
| LOW | 19.53 | - | 255 | 15.625 | - | 255 | 9.766 | - | 255 | 6.991 | - | 255 |

| BAUD RATE (K) | FOSC = 5.0688 MHz KBAUD | % ERROR | SPBRG value (decimal) | 4 MHz KBAUD | % ERROR | SPBRG value (decimal) | 3.579545 MHz KBAUD | % ERROR | SPBRG value (decimal) | 1 MHz KBAUD | % ERROR | SPBRG value (decimal) | 32.768 kHz KBAUD | % ERROR | SPBRG value (decimal) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0.3 | NA | - | - | NA | - | - | NA | - | - | NA | - | - | 0.303 | +1.14 | 26 |
| 1.2 | NA | - | - | NA | - | - | NA | - | - | 1.202 | +0.16 | 207 | 1.170 | -2.48 | 6 |
| 2.4 | NA | - | - | NA | - | - | NA | - | - | 2.404 | +0.16 | 103 | NA | - | - |
| 9.6 | 9.6 | 0 | 131 | 9.615 | +0.16 | 103 | 9.622 | +0.23 | 92 | 9.615 | +0.16 | 25 | NA | - | - |
| 19.2 | 19.2 | 0 | 65 | 19.231 | +0.16 | 51 | 19.04 | -0.83 | 46 | 19.24 | +0.16 | 12 | NA | - | - |
| 76.8 | 79.2 | +3.13 | 15 | 76.923 | +0.16 | 12 | 74.57 | -2.90 | 11 | 83.34 | +8.51 | 2 | NA | - | - |
| 96 | 97.48 | +1.54 | 12 | 1000 | +4.17 | 9 | 99.43 | +3.57 | 8 | NA | - | - | NA | - | - |
| 300 | 316.8 | +5.60 | 3 | NA | - | - | 298.3 | -0.57 | 2 | NA | - | - | NA | - | - |
| 500 | NA | - | - | NA | - | - | NA | - | - | NA | - | - | NA | - | - |
| HIGH | 1267 | - | 0 | 100 | - | 0 | 894.9 | - | 0 | 250 | - | 0 | 8.192 | - | 0 |
| LOW | 4.950 | - | 255 | 3.906 | - | 255 | 3.496 | - | 255 | 0.9766 | - | 255 | 0.032 | - | 255 |

**TABLE 12-4: BAUD RATES FOR ASYNCHRONOUS MODE (BRGH = 0)**

| BAUD RATE (K) | FOSC = 20 MHz KBAUD | % ERROR | SPBRG value (decimal) | 16 MHz KBAUD | % ERROR | SPBRG value (decimal) | 10 MHz KBAUD | % ERROR | SPBRG value (decimal) | 7.15909 MHz KBAUD | % ERROR | SPBRG value (decimal) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0.3 | NA | - | - | NA | - | - | NA | - | - | NA | - | - |
| 1.2 | 1.221 | +1.73 | 255 | 1.202 | +0.16 | 207 | 1.202 | +0.16 | 129 | 1.203 | +0.23 | 92 |
| 2.4 | 2.404 | +0.16 | 129 | 2.404 | +0.16 | 103 | 2.404 | +0.16 | 64 | 2.380 | -0.83 | 46 |
| 9.6 | 9.469 | -1.36 | 32 | 9.615 | +0.16 | 25 | 9.766 | +1.73 | 15 | 9.322 | -2.90 | 11 |
| 19.2 | 19.53 | +1.73 | 15 | 19.23 | +0.16 | 12 | 19.53 | +1.73 | 7 | 18.64 | -2.90 | 5 |
| 76.8 | 78.13 | +1.73 | 3 | 83.33 | +8.51 | 2 | 78.13 | +1.73 | 1 | NA | - | - |
| 96 | 104.2 | +8.51 | 2 | NA | - | - | NA | - | - | NA | - | - |
| 300 | 312.5 | +4.17 | 0 | NA | - | - | NA | - | - | NA | - | - |
| 500 | NA | - | - | NA | - | - | NA | - | - | NA | - | - |
| HIGH | 312.5 | - | 0 | 250 | - | 0 | 156.3 | - | 0 | 111.9 | - | 0 |
| LOW | 1.221 | - | 255 | 0.977 | - | 255 | 0.6104 | - | 255 | 0.437 | - | 255 |

| BAUD RATE (K) | FOSC = 5.0688 MHz KBAUD | % ERROR | SPBRG value (decimal) | 4 MHz KBAUD | % ERROR | SPBRG value (decimal) | 3.579545 MHz KBAUD | % ERROR | SPBRG value (decimal) | 1 MHz KBAUD | % ERROR | SPBRG value (decimal) | 32.768 kHz KBAUD | % ERROR | SPBRG value (decimal) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0.3 | 0.31 | +3.13 | 255 | 0.3005 | -0.17 | 207 | 0.301 | +0.23 | 185 | 0.300 | +0.16 | 51 | 0.256 | -14.67 | 1 |
| 1.2 | 1.2 | 0 | 65 | 1.202 | +1.67 | 51 | 1.190 | -0.83 | 46 | 1.202 | +0.16 | 12 | NA | - | - |
| 2.4 | 2.4 | 0 | 32 | 2.404 | +1.67 | 25 | 2.432 | +1.32 | 22 | 2.232 | -6.99 | 6 | NA | - | - |
| 9.6 | 9.9 | +3.13 | 7 | NA | - | - | 9.322 | -2.90 | 5 | NA | - | - | NA | - | - |
| 19.2 | 19.8 | +3.13 | 3 | NA | - | - | 18.64 | -2.90 | 2 | NA | - | - | NA | - | - |
| 76.8 | 79.2 | +3.13 | 0 | NA | - | - | NA | - | - | NA | - | - | NA | - | - |
| 96 | NA | - | - | NA | - | - | NA | - | - | NA | - | - | NA | - | - |
| 300 | NA | - | - | NA | - | - | NA | - | - | NA | - | - | NA | - | - |
| 500 | NA | - | - | NA | - | - | NA | - | - | NA | - | - | NA | - | - |
| HIGH | 79.2 | - | 0 | 62.500 | - | 0 | 55.93 | - | 0 | 15.63 | - | 0 | 0.512 | - | 0 |
| LOW | 0.3094 | - | 255 | 3.906 | - | 255 | 0.2185 | - | 255 | 0.0610 | - | 255 | 0.0020 | - | 255 |

## 13.8 Power-down Mode (SLEEP)

| Applicable Devices | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 61 | 62 | 62A | R62 | 63 | R63 | 64 | 64A | R64 | 65 | 65A | R65 | 66 | 67 |

Power-down mode is entered by executing a SLEEP instruction.

If enabled, the Watchdog Timer will be cleared but keeps running, status bit $\overline{PD}$ (STATUS<3>) is cleared, status bit $\overline{TO}$ (STATUS<4>) is set, and the oscillator driver is turned off. The I/O ports maintain the status they had before the SLEEP instruction was executed (driving high, low, or hi-impedance).

For lowest current consumption in this mode, place all I/O pins at either VDD, or VSS, ensure no external circuitry is drawing current from the I/O pin, and disable external clocks. Pull all I/O pins, that are hi-impedance inputs, high or low externally to avoid switching currents caused by floating inputs. The T0CKI input should also be at VDD or VSS for lowest current consumption. The contribution from on-chip pull-ups on PORTB should be considered.

The $\overline{MCLR}$/VPP pin must be at a logic high level (VIHMC).

### 13.8.1 WAKE-UP FROM SLEEP

The device can wake from SLEEP through one of the following events:

1. External reset input on $\overline{MCLR}$/VPP pin.
2. Watchdog Timer Wake-up (if WDT was enabled).
3. Interrupt from RB0/INT pin, RB port change, or some peripheral interrupts.

External $\overline{MCLR}$ Reset will cause a device reset. All other events are considered a continuation of program execution and cause a “wake-up”. The $\overline{TO}$ and $\overline{PD}$ bits in the STATUS register can be used to determine the cause of device reset. The $\overline{PD}$ bit, which is set on power-up is cleared when SLEEP is invoked. The $\overline{TO}$ bit is cleared if WDT time-out occurred (and caused wake-up).

The following peripheral interrupts can wake the device from SLEEP:

1. TMR1 interrupt. Timer1 must be operating as an asynchronous counter.
2. SSP (Start/Stop) bit detect interrupt.
3. SSP transmit or receive in slave mode (SPI/$I^2C$).
4. CCP capture mode interrupt.
5. Parallel Slave Port read or write.
6. USART TX or RX (synchronous slave mode).

Other peripherals can not generate interrupts since during SLEEP, no on-chip Q clocks are present.

When the SLEEP instruction is being executed, the next instruction (PC + 1) is pre-fetched. For the device to wake-up through an interrupt event, the corresponding interrupt enable bit must be set (enabled). Wake-up is regardless of the state of the GIE bit. If the GIE bit is clear (disabled), the device continues execution at the instruction after the SLEEP instruction. If the GIE bit is set (enabled), the device executes the instruction after the SLEEP instruction and then branches to the interrupt address (0004h). In cases where the execution of the instruction following SLEEP is not desirable, the user should have a NOP after the SLEEP instruction.

### 13.8.2 WAKE-UP USING INTERRUPTS

When global interrupts are disabled (GIE cleared) and any interrupt source has both its interrupt enable bit and interrupt flag bit set, one of the following will occur:

- If the interrupt occurs **before** the execution of a SLEEP instruction, the SLEEP instruction will complete as a NOP. Therefore, the WDT and WDT postscaler will not be cleared, the $\overline{TO}$ bit will not be set and $\overline{PD}$ bits will not be cleared.
- If the interrupt occurs **during or after** the execution of a SLEEP instruction, the device will immediately wake up from sleep. The SLEEP instruction will be completely executed before the wake-up. Therefore, the WDT and WDT postscaler will be cleared, the $\overline{TO}$ bit will be set and the $\overline{PD}$ bit will be cleared.

Even if the flag bits were checked before executing a SLEEP instruction, it may be possible for flag bits to become set before the SLEEP instruction completes. To determine whether a SLEEP instruction executed, test the $\overline{PD}$ bit. If the $\overline{PD}$ bit is set, the SLEEP instruction was executed as a NOP.

To ensure that the WDT is cleared, a CLRWDT instruction should be executed before a SLEEP instruction.

| Applicable Devices | 61 | 62 | 62A | R62 | 63 | R63 | 64 | 64A | R64 | 65 | 65A | R65 | 66 | 67 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|

## 15.0 ELECTRICAL CHARACTERISTICS FOR PIC16C61

**Absolute Maximum Ratings †**

Ambient temperature under bias ..... -55°C to +125°C

Storage temperature ..... -65°C to +150°C

Voltage on any pin with respect to VSS (except VDD, $\overline{MCLR}$, and RA4) ..... -0.3V to (VDD + 0.3V)

Voltage on VDD with respect to VSS ..... -0.3V to +7.5V

Voltage on $\overline{MCLR}$ with respect to VSS (Note 2) ..... 0V to +14V

Voltage on RA4 pin with respect to Vss ..... 0V to +14V

Total power dissipation (Note 1) ..... 800 mW

Maximum current out of VSS pin ..... 150 mA

Maximum current into VDD pin ..... 100 mA

Input clamp current, IIK (VI < 0 or VI > VDD) ..... ± 20 mA

Output clamp current, IOK (VO < 0 or VO > VDD) ..... ± 20 mA

Maximum output current sunk by any I/O pin ..... 25 mA

Maximum output current sourced by any I/O pin ..... 20 mA

Maximum current sunk by PORTA ..... 80 mA

Maximum current sourced by PORTA ..... 50 mA

Maximum current sunk by PORTB ..... 150 mA

Maximum current sourced by PORTB ..... 100 mA

**Note 1:** Power dissipation is calculated as follows: Pdis = VDD x {IDD - ∑ IOH} + ∑ {(VDD-VOH) x IOH} + ∑(VOl x IOL)

**Note 2:** Voltage spikes below VSS at the $\overline{MCLR}$ pin, inducing currents greater than 80 mA, may cause latch-up. Thus, a series resistor of 50-100Ω should be used when applying a "low" level to the $\overline{MCLR}$ pin rather than pulling this pin directly to VSS.

† NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

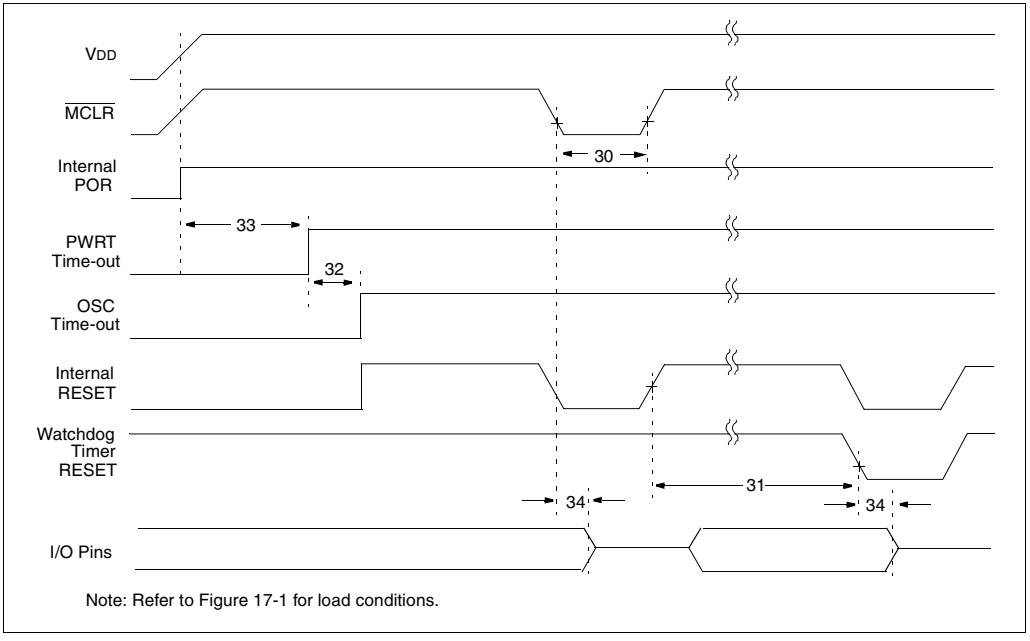
**TABLE 15-1: CROSS REFERENCE OF DEVICE SPECS FOR OSCILLATOR CONFIGURATIONS AND FREQUENCIES OF OPERATION (COMMERCIAL DEVICES)**

| OSC | PIC16C61-04 | PIC16C61-20 | PIC16LC61-04 | JW Devices |
|---|---|---|---|---|
| RC | VDD: 4.0V to 6.0V<br>IDD: 3.3 mA max. at 5.5V<br>IPD: 14 μA max. at 4V<br>Freq: 4 MHz max. | VDD: 4.5V to 5.5V<br>IDD: 1.8 mA typ. at 5.5V<br>IPD: 1.0 μA typ. at 4V<br>Freq: 4 MHz max. | VDD: 3.0V to 6.0V<br>IDD: 1.4 mA typ. at 3.0V<br>IPD: 0.6 μA typ. at 3V<br>Freq: 4 MHz max. | VDD: 4.0V to 6.0V<br>IDD: 3.3 mA max. at 5.5V<br>IPD: 14 μA max. at 4V<br>Freq: 4 MHz max. |
| XT | VDD: 4.0V to 6.0V<br>IDD: 3.3 mA max. at 5.5V<br>IPD: 14 μA max. at 4V<br>Freq: 4 MHz max. | VDD: 4.5V to 5.5V<br>IDD: 1.8 mA typ. at 5.5V<br>IPD: 1.0 μA typ. at 4V<br>Freq: 4 MHz max. | VDD: 3.0V to 6.0V<br>IDD: 1.4 mA typ. at 3.0V<br>IPD: 0.6 μA typ. at 3V<br>Freq: 4 MHz max. | VDD: 4.0V to 6.0V<br>IDD: 3.3 mA max. at 5.5V<br>IPD: 14 μA max. at 4V<br>Freq: 4 MHz max. |
| HS | VDD: 4.5V to 5.5V<br>IDD: 13.5 mA typ. at 5.5V<br>IPD: 1.0 μA typ. at 4.5V<br>Freq: 4 MHz max. | VDD: 4.5V to 5.5V<br>IDD: 30 mA max. at 5.5V<br>IPD: 1.0 μA typ. at 4.5V<br>Freq: 20 MHz max. | Not recommended for use in HS mode | VDD: 4.5V to 5.5V<br>IDD: 30 mA max. at 5.5V<br>IPD: 1.0 μA typ. at 4.5V<br>Freq: 20 MHz max. |
| LP | VDD: 4.0V to 6.0V<br>IDD: 15 μA typ. at 32 kHz, 4.0V<br>IPD: 0.6 μA typ. at 4.0V<br>Freq: 200 kHz max. | Not recommended for use in LP mode | VDD: 3.0V to 6.0V<br>IDD: 32 μA max. at 32 kHz, 3.0V<br>IPD: 9 μA max. at 3.0V<br>Freq: 200 kHz max. | VDD: 3.0V to 6.0V<br>IDD: 32 μA max. at 32 kHz, 3.0V<br>IPD: 9 μA max. at 3.0V<br>Freq: 200 kHz max. |

The shaded sections indicate oscillator selections which are tested for functionality, but not for MIN/MAX specifications. It is recommended that the user select the device type that ensures the specifications required.

| Applicable Devices | 61 | 62 | 62A | R62 | 63 | R63 | 64 | 64A | R64 | 65 | 65A | R65 | 66 | 67 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|

**FIGURE 17-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING**




Note: Refer to Figure 17-1 for load conditions.

**TABLE 17-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER REQUIREMENTS**

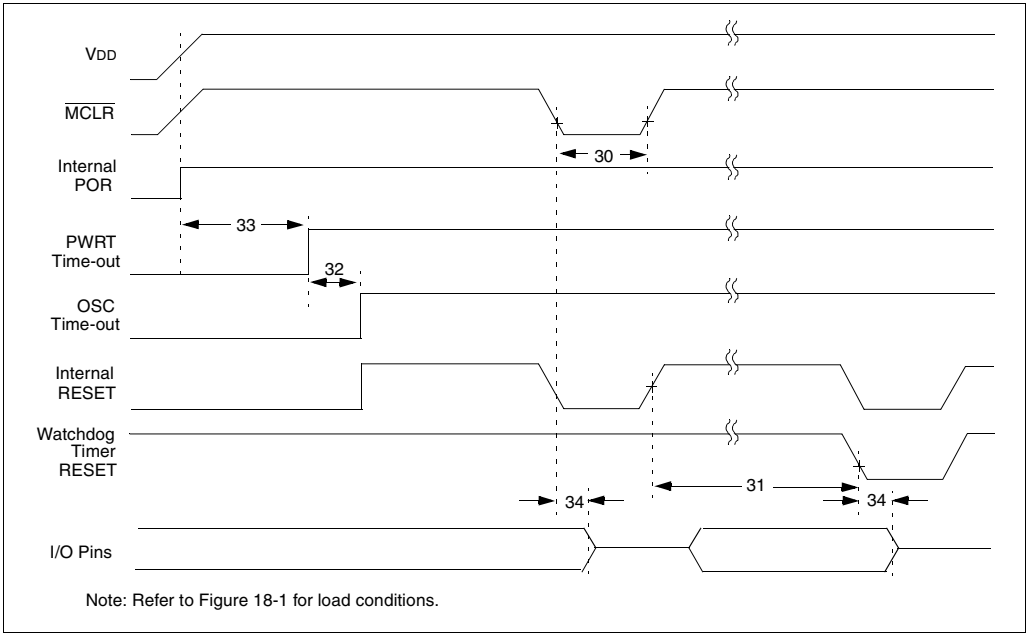
| Parameter No. | Sym | Characteristic | Min | Typ† | Max | Units | Conditions |
|---|---|---|---|---|---|---|---|
| 30* | TmcL | $\overline{MCLR}$ Pulse Width (low) | 100 | — | — | ns | VDD = 5V, -40°C to +85°C |
| 31* | Twdt | Watchdog Timer Time-out Period (No Prescaler) | 7 | 18 | 33 | ms | VDD = 5V, -40°C to +85°C |
| 32 | Tost | Oscillation Start-up Timer Period | — | 1024TOSC | — | — | TOSC = OSC1 period |
| 33* | Tpwrt | Power-up Timer Period | 28 | 72 | 132 | ms | VDD = 5V, -40°C to +85°C |
| 34* | TIOZ | I/O Hi-impedance from $\overline{MCLR}$ Low | — | — | 100 | ns | |

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

| Applicable Devices | 61 | 62 | 62A | R62 | 63 | R63 | 64 | 64A | R64 | 65 | 65A | R65 | 66 | 67 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|

**FIGURE 18-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING**




Note: Refer to Figure 18-1 for load conditions.

**FIGURE 18-5: BROWN-OUT RESET TIMING**

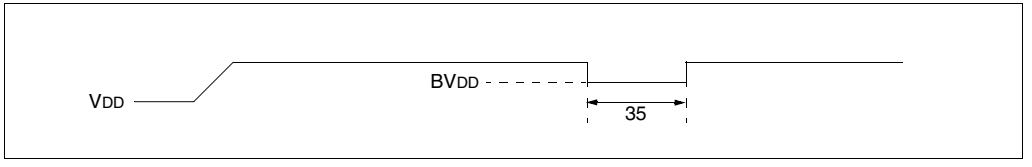



**TABLE 18-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, POWER-UP TIMER, AND BROWN-OUT RESET REQUIREMENTS**

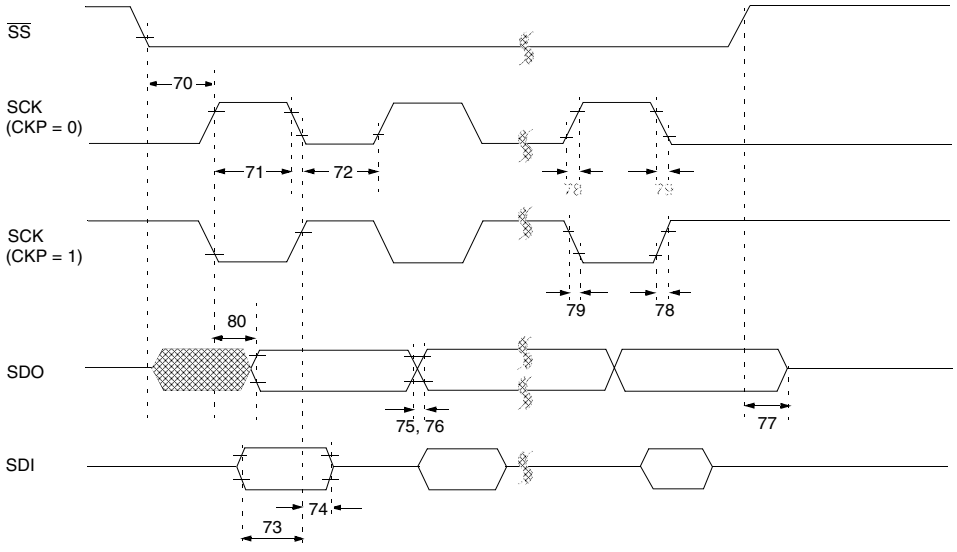
| Parameter No. | Sym | Characteristic | Min | Typ† | Max | Units | Conditions |
|---|---|---|---|---|---|---|---|
| 30 | TmcL | MCLR Pulse Width (low) | 2 | — | — | µs | VDD = 5V, -40°C to +125°C |
| 31* | Twdt | Watchdog Timer Time-out Period (No Prescaler) | 7 | 18 | 33 | ms | VDD = 5V, -40°C to +125°C |
| 32 | Tost | Oscillation Start-up Timer Period | — | 1024TOSC | — | — | TOSC = OSC1 period |
| 33* | Tpwrt | Power-up Timer Period | 28 | 72 | 132 | ms | VDD = 5V, -40°C to +125°C |
| 34 | TIOZ | I/O Hi-impedance from MCLR Low or WDT Reset | — | — | 2.1 | µs | |
| 35 | TBOR | Brown-out Reset Pulse Width | 100 | — | — | µs | VDD ≤ BVDD (param. D005) |

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

| Applicable Devices | 61 | 62 | 62A | R62 | 63 | R63 | 64 | 64A | R64 | 65 | 65A | R65 | 66 | 67 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|

**FIGURE 18-9: SPI MODE TIMING**




Note: Refer to Figure 18-1 for load conditions

**TABLE 18-8: SPI MODE REQUIREMENTS**

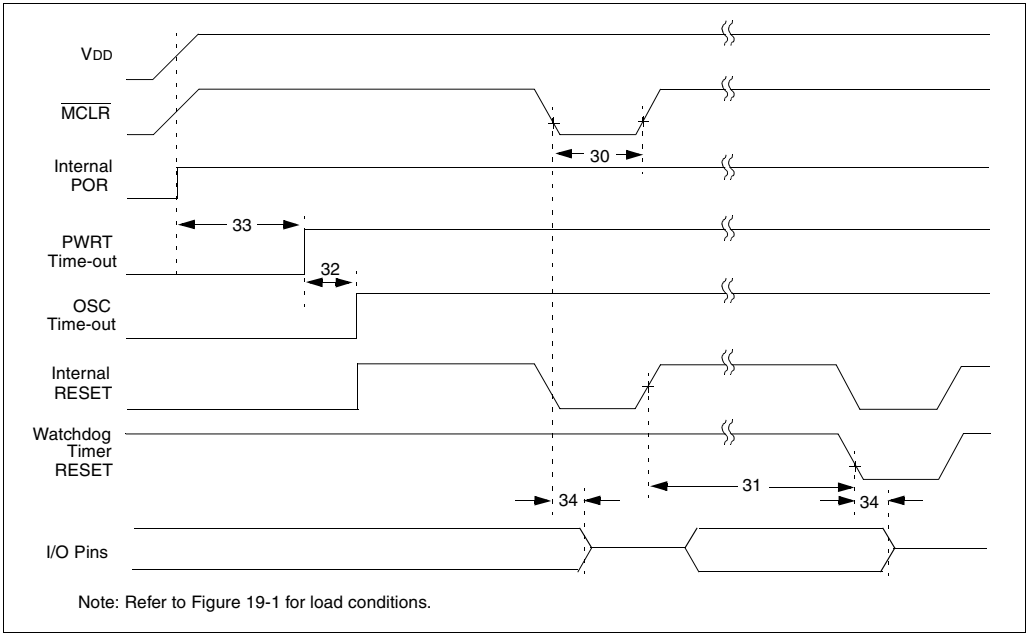
| Parameter No. | Sym | Characteristic | Min | Typ† | Max | Units | Conditions |
|---|---|---|---|---|---|---|---|
| 70* | TssL2scH, TssL2scL | $\overline{SS}\downarrow$ to SCK↓ or SCK↑ input | TCY | — | — | ns | |
| 71* | TscH | SCK input high time (slave mode) | TCY + 20 | — | — | ns | |
| 72* | TscL | SCK input low time (slave mode) | TCY + 20 | — | — | ns | |
| 73* | TdiV2scH, TdiV2scL | Setup time of SDI data input to SCK edge | 50 | — | — | ns | |
| 74* | TscH2diL, TscL2diL | Hold time of SDI data input to SCK edge | 50 | — | — | ns | |
| 75* | TdoR | SDO data output rise time | — | 10 | 25 | ns | |
| 76* | TdoF | SDO data output fall time | — | 10 | 25 | ns | |
| 77* | TssH2doZ | $\overline{SS}\uparrow$ to SDO output hi-impedance | 10 | — | 50 | ns | |
| 78* | TscR | SCK output rise time (master mode) | — | 10 | 25 | ns | |
| 79* | TscF | SCK output fall time (master mode) | — | 10 | 25 | ns | |
| 80* | TscH2doV, TscL2doV | SDO data output valid after SCK edge | — | — | 50 | ns | |

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

| Applicable Devices | 61 | 62 | 62A | R62 | 63 | R63 | 64 | 64A | R64 | 65 | 65A | R65 | 66 | 67 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|

**FIGURE 19-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING**




Note: Refer to Figure 19-1 for load conditions.

**TABLE 19-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER REQUIREMENTS**

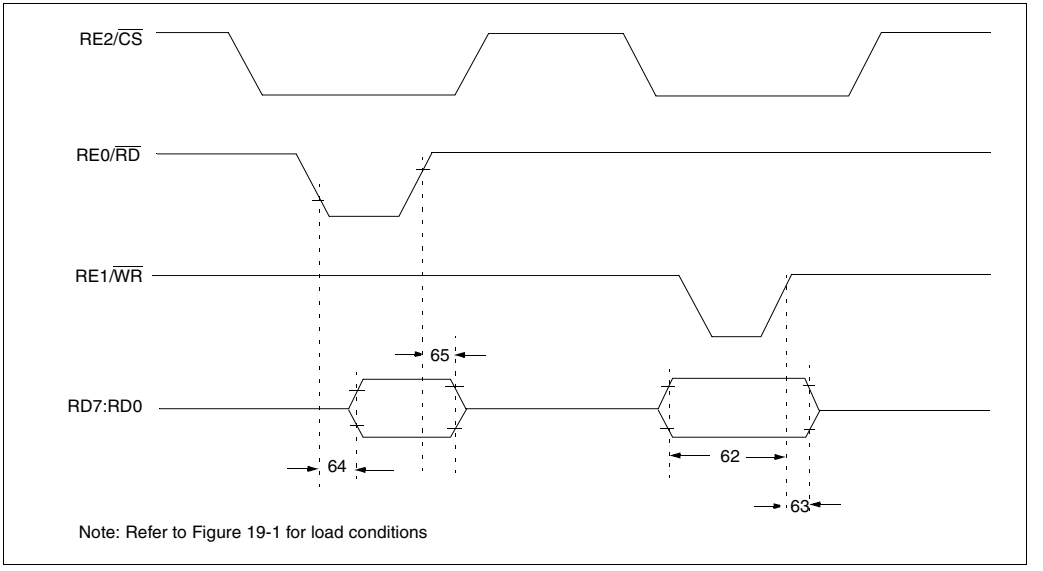
| Parameter No. | Sym | Characteristic | Min | Typ† | Max | Units | Conditions |
|---|---|---|---|---|---|---|---|
| 30* | TmcL | $\overline{MCLR}$ Pulse Width (low) | 100 | — | — | ns | VDD = 5V, -40°C to +85°C |
| 31* | Twdt | Watchdog Timer Time-out Period (No Prescaler) | 7 | 18 | 33 | ms | VDD = 5V, -40°C to +85°C |
| 32 | Tost | Oscillation Start-up Timer Period | — | 1024TOSC | — | — | TOSC = OSC1 period |
| 33* | Tpwrt | Power-up Timer Period or WDT reset | 28 | 72 | 132 | ms | VDD = 5V, -40°C to +85°C |
| 34 | TIOZ | I/O Hi-impedance from $\overline{MCLR}$ Low | — | — | 100 | ns | |

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

| Applicable Devices | 61 | 62 | 62A | R62 | 63 | R63 | 64 | 64A | R64 | 65 | 65A | R65 | 66 | 67 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|

**FIGURE 19-7: PARALLEL SLAVE PORT TIMING**




Note: Refer to Figure 19-1 for load conditions

**TABLE 19-7: PARALLEL SLAVE PORT REQUIREMENTS**

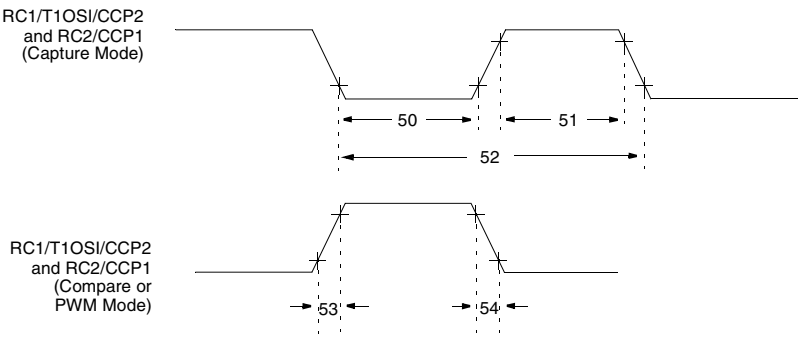
| Parameter No. | Sym | Characteristic | | Min | Typ† | Max | Units | Conditions |
|---|---|---|---|---|---|---|---|---|
| 62 | TdtV2wrH | Data in valid before $\overline{WR}\uparrow$ or $\overline{CS}\uparrow$ (setup time) | | 20 | — | — | ns | |
| 63* | TwrH2dtI | $\overline{WR}\uparrow$ or $\overline{CS}\uparrow$ to data–in invalid (hold time) | PIC16**C**65 | 20 | — | — | ns | |
| | | | PIC16**LC**65 | 35 | — | — | ns | |
| 64 | TrdL2dtV | $\overline{RD}\downarrow$ and $\overline{CS}\downarrow$ to data–out valid | | — | — | 80 | ns | |
| 65 | TrdH2dtI | $\overline{RD}\uparrow$ or $\overline{CS}\uparrow$ to data–out invalid | | 10 | — | 30 | ns | |

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

| Applicable Devices | 61 | 62 | 62A | R62 | 63 | R63 | 64 | 64A | R64 | 65 | 65A | R65 | 66 | 67 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|

**FIGURE 20-7: CAPTURE/COMPARE/PWM TIMINGS (CCP1 AND CCP2)**




Note: Refer to Figure 20-1 for load conditions.

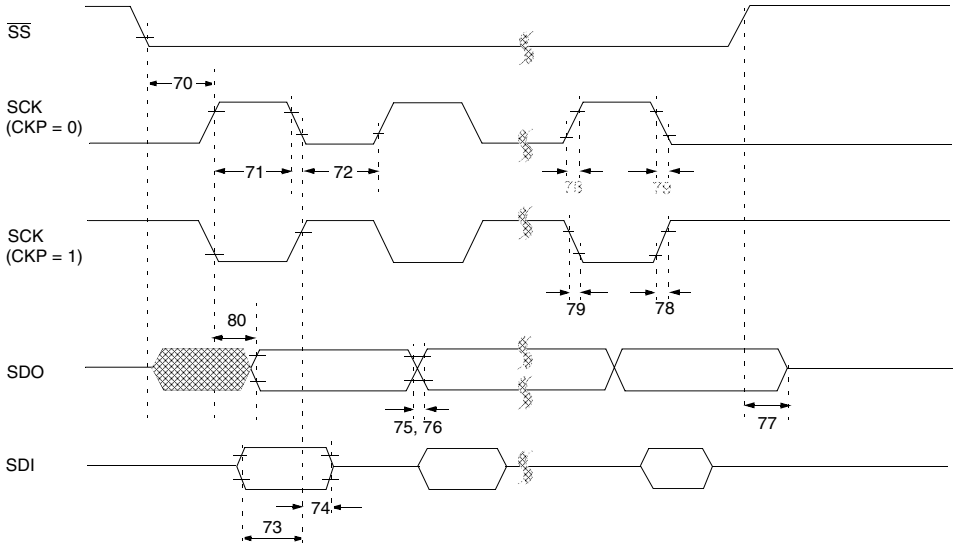
**TABLE 20-6: CAPTURE/COMPARE/PWM REQUIREMENTS (CCP1 AND CCP2)**

| Parameter No. | Sym | Characteristic | | | Min | Typ† | Max | Units | Conditions |
|---|---|---|---|---|---|---|---|---|---|
| 50* | TccL | CCP1 and CCP2 input low time | No Prescaler | | 0.5TCY + 20 | — | — | ns | |
| | | | With Prescaler | PIC16**C**63/65A | 10 | — | — | ns | |
| | | | | PIC16**LC**63/65A | 20 | — | — | ns | |
| 51* | TccH | CCP1 and CCP2 input high time | No Prescaler | | 0.5TCY + 20 | — | — | ns | |
| | | | With Prescaler | PIC16**C**63/65A | 10 | — | — | ns | |
| | | | | PIC16**LC**63/65A | 20 | — | — | ns | |
| 52* | TccP | CCP1 and CCP2 input period | | | $\frac{3T_{CY} + 40}{N}$ | — | — | ns | N = prescale value (1,4, or 16) |
| 53* | TccR | CCP1 and CCP2 output rise time | | PIC16**C**63/65A | — | 10 | 25 | ns | |
| | | | | PIC16**LC**63/65A | — | 25 | 45 | ns | |
| 54* | TccF | CCP1 and CCP2 output fall time | | PIC16**C**63/65A | — | 10 | 25 | ns | |
| | | | | PIC16**LC**63/65A | — | 25 | 45 | ns | |

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**FIGURE 21-9: SPI MODE TIMING**




Note: Refer to Figure 21-1 for load conditions

**TABLE 21-8: SPI MODE REQUIREMENTS**

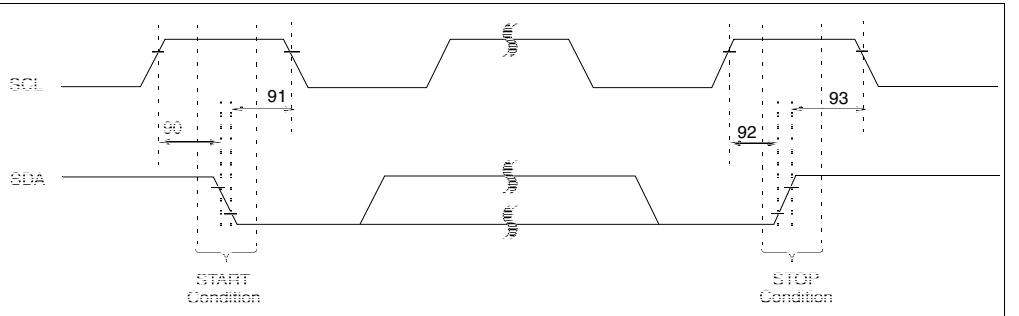
| Parameter No. | Sym | Characteristic | Min | Typ† | Max | Units | Conditions |
|---|---|---|---|---|---|---|---|
| 70* | TssL2scH, TssL2scL | $\overline{SS}$↓ to SCK↓ or SCK↑ input | TCY | — | — | ns | |
| 71* | TscH | SCK input high time (slave mode) | TCY + 20 | — | — | ns | |
| 72* | TscL | SCK input low time (slave mode) | TCY + 20 | — | — | ns | |
| 73* | TdiV2scH, TdiV2scL | Setup time of SDI data input to SCK edge | 50 | — | — | ns | |
| 74* | TscH2diL, TscL2diL | Hold time of SDI data input to SCK edge | 50 | — | — | ns | |
| 75* | TdoR | SDO data output rise time | — | 10 | 25 | ns | |
| 76* | TdoF | SDO data output fall time | — | 10 | 25 | ns | |
| 77* | TssH2doZ | $\overline{SS}$↑ to SDO output hi-impedance | 10 | — | 50 | ns | |
| 78* | TscR | SCK output rise time (master mode) | — | 10 | 25 | ns | |
| 79* | TscF | SCK output fall time (master mode) | — | 10 | 25 | ns | |
| 80* | TscH2doV, TscL2doV | SDO data output valid after SCK edge | — | — | 50 | ns | |

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

| Applicable Devices | 61 | 62 | 62A | R62 | 63 | R63 | 64 | 64A | R64 | 65 | 65A | R65 | 66 | 67 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|

**FIGURE 21-10: I²C BUS START/STOP BITS TIMING**




Note: Refer to Figure 21-1 for load conditions

**TABLE 21-9: I²C BUS START/STOP BITS REQUIREMENTS**

| Parameter No. | Sym | Characteristic | | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|---|---|
| 90* | TSU:STA | START condition Setup time | 100 kHz mode | 4700 | — | — | ns | Only relevant for repeated START condition |
| | | | 400 kHz mode | 600 | — | — | | |
| 91* | THD:STA | START condition Hold time | 100 kHz mode | 4000 | — | — | ns | After this period the first clock pulse is generated |
| | | | 400 kHz mode | 600 | — | — | | |
| 92* | TSU:STO | STOP condition Setup time | 100 kHz mode | 4700 | — | — | ns | |
| | | | 400 kHz mode | 600 | — | — | | |
| 93 | THD:STO | STOP condition Hold time | 100 kHz mode | 4000 | — | — | ns | |
| | | | 400 kHz mode | 600 | — | — | | |

* These parameters are characterized but not tested.

| Applicable Devices | 61 | 62 | 62A | R62 | 63 | R63 | 64 | 64A | R64 | 65 | 65A | R65 | 66 | 67 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|

**FIGURE 23-12: TYPICAL IDD vs. FREQUENCY (RC MODE @ 22 pF, 25°C)**

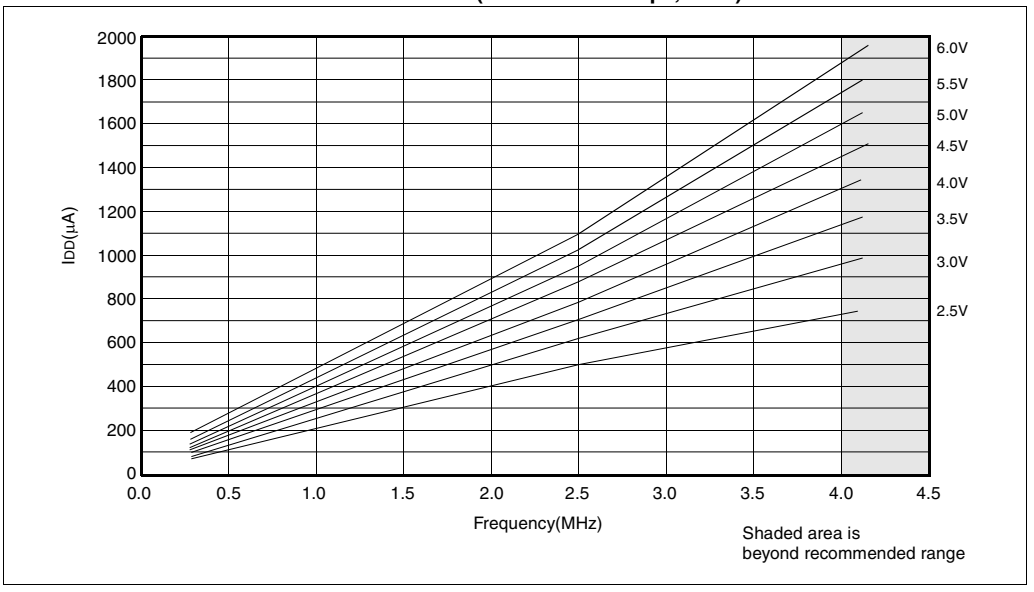
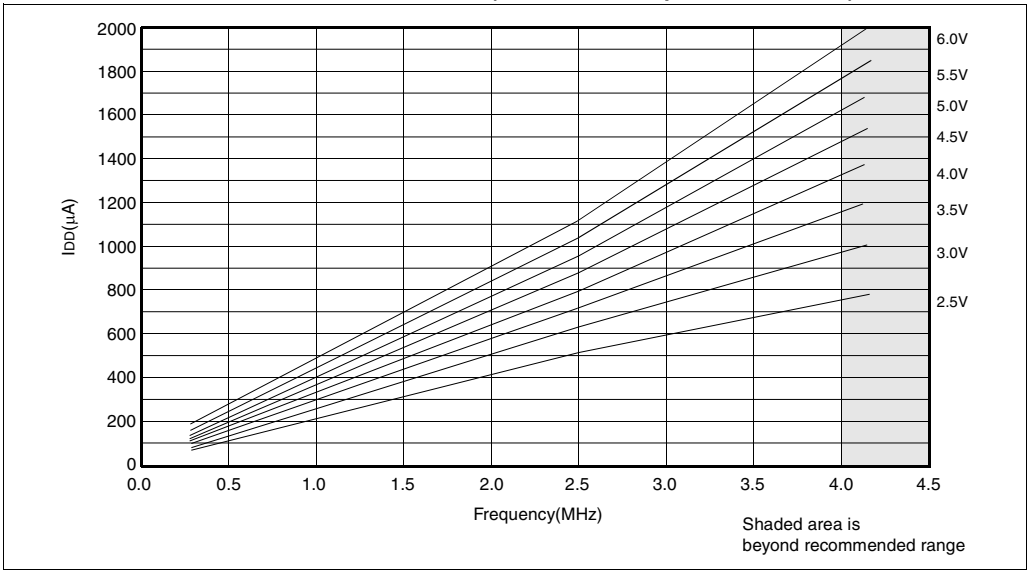


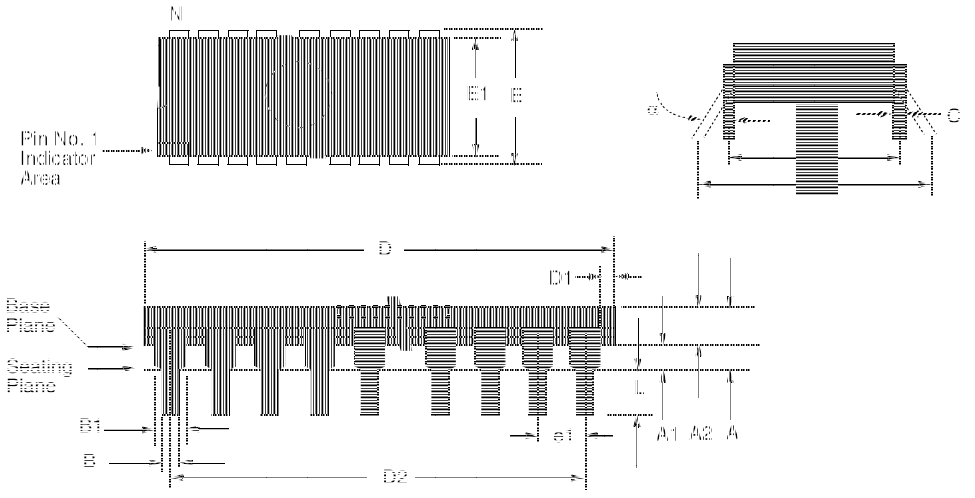

**FIGURE 23-13: MAXIMUM IDD vs. FREQUENCY (RC MODE @ 22 pF, -40°C TO 85°C)**




Data based on matrix samples. See first page of this section for details.

### 24.7 28-Lead Ceramic CERDIP Dual In-line with Window (300 mil)) (JW)

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




| Package Group: Ceramic CERDIP Dual In-Line (CDP) | | | | | | |
|---|---|---|---|---|---|---|
| | Millimeters | | | Inches | | |
| Symbol | Min | Max | Notes | Min | Max | Notes |
| α | 0° | 10° | | 0° | 10° | |
| A | 3.30 | 5.84 | | .130 | 0.230 | |
| A1 | 0.38 | — | | 0.015 | — | |
| A2 | 2.92 | 4.95 | | 0.115 | 0.195 | |
| B | 0.35 | 0.58 | | 0.014 | 0.023 | |
| B1 | 1.14 | 1.78 | **Typical** | 0.045 | 0.070 | **Typical** |
| C | 0.20 | 0.38 | **Typical** | 0.008 | 0.015 | **Typical** |
| D | 34.54 | 37.72 | | 1.360 | 1.485 | |
| D2 | 32.97 | 33.07 | **Reference** | 1.298 | 1.302 | **Reference** |
| E | 7.62 | 8.25 | | 0.300 | 0.325 | |
| E1 | 6.10 | 7.87 | | 0.240 | 0.310 | |
| e | 2.54 | 2.54 | **Typical** | 0.100 | 0.100 | **Typical** |
| eA | 7.62 | 7.62 | **Reference** | 0.300 | 0.300 | **Reference** |
| eB | — | 11.43 | | — | 0.450 | |
| L | 2.92 | 5.08 | | 0.115 | 0.200 | |
| N | 28 | 28 | | 28 | 28 | |
| D1 | 0.13 | — | | 0.005 | — | |

## D



## E



## F



## G



## H



## I