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Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	33
Program Memory Size	14KB (8K x 14)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	368 x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 6V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lc67t-04i-pt

5.4 PORTD and TRISD Register

Applicable Devices															
61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67		

PORTD is an 8-bit port with Schmitt Trigger input buffers. Each pin is individually configurable as input or output.

PORTD can be configured as an 8-bit wide microprocessor port (parallel slave port) by setting control bit PSMODE (TRISE<4>). In this mode, the input buffers are TTL.

FIGURE 5-7: PORTD BLOCK DIAGRAM (IN I/O PORT MODE)

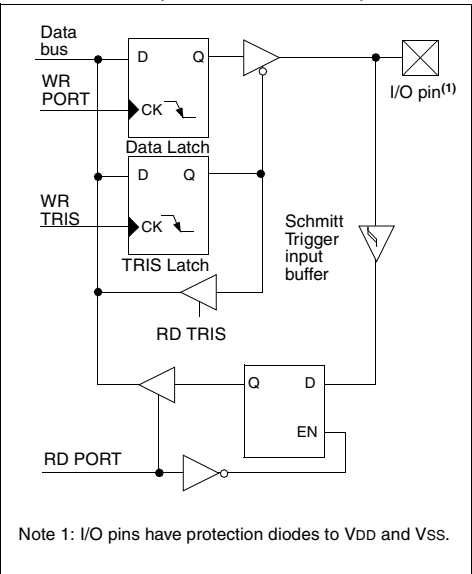


TABLE 5-9: PORTD FUNCTIONS

Name	Bit#	Buffer Type	Function
RD0/PSP0	bit0	ST/TTL ⁽¹⁾	Input/output port pin or parallel slave port bit0
RD1/PSP1	bit1	ST/TTL ⁽¹⁾	Input/output port pin or parallel slave port bit1
RD2/PSP2	bit2	ST/TTL ⁽¹⁾	Input/output port pin or parallel slave port bit2
RD3/PSP3	bit3	ST/TTL ⁽¹⁾	Input/output port pin or parallel slave port bit3
RD4/PSP4	bit4	ST/TTL ⁽¹⁾	Input/output port pin or parallel slave port bit4
RD5/PSP5	bit5	ST/TTL ⁽¹⁾	Input/output port pin or parallel slave port bit5
RD6/PSP6	bit6	ST/TTL ⁽¹⁾	Input/output port pin or parallel slave port bit6
RD7/PSP7	bit7	ST/TTL ⁽¹⁾	Input/output port pin or parallel slave port bit7

Legend: ST = Schmitt Trigger input, TTL = TTL input

Note 1: Buffer is a Schmitt Trigger when in I/O mode, and a TTL buffer when in Parallel Slave Port mode.

TABLE 5-10: SUMMARY OF REGISTERS ASSOCIATED WITH PORTD

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other resets
08h	PORTD	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	xxxx xxxx	uuuu uuuu
88h	TRISD	PORTD Data Direction Register								1111 1111	1111 1111
89h	TRISE	IBF	OBF	IBOV	PSPMODE	—	PORTE Data Direction Bits			0000 -111	0000 -111

Legend: x = unknown, u = unchanged, - = unimplemented locations read as '0'. Shaded cells are not used by PORTD.

10.0 CAPTURE/COMPARE/PWM (CCP) MODULE(s)

Applicable Devices															
61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67	CCP1	
61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67	CCP2	

Each CCP (Capture/Compare/PWM) module contains a 16-bit register which can operate as a 16-bit capture register, as a 16-bit compare register, or as a PWM master/slave duty cycle register. Both the CCP1 and CCP2 modules are identical in operation, with the exception of the operation of the special event trigger. Table 10-1 and Table 10-2 show the resources and interactions of the CCP modules(s). In the following sections, the operation of a CCP module is described with respect to CCP1. CCP2 operates the same as CCP1, except where noted.

CCP1 module:

Capture/Compare/PWM Register1 (CCPR1) is comprised of two 8-bit registers: CCPR1L (low byte) and CCPR1H (high byte). The CCP1CON register controls the operation of CCP1. All are readable and writable.

CCP2 module:

Capture/Compare/PWM Register2 (CCPR2) is comprised of two 8-bit registers: CCPR2L (low byte) and CCPR2H (high byte). The CCP2CON register controls the operation of CCP2. All are readable and writable.

For use of the CCP modules, refer to the *Embedded Control Handbook*, "Using the CCP Modules" (AN594).

TABLE 10-1: CCP MODE - TIMER RESOURCE

CCP Mode	Timer Resource
Capture	Timer1
Compare	Timer1
PWM	Timer2

TABLE 10-2: INTERACTION OF TWO CCP MODULES

CCPx Mode	CCPy Mode	Interaction
Capture	Capture	Same TMR1 time-base.
Capture	Compare	The compare should be configured for the special event trigger, which clears TMR1.
Compare	Compare	The compare(s) should be configured for the special event trigger, which clears TMR1.
PWM	PWM	The PWMs will have the same frequency, and update rate (TMR2 interrupt).
PWM	Capture	None
PWM	Compare	None

12.4 USART Synchronous Slave Mode

Applicable Devices

61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67
----	----	-----	-----	----	-----	----	-----	-----	----	-----	-----	----	----

Synchronous Slave Mode differs from Master Mode in the fact that the shift clock is supplied externally at the CK pin (instead of being supplied internally in master mode). This allows the device to transfer or receive data while in SLEEP mode. Slave mode is entered by clearing bit CSRC (TXSTA<7>).

12.4.1 USART SYNCHRONOUS SLAVE TRANSMIT

The operation of the synchronous master and slave modes are identical except in the case of the SLEEP mode.

If two words are written to the TXREG and then the SLEEP instruction is executed, the following will occur:

- The first word will immediately transfer to the TSR register and transmit.
- The second word will remain in TXREG register.
- Flag bit TXIF will not be set.
- When the first word has been shifted out of TSR, the TXREG register will transfer the second word to the TSR and flag bit TXIF will now be set.
- If enable bit TXIE is set, the interrupt will wake the chip from SLEEP and if the global interrupt is enabled, the program will branch to the interrupt vector (0004h).

Steps to follow when setting up Synchronous Slave Transmission:

- Enable the synchronous slave serial port by setting bits SYNC and SPEN, and clearing bit CSRC.
- Clear bits CREN and SREN.
- If interrupts are desired, then set enable bit TXIE.
- If 9-bit transmission is desired, then set bit TX9.
- Enable the transmission by setting bit TXEN.
- If 9-bit transmission is selected, the ninth bit should be loaded in bit TX9D.
- Start transmission by loading data to the TXREG register.

12.4.2 USART SYNCHRONOUS SLAVE RECEPTION

The operation of the synchronous master and slave modes is identical except in the case of the SLEEP mode. Also, enable bit SREN is a don't care in slave mode.

If receive is enabled by setting bit CREN prior to the SLEEP instruction, then a word may be received during SLEEP. On completely receiving the word, the RSR register will transfer the data to the RCREG register and if enable bit RCIE is set, the interrupt generated will wake the chip from SLEEP. If the global interrupt is enabled, the program will branch to the interrupt vector (0004h).

Steps to follow when setting up a Synchronous Slave Reception:

- Enable the synchronous master serial port by setting bits SYNC and SPEN, and clearing bit CSRC.
- If interrupts are desired, then set enable bit RCIE.
- If 9-bit reception is desired, then set bit RX9.
- To enable reception, set enable bit CREN.
- Flag bit RCIF will be set when reception is complete, and an interrupt will be generated if enable bit RCIE was set.
- Read the RCSTA register to get the ninth bit (if enabled) and determine if any error occurred during reception.
- Read the 8-bit received data by reading the RCREG register.
- If any error occurred, clear the error by clearing enable bit CREN.

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13.4.5 TIME-OUT SEQUENCE

On power-up the time-out sequence is as follows: First a PWRT time-out is invoked after the POR time delay has expired. Then OST is activated. The total time-out will vary based on oscillator configuration and the status of the PWRT. For example, in RC mode, with the PWRT disabled, there will be no time-out at all. Figure 13-11, Figure 13-12, and Figure 13-13 depict time-out sequences on power-up.

Since the time-outs occur from the POR pulse, if the MCLR/VPP pin is kept low long enough, the time-outs will expire. Then bringing the MCLR/VPP pin high will begin execution immediately (Figure 13-14). This is useful for testing purposes or to synchronize more than one PIC16CXX device operating in parallel.

Table 13-10 and Table 13-11 show the reset conditions for some special function registers, while Table 13-12 shows the reset conditions for all the registers.

13.4.6 POWER CONTROL/STATUS REGISTER (PCON)

Applicable Devices

61|62|62A|R62|63|R63|64|64A|R64|65|65A|R65|66|67

The Power Control/Status Register, PCON has up to two bits, depending upon the device. Bit0 is not implemented on the PIC16C62/64/65.

Bit0 is $\overline{\text{BOR}}$ (Brown-out Reset Status bit). $\overline{\text{BOR}}$ is unknown on Power-on Reset. It must then be set by the user and checked on subsequent resets to see if $\overline{\text{BOR}}$ cleared, indicating that a brown-out has occurred. The $\overline{\text{BOR}}$ status bit is a “Don't Care” and is not necessarily predictable if the Brown-out Reset circuitry is disabled (by clearing bit BODEN in the Configuration Word).

Bit1 is $\overline{\text{POR}}$ (Power-on Reset Status bit). It is cleared on a Power-on Reset and unaffected otherwise. The user must set this bit following a Power-on Reset.

TABLE 13-5: TIME-OUT IN VARIOUS SITUATIONS, PIC16C61/62/64/65

Oscillator Configuration	Power-up		Wake-up from SLEEP
	PWRT = 1	PWRT = 0	
XT, HS, LP	72 ms + 1024TOSC	1024TOSC	1024 TOSC
RC	72 ms	—	—

TABLE 13-6: TIME-OUT IN VARIOUS SITUATIONS, PIC16C62A/R62/63/R63/64A/R64/65A/R65/66/67

Oscillator Configuration	Power-up		Brown-out	Wake up from SLEEP
	PWRT = 0	PWRT = 1		
XT, HS, LP	72 ms + 1024TOSC	1024TOSC	72 ms + 1024TOSC	1024 TOSC
RC	72 ms	—	72 ms	—

TABLE 13-7: STATUS BITS AND THEIR SIGNIFICANCE, PIC16C61

TO	PD	
1	1	Power-on Reset or MCLR reset during normal operation
0	1	WDT Reset
0	0	WDT Wake-up
1	0	MCLR reset during SLEEP or interrupt wake-up from SLEEP

TABLE 13-8: STATUS BITS AND THEIR SIGNIFICANCE, PIC16C62/64/65

POR	TO	PD	
0	1	1	Power-on Reset
0	0	x	Illegal, TO is set on a Power-on Reset
0	x	0	Illegal, PD is set on a Power-on Reset
1	0	1	WDT Reset
1	0	0	WDT Wake-up
1	u	u	MCLR reset during normal operation
1	1	0	MCLR reset during SLEEP or interrupt wake-up from SLEEP

Legend: x = unknown, u = unchanged

TABLE 13-9: STATUS BITS AND THEIR SIGNIFICANCE FOR PIC16C62A/R62/63/R63/64A/R64/65A/R65/66/67

POR	BOR	TO	PD	
0	x	1	1	Power-on Reset
0	x	0	x	Illegal, TO is set on a Power-on Reset
0	x	x	0	Illegal, PD is set on a Power-on Reset
1	0	x	x	Brown-out Reset
1	1	0	1	WDT Reset
1	1	0	0	WDT Wake-up
1	1	u	u	MCLR reset during normal operation
1	1	1	0	MCLR reset during SLEEP or interrupt wake-up from SLEEP

Legend: x = unknown, u = unchanged

TABLE 13-10: RESET CONDITION FOR SPECIAL REGISTERS ON PIC16C61/62/64/65

	Program Counter	STATUS	PCON ⁽²⁾
Power-on Reset	000h	0001 1xxx	---- --0-
MCLR reset during normal operation	000h	000u uuuu	---- --u-
MCLR reset during SLEEP	000h	0001 0uuu	---- --u-
WDT Reset	000h	0000 1uuu	---- --u-
WDT Wake-up	PC + 1	uuu0 0uuu	---- --u-
Interrupt wake-up from SLEEP	PC + 1 ⁽¹⁾	uuu1 0uuu	---- --u-

Legend: u = unchanged, x = unknown, - = unimplemented bit read as '0'.

Note 1: When the wake-up is due to an interrupt and the global enable bit, GIE is set, the PC is loaded with the interrupt vector (0004h) after execution of PC+1.

2: The PCON register is not implemented on the PIC16C61.

TABLE 13-11: RESET CONDITION FOR SPECIAL REGISTERS ON PIC16C62A/R62/63/R63/64A/R64/65A/R65/66/67

	Program Counter	STATUS	PCON
Power-on Reset	000h	0001 1xxx	---- --0x
MCLR reset during normal operation	000h	000u uuuu	---- --uu
MCLR reset during SLEEP	000h	0001 0uuu	---- --uu
WDT Reset	000h	0000 1uuu	---- --uu
Brown-out Reset	000h	0001 1uuu	---- --u0
WDT Wake-up	PC + 1	uuu0 0uuu	---- --uu
Interrupt wake-up from SLEEP	PC + 1 ⁽¹⁾	uuu1 0uuu	---- --uu

Legend: u = unchanged, x = unknown, - = unimplemented bit read as '0'.

Note 1: When the wake-up is due to an interrupt and global enable bit, GIE is set, the PC is loaded with the interrupt vector (0004h) after execution of PC+1.

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IORWF Inclusive OR W with f

Syntax:	[<i>label</i>] IORWF f,d							
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$							
Operation:	(W) .OR. (f) \rightarrow (destination)							
Status Affected:	Z							
Encoding:	<table><tr><td>00</td><td>0100</td><td>dfff</td><td>ffff</td></tr></table>				00	0100	dfff	ffff
00	0100	dfff	ffff					
Description:	Inclusive OR the W register with register 'f'. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'.							
Words:	1							
Cycles:	1							
Q Cycle Activity:	Q1	Q2	Q3	Q4				
	Decode	Read register 'f'	Process data	Write to destination				

Example IORWF RESULT, 0

Before Instruction

RESULT = 0x13
W = 0x91

After Instruction

RESULT = 0x13
W = 0x93
Z = 1

MOVF Move f

Syntax:	[<i>label</i>] MOVF f,d			
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$			
Operation:	(f) \rightarrow (destination)			
Status Affected:	Z			
Encoding:	00	1000	dfff	ffff
Description:	The contents of register f is moved to a destination dependant upon the status of d. If d = 0, destination is W register. If d = 1, the destination is file register f itself. d = 1 is useful to test a file register since status flag Z is affected.			
Words:	1			
Cycles:	1			
Q Cycle Activity:	Q1	Q2	Q3	Q4
	Decode	Read register 'f'	Process data	Write to destination

Example MOVF FSR, 0

After Instruction

W = value in FSR register
Z = 1

MOVLW Move Literal to W

Syntax:	[<i>label</i>] MOVLW k			
Operands:	0 ≤ k ≤ 255			
Operation:	k → (W)			
Status Affected:	None			
Encoding:	11	00xx	kkkk	kkkk
Description:	The eight bit literal 'k' is loaded into W register. The don't cares will assemble as 0's.			
Words:	1			
Cycles:	1			
Q Cycle Activity:	Q1	Q2	Q3	Q4
	Decode	Read literal 'k'	Process data	Write to W

Example

MOVLW 0x5A

After Instruction

W = 0x5A

MOVWF Move W to f

Syntax:	[<i>label</i>] MOVWF f			
Operands:	$0 \leq f \leq 127$			
Operation:	(W) → (f)			
Status Affected:	None			
Encoding:	00	0000	1fff	ffff
Description:	Move data from W register to register 'f'.			
Words:	1			
Cycles:	1			
Q Cycle Activity:	Q1	Q2	Q3	Q4
	Decode	Read register 'f'	Process data	Write register 'f'

Example

MOVWF OPTION_REG

Before Instruction

OPTION = 0xFF
W = 0x4F

After Instruction

OPTION = 0x4F
W = 0x4F

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SLEEP

Syntax: [*label*] SLEEP

Operands: None

Operation: 00h → WDT,
0 → WDT prescaler,
1 → \overline{TO} ,
0 → \overline{PD}

Status Affected: \overline{TO} , \overline{PD}

Encoding:

00	0000	0110	0011
----	------	------	------

Description: The power-down status bit, \overline{PD} is cleared. Time-out status bit, \overline{TO} is set. Watchdog Timer and its prescaler are cleared.
The processor is put into SLEEP mode with the oscillator stopped. See Section 13.8 for more details.

Words: 1

Cycles: 1

Q Cycle Activity:

	Q1	Q2	Q3	Q4
Decode	No-Operation	No-Operation	Go to Sleep	

Example: SLEEP

SUBLW

Subtract W from Literal

Syntax: [*label*] SUBLW k

Operands: $0 \leq k \leq 255$

Operation: $k - (W) \rightarrow (W)$

Status Affected: C, DC, Z

Encoding:

11	110x	kkkk	kkkk
----	------	------	------

Description: The W register is subtracted (2's complement method) from the eight bit literal 'k'. The result is placed in the W register.

Words: 1

Cycles: 1

Q Cycle Activity:

	Q1	Q2	Q3	Q4
Decode	Read literal 'k'	Process data	Write to W	

Example 1: SUBLW 0x02

Before Instruction

W = 1
C = ?
Z = ?

After Instruction

W = 1
C = 1; result is positive
Z = 0

Example 2: Before Instruction

W = 2
C = ?
Z = ?

After Instruction

W = 0
C = 1; result is zero
Z = 1

Example 3: Before Instruction

W = 3
C = ?
Z = ?

After Instruction

W = 0xFF
C = 0; result is negative
Z = 0

PIC16C6X

Applicable Devices 61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

FIGURE 16-2: TYPICAL RC OSCILLATOR
FREQUENCY vs. VDD

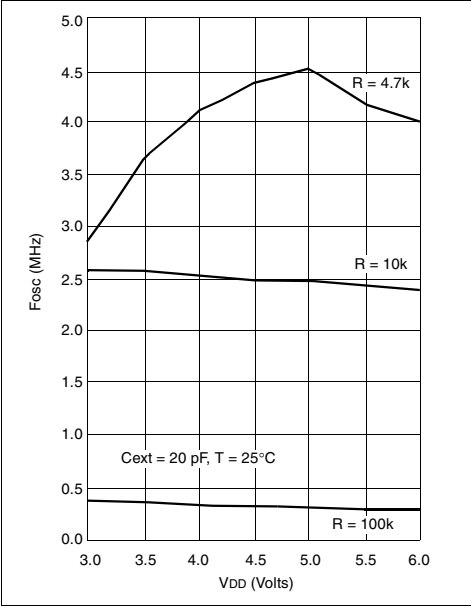


FIGURE 16-3: TYPICAL RC OSCILLATOR
FREQUENCY vs. VDD

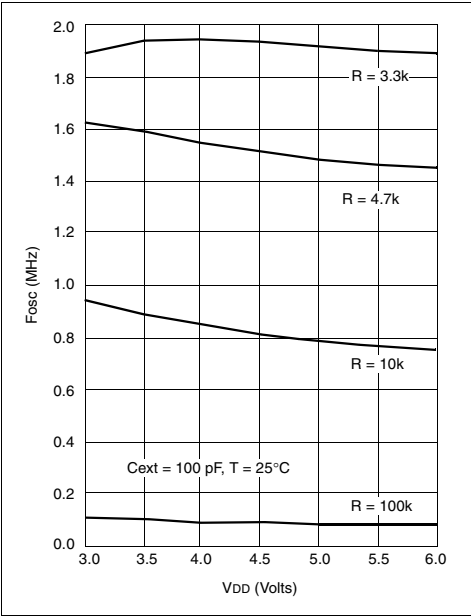


FIGURE 16-4: TYPICAL RC OSCILLATOR
FREQUENCY vs. VDD

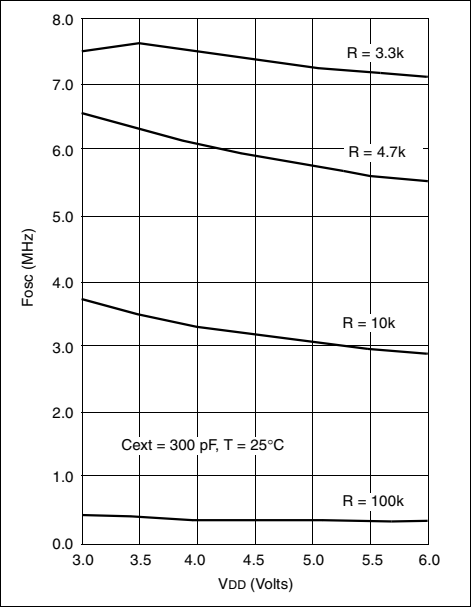
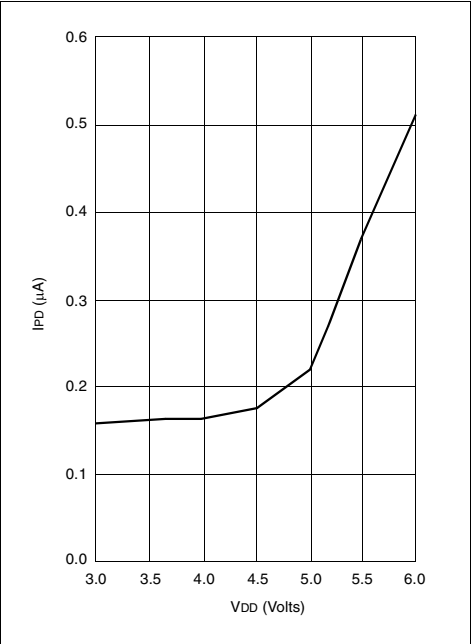


FIGURE 16-5: TYPICAL IPD vs. VDD
WATCHDOG TIMER
DISABLED 25°C



Data based on matrix samples. See first page of this section for details.

PIC16C6X

Applicable Devices 61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

17.3 DC Characteristics: PIC16C62/64-04 (Commercial, Industrial) PIC16C62/64-10 (Commercial, Industrial) PIC16C62/64-20 (Commercial, Industrial) PIC16LC62/64-04 (Commercial, Industrial)

Standard Operating Conditions (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for industrial and $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ for commercial Operating voltage V_{DD} range as described in DC spec Section 17.1 and Section 17.2							
DC CHARACTERISTICS							
Param No.	Characteristic	Sym	Min	Typ †	Max	Units	Conditions
D030 D030A D031 D032 D033	Input Low Voltage I/O ports with TTL buffer with Schmitt Trigger buffer MCLR, OSC1 (in RC mode) OSC1 (in XT, HS and LP)	V_{IL}	V_{SS} V_{SS} V_{SS} V_{SS} V_{SS}	- - - - -	$0.15V_{DD}$ $0.8V$ $0.2V_{DD}$ $0.2V_{DD}$ $0.3V_{DD}$	V V V V V	For entire V_{DD} range $4.5V \leq V_{DD} \leq 5.5V$ Note1
D040 D040A D041 D042 D042A D043 D070	Input High Voltage I/O ports with TTL buffer with Schmitt Trigger buffer MCLR OSC1 (XT, HS and LP) OSC1 (in RC mode) PORTB weak pull-up current	V_{IH}	2.0 $0.25V_{DD} + 0.8V$ $0.8V_{DD}$ $0.8V_{DD}$ $0.7V_{DD}$ $0.9V_{DD}$ 50	- - - - - - 200	V_{DD} V_{DD} V_{DD} V_{DD} V_{DD} V_{DD} 400	V V V V V V μA	$4.5V \leq V_{DD} \leq 5.5V$ For entire V_{DD} range For entire V_{DD} range Note1 $V_{DD} = 5V, V_{PIN} = V_{SS}$
D060 D061 D063	Input Leakage Current (Notes 2, 3) I/O ports MCLR, RA4/T0CKI OSC1	I_{IL}	-	-	± 1	μA	$V_{SS} \leq V_{PIN} \leq V_{DD}$, Pin at hi-impedance
			-	-	± 5	μA	$V_{SS} \leq V_{PIN} \leq V_{DD}$
			-	-	± 5	μA	$V_{SS} \leq V_{PIN} \leq V_{DD}$, XT, HS and LP osc configuration
D080 D083	Output Low Voltage I/O ports OSC2/CLKOUT (RC osc config)	V_{OL}	-	-	0.6	V	$I_{OL} = 8.5\text{ mA}$, $V_{DD} = 4.5V$, -40°C to $+85^{\circ}\text{C}$
			-	-	0.6	V	$I_{OL} = 1.6\text{ mA}$, $V_{DD} = 4.5V$, -40°C to $+85^{\circ}\text{C}$
D090 D092	Output High Voltage I/O ports (Note 3) OSC2/CLKOUT (RC osc config)	V_{OH}	$V_{DD}-0.7$	-	-	V	$I_{OH} = -3.0\text{ mA}$, $V_{DD} = 4.5V$, -40°C to $+85^{\circ}\text{C}$
			$V_{DD}-0.7$	-	-	V	$I_{OH} = -1.3\text{ mA}$, $V_{DD} = 4.5V$, -40°C to $+85^{\circ}\text{C}$
D150*	Open-Drain High Voltage	V_{OD}	-	-	14	V	RA4 pin

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C6X be driven with external clock in RC mode.

2: The leakage current on the MCLR/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as current sourced by the pin.

Applicable Devices 61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

FIGURE 17-10: I²C BUS DATA TIMING

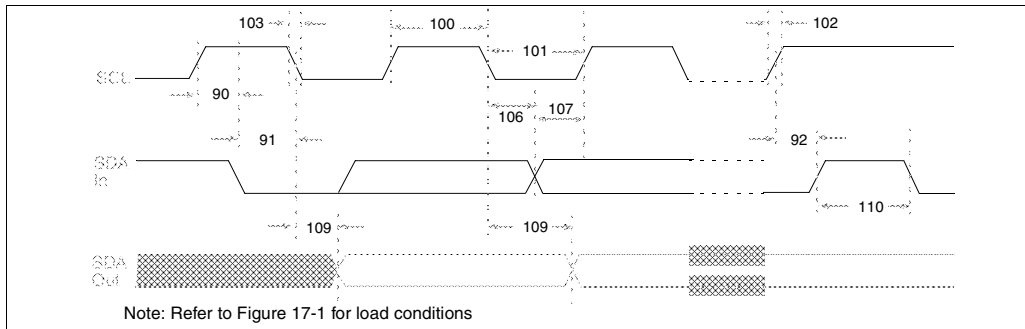


TABLE 17-10: I²C BUS DATA REQUIREMENTS

Parameter No.	Sym	Characteristic		Min	Max	Units	Conditions
100	THIGH	Clock high time	100 kHz mode	4.0	—	μs	Device must operate at a minimum of 1.5 MHz
			400 kHz mode	0.6	—	μs	Device must operate at a minimum of 10 MHz
			SSP Module	1.5TCY	—		
101	TLOW	Clock low time	100 kHz mode	4.7	—	μs	Device must operate at a minimum of 1.5 MHz
			400 kHz mode	1.3	—	μs	Device must operate at a minimum of 10 MHz
			SSP Module	1.5TCY	—		
102	Tr	SDA and SCL rise time	100 kHz mode	—	1000	ns	
			400 kHz mode	20 + 0.1Cb	300	ns	Cb is specified to be from 10 to 400 pF
103	TF	SDA and SCL fall time	100 kHz mode	—	300	ns	
			400 kHz mode	20 + 0.1Cb	300	ns	Cb is specified to be from 10 to 400 pF
90	TSU:STA	START condition setup time	100 kHz mode	4.7	—	μs	Only relevant for repeated START condition
			400 kHz mode	0.6	—	μs	
91	THD:STA	START condition hold time	100 kHz mode	4.0	—	μs	After this period the first clock pulse is generated
			400 kHz mode	0.6	—	μs	
106	THD:DAT	Data input hold time	100 kHz mode	0	—	ns	
			400 kHz mode	0	0.9	μs	
107	TSU:DAT	Data input setup time	100 kHz mode	250	—	ns	Note 2
			400 kHz mode	100	—	ns	
92	TSU:STO	STOP condition setup time	100 kHz mode	4.7	—	μs	
			400 kHz mode	0.6	—	μs	
109	TAA	Output valid from clock	100 kHz mode	—	3500	ns	Note 1
			400 kHz mode	—	—	ns	
110	TBUF	Bus free time	100 kHz mode	4.7	—	μs	Time the bus must be free before a new transmission can start
			400 kHz mode	1.3	—	μs	
	Cb	Bus capacitive loading		—	400	pF	

- Note 1: As a transmitter, the device must provide this internal minimum delay time to bridge the undefined region (min. 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.
- Note 2: A fast-mode (400 kHz) I²C-bus device can be used in a standard-mode (100 kHz) I²C-bus system, but the requirement tsu:DAT ≥ 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line Tr max. + tsu:DAT = 1000 + 250 = 1250 ns (according to the standard-mode I²C bus specification) before the SCL line is released.

18.5 Timing Diagrams and Specifications

FIGURE 18-2: EXTERNAL CLOCK TIMING

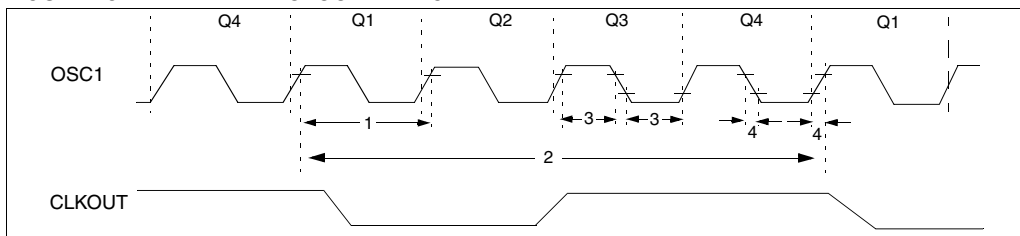


TABLE 18-2: EXTERNAL CLOCK TIMING REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
	Fosc	External CLKIN Frequency (Note 1)	DC	—	4	MHz	XT and RC osc mode
			DC	—	4	MHz	HS osc mode (-04)
			DC	—	10	MHz	HS osc mode (-10)
			DC	—	20	MHz	HS osc mode (-20)
			DC	—	200	kHz	LP osc mode
		Oscillator Frequency (Note 1)	DC	—	4	MHz	RC osc mode
			0.1	—	4	MHz	XT osc mode
			4	—	20	MHz	HS osc mode
			5	—	200	kHz	LP osc mode
			5	—	—	μs	LP osc mode
1	Tosc	External CLKIN Period (Note 1)	250	—	—	ns	XT and RC osc mode
			250	—	—	ns	HS osc mode (-04)
			100	—	—	ns	HS osc mode (-10)
			50	—	—	ns	HS osc mode (-20)
			5	—	—	μs	LP osc mode
		Oscillator Period (Note 1)	250	—	—	ns	RC osc mode
			250	—	10,000	ns	XT osc mode
			250	—	250	ns	HS osc mode (-04)
			100	—	250	ns	HS osc mode (-10)
			50	—	250	ns	HS osc mode (-20)
2	Tcy	Instruction Cycle Time (Note 1)	200	Tcy	DC	ns	Tcy = 4/Fosc
			200	Tcy	DC	ns	Tcy = 4/Fosc
3	TosL, TosH	External Clock in (OSC1) High or Low Time	100	—	—	ns	XT oscillator
			2.5	—	—	μs	LP oscillator
			15	—	—	ns	HS oscillator
4	TosR, TosF	External Clock in (OSC1) Rise or Fall Time	—	—	25	ns	XT oscillator
			—	—	50	ns	LP oscillator
			—	—	15	ns	HS oscillator

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Instruction cycle period (Tcy) equals four times the input oscillator time-base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min." values with an external clock applied to the OSC1/CLKIN pin. When an external clock input is used, the "Max." cycle time limit is "DC" (no clock) for all devices.

FIGURE 18-9: SPI MODE TIMING

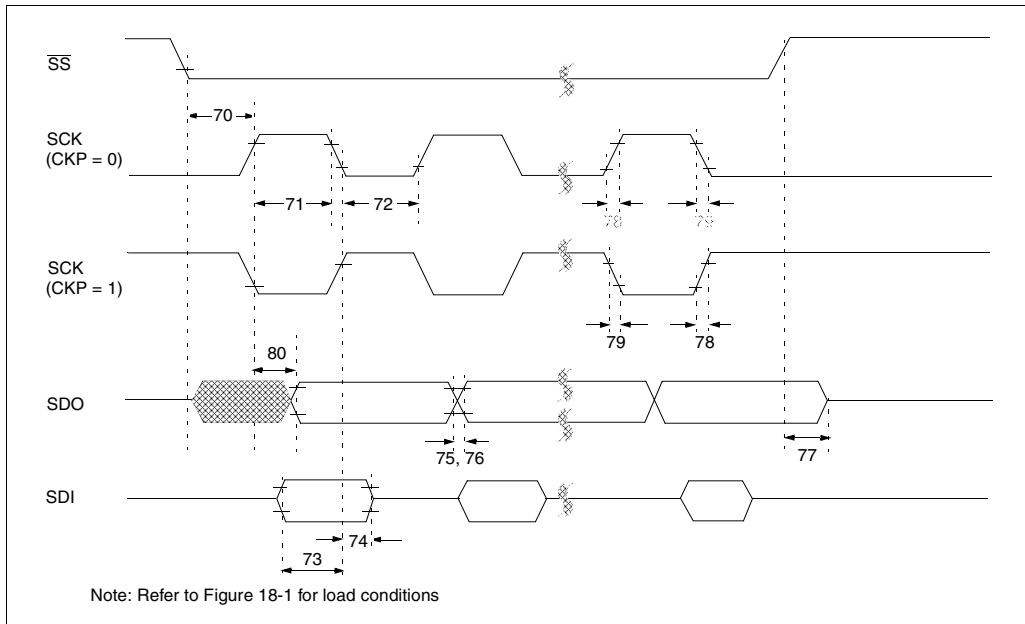


TABLE 18-8: SPI MODE REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
70*	TssL2scH, TssL2scL	$\overline{SS}\downarrow$ to SCK \downarrow or SCK \uparrow input	Tcy	—	—	ns	
71*	TscH	SCK input high time (slave mode)	Tcy + 20	—	—	ns	
72*	TscL	SCK input low time (slave mode)	Tcy + 20	—	—	ns	
73*	TdiV2scH, TdiV2scL	Setup time of SDI data input to SCK edge	50	—	—	ns	
74*	Tsch2diL, TscL2diL	Hold time of SDI data input to SCK edge	50	—	—	ns	
75*	TdoR	SDO data output rise time	—	10	25	ns	
76*	TdoF	SDO data output fall time	—	10	25	ns	
77*	TssH2doZ	$\overline{SS}\uparrow$ to SDO output hi-impedance	10	—	50	ns	
78*	TscR	SCK output rise time (master mode)	—	10	25	ns	
79*	TscF	SCK output fall time (master mode)	—	10	25	ns	
80*	Tsch2doV, TscL2doV	SDO data output valid after SCK edge	—	—	50	ns	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Applicable Devices 61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

FIGURE 18-11: I²C BUS DATA TIMING

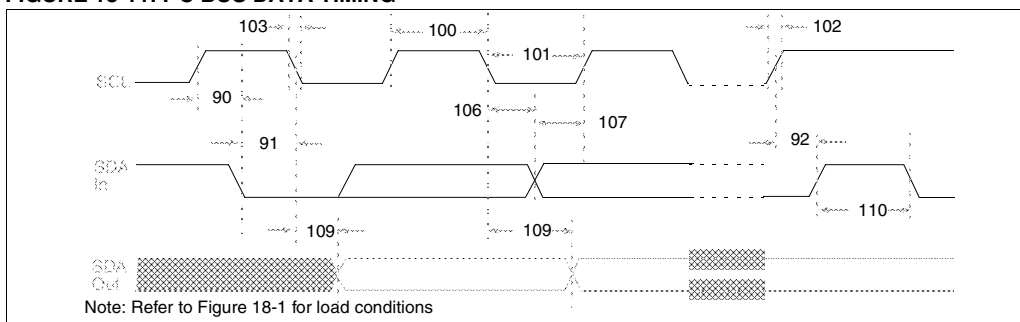


TABLE 18-10: I²C BUS DATA REQUIREMENTS

Parameter No.	Sym	Characteristic		Min	Max	Units	Conditions
100*	THIGH	Clock high time	100 kHz mode	4.0	—	μs	Device must operate at a minimum of 1.5 MHz
			400 kHz mode	0.6	—	μs	Device must operate at a minimum of 10 MHz
			SSP Module	1.5Tcy	—		
101*	TLOW	Clock low time	100 kHz mode	4.7	—	μs	Device must operate at a minimum of 1.5 MHz
			400 kHz mode	1.3	—	μs	Device must operate at a minimum of 10 MHz
			SSP Module	1.5Tcy	—		
102*	Tr	SDA and SCL rise time	100 kHz mode	—	1000	ns	
			400 kHz mode	20 + 0.1Cb	300	ns	Cb is specified to be from 10-400 pF
103*	TF	SDA and SCL fall time	100 kHz mode	—	300	ns	
			400 kHz mode	20 + 0.1Cb	300	ns	Cb is specified to be from 10-400 pF
90*	TSU:STA	START condition setup time	100 kHz mode	4.7	—	μs	Only relevant for repeated
			400 kHz mode	0.6	—	μs	START condition
91*	THD:STA	START condition hold time	100 kHz mode	4.0	—	μs	After this period the first clock
			400 kHz mode	0.6	—	μs	pulse is generated
106*	THD:DAT	Data input hold time	100 kHz mode	0	—	ns	
			400 kHz mode	0	0.9	μs	
107*	TSU:DAT	Data input setup time	100 kHz mode	250	—	ns	Note 2
			400 kHz mode	100	—	ns	
92*	TSU:STO	STOP condition setup time	100 kHz mode	4.7	—	μs	
			400 kHz mode	0.6	—	μs	
109*	TAA	Output valid from clock	100 kHz mode	—	3500	ns	Note 1
			400 kHz mode	—	—	ns	
110*	TBUF	Bus free time	100 kHz mode	4.7	—	μs	Time the bus must be free
			400 kHz mode	1.3	—	μs	before a new transmission can start
	Cb	Bus capacitive loading		—	400	pF	

* These parameters are characterized but not tested.

- Note 1: As a transmitter, the device must provide this internal minimum delay time to bridge the undefined region (min. 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.
- Note 2: A fast-mode (400 kHz) I²C-bus device can be used in a standard-mode (100 kHz) I²C-bus system, but the requirement tsu;DAT ≥ 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line Tr max.+tsu;DAT = 1000 + 250 = 1250 ns (according to the standard-mode I²C bus specification) before the SCL line is released.

PIC16C6X

Applicable Devices 61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

19.3 DC Characteristics: **PIC16C65-04 (Commercial, Industrial)**
PIC16C65-10 (Commercial, Industrial)
PIC16C65-20 (Commercial, Industrial)
PIC16LC65-04 (Commercial, Industrial)

DC CHARACTERISTICS		Standard Operating Conditions (unless otherwise stated)					
		Operating temperature -40°C ≤ TA ≤ +85°C for industrial and 0°C ≤ TA ≤ +70°C for commercial					
		Operating voltage VDD range as described in DC spec Section 19.1 and Section 19.2					
Param No.	Characteristic	Sym	Min	Typ †	Max	Units	Conditions
D030 D030A D031 D032 D033	Input Low Voltage I/O ports with TTL buffer with Schmitt Trigger buffer MCLR, OSC1 (in RC mode) OSC1 (in XT, HS and LP)	VIL	VSS VSS VSS VSS Vss	- - - - -	0.15VDD 0.8V 0.2VDD 0.2VDD 0.3VDD	V V V V V	For entire VDD range 4.5V ≤ VDD ≤ 5.5V Note1
D040 D040A D041 D042 D042A D043	Input High Voltage I/O ports with TTL buffer with Schmitt Trigger buffer MCLR OSC1 (XT, HS and LP) OSC1 (in RC mode)	VIH	2.0 0.25VDD + 0.8V 0.8VDD 0.8VDD 0.7 VDD 0.9VDD	- - - - - -	VDD VDD VDD VDD VDD VDD	V V V V V V	4.5V ≤ VDD ≤ 5.5V For entire VDD range For entire VDD range Note1
D070	PORTB weak pull-up current	IPURB	50	250	400	μA	VDD = 5V, VPIN = VSS
D060 D061 D063	Input Leakage Current (Notes 2, 3) I/O ports MCLR, RA4/T0CKI OSC1	IIL	- - -	- - -	±1 ±5 ±5	μA μA μA	VSS ≤ VPIN ≤ VDD, Pin at hi-impedance VSS ≤ VPIN ≤ VDD VSS ≤ VPIN ≤ VDD, XT, HS, and LP osc configuration
D080 D083	Output Low Voltage I/O ports OSC2/CLKOUT (RC osc config)	VOL	- -	- -	0.6 0.6	V V	IOL = 8.5 mA, VDD = 4.5V, -40°C to +85°C IOL = 1.6 mA, VDD = 4.5V, -40°C to +85°C
D090 D092	Output High Voltage I/O ports (Note 3) OSC2/CLKOUT (RC osc config)	VOH	VDD-0.7 VDD-0.7	- -	- -	V V	IOH = -3.0 mA, VDD = 4.5V, -40°C to +85°C IOH = -1.3 mA, VDD = 4.5V, -40°C to +85°C
D150*	Open-Drain High Voltage	VOD	-	-	14	V	RA4 pin

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C6X be driven with external clock in RC mode.

2: The leakage current on the MCLR/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as current sourced by the pin.

20.5 Timing Diagrams and Specifications

FIGURE 20-2: EXTERNAL CLOCK TIMING

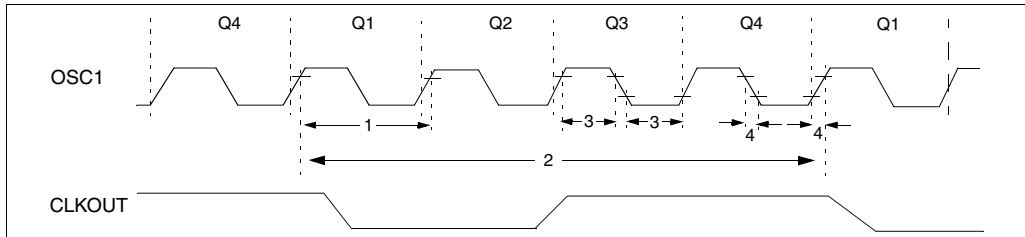


TABLE 20-2: EXTERNAL CLOCK TIMING REQUIREMENTS

Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
	Fosc	External CLKIN Frequency (Note 1)	DC	—	4	MHz	XT and RC osc mode
			DC	—	4	MHz	HS osc mode (-04)
			DC	—	10	MHz	HS osc mode (-10)
			DC	—	20	MHz	HS osc mode (-20)
			DC	—	200	kHz	LP osc mode
		Oscillator Frequency (Note 1)	DC	—	4	MHz	RC osc mode
			0.1	—	4	MHz	XT osc mode
			4	—	20	MHz	HS osc mode
1	Tosc	External CLKIN Period (Note 1)	5	—	200	kHz	LP osc mode
			250	—	—	ns	XT and RC osc mode
			250	—	—	ns	HS osc mode (-04)
			100	—	—	ns	HS osc mode (-10)
			50	—	—	ns	HS osc mode (-20)
			5	—	—	μs	LP osc mode
		Oscillator Period (Note 1)	250	—	—	ns	RC osc mode
			250	—	10,000	ns	XT osc mode
2	Tcy	Instruction Cycle Time (Note 1)	250	—	250	ns	HS osc mode (-04)
			100	—	250	ns	HS osc mode (-10)
			50	—	250	ns	HS osc mode (-20)
			5	—	—	μs	LP osc mode
			200	Tcy	DC	ns	Tcy = 4/Fosc
		External Clock in (OSC1) High or Low Time	100	—	—	ns	XT oscillator
			2.5	—	—	μs	LP oscillator
			15	—	—	ns	HS oscillator
4*	TosR, TosF	External Clock in (OSC1) Rise or Fall Time	—	—	25	ns	XT oscillator
			—	—	50	ns	LP oscillator
			—	—	15	ns	HS oscillator

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Instruction cycle period (Tcy) equals four times the input oscillator time-base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min." values with an external clock applied to the OSC1/CLKIN pin. When an external clock input is used, the "Max." cycle time limit is "DC" (no clock) for all devices.

FIGURE 20-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING

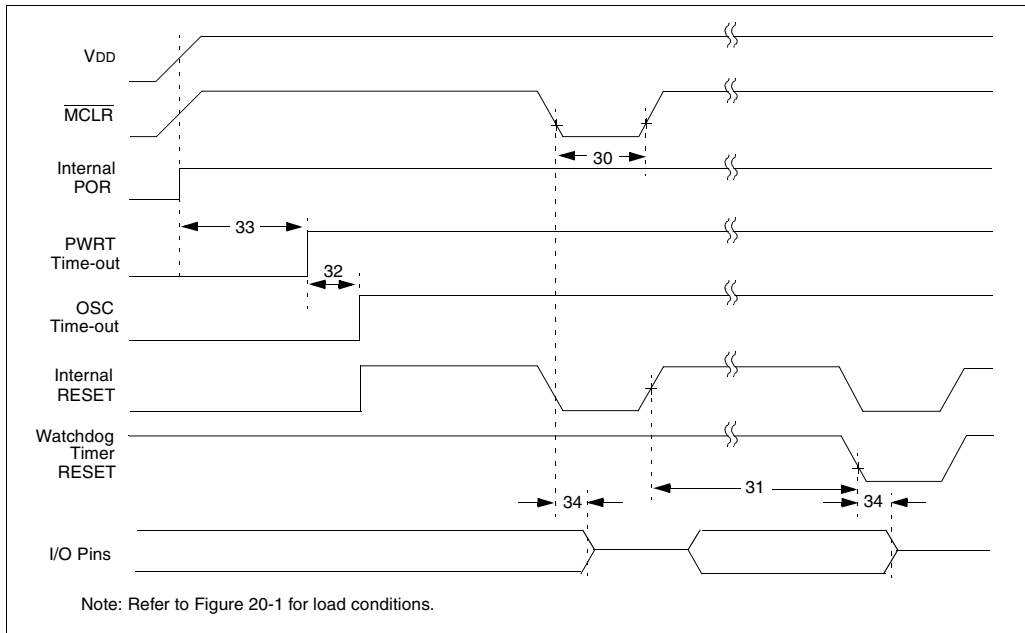


FIGURE 20-5: BROWN-OUT RESET TIMING

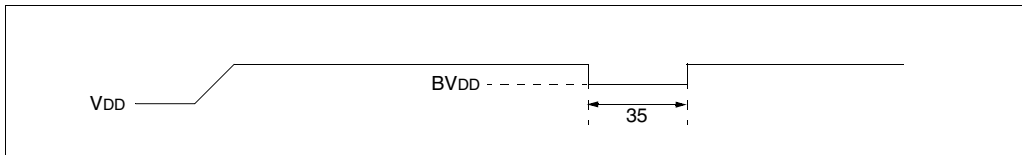


TABLE 20-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, POWER-UP TIMER, AND BROWN-OUT RESET REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
30	Tmcl	MCLR Pulse Width (low)	2	—	—	μs	VDD = 5V, -40°C to +125°C
31*	Twdt	Watchdog Timer Time-out Period (No Prescaler)	7	18	33	ms	VDD = 5V, -40°C to +125°C
32	Tost	Oscillation Start-up Timer Period	—	1024 TOSC	—	—	TOSC = OSC1 period
33*	Tpwrt	Power-up Timer Period	28	72	132	ms	VDD = 5V, -40°C to +125°C
34	Tioz	I/O Hi-impedance from MCLR Low or WDT reset	—	—	2.1	μs	
35	TBOR	Brown-out Reset Pulse Width	100	—	—	μs	VDD ≤ BVDD (D005)

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 21-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING

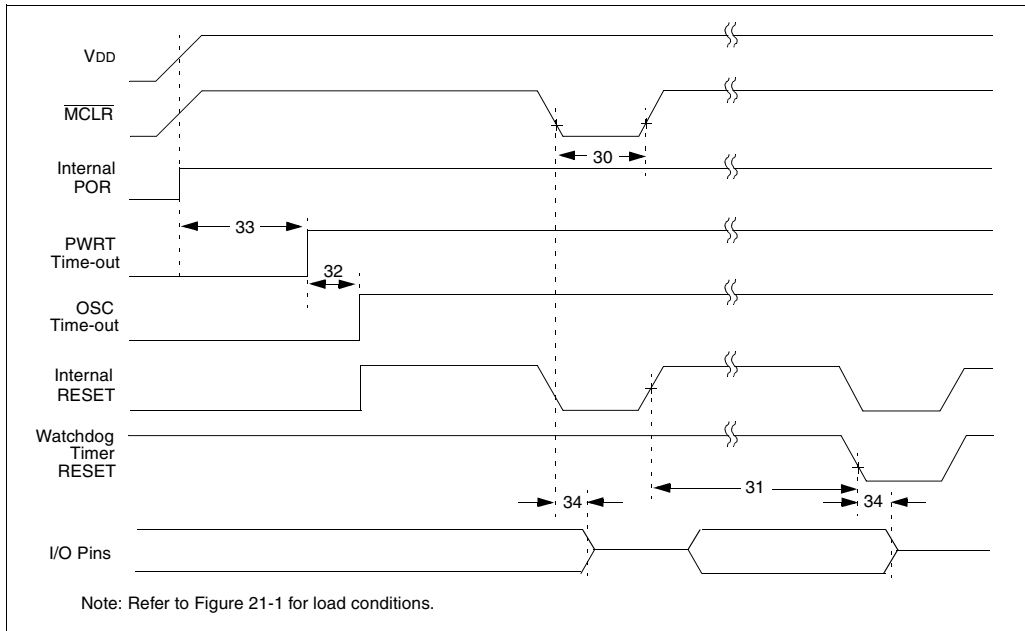


FIGURE 21-5: BROWN-OUT RESET TIMING

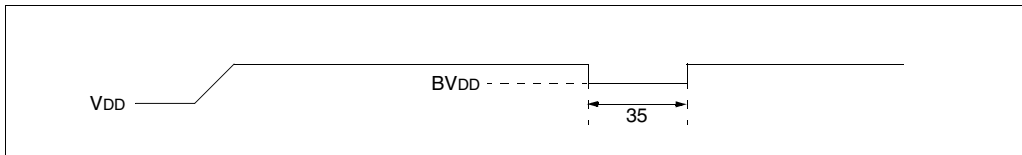


TABLE 21-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, POWER-UP TIMER, AND BROWN-OUT RESET REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
30	Tmcl	MCLR Pulse Width (low)	2	—	—	μs	VDD = 5V, -40°C to +125°C
31*	Twdt	Watchdog Timer Time-out Period (No Prescaler)	7	18	33	ms	VDD = 5V, -40°C to +125°C
32	Tost	Oscillation Start-up Timer Period	—	1024 TOSC	—	—	TOSC = OSC1 period
33*	Tpwrt	Power-up Timer Period	28	72	132	ms	VDD = 5V, -40°C to +125°C
34	Tioz	I/O Hi-impedance from MCLR Low or WDT reset	—	—	2.1	μs	
35	TBOR	Brown-out Reset Pulse Width	100	—	—	μs	VDD ≤ BVDD (D005)

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 23-8: TYPICAL I_{PD} vs. V_{DD} BROWN-OUT DETECT ENABLED (RC MODE)

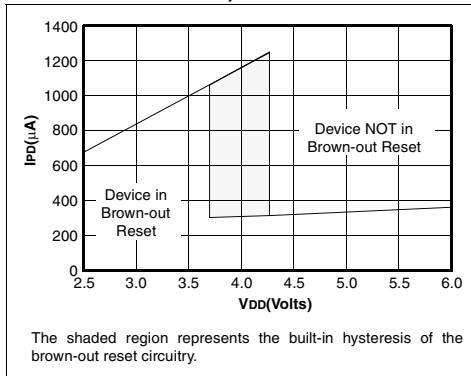


FIGURE 23-9: MAXIMUM I_{PD} vs. V_{DD} BROWN-OUT DETECT ENABLED (85°C TO -40°C, RC MODE)

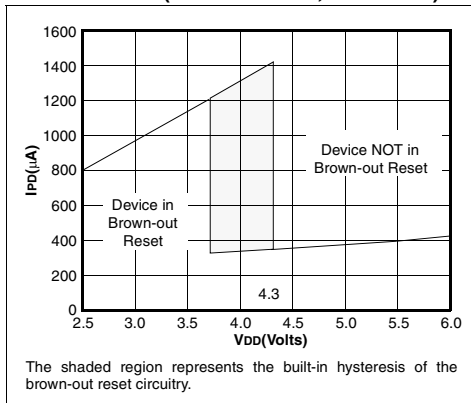


FIGURE 23-10: TYPICAL I_{PD} vs. TIMER1 ENABLED (32 kHz, RC0/RC1 = 33 pF/33 pF, RC MODE)

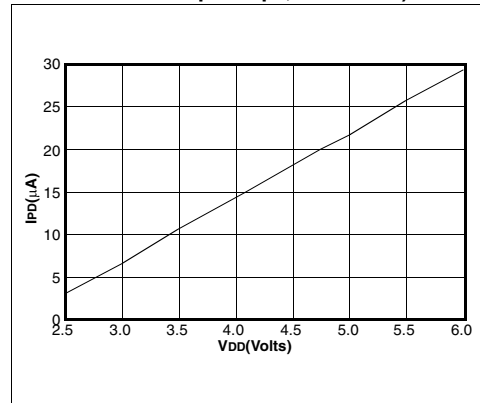
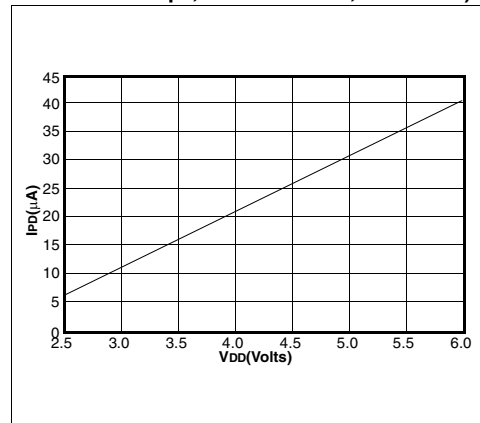


FIGURE 23-11: MAXIMUM I_{PD} vs. TIMER1 ENABLED (32 kHz, RC0/RC1 = 33 pF/33 pF, 85°C TO -40°C, RC MODE)



Data based on matrix samples. See first page of this section for details.

PIN COMPATIBILITY

Devices that have the same package type and VDD, VSS and MCLR pin locations are said to be pin compatible. This allows these different devices to operate in the same socket. Compatible devices may only requires minor software modification to allow proper operation in the application socket (ex., PIC16C56 and PIC16C61 devices). Not all devices in the same package size are pin compatible; for example, the PIC16C62 is compatible with the PIC16C63, but not the PIC16C55.

Pin compatibility does not mean that the devices offer the same features. As an example, the PIC16C54 is pin compatible with the PIC16C71, but does not have an A/D converter, weak pull-ups on PORTB, or interrupts.

TABLE F-1: PIN COMPATIBLE DEVICES

Pin Compatible Devices	Package
PIC12C508, PIC12C509, PIC12C671, PIC12C672	8-pin
PIC16C154, PIC16CR154, PIC16C156, PIC16CR156, PIC16C158, PIC16CR158, PIC16C52, PIC16C54, PIC16C54A, PIC16CR54A, PIC16C56, PIC16C58A, PIC16CR58A, PIC16C61, PIC16C554, PIC16C556, PIC16C558 PIC16C620, PIC16C621, PIC16C622 PIC16C641, PIC16C642, PIC16C661, PIC16C662 PIC16C710, PIC16C71, PIC16C711, PIC16C715 PIC16F83, PIC16CR83, PIC16F84A, PIC16CR84	18-pin, 20-pin
PIC16C55, PIC16C57, PIC16CR57B	28-pin
PIC16CR62, PIC16C62A, PIC16C63, PIC16CR63, PIC16C66, PIC16C72, PIC16C73A, PIC16C76	28-pin
PIC16CR64, PIC16C64A, PIC16C65A, PIC16CR65, PIC16C67, PIC16C74A, PIC16C77	40-pin
PIC17CR42, PIC17C42A, PIC17C43, PIC17CR43, PIC17C44	40-pin
PIC16C923, PIC16C924	64/68-pin
PIC17C756, PIC17C752	64/68-pin

PIC16C6X

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